M74HCT241-1P/FP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT241-1 is an integrated circuit chip consisting of two blocks of 3-state noninverting buffers with four independent circuits that share a common enable input.

FEATURES

- TTL level input V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 11ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range : T_a=−40~+85℃

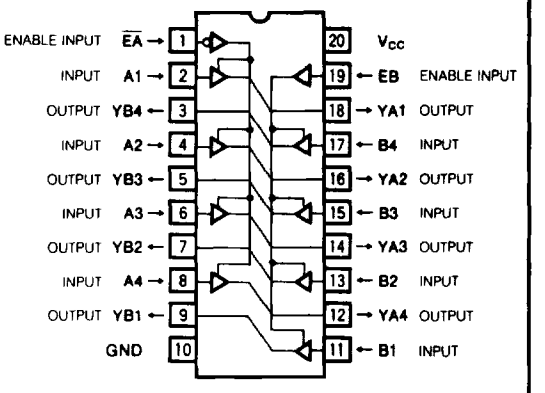
APPLICATION

General purpose, for use in industrial and consumer digital equipment

FUNCTION

Use of silicon gate technology allows the M74HCT241-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS241.The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. When used as such, no pull-up resistors are required.
The M74HCT241-1 consists of two independent blocks with each block containing four buffers.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N

When enable input $\overline{EA}$ is low and input A is low, then output YA will be set low. However, if A is high, then YA will be set high. Inverted in the other block, a high enable input EB signal causes operation the same as that just described with input B signal output at YB.
When $\overline{EA}$ is high or EB is low, all output within the block become high-impedance state, irrespective A or B.

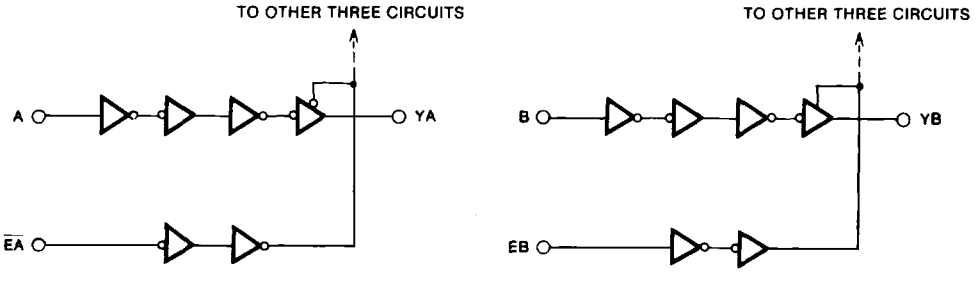
FUNCTION TABLE (Note 1)

Inputs		Output
A	$\overline{EA}$	YA
L	L	L
H	L	H
X	H	Z

Inputs		Output
B	EB	YB
L	H	L
H	H	H
X	L	Z

Note 1 : Z : High impedance
X : Irrelevant

LOGIC DIAGRAM (EACH BUFFER)



MITSUBISHI ELECTRIC

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS (T_a=−40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I<0V	−20	mA
		V_I>V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O<0V	−20	mA
		V_O>V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
T_{stg}	Storage temperature		−65∼+150	℃

Note 2 : M74HCT241-1FP : T_a=−40∼+75℃ and T_a=75∼85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a=−40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O=0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.83			3.70		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.44		0.53	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	μA
I_{CC}	Static supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
ΔI_{CC}	Maximum static supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value. All others are fixed to V_{CC} or GND.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃)

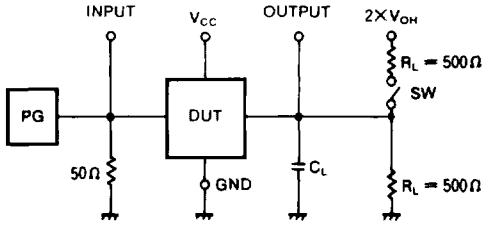
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-to high-level and high-to low-level	C_L=50pF (Note 5)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-to high-level and high-to low-level				17	ns
t_{PHL}	output propagation time (A−YA, B−YB)				19	ns
t_{PLZ}	Low-level and high-level output	C_L= 5 pF (Note 5)			20	ns
t_{PHZ}	disable time (EA−YA, EB−YB)				20	ns
t_{PZL}	Low-level and high-level output	C_L=50pF (Note 5)			22	ns
t_{PZH}	enable time (EA−YA, EB−YB)				22	ns

SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=−40∼+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40∼+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 5)		5	12		15	ns
t_{THL}				5	12		15	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A−YA, B−YB)			8	18		23	ns
t_{PHL}				11	20		25	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{EA}$−YA, EB−YB)			8	23		29	ns
t_{PHZ}				10	23		29	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{EA}$−YA, EB−YB)			9	23		29	ns
t_{PZH}				7	23		29	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$ = V_{CC}, EB = GND			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)			43.8				pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer). The power dissipated during opration under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 5 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%∼90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM