

# MITSUBISHI LSTTLs

## M74LS259P

### 8-BIT ADDRESSABLE LATCH

#### DESCRIPTION

The M74LS259P is a semiconductor integrated circuit containing 8 latch circuits and a demultiplexer which designates the latches with a 3-bit binary code.

#### FEATURES

- Easy bit expansion
- Usable as 3-bit binary/octal decoder/demultiplexer
- Direct reset input provided
- Wide operating temperature range ( $T_a = -20 \sim +75^\circ\text{C}$ )

#### APPLICATION

General purpose, for use in industrial and consumer equipment.

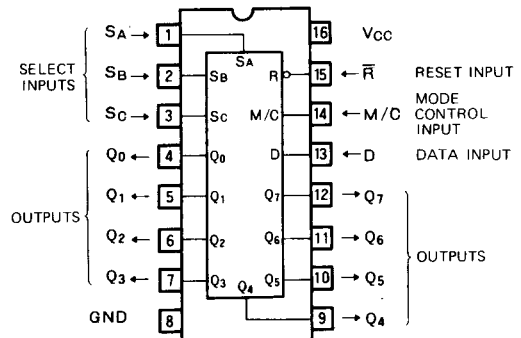
#### FUNCTIONAL DESCRIPTION

This device is composed of a 3-bit binary/octal demultiplexer and 8 latch circuits. The following operational modes can be selected by combining the mode control input M/C with the reset input  $\bar{R}$

- |  |                                |
|--|--------------------------------|
| (1) 3-bit binary/octal decoder/demultiplexer | M/C: Low;<br>$\bar{R}$ : Low   |
| (2) Addressable latch                        | M/C: Low;<br>$\bar{R}$ : High  |
| (3) Data input inhibit                       | M/C: High;<br>$\bar{R}$ : High |
| (4) Reset                                    | M/C: High;<br>$\bar{R}$ : Low  |

When this device is used as a 3-bit binary/octal decoder/demultiplexer and the select inputs  $S_A \sim S_C$  are designated by a 3-bit binary number, the same signal as the data input

#### PIN CONFIGURATION (TOP VIEW)



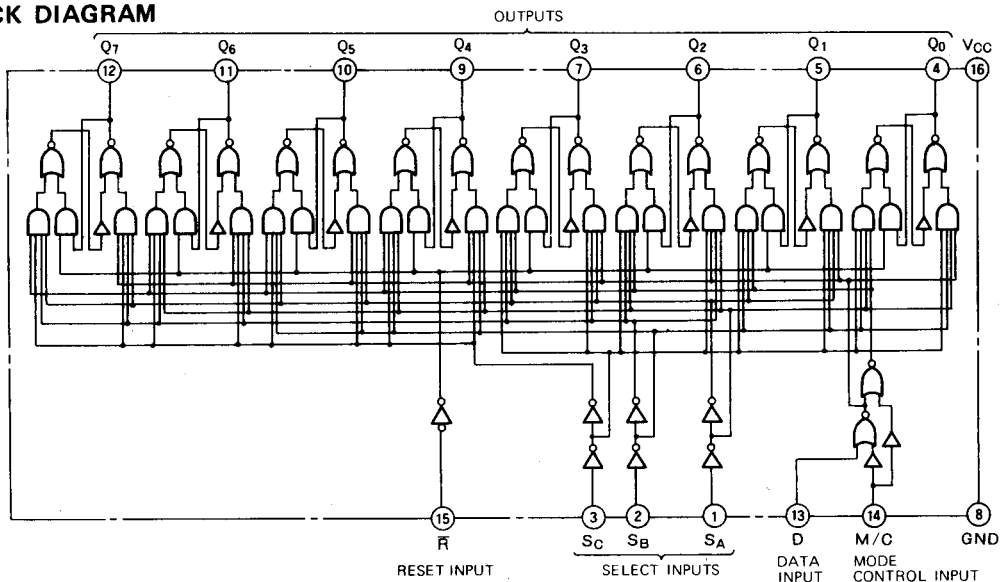
Outline 16P4

D appears in one of the outputs  $Q_0 \sim Q_7$  corresponding to that number and all the other outputs are set low. There is no latch operation in this mode.

When used as an addressable latch and inputs  $S_A \sim S_C$  are designated as above, the corresponding latch is selected and the same signal as D appears in the output. When M/C changes from low to high (data inhibit mode), the information from the data input D immediately before the change is latched. When M/C is low, the signal appearing in Q is also changed if the signal D is changed.

In the data input inhibit mode  $Q_0 \sim Q_7$  do not change

#### BLOCK DIAGRAM



**8-BIT ADDRESSABLE LATCH**

even if D is changed and the status before M/C is set high is held.

With direct resetting, all the outputs are reset low irrespective of the status of D and  $S_A \sim S_C$ .

**FUNCTION TABLE** (Note 1)

Operational mode	R	M/C	D	S <sub>A</sub>	S <sub>B</sub>	S <sub>C</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>
Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
3-bit binary/octal decoder/demultiplexer	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	H	L	L	L	L	L	L	L	L	L	L
	L	L	H	H	L	L	L	H	L	L	L	L	L	L
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	L	L	L	H	H	H	L	L	L	L	L	L	L	L
Data input inhibit	H	H	X	X	X	X	Q <sub>0</sub> <sup>0</sup>	Q <sub>1</sub> <sup>0</sup>	Q <sub>2</sub> <sup>0</sup>	Q <sub>3</sub> <sup>0</sup>	Q <sub>4</sub> <sup>0</sup>	Q <sub>5</sub> <sup>0</sup>	Q <sub>6</sub> <sup>0</sup>	Q <sub>7</sub> <sup>0</sup>
Addressable latch	H	L	L	L	L	L	L	Q <sub>1</sub> <sup>0</sup>	Q <sub>2</sub> <sup>0</sup>	Q <sub>3</sub> <sup>0</sup>	Q <sub>4</sub> <sup>0</sup>	Q <sub>5</sub> <sup>0</sup>	Q <sub>6</sub> <sup>0</sup>	Q <sub>7</sub> <sup>0</sup>
	H	L	H	L	L	L	H	Q <sub>1</sub> <sup>0</sup>	Q <sub>2</sub> <sup>0</sup>	Q <sub>3</sub> <sup>0</sup>	Q <sub>4</sub> <sup>0</sup>	Q <sub>5</sub> <sup>0</sup>	Q <sub>6</sub> <sup>0</sup>	Q <sub>7</sub> <sup>0</sup>
	H	L	L	H	L	L	Q <sub>0</sub> <sup>0</sup>	L	Q <sub>2</sub> <sup>0</sup>	Q <sub>3</sub> <sup>0</sup>	Q <sub>4</sub> <sup>0</sup>	Q <sub>5</sub> <sup>0</sup>	Q <sub>6</sub> <sup>0</sup>	Q <sub>7</sub> <sup>0</sup>
	H	L	H	H	L	L	Q <sub>0</sub> <sup>0</sup>	H	Q <sub>2</sub> <sup>0</sup>	Q <sub>3</sub> <sup>0</sup>	Q <sub>4</sub> <sup>0</sup>	Q <sub>5</sub> <sup>0</sup>	Q <sub>6</sub> <sup>0</sup>	Q <sub>7</sub> <sup>0</sup>
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	H	L	L	H	H	H	Q <sub>0</sub> <sup>0</sup>	Q <sub>1</sub> <sup>0</sup>	Q <sub>2</sub> <sup>0</sup>	Q <sub>3</sub> <sup>0</sup>	Q <sub>4</sub> <sup>0</sup>	Q <sub>5</sub> <sup>0</sup>	Q <sub>6</sub> <sup>0</sup>	L
H	L	H	H	H	H	Q <sub>0</sub> <sup>0</sup>	Q <sub>1</sub> <sup>0</sup>	Q <sub>2</sub> <sup>0</sup>	Q <sub>3</sub> <sup>0</sup>	Q <sub>4</sub> <sup>0</sup>	Q <sub>5</sub> <sup>0</sup>	Q <sub>6</sub> <sup>0</sup>	H	

Note 1 X : Irrelevant

Q<sup>0</sup> : Level of Q before the indicated steady-state input conditions were established.

**ABSOLUTE MAXIMUM RATINGS** (T<sub>a</sub> = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V <sub>CC</sub>	Supply voltage		-0.5 ~ +7	V
V <sub>I</sub>	Input voltage		-0.5 ~ +15	V
V <sub>O</sub>	Output voltage	High-level state	-0.5 ~ V <sub>CC</sub>	V
T <sub>opr</sub>	Operating free-air ambient temperature range		-20 ~ +75	°C
T <sub>stg</sub>	Storage temperature range		-65 ~ +150	°C

**RECOMMENDED OPERATING CONDITIONS** (T<sub>a</sub> = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V <sub>CC</sub>	Supply voltage	4.75	5	5.25	V
I <sub>OH</sub>	High-level output current	V <sub>OH</sub> ≥ 2.7V	0	-400	μA
I <sub>OL</sub>	Low-level output current	V <sub>OL</sub> ≤ 0.4V	0	4	mA
		V <sub>OL</sub> ≤ 0.5V	0	8	mA

**8-BIT ADDRESSABLE LATCH**
**ELECTRICAL CHARACTERISTICS** ( $T_a = -20 \sim +75^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
$V_{IH}$	High-level input voltage		2			V
$V_{IL}$	Low-level input voltage				0.8	V
$V_{IC}$	Input clamp voltage	$V_{CC} = 4.75\text{V}$ , $I_{IC} = -18\text{mA}$			1.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = 4.75\text{V}$ , $V_I = 0.8\text{V}$ $V_I = 2\text{V}$ , $I_{OH} = -400\mu\text{A}$	2.7	3.4		V
$V_{OL}$	Low-level output voltage	$V_{CC} = 4.75\text{V}$		0.25	0.4	V
		$V_I = 0.8\text{V}$ , $V_I = 2\text{V}$		0.35	0.5	V
$I_{IH}$	High-level input current	$V_{CC} = 5.25\text{V}$ , $V_I = 2.7\text{V}$			20	$\mu\text{A}$
		$V_{CC} = 5.25\text{V}$ , $V_I = 10\text{V}$			0.1	mA
$I_{IL}$	Low-level input current	$V_{CC} = 5.25\text{V}$ , $V_I = 0.4\text{V}$			-0.4	mA
$I_{OS}$	Short-circuit output current (Note 2)	$V_{CC} = 5.25\text{V}$ , $V_O = 0\text{V}$	-20		100	mA
$I_{CC}$	Supply current	$V_{CC} = 5.25\text{V}$ (Note 3)		22	36	mA

\* : All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3:  $I_{CC}$  is measured with all inputs at 0V.

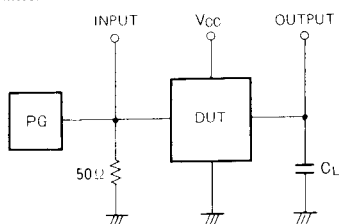
**SWITCHING CHARACTERISTICS** ( $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PHL}$	High-to-low-level output propagation time, from input $\bar{R}$ to outputs $Q_0 \sim Q_7$			9	27	ns
$t_{PLH}$	Low-to-high-level, high-to-low-level output propagation time, from input D to outputs $Q_0 \sim Q_7$	$C_L = 15\text{pF}$		15	32	ns
$t_{PHL}$	Low-to-high-level, high-to-low-level output propagation time, from inputs $S_A$ , $S_B$ , $S_C$ to outputs $Q_0 \sim Q_7$			12	21	ns
$t_{PLH}$	Low-to-high-level, high-to-low-level output propagation time, from input M/C to outputs $Q_0 \sim Q_7$			15	38	ns
$t_{PHL}$	Low-to-high-level, high-to-low-level output propagation time from input D to outputs $Q_0 \sim Q_7$			12	29	ns
$t_{PLH}$	Low-to-high-level, high-to-low-level output propagation time from input M/C to outputs $Q_0 \sim Q_7$			14	35	ns
$t_{PHL}$	Low-to-high-level, high-to-low-level output propagation time from input M/C to outputs $Q_0 \sim Q_7$			13	24	ns

**TIMING REQUIREMENTS** ( $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su}(DH)$	Setup time D high to M/C		15	10		ns
$t_h(DH)$	Hold time D high to M/C		5	-5		ns
$t_{su}(DL)$	Setup time D low to M/C		15	8		ns
$t_h(DL)$	Hold time D low to M/C		5	-7		ns
$t_{su}(S)$	Setup time $S_A$ , $S_B$ to M/C		15	7		ns
$t_h(S)$	Hold time $S_A$ , $S_B$ to M/C		5	-5		ns
$t_w(M/C)$	M/C input pulse width		15	8		ns
$t_w(\bar{R})$	$\bar{R}$ input pulse width		15	7		ns

Note 4: Measurement circuit



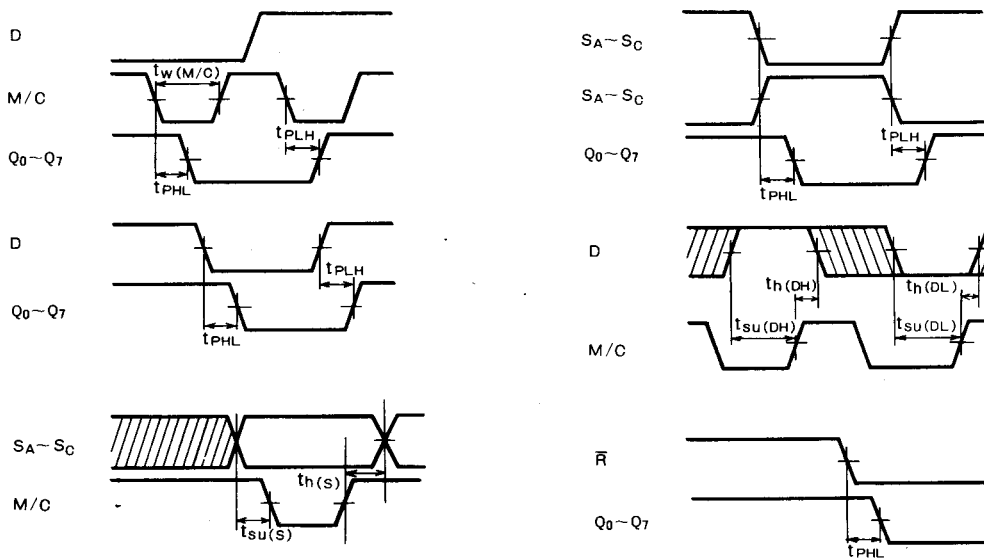
(1) The pulse generator (PG) has the following characteristics:

PRR = 1MHz,  $t_r = 6\text{ns}$ ,  $t_f = 6\text{ns}$ ,  $t_w = 500\text{ns}$ ,  
 $V_p = 3V_{p-p}$ ,  $Z_0 = 50\Omega$ .

(2)  $C_L$  includes probe and jig capacitance.

**8-BIT ADDRESSABLE LATCH**

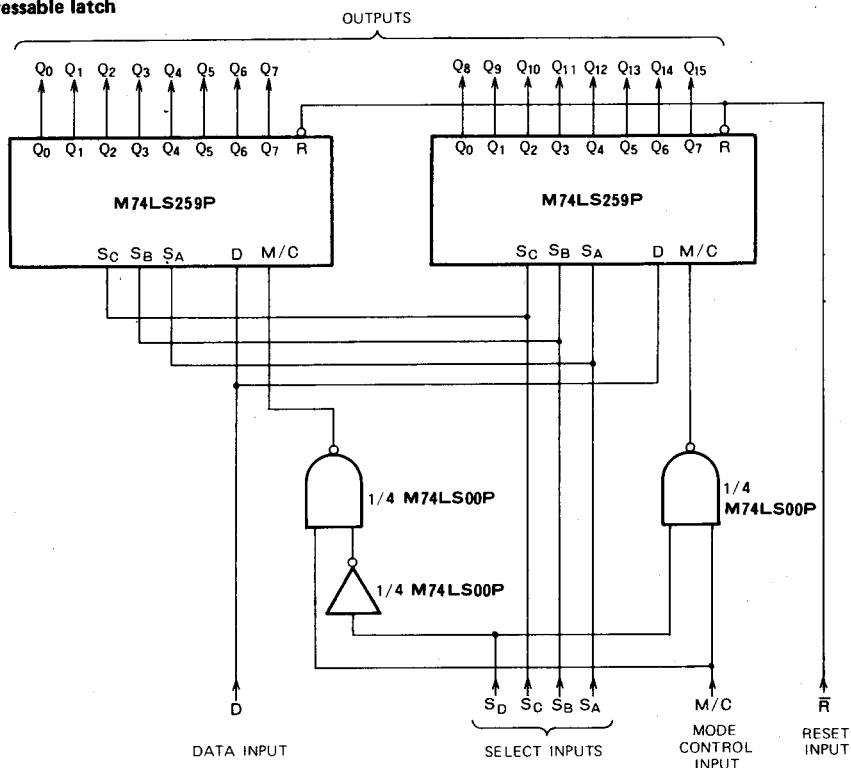
**TIMING DIAGRAM (Reference level = 1.3V)**



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

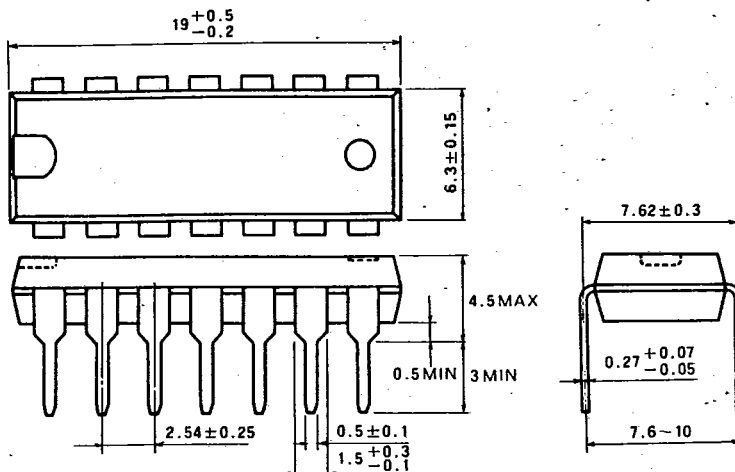
**APPLICATION EXAMPLE**

**16-bit addressable latch**

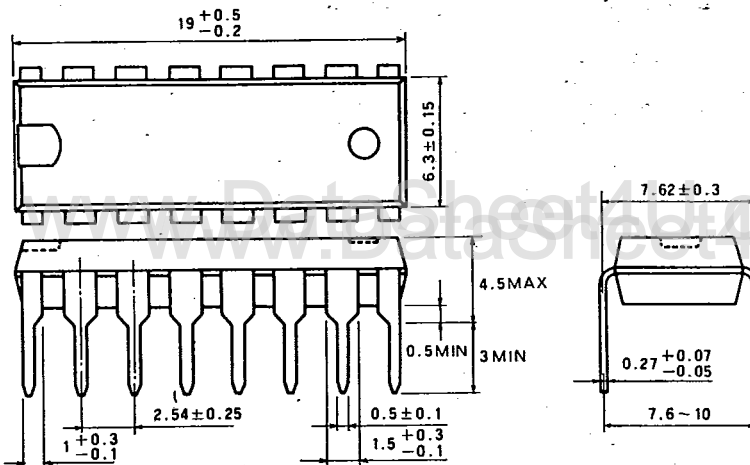


**TYPE 14P4 14-PIN MOLDED PLASTIC DIL**

Dimension in mm

**TYPE 16P4 16-PIN MOLDED PLASTIC DIL**

Dimension in mm

**TYPE 20P4 20-PIN MOLDED PLASTIC DIL**

Dimension in mm

