

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH RESET

DESCRIPTION

The M74LS73AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input \bar{T} , inputs J and K and direct reset input \bar{R}_D .

FEATURES

- Negative edge-triggering
- Each flip-flop can be used independently
- Direct reset input
- Q and \bar{Q} outputs
- Wide operating temperature range ($T_a = -20 \sim +75^\circ\text{C}$)

APPLICATION

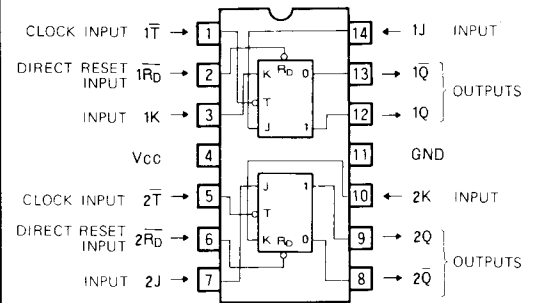
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

While \bar{T} is high, signals J and K are put in the read-in state, and when \bar{T} changes from high to low, the J and K signals immediately before the change emerge in outputs Q and \bar{Q} in accordance with the function table. By setting \bar{R}_D low, Q and \bar{Q} are set low and high respectively irrespective of the status of the other input signals. For use as a J-K flip-flop, \bar{R}_D must be kept high.

Also available is M74LS107AP with the same functions and electrical characteristics. This offers easy mounting with V_{CC} positioned at pin 14 and GND at pin 7.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

FUNCTIONAL TABLE (Note 1)

\bar{T}	\bar{R}_D	J	K	Q	\bar{Q}
X	L	X	X	L	H
↓	H	H	H	Toggle	
↓	H	L	H	L	H
↓	H	H	L	H	L
↓	H	L	L	Q^0	\bar{Q}^0
H	H	X	X	Q^0	\bar{Q}^0

Note 1 ↓ : Transition from high to low-level (negative edge trigger)

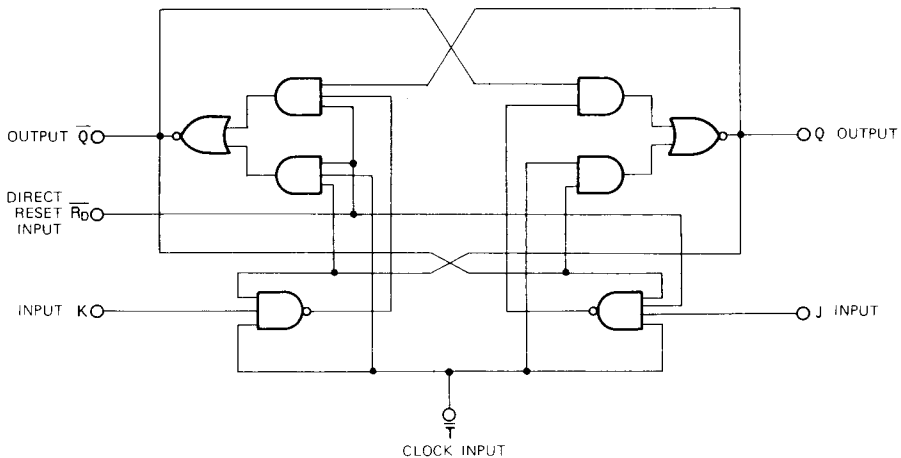
X : Irrelevant

Q^0 : level of Q before the indicated steady-state input conditions were established.

\bar{Q}^0 : level of \bar{Q} before the indicated steady-state input conditions were established.

Toggle : complement of previous state with ↓ transition of outputs

BLOCK DIAGRAM (EACH FLIP-FLOP)



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ABSOLUTE MAXIMUM RATINGS (Ta = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V _{CC}	Supply voltage		-0.5 ~ +7	V
V _I	Input voltage		-0.5 ~ +15	V
V _O	Output voltage	High-level state	-0.5 ~ V _{CC}	V
T _{opr}	Operating free-air ambient temperature range		-20 ~ +75	°C
T _{stg}	Storage temperature range		-65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V _{CC}	Supply voltage		4.75	5	5.25	V
I _{OH}	High-level output current	V _{OH} ≥ 2.7V	0		-400	μA
I _{OL}	Low-level output current	V _{OL} ≤ 0.4V	0		4	mA
		V _{OL} ≤ 0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ *	Max	
V _{IH}	High-level input voltage			2			V
V _{IL}	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage		V _{CC} = 4.75V, I _{IC} = -18mA			-1.5	V
V _{OH}	High-level output voltage		V _{CC} = 4.75V, V _I = 0.8V V _I = 2V, I _{OH} = -400μA	2.7	3.4		V
V _{OL}	Low-level output voltage		V _{CC} = 4.75V V _I = 0.8V, V _I = 2V	I _{OL} = 4mA	0.25	0.4	V
				I _{OL} = 8mA	0.35	0.5	V
I _{IH}	High-level input current	J, K	V _{CC} = 5.25V V _I = 2.7V			20	μA
		$\overline{R_D}$				60	μA
		\overline{T}				80	μA
		J, K	V _{CC} = 5.25V V _I = 10V			0.1	mA
		$\overline{R_D}$				0.3	mA
		\overline{T}				0.4	mA
I _{IL}	Low-level input current	J, K	V _{CC} = 5.25V			-0.4	mA
		$\overline{R_D}$, \overline{T}	V _I = 0.4V			-0.8	mA
I _{OS}	Short-circuit output current (Note 2)		V _{CC} = 5.25V, V _O = 0V	-20		-100	mA
I _{CC}	Supply current		V _{CC} = 5.25V (Note 3)		4	6	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

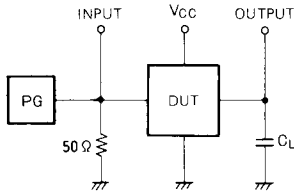
Note 3: Supply current measurements should be done with Q and \overline{Q} set alternately high and \overline{T} should be set low during actual measurement.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
f _{max}	Maximum clock frequency		C _L = 15pF (Note 4)	30	45		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from \overline{T} to Q, \overline{Q}				8	20	ns
t _{PHL}	Low-to-high-level, high-to-low-level output propagation time, from \overline{T} to Q, \overline{Q}				6	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{R_D}$ to Q, \overline{Q}				10	20	ns
t _{PHL}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{R_D}$ to Q, \overline{Q}				7	20	ns
t _{PHL}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{R_D}$ to Q, \overline{Q}						

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Note 4: Measurement circuit

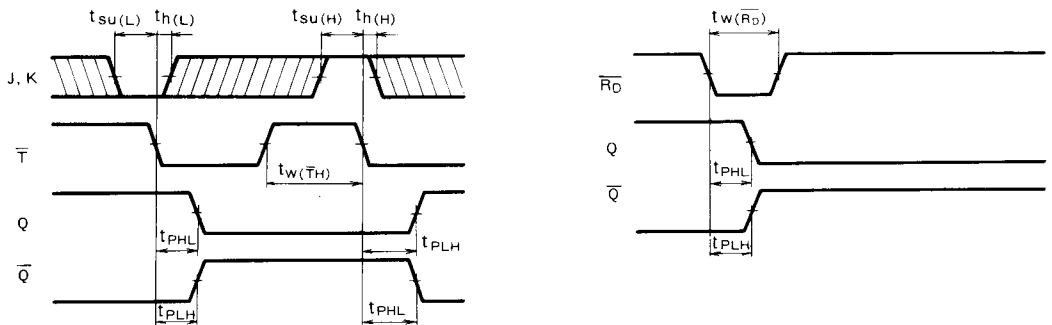


- (1) The pulse generator (PG) has the following characteristics:
 PRR = 1MHz, $t_r = 6ns$, $t_f = 6ns$, $t_w = 500ns$,
 $V_p = 3V_{p.p.}$, $Z_o = 50\Omega$.
 (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{CC} = 5V$, $T_a = 25^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_w(\bar{T}H)$	Clock input \bar{T} high pulse width		20	12		ns
$t_w(\bar{R}D)$	Direct reset input pulse width		25	4		ns
t_r	Clock rise time			650	100	ns
t_f	Clock fall time			900	100	ns
$t_{su}(H)$	Setup time high \bar{T} to J, K		20	9		ns
$t_{su}(L)$	Setup time low \bar{T} to J, K		20	10		ns
$t_h(H)$	Hold time high \bar{T} to J, K		0	- 8		ns
$t_h(L)$	Hold time low \bar{T} to J, K		0	- 5		ns

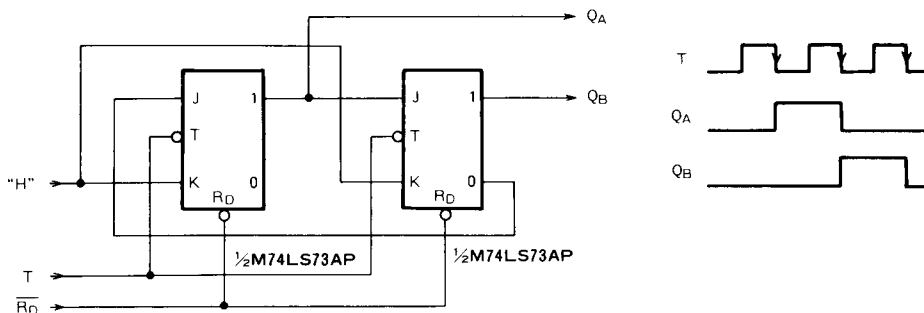
TIMING DIAGRAM (Reference level = 1.3V)



Note: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

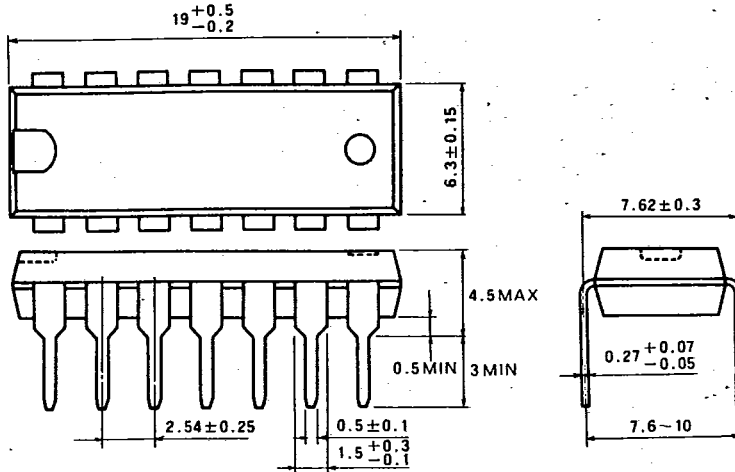
High-speed 1/3 divider



T-90-20

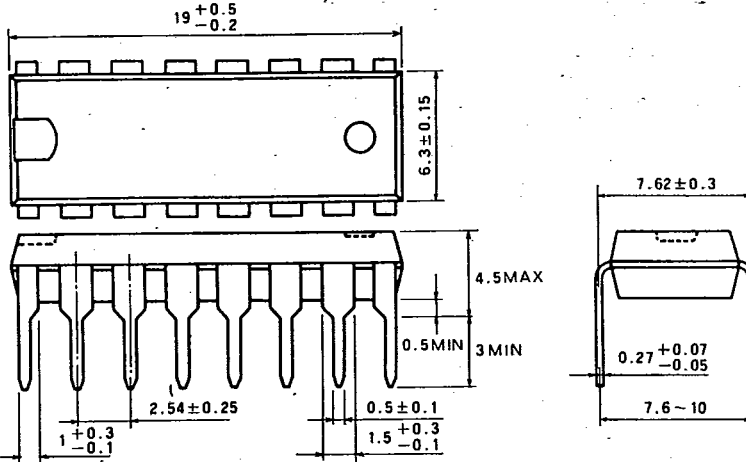
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm

