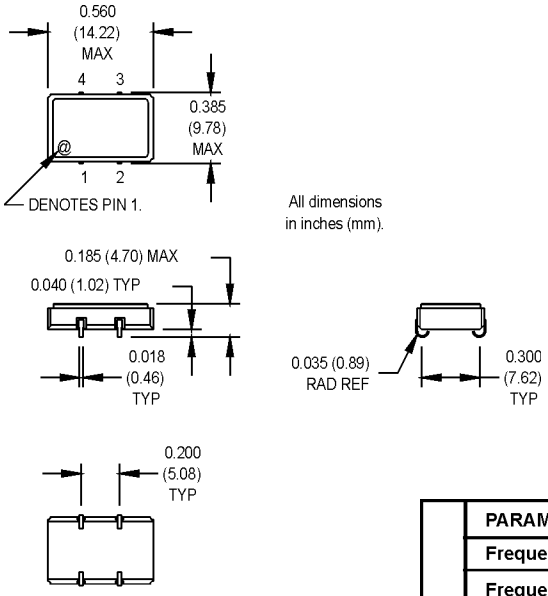
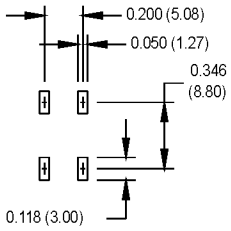
M7R Series 5.0 Volt HCMOS/TTL Compatible Surface Mount Oscillators

These are non-PLL based high frequency oscillators intended for applications that require low phase jitter. For frequencies 80.000 MHz and below, please see the M7S series.



SUGGESTED SOLDER PAD LAYOUT



Ordering Information

00.0000 MHz

M7R 1 3 F A J

- **Product Series**
- **Temperature Range**
  - **1:** 0°C to +70°C
  - **2:** -40°C to +85°C
  - **5:** -10°C to +85°C
  - **6:** -20°C to +70°C
  - **7:** 0°C to +85°C
- **Stability**
  - **1:** ±1000 ppm
  - **2:** ±500 ppm
  - **3:** ±100 ppm
  - **4:** ±50 ppm
  - **5:** ±35 ppm
  - **6:** ±25 ppm
  - ***8:** ±20 ppm
- **Output Type**
  - **F:** Fixed
  - **T:** Tristate
- **Symmetry/Logic Compatibility**
  - **A:** 40/60 CMOS/TTL
  - **C:** 45/55 CMOS
- **Package/Lead Configurations**
  - **J:** J Lead (Gold Flash Leads)
- **Frequency (customer specified)**

*Consult factory for availability.

Pin Connections

PIN	FUNCTION
1	N/C or Tri-state
2	Ground
3	Output
4	+Vdd

	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition
Electrical Specifications	Frequency Range	F	80.001		125	MHz	
	Frequency Stability	ΔF/F	(See Ordering Information)				
	Operating Temperature	TA	(See Ordering Information)				
	Storage Temperature	Ts	-55		+125	°C	
	Input Voltage	Vdd	4.5	5.0	5.5	V	
	Input Current	Idd			90	mA	
	Symmetry (Duty Cycle)		(See Ordering Information)				See Note 1
	Load		10 TTL or 15 pF				See Note 2
	Rise/Fall Time	Tr/Tf			5	ns	See Note 3
	Logic "1" Level	Voh	90% Vdd Vdd -0.5			V V	HCMOS load TTL load
	Logic "0" Level	Vol			10% Vdd 0.5	V V	HCMOS load TTL load
	Cycle to Cycle Jitter			5	20	ps RMS	1 Sigma
	Tri-state Function		Pin 1 logic "1" or floating; output active Pin 1 logic "0"; output disables to high-Z				
Environmental	Mechanical Shock		Per MIL-STD-202, Method 213, Condition C				
	Vibration		Per MIL-STD-202, Method 201 & 204				
	Reflow Solder Conditions		240°C for 10 s max.				
	Hermeticity		Per MIL-STD-202, Method 112 (1 x 10^{-8} atm.cc/s of helium)				
	Solderability		Per EIAJ-STD-002				

1. Symmetry is measured at 1.4 V with TTL load, and at 50% Vdd with HCMOS load.
2. TTL load - See load circuit diagram #1 on page 92. HCMOS load - See load circuit diagram #2 on page 92.
3. Rise/Fall times are measured between 0.5 V and 2.4 V with TTL load, and between 10% Vdd and 90% Vdd with HCMOS load.

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