

M81723FP

HIGH VOLTAGE HALF BRIDGE DRIVER

DESCRIPTION

M81723FP is high voltage Power MOSFET and IGBT module driver for half bridge applications.

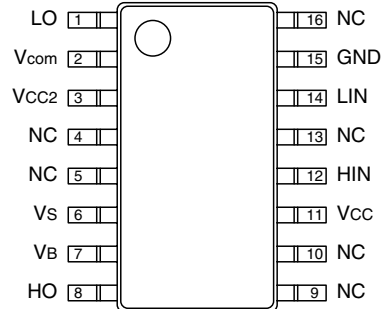
FEATURES

- FLOATING SUPPLY VOLTAGE 600V
- OUTPUT CURRENT +130mA/-100mA (typ)
- UNDERVOLTAGE LOCKOUT
- SOP-16 PACKAGE

APPLICATIONS

IGBT/MOSFET driver

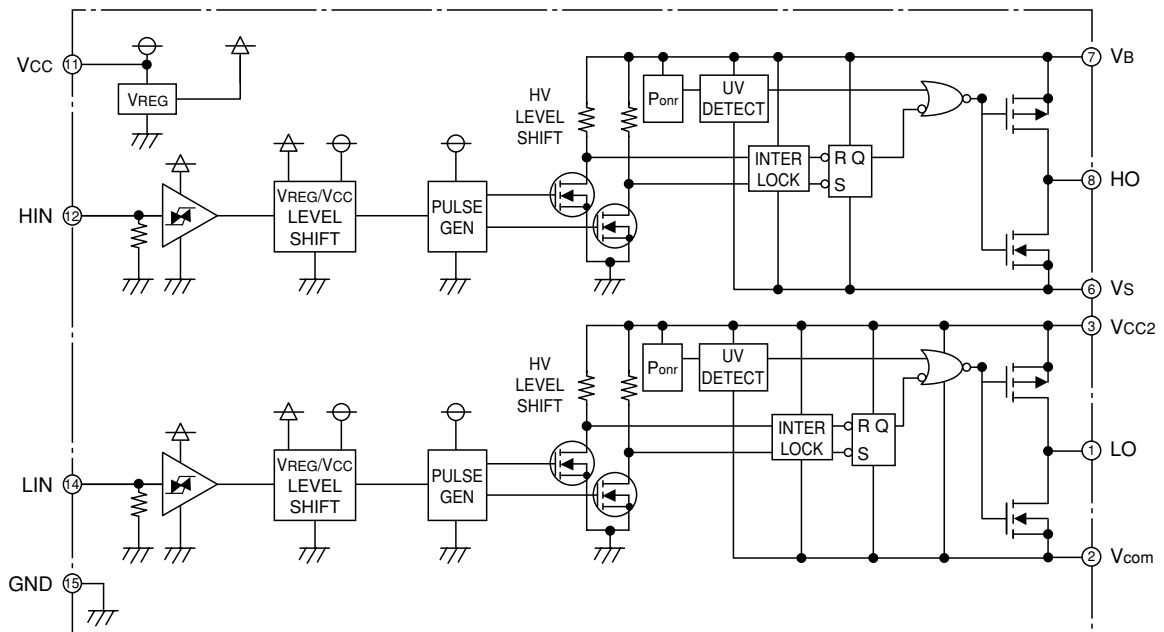
PIN CONFIGURATION (TOP VIEW)



NC:NO CONNECTION

Outline:16P2N

BLOCK DIAGRAM



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HIGH VOLTAGE HALF BRIDGE DRIVER

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Ratings	Unit
V _B	High Side Floating Supply Absolute Voltage		-0.5 ~ 624	V
V _S	High Side Floating Supply Offset Voltage		V _B -24 ~ V _B +0.5	V
V _{BS}	High Side Floating Supply Voltage	V _{BS} = V _B -V _S	-0.5 ~ 24	V
V _{HO}	High Side Output Voltage		V _S -0.5 ~ V _B +0.5	V
V _{CC2}	Low Side Floating Supply Absolute Voltage		-0.5 ~ 624	V
V _{com}	Output Standard Voltage		V _{CC2} -24 ~ V _{CC2} +0.5	V
V _{CC2com}	Low Side Floating Supply Voltage	V _{CC2com} = V _{CC2} -V _{com}	-0.5 ~ 24	V
V _{LO}	Low Side Output Voltage		V _{com} -0.5 ~ V _{CC2} +0.5	V
V _{CC}	Low Side Fixed Supply Voltage		-0.5 ~ 24	V
V _{IN}	Logic Input Voltage	HIN, LIN	-0.5 ~ V _{CC} +0.5	V
dV _S /dt	Allowable Offset Voltage Transient		±50	V/ns
P _d	Package Power Dissipation	Ta = 25°C, On Board	0.11	W
K _θ	Linear Derating Factor	Ta > 25°C, On Board	-8.9	mW/°C
R _{th(j-c)}	Junction-Case Thermal Resistance		45	°C/W
T _j	Junction Temperature		-40 ~ 125*	°C
T _{opr}	Operation Temperature		-40 ~ 100	°C
T _{stg}	Storage Temperature		-55 ~ 150	°C
TL	Solder Heat-proof (Reflow)	Pb Free	255:10s, max 260	°C

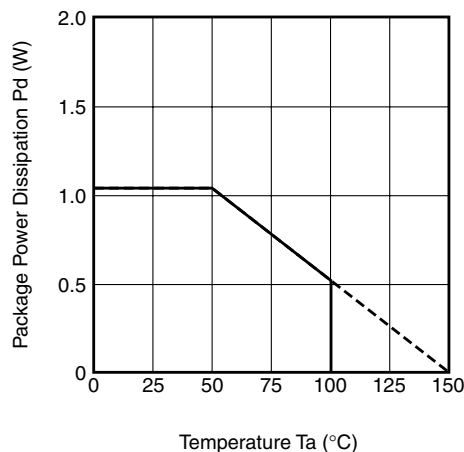
* Please adjust the V_S potential to 500V or less when the junction temperature (T_j) exceeds 125°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _B	High Side Floating Supply Absolute Voltage		V _S +10	—	V _S +20	V
V _S	High Side Floating Supply Offset Voltage	V _B > 10V	-5	—	500	V
V _{BS}	High Side Floating Supply Voltage	V _{BS} = V _B -V _S	10	—	20	V
V _{HO}	High Side Output Voltage		V _S	—	V _B	V
V _{CC2}	Low Side Floating Supply Absolute Voltage		V _{com} +10	—	V _{com} +20	V
V _{com}	Output Standard Voltage	V _{CC2} > 10V	-5	—	500	V
V _{CC2com}	Low Side Floating Supply Voltage	V _{CC2com} = V _{CC2} -V _{com}	10	—	20	V
V _{LO}	Low Side Output Voltage		V _{com}	—	V _{CC2}	V
V _{CC}	Low Side Fixed Supply Voltage		10	—	20	V
V _{IN}	Logic Input Voltage	HIN, LIN	0	—	V _{CC}	V

* For proper operation, the device should be used within the recommended conditions.

THERMAL DERATING FACTOR CHARACTERISTIC (MAXIMUM RATING)



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ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$, $V_{CC} = V_{CC2com} (= V_{CC2} - V_{com}) = V_{BS} (= V_B - V_S) = 15\text{V}$, $V_S = V_{com} = 0\text{V}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.*	Max.	
IFS	Floating Supply Leakage Current	$V_B = V_S = 600\text{V}$	—	—	1.0	μA
IFcom	V_{com} Floating Supply Leakage Current	$V_{CC2} = V_{com} = 600\text{V}$	—	—	1.0	μA
IBS	V_{BS} Standby Current	$HIN = LIN = 0\text{V}$	—	0.20	0.4	mA
ICC	V_{CC} Standby Current	$HIN = LIN = 0\text{V}$	—	0.30	0.6	mA
ICC2	V_{CC2} Standby Current	$HIN = LIN = 0\text{V}$	—	0.20	0.4	mA
IBSH	V_{BS} Standby Current H	$HIN = 5\text{V}$	—	0.25	0.5	mA
ICCH	V_{CC} Standby Current H	$HIN = 5\text{V}$	—	0.37	0.75	mA
ICC2H	V_{CC2} Standby Current H	$HIN = 5\text{V}$	—	0.20	0.4	mA
IBSL	V_{BS} Standby Current L	$LIN = 5\text{V}$	—	0.20	0.4	mA
ICCL	V_{CC} Standby Current L	$LIN = 5\text{V}$	—	0.37	0.75	mA
ICC2L	V_{CC2} Standby Current L	$LIN = 5\text{V}$	—	0.25	0.5	mA
VOH	High Level Output Voltage	$I_O = 0\text{A}$, LO, HO	14.9	—	—	V
VOL	Low Level Output Voltage	$I_O = 0\text{A}$, LO, HO	—	—	0.1	V
VIH	High Level Input Threshold Voltage	HIN, LIN	4.0	—	—	V
VIL	Low Level Input Threshold Voltage	HIN, LIN	—	—	0.6	V
VINh	Input Hysteresis Voltage	$V_{INh} = V_{IH} - V_{IL}$	1.0	1.5	2.0	V
IiH5	High Level Input Bias Current 5	$V_{IN} = 5\text{V}$	—	25	75	μA
IiH15	High Level Input Bias Current 15	$V_{IN} = 15\text{V}$	—	75	150	μA
IiL	Low Level Input Bias Current	$V_{IN} = 0\text{V}$	—	—	1.0	μA
VBSuvr	V_{BS} Supply UV Reset Voltage		7.2	8.4	9.7	V
VBSuvh	V_{BS} Supply UV Hysteresis Voltage		0.1	0.4	0.7	V
tVBSuv	V_{BS} Supply UV Filter Time		—	7.5	—	μs
VCC2uvr	V_{CC2} Supply UV Reset Voltage		7.2	8.4	9.7	V
VCC2uvh	V_{CC2} Supply UV Hysteresis Voltage		0.1	0.4	0.7	V
tVCC2ur	V_{CC2} Supply UV Filter Time		—	7.5	—	μs
VPonr	Power-On Reset Voltage		—	—	6.0	V
tPonr(FIL)	Power-On Reset Filter Time		300	—	—	ns
IOH	Output High Level Short Circuit Pulsed Current	$V_O = 0\text{V}$, $V_{IN} = 5\text{V}$, $PW < 10\mu\text{s}$	80	130	180	mA
IOL	Output Low Level Short Circuit Pulsed Current	$V_O = 15\text{V}$, $V_{IN} = 0\text{V}$, $PW < 10\mu\text{s}$	60	100	140	mA
ROH	Output High Level On Resistance	$I_O = -20\text{mA}$, $ROH = (V_{OH} - V_O)/I_O$	—	55	100	Ω
ROL	Output Low Level On Resistance	$I_O = 20\text{mA}$, $ROL = V_O/I_O$	—	45	70	Ω
tdLH(HO)	High Side Turn-On Propagation Delay	$CL = 200\text{pF}$ between HO- V_S	75	95	120	ns
tdHL(HO)	High Side Turn-Off Propagation Delay	$CL = 200\text{pF}$ between HO- V_S	85	115	145	ns
trH	High Side Turn-On Rise Time	$CL = 200\text{pF}$ between HO- V_S	15	35	70	ns
tfH	High Side Turn-Off Fall Time	$CL = 200\text{pF}$ between HO- V_S	10	30	80	ns
tdLH(LO)	Low Side Turn-On Propagation Delay	$CL = 200\text{pF}$ between LO- V_{com}	70	95	120	ns
tdHL(LO)	Low Side Turn-Off Propagation Delay	$CL = 200\text{pF}$ between LO- V_{com}	85	115	145	ns
trL	Low Side Turn-On Rise Time	$CL = 200\text{pF}$ between LO- V_{com}	15	35	70	ns
tfL	Low Side Turn-Off Fall Time	$CL = 200\text{pF}$ between LO- V_{com}	10	30	80	ns
Δt_{dLH}	Delay Matching, High Side and Low Side Turn-On	$ t_{dLH}(HO) - t_{dLH}(LO) $	—	—	15	ns
Δt_{dHL}	Delay Matching, High Side and Low Side Turn-Off	$ t_{dHL}(HO) - t_{dHL}(LO) $	—	—	15	ns
VOPW	Output Pulse Width	$V_{IN} : PW = 200\text{ns}$	200	220	240	ns

* Typ. is not specified.

FUNCTION TABLE

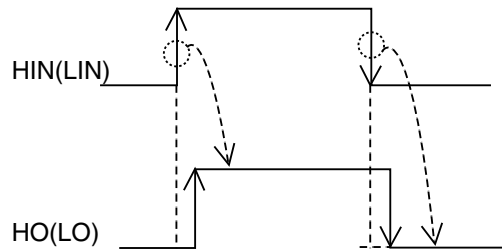
HIN	LIN	VBS UV	VCC2com UV	HO	LO	Behavioral state
H→L	H→L	H	H	L	L	LO = HO = Low
H→L	L→H	H	H	L	H	LO = High
L→H	H→L	H	H	H	L	HO = High
L→H	L→H	H	H	H	H	LO = HO = High
X	H→L	L	H	L	L	HO = Low, VBS UV tripped
X	L→H	L	H	L	H	LO = High, VBS UV tripped
H→L	X	H	L	L	L	LO = Low, VCC2com UV tripped
L→H	X	H	L	H	L	HO = High, VCC2com UV tripped

Note1 : "L" state of Vbs UV, Vcc UV means that UV trip voltage.

2 : In the case of both input signals (HIN and LIN) are "H", output signals (HO and LO) become "H".

3 : X : L→H or H→L.

4 : Output signal (HO, LO) is triggered by the edge of input signal.

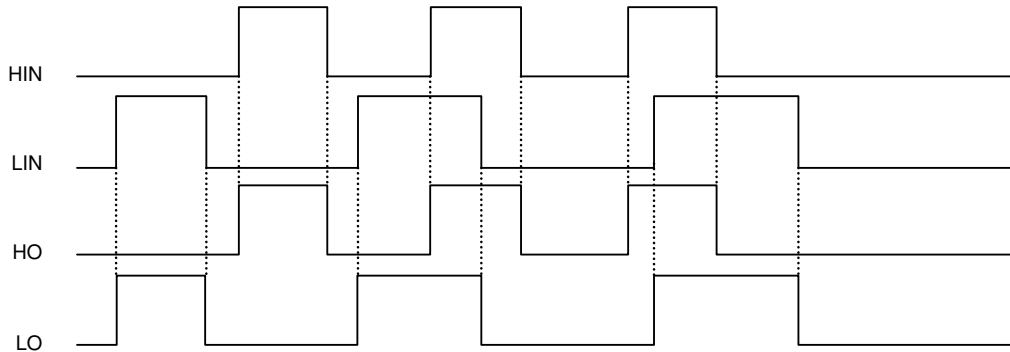


TIMING DIAGRAM

1. Input/Output Timing Diagram

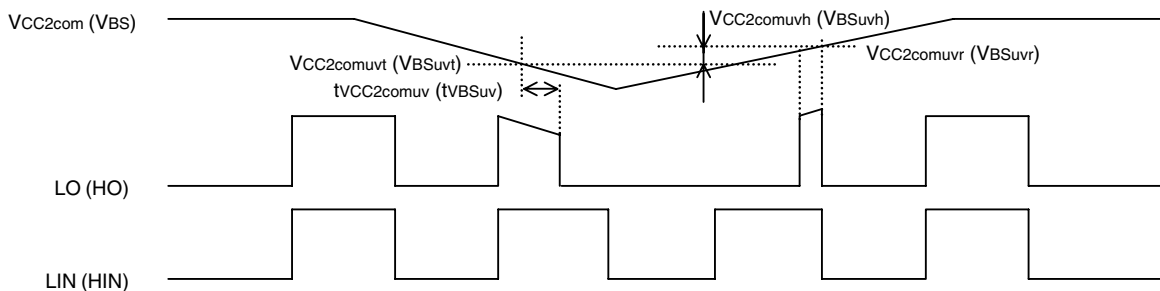
HIGH ACTIVE (When input signal (HIN or LIN) is "H", then output signal (HO or LO) is "H".)

In the case of both input signals (HIN and LIN) are "H", output signals (HO and LO) become "H".



2. VCC2com (VBS) Supply Under Voltage Lockout Timing Diagram

If supply voltage drops below UV trip voltage (** t_{uvt} = ** t_{uvr} - ** t_{uvh}) for supply UV filter time, output signal becomes "L". As soon as supply voltage is higher than UV reset voltage, output becomes normal.



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3. Allowable Supply Voltage Transient

It is recommended to supply VCC firstly and supply VCC2com secondly and supply VBS at last. In the case of shutting off supply voltage, please shut off VBS supply voltage firstly. Secondly, shut off VCC2com Supply Voltage. And at last, shutting off VCC supply voltage.

When applying VCC2com and VBS, power supply should be applied slowly. If it rises rapidly, output signal (HO or LO) may be malfunction.

PACKAGE OUTLINE

