Features

- Single chip 8-bit CPU
- Operation voltage: 1.8V to 3.6V
- Memory:
  - ◆ ROM 48K Bytes
  - ◆ Data RAM: 128 Bytes (shared with stack)
- 8 inputs with pull high resister, 4 open-drain output pins with pull high resistor, 4 output pins with NMOS/CMOS selection, 2 quasi-bi-directional NMOS output pins with pull high resistor.
- 1 dedicated push pull output
- Stop mode: micro-controller no operation (Oscillators stop oscillating)
- Watchdog timer built-in
- One re-loadable 8-bit timer
- Build-in low voltage detector (Max. 2.4V) and low voltage reset (typical voltage: below 1.85V)
- Oscillator (455K resonator or 3.58M/4M crystal)

Selection Information

	MA014B
ROM (Program ROM)	48K x 8-bit (48K x 8-bit)
I/O	19

Application Field

Toy controller

General IR controller

General Description

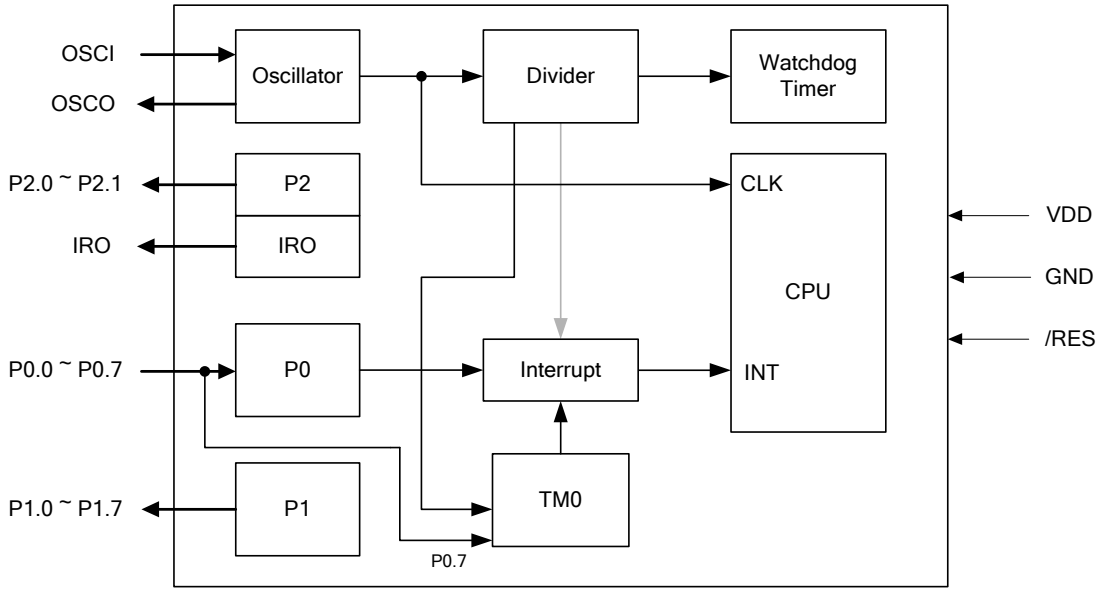
MA014B integrates an 8-bit CPU core, SRAM, timer and system control circuits by a CMOS silicon gate technology. The ROM can store data table and program.

Nineteen I/O and one large sink output pin make this chip very suitable for IR application.

Pad Description

Pad No.	Pad Name	I/O	Description
10, 9	OSCO, OSCI	O, I	Resonator or crystal oscillator pins
14,15	VDD, VDD_1	P	Positive power pins
11	/RES	I	System reset pin (low active). Built in pull up 10K ohms.
12	GND	P	Ground pin
13	IRO	O	IRO output pin. Direct sink (sink current: 100mA) for IR LED. Default value is high after reset. The IRO output pin is inverting bit0 of IRO Buffer. So, write “1” to bit0 of the IRO buffer the IRO is output “0” and write “0” to bit0 of the IRO buffer the IRO is output “1”.
18 ~ 25	P1.0 ~ P1.7	O	Output pins with open drain type. P1.4~P1.7 output pin with NMOS/CMOS selectable.
16 ~ 17	P2.0 ~ P2.1	O	Quasi-bi-directional NMOS output pins with pull high.
1 ~ 8	P0.0 ~ P0.7	I	Input ports with internal pull high and interrupt function.

Block Diagram



Function Description

Registers

	A
	Y
	X
	P
PCH	PCL
1	S

Accumulator
The accumulator is a general-purpose 8-bit register, which stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of two data words, which are used in these operations.

Index Register (X, Y)
There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address. When executing an instruction, which specifies indexed addressing, the CPU fetches the OP Code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-index of index address is possible.

Processor Status Register (P)
The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both the program and the CPU.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N	V	1	B	D	I	Z	C

N: Signed flag, 1 = negative, 0 = positive
V: Overflow flag, 1 = true, 0 = false
B: BRK interrupt command, 1 = BRK, 0 = IRQB
D: Decimal mode, 1 = true, 0 = false
I: IRQB disable flag, 1 = disable, 0 = enable
Z: Zero flag, 1 = true, 0 = false
C: Carry flag, 1 = true, 0 = false

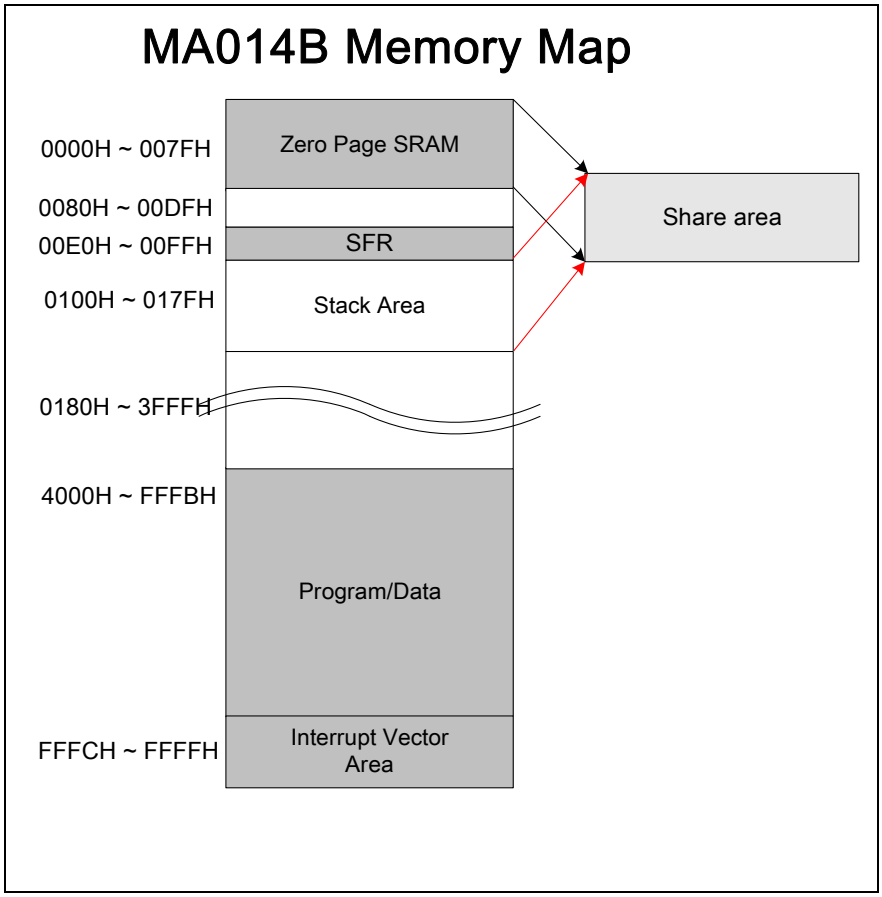
Program Counter (PC)
The 16-bit program counter register provides the addresses, which step the micro-controller through sequential program instructions. Each time the micro-controller fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order 8 bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

Stack Pointer (S)
The stack pointer is an 8-bit register, which is used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the micro-controller to perform stack manipulations under direction of either the program or interrupts (/IRQ). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer is initialized by the user's software.

Memory Map

There are 128 bytes SRAM in MA014B. They are working RAM (0000H to 007FH) and stacks (0100H to 017FH). The stack areas are shared with address 0000H to 007FH. The address 00E0H to 00FFH are special function registers area. Bit-manipulation instruction is available on SRAM except SFR.

There are 48K bytes program/data ROM in MA014B. The ROM address from 4000H to FFFFH can store program and data. The address mapping of MA014B is shown as below.



Low Voltage Reset:

The MA014B provides low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device is within the range 0.9V ~ V_{LVR} , such as changing a battery, the LVR will automatically reset the device internally.

The LVR includes the following specifications:

1. The low voltage (0.9V~V_{LVR}) has to remain in their original state to exceed 1ms. If the low voltage state does not exceed 1ms, the LVR will ignore it and do not perform a reset function.
2. In the LVR mode, the on-chip oscillator is stopped and the on-chip SRAM is held. Port1 set to high, port0 set to input mode with weakly pull high and IRO is output high.

Low Voltage Detector:

The low voltage detector (2.1V) has no de-bounce ability. When V_{DD} is equal or lower than LVD, the LVD flag to be set high immediately. De-bounce should be implemented by software.

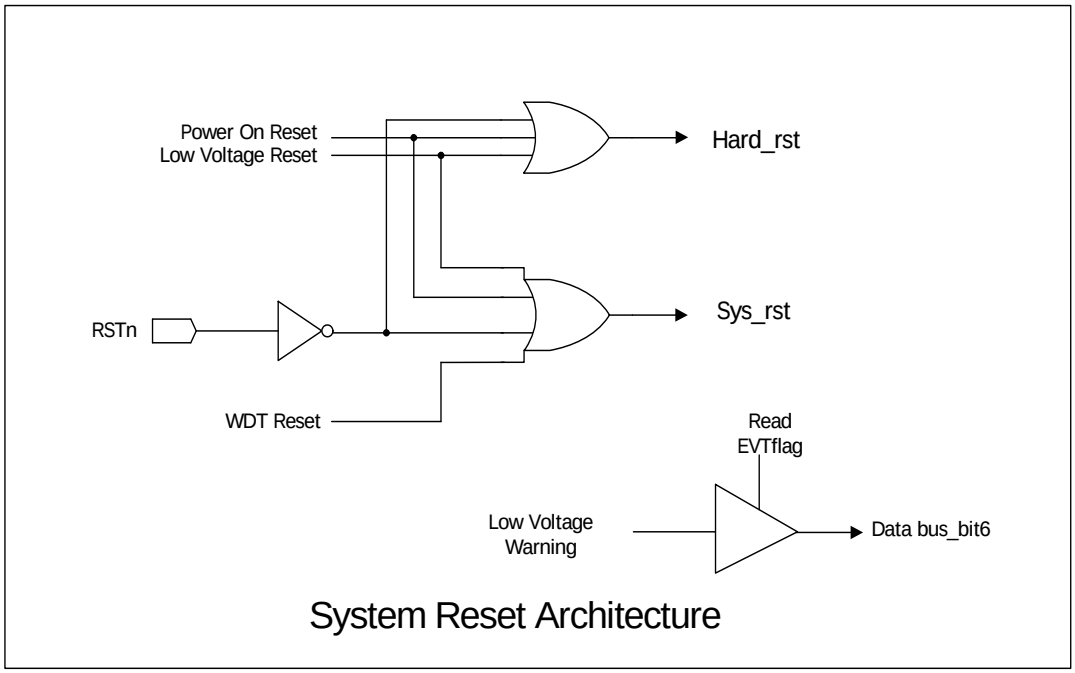
Special Function Register (SFR)

The address 00E0H to 00FFH are reserved for special function registers (SFR). The SFR is used to control or store the status of I/O, system clock and other peripheral.

※ All SFRs are not supported by bit-manipulation instructions.

SFR (special function register): 00E0H ~ 00FFH (page 0 area)

Address	Content	Default	Address	Content	Default
00E0	MCLKmgr	---0---0	00F0		--------
00E1	RESOK	--------	00F1	P0pad	XXXXXXXX
00E2	IRQen	---0---0	00F2		--------
00E3	EVTflag & EVTclr (Hard_rst)	-X00---0	00F3		--------
00E4		--------	00F4		--------
00E5		--------	00F5	P1obuf	11111111
00E6		--------	00F6	P1opd	1111----
00E7		--------	00F7	P1plh	00000000
00E8	TM0	00000000	00F8		--------
00E9	TM0_CTL	00000000	00F9		--------
00EA		--------	00FA	IRO	0-------
00EB		--------	00FB		--------
00EC		--------	00FC	P2obuf	------11
00ED		--------	00FD	P2pad	------XX
00EE		--------	00FE		--------
00EF		--------	00FF		--------



System Reset Architecture

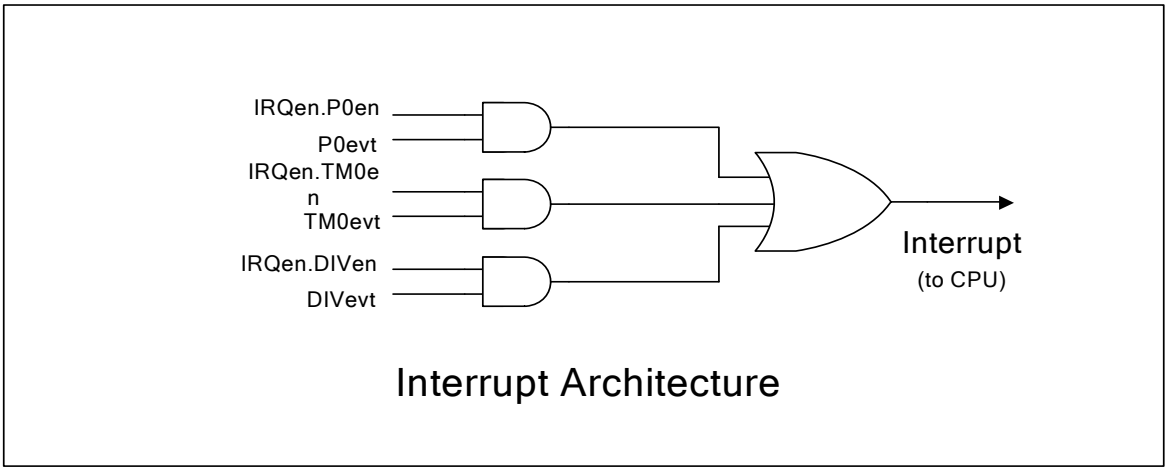
Interrupt

The MA014B provides 3 interrupt sources: port0, timer0 and divider. Each of the Interrupt sources can be individually enabled or disabled by setting or clearing a bit in the IRQen Three interrupts share the interrupt vector FFFEH/FFFFH.

DIV interrupt: IRQen.4 (DIVen) = 1 and DIVevt = 1.
P0 interrupt: IRQen.0 (P0en) = 1 and P0evt = 1.
TM0 interrupt IRQen.3 (TM0en) = 1 and TM0evt = 1.

Interrupt Vectors

Vector Address	Item	Flag	Properties	Memo
FFFCH, FFFDH	RESET	None	Ext.	Initial reset
"	WDT	WDTirq	Int.	Watchdog reset
"	LVR	None	Ext.	Low voltage reset
FFFEH, FFFFH	P0	P0irq	Ext.	Port P0 interrupt vector
"	DIV	DIVirq	Int.	Divider carry out interrupt
"	TM0	TM0irq	Int.	TM0 underflow interrupt



Interrupt Architecture

IRQ enable flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E2H	IRQen	-	-	-	DIVen	TM0en	-	-	P0en	-	√

Program can enable or disable the ability of triggering IRQ through this register.
0: Disable (default "0" at initialization)
1: Enable
P0en: Falling edge occurs at port 0 (input mode)
TM0en: Timer0 underflow occurred.
DIVen: DIV interrupt frequency occurred

IRQ status flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E3H	EVTflag	-	LVD	WDT	DIV	TM0	-	-	P0	√	-

When IRQ occurs, program can read this register to know which source triggering IRQ.

P0:P0 interrupt flag. Set by falling edge on any pin of port0. Clear by software.
DIV: Divider interrupts flag. Clear by software.
WDT: WDT time-out flag. Clear flag and WDT counter by software.
TM0: Timer0 underflow flag and the flag clear by software.

LVD: Low voltage detected. 1:V_{DD} is under 2.1V. 0:V_{DD} is above 2.1V. It is set by hardware and read only. (Note: The maximum LVD voltage will below 2.4V)

IRQ clear flag

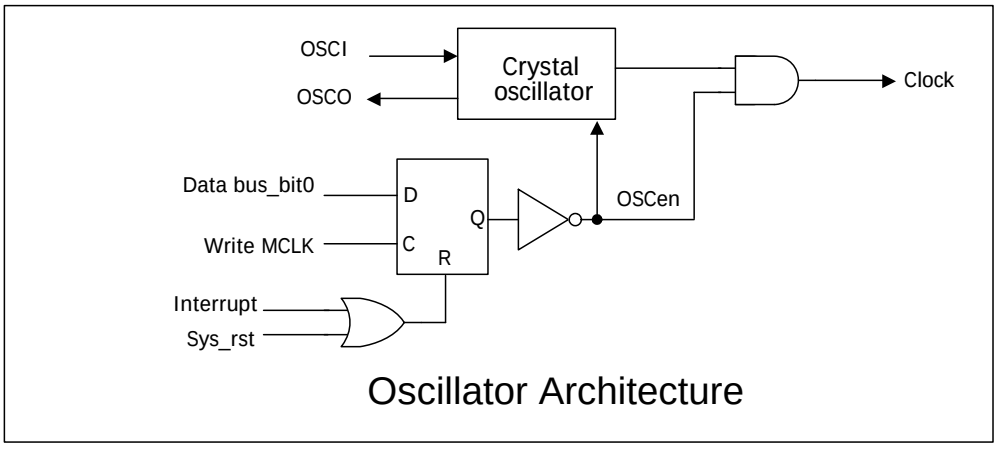
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E3H	EVTclr	-	-	WDT	DIV	TM0	-	-	P0	-	√

Program can clear the interrupt event by writing '0' into the corresponding bit.

Main Clock Manager

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E0H	MCLKmgr	-	-	-	DIVsel	-	-	-	OSCen	-	√

OSCen: 0:The oscillator is free run. 1:The oscillator is frozen (stop mode).
When system clocks stop oscillating. The uC can be awakened from stop mode by 3-ways: port 0 interrupt, hardware reset, or power-on reset.
DIVsel: Divider interrupt frequency selector
0: The Fosc/4096 interrupt frequency is selected
1: The Fosc/256 interrupt frequency is selected



Oscillator Architecture

Reset OK

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E1H	RESOK	RK7	RK6	RK5	RK4	-	-	-	-	-	√

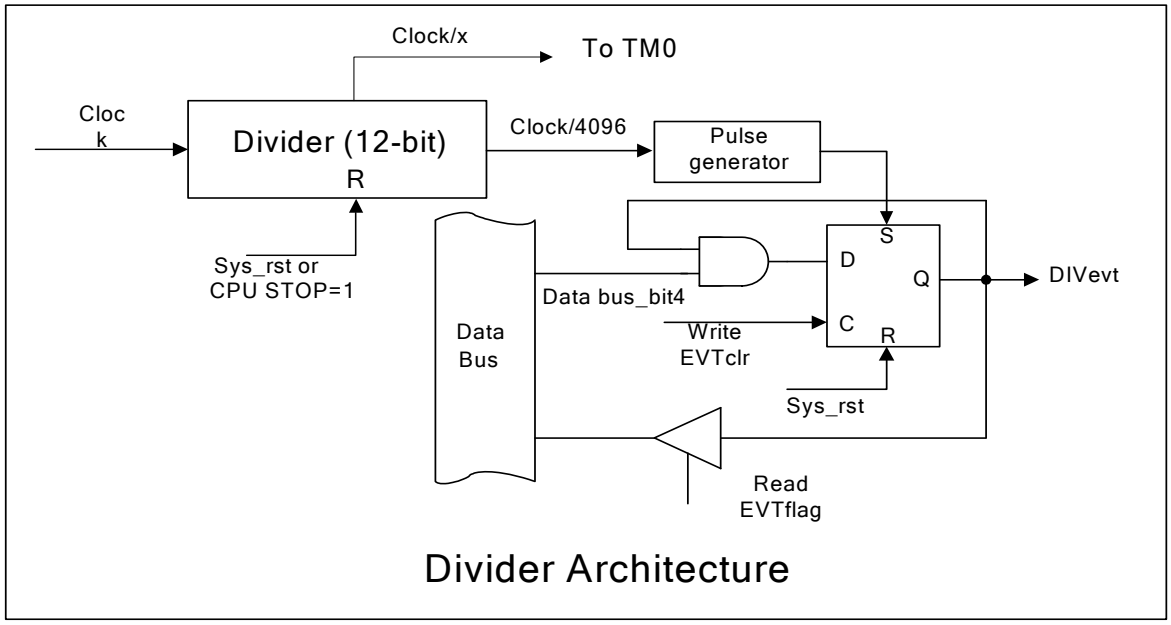
RESOK (Reset OK): If the device reset OK and work well, **must** write #$90 into this register.
For example:

```
Program_start:    LDA    #10010000b
                  STA    $E1
```

Divider (The example is base on 3. 579545MHz) **Unite:Hz**

Name	/256	/128	/64	/32	/16	/8	/4	/2	R	W
DIVlow	13984	227968	55937	111875	223750	447500	895000	1790000	-	-
Name					/4096	/2048	/1024	/512	R	W
DIVhigh	-	-	-	-	874	1748	3496	6992	-	-

The time-out period is obtained by the equation: 4096/OSC.
The DIV flag will be set when 4096/OSC or 256 /OSC (selected by DIVsel) is met.

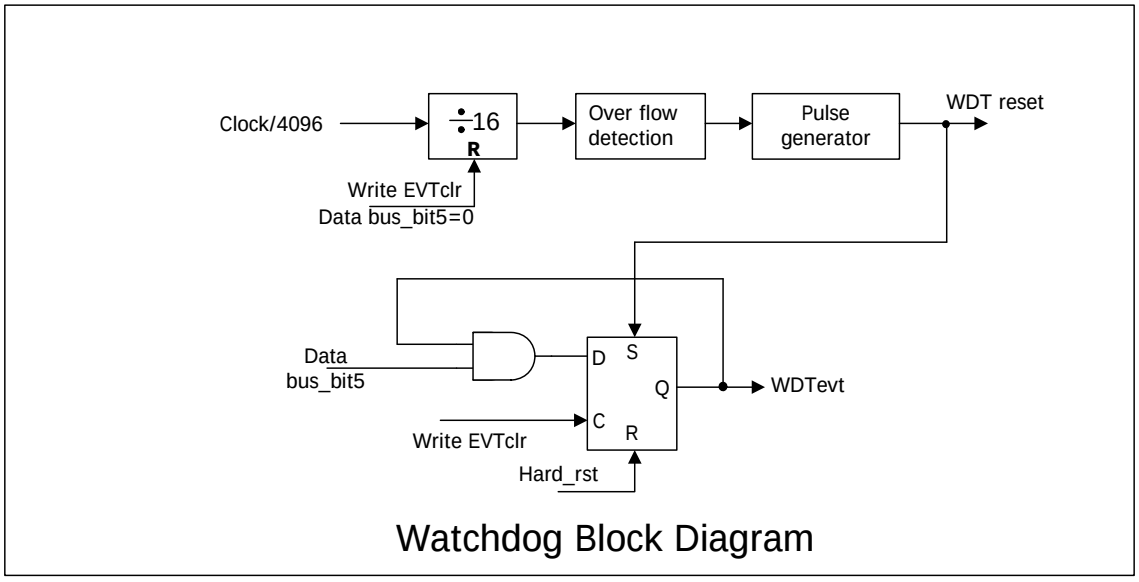


Divider Architecture

Watchdog Timer (WDT, The example is base on 3.579545MHz) **Unite:Hz**

Name					(F_{OSC} /4096)/16				R	W
WDT	-	-	-	-	55	109	218	437	-	-

The watchdog timer time-out period is obtained by the equation: (F_{OSC} / 4096)/16
Before watchdog timer time-out occurs, the program must clear the 4-bit WDT timer by writing 0 to EVTclr.5. WDT overflow will cause system reset and set EVTflag.5 to high.



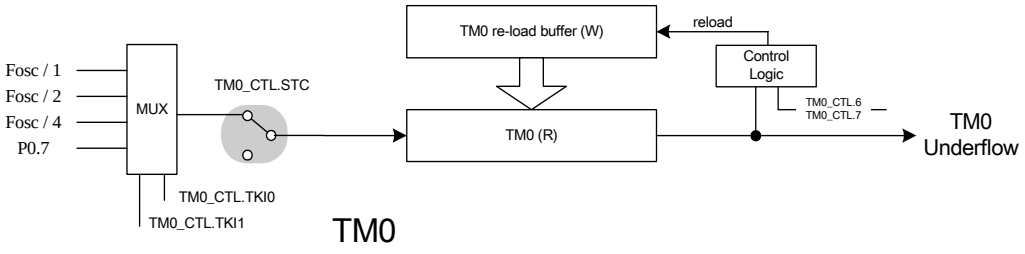
Watchdog Block Diagram

Timer0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E8H	TM0	T7	T6	T5	T4	T3	T2	T1	T0		√
00E9H	TM0_CTL	STC	RL/S	TKES	-	-	-	TKI1	TKI0		√

STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock (set this bit to 1 will be ignored when this bit already set to 1)
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload
TKES: Event or series input clock-in trigger edge selector; 0: rising edge, 1: falling edge

TKI1	TKI0	Selected TM0 input clock source
0	0	Fosc / 1
0	1	Fosc / 2
1	0	Fosc / 4
1	1	P0.7



I/O Ports

Port 0 Pad

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F1H	P0pad	P07	P06	P05	P04	P03	P02	P01	P00	√	-

Port 0 is an 8-bit input port with pull high resistors. Reading P0pad.n would always read the logic value from pad.

Port 1 Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F5H	P1obuf	P17	P16	P15	P14	P13	P12	P11	P10	-	√

Port 1 is an 8-bit output port with selectable pull-high resistors. This register is used to buffer the out value of P1.0 ~ P1.7 and it is write-only. **The pull-high resistors will be temporarily disable if the output value is low.**

※ Bit-manipulation instructions are not available on this register.

Port 1 Open-Drain Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F6H	P1opd	OD7	OD6	OD5	OD4	-	-	-	-	-	√

0: Disable open-drain output (CMOS output), 1: Enable open-drain output

OD4 ~ OD7: These control bits are used to enable the open-drain of P1.4 ~ P1.7 pin.

※ Bit-manipulation instructions are not available on this register.

Port 1 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F7H	P1plh	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	-	√

0: Disable internal pull-high, 1: Enable internal pull-high

PH0 ~ PH7: These control bits are used to enable the pull-high of P1.0 ~ P1.7 pin.

※ Bit-manipulation instructions are not available on this register.

Port 2 Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FCH	P2obuf	-	-	-	-	-	-	P21	P20	-	√

Port 2 is a 2-bit quasi-bi-directional open drain output port with internal pull-high resistors. This register is used to buffer the out value of P2.0 ~ P2.1 and it is write-only. Reading from the P2obuf would always read “0” from buffer. **The pull-high resistors will be temporarily disable if the output value is low.**

※ Bit-manipulation instructions are not available on this register.

Port 2 pad

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FDH	P2pad	-	-	-	-	-	-	P21	P20	√	-

When P2 is used as an input, the corresponding bit of P2obuf must be 1. In this condition, the corresponding pin is pulled to high by the internal pull-high resistor and it can be pulled to low by an external source. Reading P2pad.n would always read the logic value from pad.

※ Bit-manipulation instructions are not available on this register.

IRO Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FAH	IRO	IR	-	-	-	-	-	-	-	-	√

Note: The IRO pin output status is the inverted value of IRO.7. So, write “1” to bit7 of the IRO buffer the IRO will output low voltage and write “0” to bit7 of the IR buffer the IRO will output high voltage.

Programming Notice

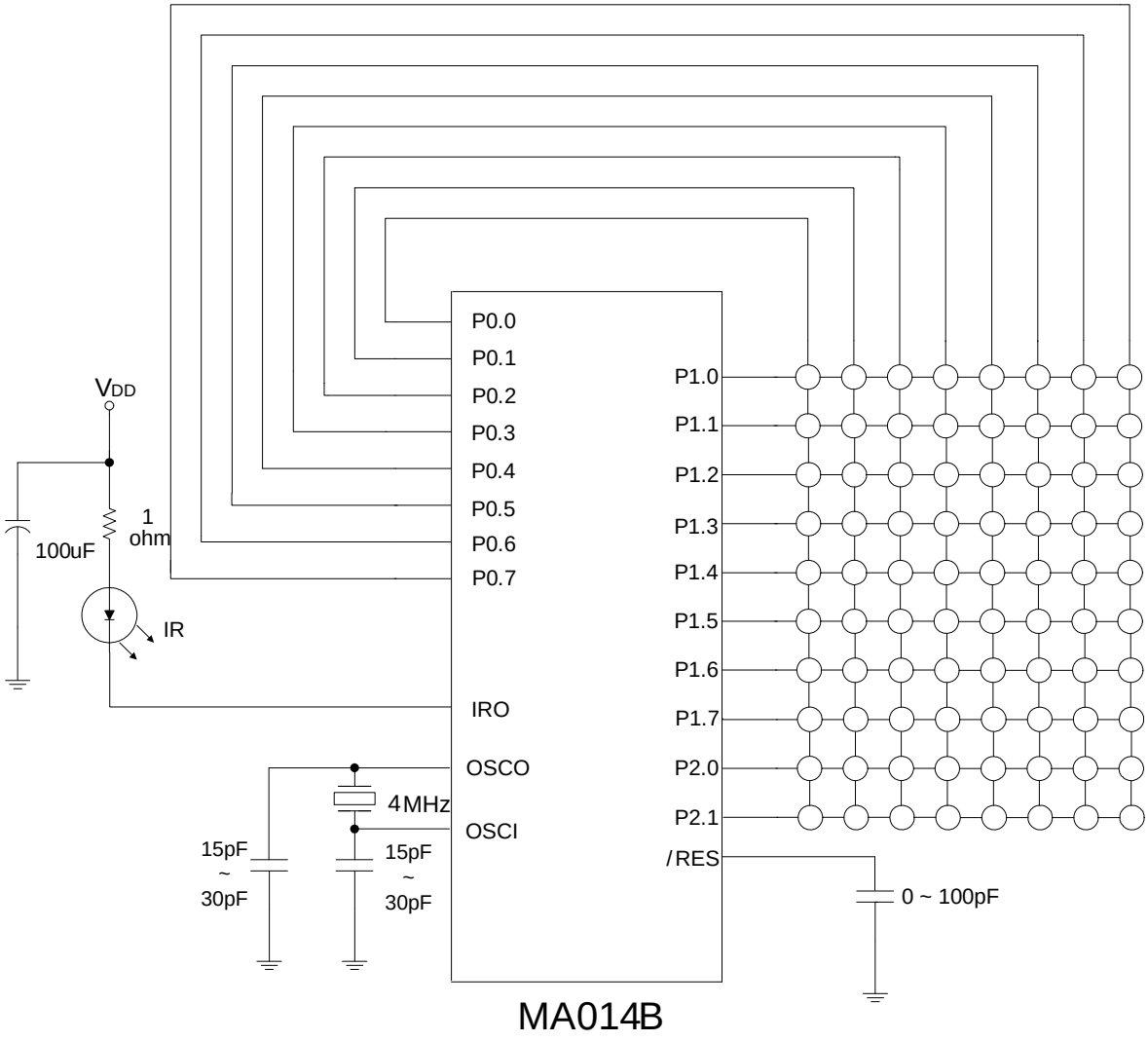
The status after different reset condition is listed below:

	Power on reset	**CPU /RES pin reset**
SRAM Data	Unknown	Unchanged
CPU Register	Unknown	Unknown
Special Function Register	Default value	Default value

Mask Option

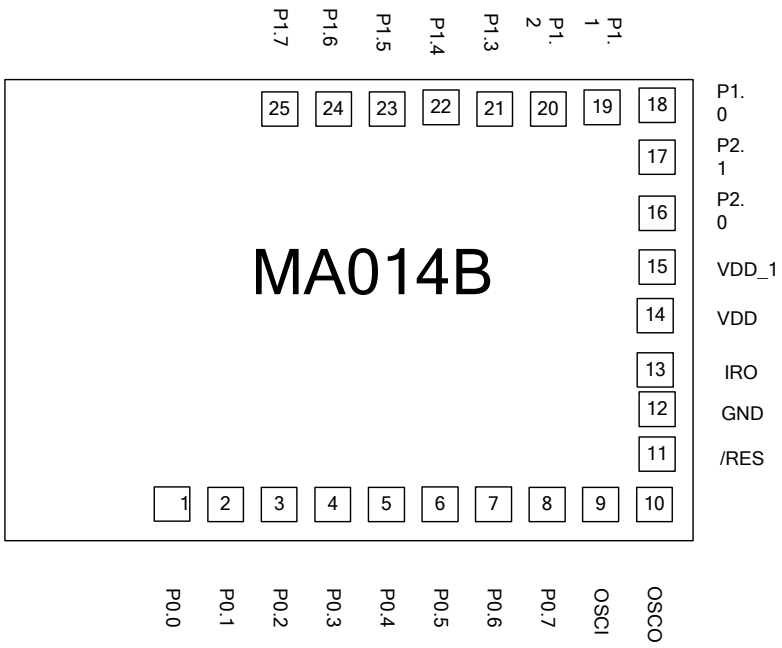
WDT	Enable / Disable

Application Circuit



Note: No capacitor or below 100pF capacitor is strongly recommended to connected on /RES pin.

Pad Assignment



Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	VSS-0.3 to VSS+4.0	V
Applied Input / Output Voltage	VSS-0.3 to VDD+0.3	V
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-50 to +125	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Characteristics

(V_{DD}-GND = 3.0 V, F_{OSC} = 4MHz, Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V_{DD}	When LVR is disabled	1.7	-	3.6	V
Op. Current	I_{OP}	No load (Ext.-V) In normal operation	-	1.3	5	mA
Standby Current	I_{STB}	No load (Ext.-V)	-	1	3	μA
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	-	0	-	0.3V_{DD}	V
Port 1.4~1.7 Drive Current	I_{OH0}	V_{OH} = 2.7V, V_{DD} = 3.0V (CMOS output mode)	7.0	-	-	mA
Port 1.0~1.7, Port 2.0~2.1 Sink Current	I_{OL0}	V_{OL} = 0.4V, V_{DD} = 3.0V	10.0	-	-	mA
IRO Drive Current	I_{OH2}	V_{OH} = 2.7V, V_{DD} = 3.0V	10.0	-	-	mA
IRO Sink Current	I_{OL2}	V_{OL} = 0.4V, V_{DD} = 3.0V	100.0	-	-	mA
P0/P1/P2 Pull-high Resistor	R_{PH}	V_{IL} = 0V	-	100K	-	Ω
/RES Pull-high Resistor	R_{RES}	V_{IL} = 0V	-	20K	-	Ω
Low Voltage Detector	V_{LVD}	V_{DD} > 2.1V	-	-	2.40	V
Low Voltage Reset	V_{LVR}	-	-	-	2.05	V

AC Characteristics

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CPU Op. Frequency	F_{CPU}	V_{DD} = 3.0V	0.4	4	8	MHz
System Start-Up Time	T_{SST}	Power-up, reset or wake-up from STOP mode	-	2048	-	1/ F_{CPU}

History:

Ver 0.10: MA014B original version
Ver 0.11: Modified the logic structure as MA011B
Ver 0.12: Modified the SFR initial value (typing error)
Ver 0.14: Modified MA014B function is compatible with MA011C
Ver 0.15: Modify I/O port. Add P2.0~ P2.1
Ver 0.16: Modify P2 function
Ver 0.17: Modify P2 pull-high resistance from 10K to 100K
Ver 0.18: Add TM0
Ver 0.19: Modify the PAD number
Ver 0.20: Modify the DC Characteristics
Ver 0.21: Bit-manipulation instructions are available on the P0pad register, modify the application circuit and DC characteristics.