Version: 2.00

MA015

Data Sheet

8-Bit Micro-Controller with IR function

Version 2.00

Table of Contents

1 Features

- Single Chip 8-bit CPU
- Memory
  - ROM (shared by program and data) : 128K Bytes
  - Data RAM : 320 Bytes
- Operating voltage: 1.8V to 3.6V
- 31 input/output pins with 15 input pins with wake-up function.
  - Port 0 and Port 3 I/O pins with input wake-up function.
  - Ports 1.3, P1.6 and P1.7 are multi-function with Timer 0, Timer 1 and Timer 2 carry out.
  - Port 3.6 can be clock source of timer.
- Two power-down modes for saving power consumption:
  - Halt mode: micro-controller no operation (main- oscillator still oscillating)
  - Stop mode: micro-controller no operation (all oscillators stop oscillating)
- Three re-loadable 16-bit countdown timers with interrupt function.
- Build-in watchdog timer
- Build-in low voltage detector (2.2V), low voltage reset (typical voltage: 1.8V)
- Oscillator
  - Single clock
  - Main oscillator operation at crystal or RC mode is selected by mask option
  - Crystal/Ceramic oscillator up to 4MHz @ 1.8V

Selection Information

	MA015
ROM (Program ROM)	128K x 8-bit (32K x 8-bit)
I/O	32

1.1 Application Field

General IR controller, Toy controller

2 General Description

MA015 integrates an 8-bit CPU core, SRAM, timer and system control circuits by a CMOS silicon gate technology. The ROM can store both data table and program.

Thirty-one I/O pins can be used for keypad control, motor control, IR application, LED indicators or communication with other systems.

This chip is very suitable for IR application or other serial control application.

3 Pin Configurations

3.1 Pad Assignment

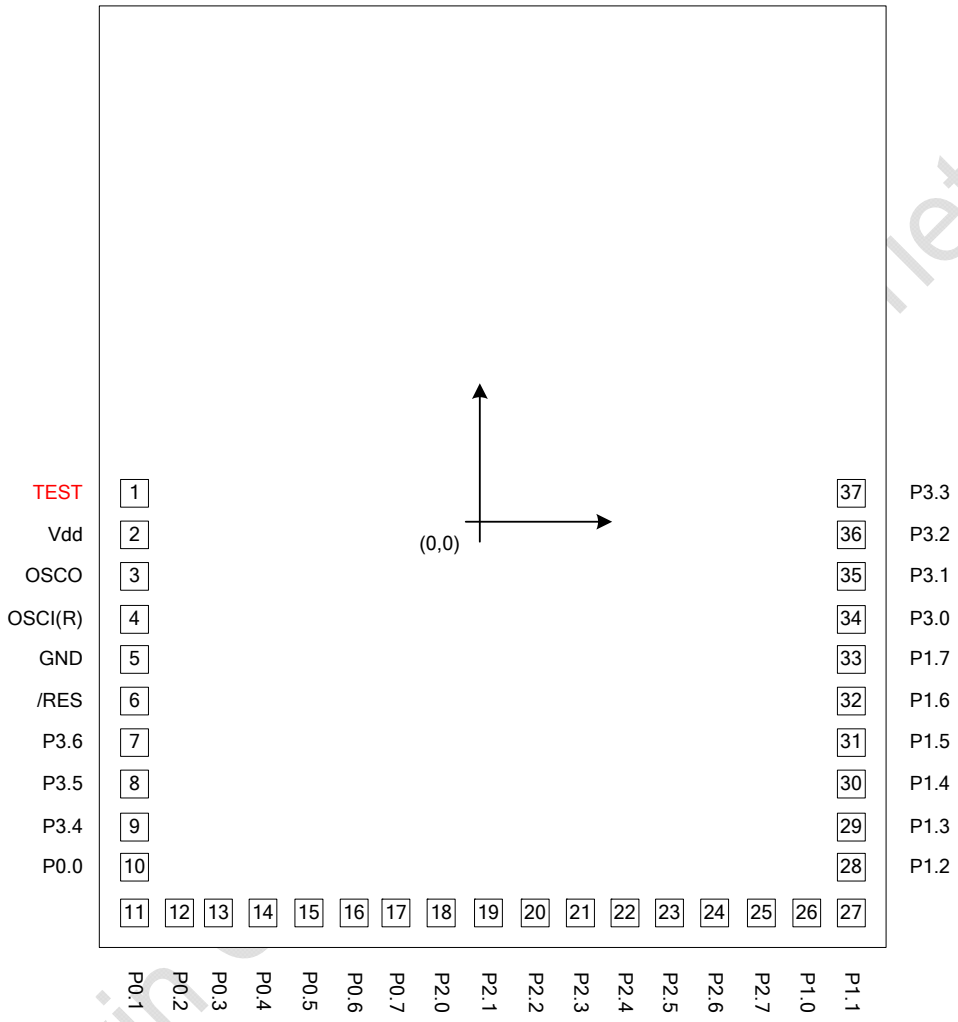


Figure 3-1 Pad Assignment

3.2 Pin Description

Table 3-1 Pin Description

Pad No.	Pad Name	I/O	Description
5	GND	P	Ground pin
2	V_{DD}	P	Positive power pins
3, 4	OSCO, OSCI	O, I	RC or crystal oscillator pins
6	/RES	I	System reset pin (low active)
1	TEST	-	For test mode only.
7~ 9	P3.6 ~ P3.4	I/O	Programmable I/O ports with interrupt function. Port 3.6 can be clock source of timer.
33 ~ 36	P3.0 ~ P3.3	I/O	Programmable I/O ports with interrupt function.
10 ~ 17	P0.0 ~ P0.7	I/O	Programmable I/O ports with interrupt function.
18 ~ 25	P1.0 ~ P1.7	I/O	Programmable I/O ports. Port 1.3 is multi-function with Timer 0 carry out. Port 1.6 is multi-function with Timer 1 carry out. Port 1.7 is multi-function with Timer 2 carry out.
26 ~ 33	P2.0 ~ P2.7	I/O	Programmable I/O ports.

Note: In the “Type” field,
“I” means input only.
“O” means output only.
“B” means bi-direction.
“P” means Power, “G” means Ground.

4 Block Diagram

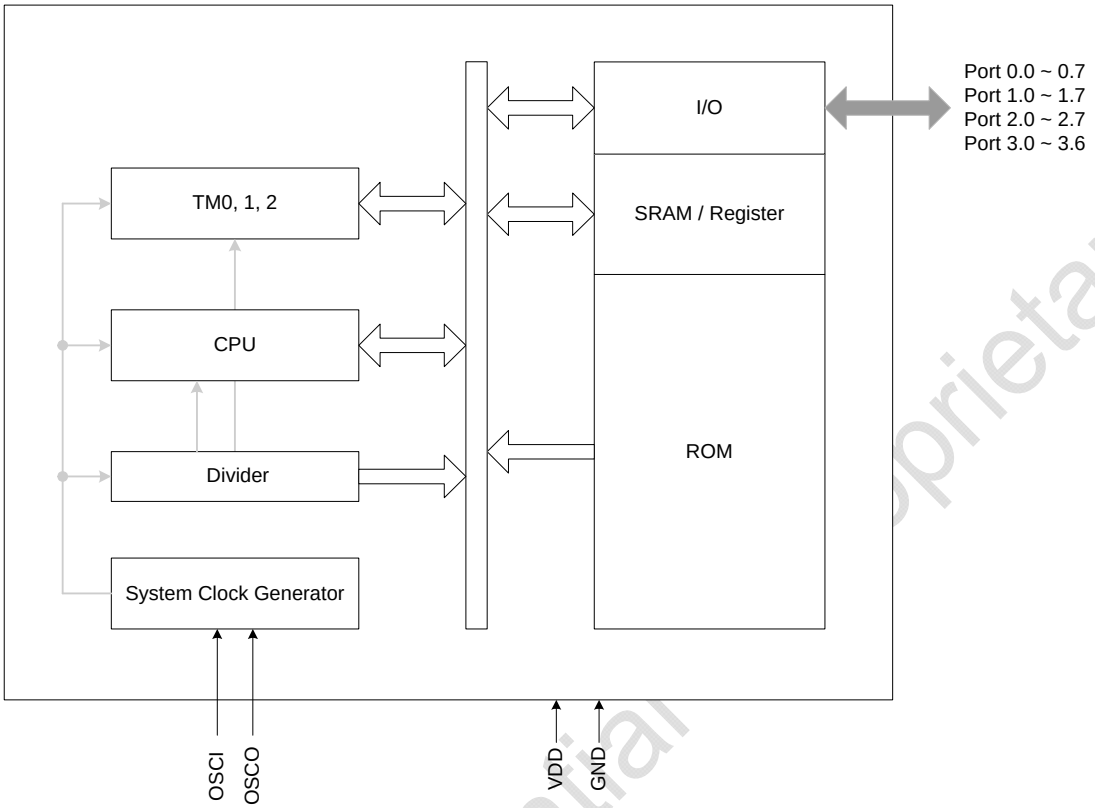


Figure 4-1 Block Diagram

5 Function Description

5.1 Registers

	A
	Y
	X
	P
PCH	PCL
1	S

5.2 Accumulator

The accumulator is a general-purpose 8-bit register, which stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of two data words used in these operations.

5.3 Index Register(X,Y)

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address. When executing an instruction, which specifies indexed addressing, the CPU fetches the OP Code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-index of index address is possible.

5.4 Processor Status Register

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both the program and the CPU.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N	V	1	B	D	I	Z	C

N: Signed flag, 1 = negative, 0 = positive
V: Overflow flag, 1 = true, 0 = false
B: BRK interrupt command, 1 = BRK, 0 = IRQB
D: Decimal mode, 1 = true, 0 = false
I: IRQB disable flag, 1 = disable, 0 = enable
Z: Zero flag, 1 = true, 0 = false
C: Carry flag, 1 = true, 0 = false

5.5 Program Counter(PC)

The 16-bit program counter register provides the addresses, which step the micro-controller through sequential program instructions. Each time the micro-controller fetch an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order 8 bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

5.6 Stack Point(S)

The stack pointer is an 8-bit register, which is used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the micro-controller to perform stack manipulations under direction of either the program or interrupts (/NMI or /IRQ). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer is initialized by the user's firmware.

6 Memory Organization

There are 320 bytes SRAM in MA015. They are working RAM (0000H to 00BFH), stacks (01C0H to 01FFH) and general purpose RAM (0200H to 023FH). The address 0100H to 1BFH are shared with address 0000H to 00BFH. The address 00C0H to 00FFH are special function registers area.

There are 128K bytes program/data ROM in MA015. It is combined with 32K program/data ROM and bank switching data ROM. The ROM address from 8000H to FFEDH can store program and other data. There are six banks in MA015 that is index by SFR. The default bank number is 00H after power on or reset. The bank select function, ranged from 4000H to 7FFFH (16Kbyte/bank), is used for extending memories if the ROM size is more than 32K bytes in MA015. The address mapping of MA015 is shown as below.

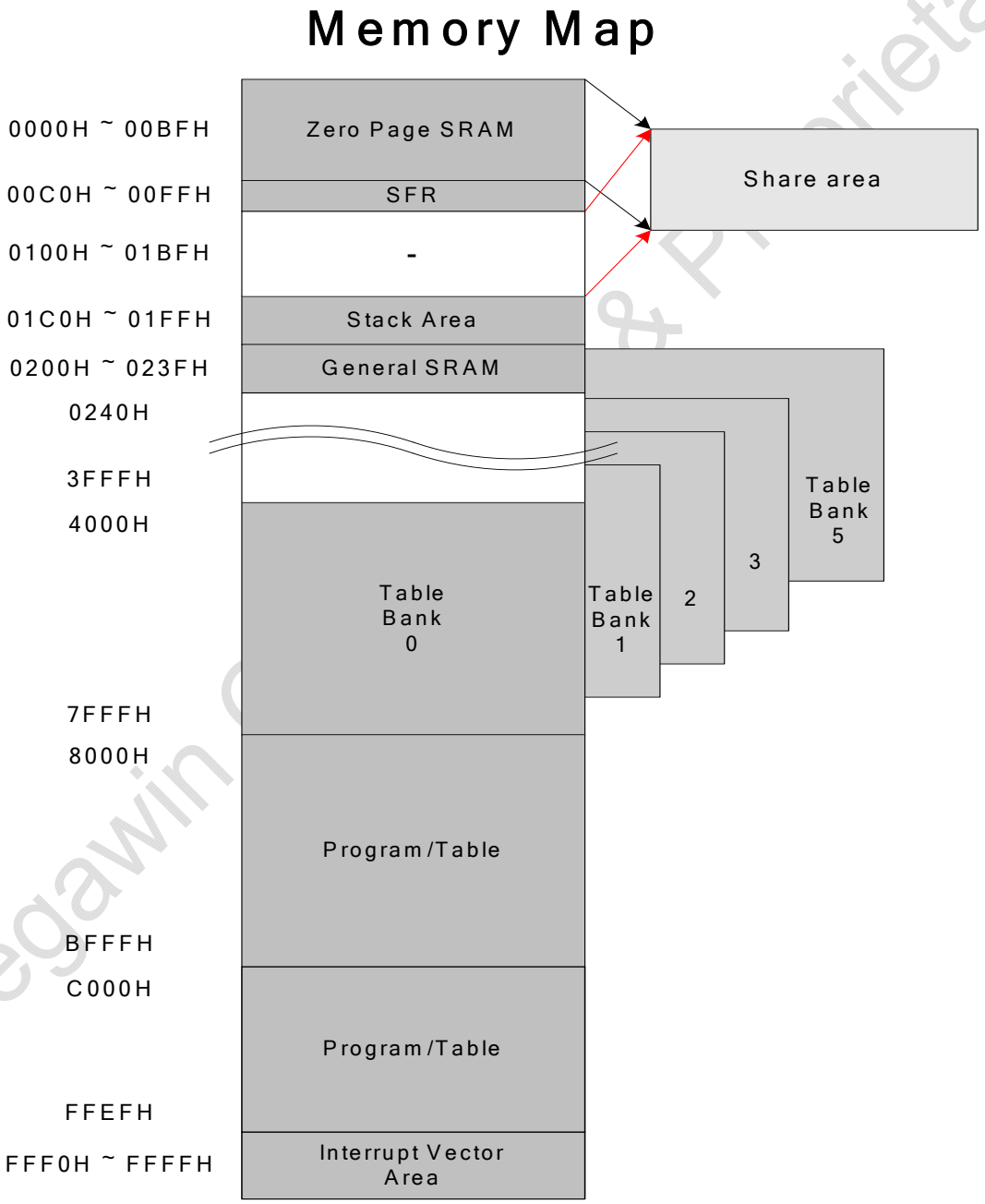


Figure 6-1 Memory Map

6.1 SFR Mapping

The address 00C0H to 00FFH are reserved for special function registers (SFR). The SFR is used to control or store the status of I/O, timers, system clock and other peripheral.

※ All SFRs are not supported by bit-manipulation instructions.

Table 6-1 SFR Table

SFR (special function register): 00C0H~00FFH

Address	Content	Default	Address	Content	Default
00C0	IRQ_EN	---0 000-	00D0	TM2L	0000 0000
00C1	IRQ_ST / IRQ_CLR	---0 000X	00D1	TM2H	0000 0000
00C2		---- ----	00D2	TM2_CTL	000- -000
00C3	RESOK	---- ----	00D3		---- ----
00C4	WDT_CTL	0--- -000	00D4		---- ----
00C5	PWR_CR	---- --00	00D5	BANK	---- -000
00C6	RLH_EN	---0 000-	00D6		---- ----
00C7		---- ----	00D7		---- ----
00C8	TM0L	0000 0000	00D8		---- ----
00C9	TM0H	0000 0000	00D9		---- ----
00CA	TM0_CTL	000- -000	00DA		---- ----
00CB		---- ----	00DB		---- ----
00CC	TM1L	0000 0000	00DC		---- ----
00CD	TM1H	0000 0000	00DD		---- ----
00CE	TM1_CTL	000- -000	00DE		---- ----
00CF		---- ----	00DF		---- ----

Address	Content	Default	Address	Content	Default
00E0	P0	0000 0000	00F0		---- ----
00E1	P0CR	0000 0000	00F1		---- ----
00E2	P0MR	--00 --00	00F2		---- ----
00E3	P0IEN	0000 0000	00F3		---- ----
00E4	P1	0000 0000	00F4		---- ----
00E5	P1CR	0000 0000	00F5		---- ----
00E6	P1MR	--00 --00	00F6		---- ----
00E7	P1_MFR	00-- 0---	00F7		---- ----
00E8	P2	0000 0000	00F8		---- ----
00E9	P2CR	0000 0000	00F9		---- ----
00EA	P2MR	--00 --00	00FA		---- ----
00EB		---- ----	00FB		---- ----
00EC	P3	-000 0000	00FC		---- ----
00ED	P3CR	-000 0000	00FD		---- ----
00EE	P3MR	--00 --00	00FE		---- ----
00EF	P3IEN	-000 0000	00FF		---- ----

7 System Control Registers

Bank select

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D5H	BANK	-	-	-	-	-	BK2	BK1	BK0	√	√

Program can switch the memory bank through this register. After power on reset, this register in initialized as 00H. The maximum bank numbers in MA015 is show as below:

Part No.	MA015
Max. Bank	101b
Inhibited	110b, 111b

8 Interrupt

There are four kinds of interrupt sources are provided in MA015. The flag IRQ_EN and IRQ_ST are used to control the interrupts. When flag IRQ_ST is set to '1' by hardware and the corresponding bits of flag IRQ_EN has been set by software, an interrupt is generated. When an interrupt occurs, all of the interrupts are inhibited until the CLI or STA IRQ_EN, #I instruction is invoked. Executing the SEI instruction can also disable the interrupts.

Table 8-1 Interrupt Vector Table

Vector Address	Item	Priority	Properties	Memo
FFFEH, FFFFH	-	-	-	Reserve
FFFCH, FFFDH	PAD RESET	1	Ext.	Initial reset
FFFCH, FFFDH	LVR	1	Int.	Initial reset
FFFCH, FFFDH	POR	1	Int.	Initial reset
FFFCH, FFFDH	WDT	1	Int.	Initial reset
FFFCH, FFFDH	RESET OK	1	Int.	Initial reset
FFFAH, FFFBH	-	-	-	Reserve
FFF8H, FFF9H	-	-	-	Reserve
FFF6H, FFF7H	TM0	2	Int.	Timer 0 overflow interrupt
FFF4H, FFF5H	Port	3	Ext.	Port P0, P3 interrupt vector
FFF2H, FFF3H	TM1	4	Int.	Timer 1 overflow interrupt
FFF1H, FFF0H	TM2	5	Int.	Timer 2 overflow interrupt

8.1 Interrupt Register

IRQ enable flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C0H	IRQ_EN	-	-	-	TM2	TM1	Port	TM0	-	-	√

Program can enable or disable the ability of triggering IRQ through this register.
0: Disable (default "0" at initialization)
1: Enable
Port: Raising or falling edge occurs at port 0 (or port 3) input mode.
TM0, TM1, TM2: Timer 0/1/2 underflow

IRQ status flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C1H	IRQ_ST	-	-	-	TM2	TM1	Port	TM0	LVD	√	-

When IRQ occurs, program can read this register to know which source triggering IRQ.

LVD flag:
The Low Voltage Detector has no de-bounce ability. When V_{DD} is equal or lower than the condition of LVD, the LVD flag will be set to high immediately. De-bounce could be implement by firmware. The LVD flag has not interrupt ability and set by hardware. When V_{DD} is higher than the condition of LVD, the LVD flag will be clear by hardware.

IRQ clear flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C1H	IRQ_CLR	-	-	-	TM2	TM1	Port	TM0	LVD	-	√

Program can clear the interrupt event by writing '1' into the corresponding bit (except LVD bit).

8.2 Interrupt System

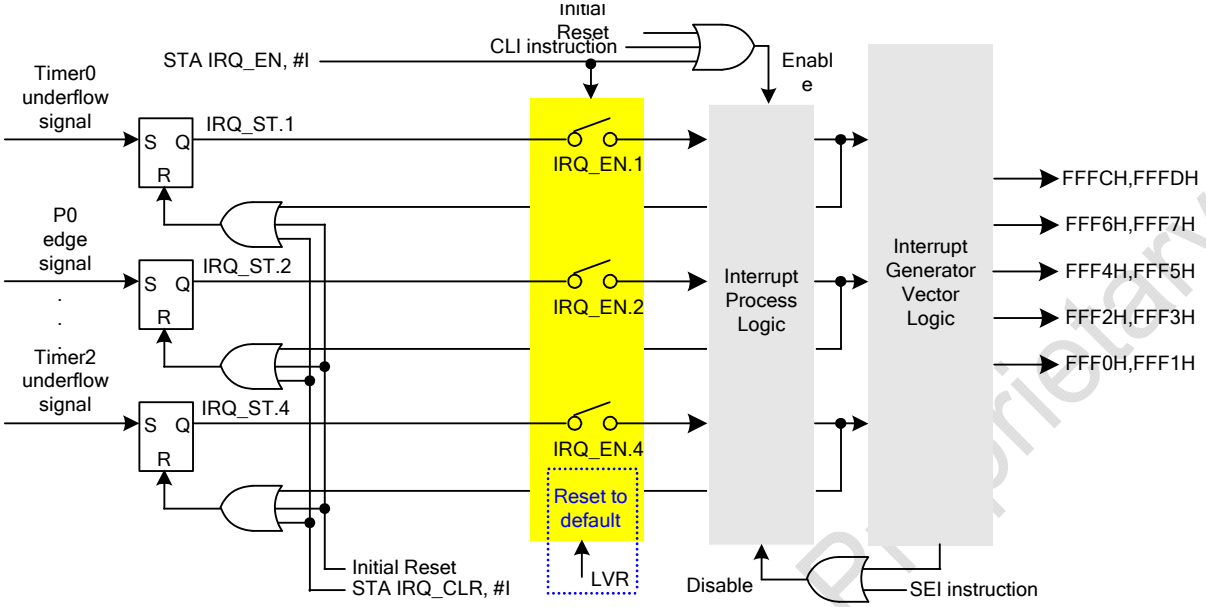


Figure 8-1 Interrupt System Diagram

9 Reset

9.1 Low Voltage Reset (LVR)

The MA015 provides low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device is within the range of 0.9V ~ VLVR (such as changing the battery), the LVR will automatically reset the device internally.

In the LVR active period, the on-chip oscillator is stopped. All I/O port will be set as **input tri-state mode** and the leakage current will below 0.1 μA. If an external capacitor (example: 47μF) is connected between V_{DD} and GND in this condition, the contents of on-chip RAM will be kept.

9.2 Watchdog Timer (WDT)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C4H	WDT_CTL	RSTS	-	-	-	-	-	-	-	√	-
		CLR	-	-	-	-	RSEL	CKI1	CKI0	-	√

RSTS: WDT reset status, set by hardware when WDT overflows and clear by hardware reset or set WDT_CLR.7 to one (this bit is read only)
RSEL: WDT reset selector, = 0 Reset whole chip except RSTS (WDT_CTL.7)
= 1 Reset PC and IRQ_EN only
CKI1, CKI0: WDT clock selector, = 00 Fosc / (131072*16) selected (1.90Hz = 526ms @ Fosc = 4MHz)
= 01 Fosc / (65536*16) selected (3.81Hz = 262ms @ Fosc = 4MHz)
= 10 Fosc / (32768*16) selected (7.63Hz = 131ms @ Fosc = 4MHz)
= 11 Fosc / (16384*16) selected (15.26Hz = 65.5ms @ Fosc = 4MHz)
CLR: RSTS clear control bit, program can clear RSTS by program "1" into this bit (this bit is write only)

The watchdog timer (WDT), which is organized as a 4-bit counter, is designed to prevent the program from unknown errors. The WDT is enabling by code option. If the WDT overflows, the WDT reset function will be performed. The watchdog timer control register (WDT_CTL) controls the WDT reset function. RSTS (WDT_CTL.7) is set by hardware when the WDT overflows and is cleared by store one to the bit 7 of WDT_CLR register or hardware reset. There are two types of WDT reset, which is selected by RSEL (bit2 of WDT_CTL). WDT overflow will cause two types reset depending on the setting of RSEL — if RSEL is equal to 0, the reset is the same as hardware reset except the setting of WDT_CTL and WDT_CLR; If RSEL is equal to 1, the reset only acts on program counter (PC) and IRQ_EN. The WDT clock frequency is decided by bit1 and bit0 of WDT_CTL register. Store one to the bit 7 of WDT_CLR register will also reset the contents of the WDT. In normal operation, the application program must reset WDT before it overflows. The organization of the divider1 and watchdog timer is shown as below.

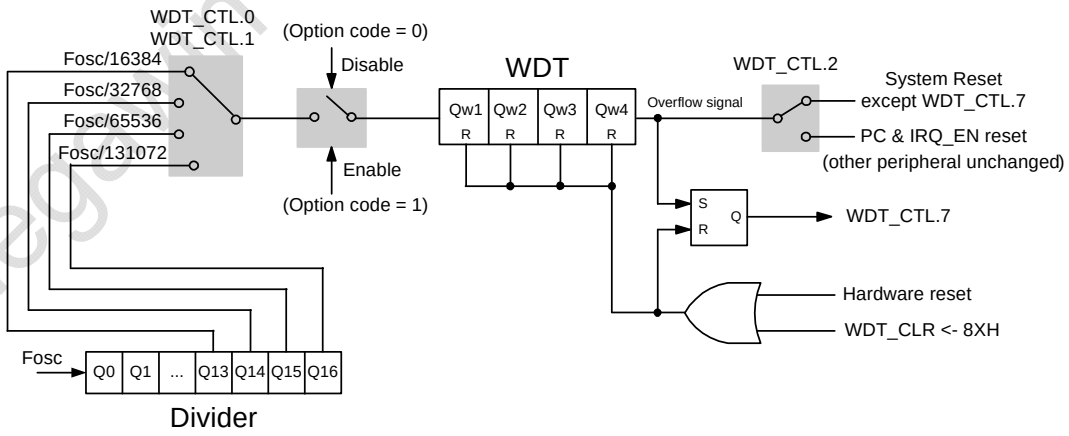


Figure 9-1 Watch Dog Diagram

9.3 Reset OK

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C3H	RESOK	RK7	RK6	RK5	RK4	-	-	-	-	-	√

RESOK (Reset OK): If the device reset OK and work well, **must** write #$90 into this register at program start.
The RESOK is enabling by code option.
For example:

```
Program_start:    LDA   #10010000b
                  STA   $C3
```

Programming Notice
The status after different reset condition is listed below:

	Power on reset	CPU /RST pin reset
SRAM Data	Unknown	Unchanged
CPU Register	Unknown	Unknown
Special Function Register	Default value	Default value

10 Power Control

10.1 Power Control Register

Power saving control

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C5H	PWR_CR	-	-	-	-	-	-	CKC0	HALT	-	√

CKC0	System clock control
0	F_{OSC} enable, (Normal mode)
1	F_{OSC} disable, (Stop mode)

HALT: F_{CPU} off-line control bit. 1: F_{CPU} off-line, 0: F_{CPU} on-line

Program can switch the normal operation mode to the power-saving mode for saving power consumption through this register. There are two power saving modes in this system.

Stop mode: *(PWR_CR.CKC0 = 1)*
All system clocks stop oscillating. The uC can be awakened from stop mode by 3-ways: Port interrupt, hardware reset, or power-on reset.

Halt mode: *(PWR_CR.HALT = 1)*
The F_{CPU} clock in off-line status. The oscillator still oscillating if the PWR_CR.CKC0 keep low. The uC can be awakened from halt mode by 3-ways: all interrupt events (Timer 0, Timer 1, Timer 2, Port), hardware reset, or power-on reset.

Release halt mode enable flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C6H	RLH_EN	-	-	-	TM2	TM1	Port	TM0	-	-	√

Set IRQ_CLR register to clear the halt release event.

Release halt status flag is the IRQ_ST register.

11 Timer

11.1 Timer0

Timer0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C8H	TM0L	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00C9H	TM0H	T15	T14	T13	T12	T11	T10	T9	T8	√	√
00CAH	TM0_CTL	STC	RL/S	TKES	-	-	TKI2	TKI1	TKI0	√	√

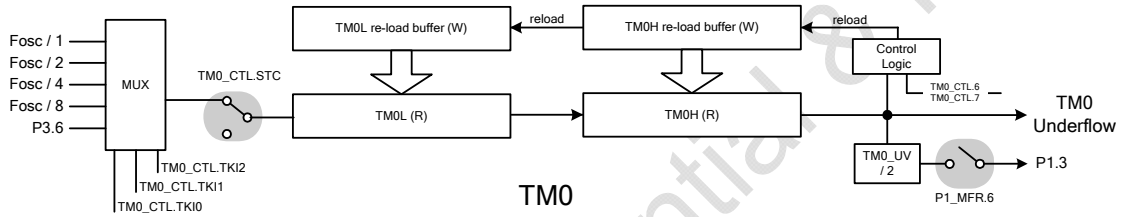
Timer 0 is a 16-bit **down-count** counter. The counter underflow frequency of Timer 0 can be calculated with the equation: $F_{TM0\_UV} = F_{TM0} / (TM0+1)$

STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock (set this bit to 1 will be ignored when this bit already set to 1)

RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload

TKES: Event or series input clock-in trigger edge selector; 0: rising edge, 1: falling edge

TKI2	TKI1	TKI0	Selected TM0 input clock source
0	0	0	Fosc / 1
0	0	1	Fosc / 2
0	1	0	Fosc / 4
0	1	1	Fosc / 8
1	0	0	P3.6



11.2 Timer1

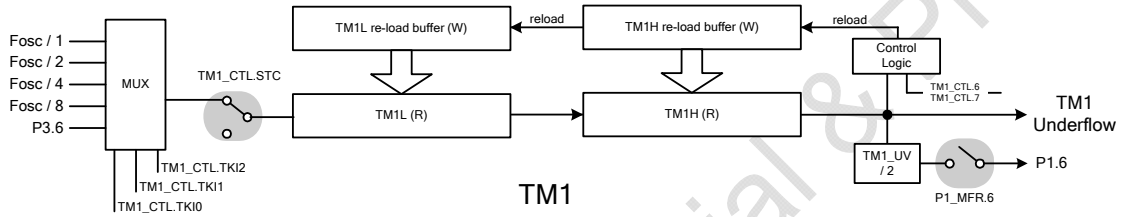
Timer1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00CCH	TM1L	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00CDH	TM1H	T15	T14	T13	T12	T11	T10	T9	T8	√	√
00CEH	TM1_CTL	STC	RL/S	TKES	-	-	TKI2	TKI1	TKI0	√	√

Timer 1 is a 16-bit **down-count** counter. The counter underflow frequency of Timer 1 can be calculated with the equation:
$F_{TM1\_UV} = F_{TM1} / (TM1+1)$

STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload
TKES: Event or series input clock-in trigger edge selector; 0: rising edge, 1: falling edge

TKI2	TKI1	TKI0	Selected TM1 input clock source
0	0	0	Fosc / 1
0	0	1	Fosc / 2
0	1	0	Fosc / 4
0	1	1	Fosc / 8
1	0	0	P3.6



11.3 Timer2

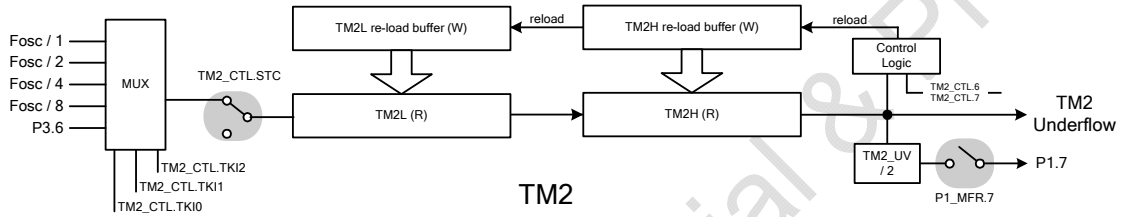
Timer2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D0H	TM2L	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00D1H	TM2H	T15	T14	T13	T12	T11	T10	T9	T8	√	√
00D2H	TM2_CTL	STC	RL/S	TKES	-	-	TKI2	TKI1	TKI0	√	√

Timer 2 is a 16-bit **down-count** counter. The counter underflow frequency of timer 2 can be calculated with the equation:
$F_{TM2\_UV} = F_{TM2} / (TM2+1)$

STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload
TKES: Event or series input clock-in trigger edge selector; 0: rising edge, 1: falling edge

TKI2	TKI1	TKI0	Selected TM1 input clock source
0	0	0	Fosc / 1
0	0	1	Fosc / 2
0	1	0	Fosc / 4
0	1	1	Fosc / 8
1	0	0	P3.6



For example: (if Fosc = 4.096MHz)

TM2	Frequency
00 00H	Invalid
00 01H	2.048MHz
00 02H	1.365MHz
…	…
00 FFH	16KHz
…	…
FF FFH	62.5Hz

12 Configurable I/O Ports

12.1 Port 0

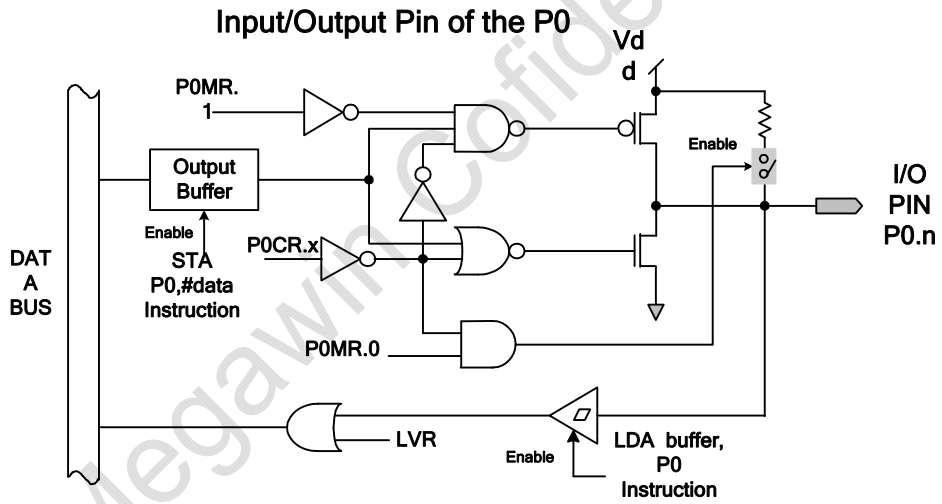
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E0H	P0	P07	P06	P05	P04	P03	P02	P01	P00	√	√
00E1H	P0CR	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00	√	√
00E2H	P0MR	-	-	MP05	MP04	-	-	MP01	MP00	√	√
00E3H	P0IEN	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0	√	√

Port 0 is an 8-bit I/O port; each pin can be programmed as input or output individually.
P0CR: P0.0 ~ P0.7 is input or output. 0: input, 1: output
P0MR: P0.0 ~ P0.7, pull-high and CMOS/NMOS setting
P0MR.0: P0.0 ~ P0.3 Pull-high control, 0: disable, 1:enable
P0MR.1: P0.0 ~ P0.3 CMOS/NMOS selector, 0: CMOS, 1:NMOS
P0MR.4: P0.4 ~ P0.7 Pull-high control, 0: disable, 1: enable
P0MR.5: P0.4 ~ P0.7 CMOS/NMOS selector, 0: CMOS, 1:NMOS

P0IEN: P0.0 ~ P0.7 interrupt enable, 0:disable, 1:enable

At initial reset, the Port 0 is all in input mode. Each pin of Port 0 can be specified as input or output mode independently by the P0CR registers. When Port 0 is used as output port, CMOS or NMOS open drain output type can be selected by the P0MR register. Port 0 has the internal pull-high resistors that can be enabled/disabled by specifying the P0MR.0 and P0MR.4 respectively. The pull-high resistors will be temporarily disable if the port is specified as output mode. **The read value will be the output buffer status in output mode.** When Port 0 is used as input mode, P0IEN (is set to enable), the RLH_EN, and IRQ_EN corresponding to the Port 0 are set, a signal change at the Port 0 (any pin) will execute the halt mode release or interrupt subroutine. Both the raising or falling signal will set the Port 0 event. The Schmitt trigger circuit is added in the input port part of all I/O pins.

Please set Port 0 as output high before set it as input mode, if speeds up the internal pull-high effect is needed. If the I/O ports are not used in your application, please set them as input with pull-high or output mode to avoid unnecessary power consumption.



12.2 Port 1

Port 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E4H	P1	P17	P16	P15	P14	P13	P12	P11	P10	√	√
00E5H	P1CR	CP17	CP16	CP15	CP14	CP13	CP12	CP11	CP10	√	√
00E6H	P1MR	-	-	MP15	MP14	-	-	MP11	MP10	√	√

Port 1 is an 8-bit I/O port; refer to port 0 for more information.
P1CR: P1.0 ~ P1.7 is input or output. 0: input, 1: output
P1MR: P1.0 ~ P1.7, pull-high and CMOS/NMOS setting
P1MR.0: P1.0 ~ P1.3 Pull-high control, 0: disable, 1:enable
P1MR.1: P1.0 ~ P1.3 CMOS/NMOS selector, 0: CMOS, 1:NMOS
P1MR.4: P1.4 ~ P1.7 Pull-high control, 0: disable, 1: enable
P1MR.5: P1.4 ~ P1.7 CMOS/NMOS selector, 0: CMOS, 1:NMOS

Port 1 multi-function selector (Normal I/O or Timer carrier out)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E7H	P1_MFR	PS7	PS6	-	-	PS3	-	-	-	-	√

PS7: Port 1.7 is normal I/O or TM2 carrier output selector. 0:normal I/O, 1: carrier output
PS6: Port 1.6 is normal I/O or TM1 carrier output selector. 0:normal I/O, 1: carrier output
PS3: Port 1.3 is normal I/O or TM0 carrier output selector. 0:normal I/O, 1: carrier output

12.3 Port 2

Port 2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E8H	P2	P27	P26	P25	P24	P23	P22	P21	P20	√	√
00E9H	P2CR	CP27	CP26	CP25	CP24	CP23	CP22	CP21	CP20	√	√
00EAH	P2MR	-	-	MP25	MP24	-	-	MP21	MP20	√	√

Port 2 is an 8-bit I/O port; refer to port 0 for more information.
P2CR: P2.0 ~ P2.7 is input or output. 0: input, 1: output
P2MR: P2.0 ~ P2.7, pull-high and CMOS/NMOS setting
P2MR.0: P2.0 ~ P2.3 Pull-high control, 0: disable, 1:enable
P2MR.1: P2.0 ~ P2.3 CMOS/NMOS selector, 0: CMOS, 1:NMOS
P2MR.4: P2.4 ~ P2.7 Pull-high control, 0: disable, 1: enable
P2MR.5: P2.4 ~ P2.7 CMOS/NMOS selector, 0: CMOS, 1:NMOS

12.4 Port 3

Port 3

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00ECH	P3	-	P36	P35	P34	P33	P32	P31	P30	√	√
00EDH	P3CR	-	CP36	CP35	CP34	CP33	CP32	CP31	CP30	√	√
00EEH	P3MR	-	-	MP35	MP34	-	-	MP31	MP30	√	√
00EFH	P3IEN	-	IE6	IE5	IE4	IE3	IE2	IE1	IE0	√	√

Port 3 is a 7-bit I/O port; refer to port 0 for more information.
P3CR: P3.0 ~ P3.6 are input or output. 0: input, 1: output
P3MR: P3.0 ~ P3.6, pull-high and CMOS/NMOS setting
P3MR.0: P3.0 ~ P3.3 Pull-high control, 0: disable, 1:enable
P3MR.1: P3.0 ~ P3.3 CMOS/NMOS selector, 0: CMOS, 1:NMOS
P3MR.4: P3.4 ~ P3.6 Pull-high controls, 0: disable, 1: enable
P3MR.5: P3.4 ~ P3.6 CMOS/NMOS selector, 0: CMOS, 1:NMOS

P3IEN: P3.0~P3.6 interrupt enable, 0:disable, 1:enable

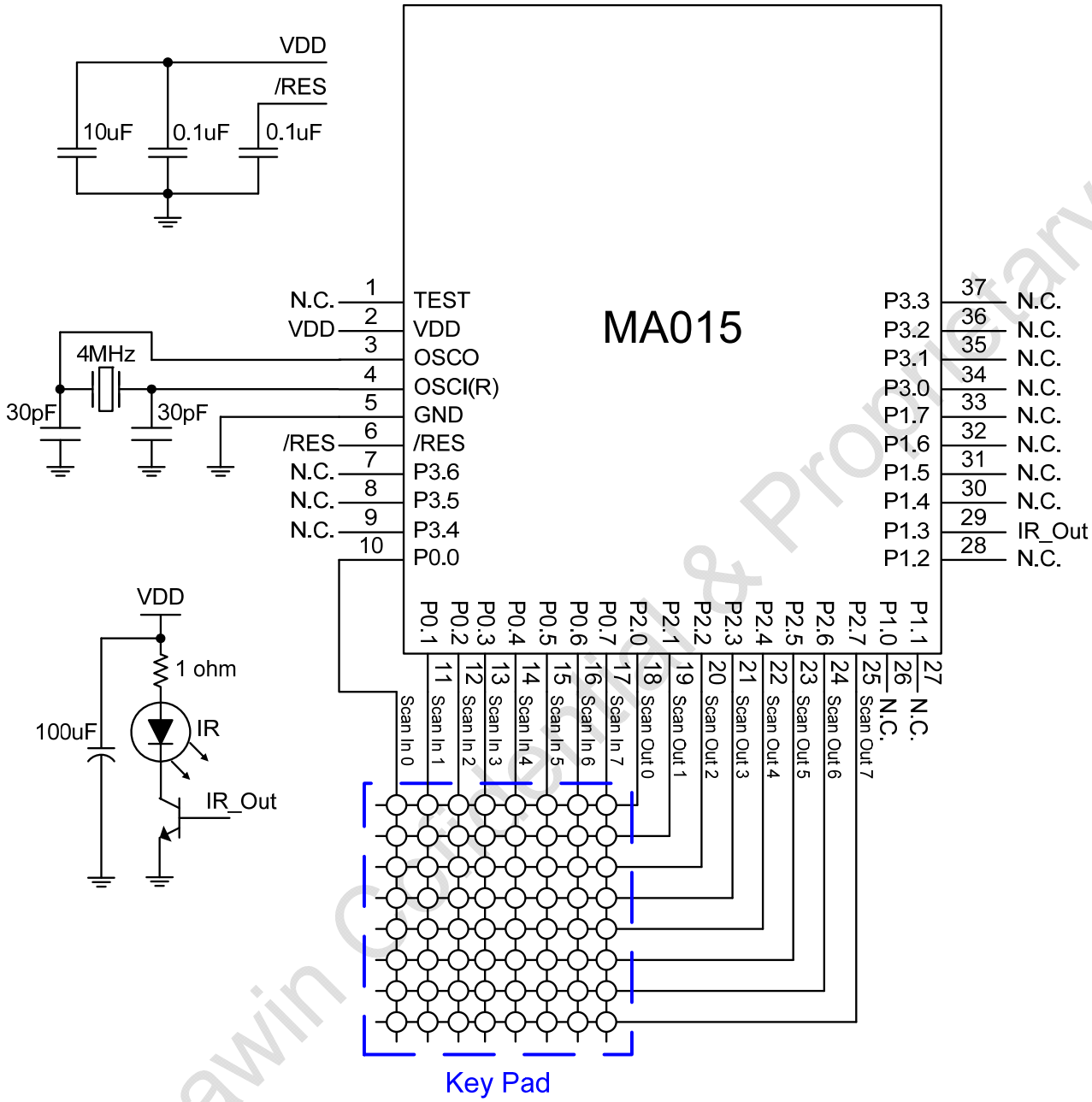
When Port 3 is used as input mode, P3IEN (is set to enable), the RLH_EN, and IRQ_EN corresponding to the Port 3 are set, a signal change at the Port 3 (any pin) will execute the halt mode release or interrupt subroutine. Both the raising or falling signal will set the Port event. The Schmitt trigger circuit is added in the input port part of all I/O pins.

Please set Port 3 as output high before set it as input mode, if a speed up the internal pull-high effect is needed. If the I/O ports are not used in your application, please set them as input with pull-high or output mode to avoid unnecessary power consumption.

13 Mask Option

Item	1	0	Note
F_{OSC}	Crystal	RC	In RC mode the OSCO will be the oscillating frequency output.
WDT	Enable	Disable	Watchdog timer.
RESOK	Enable	Disable	Reset OK function.

14 Application Circuit



15 Electrical Characteristics

15.1 Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +4.0	V
Applied Input / Output Voltage	-0.3 to +3.6	V
Power Dissipation	60	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

15.2 DC Characteristics

(VDD-VSS = 3.0 V, FOSC = 4MHz, Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V_{DD}	When LVR is disabled	1.8	-	3.6	V
Op. Current	I_{OP}	No load (Ext.-V) In normal operation	-	2.0	5.1	mA
Standby Current	I_{STB}	No load (Ext.-V)	-	-	1	μA
Input High Voltage	V_{IH1}	-	0.8 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL1}	-	0	-	0.2 V_{DD}	V
Port 0, Port 1, Port 2 and Port 3 drive current	I_{OH}	V_{OH} = 2.4V, V_{DD} = 3.0V	-	12	-	mA
Port 0, Port 1, Port 2 and Port 3 sink current	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.0V	-	12	-	mA
I/O Port Pull-high Resistor	R_{PH1}	V_{IL} = 0V	-	100K	-	Ω
Reset pin Internal Pull-high Resistor	R_{PH2}	V_{IL} = 0V	-	30K	-	Ω
Low Voltage Detector (note)	V_{LVD}	-	2.0	2.2	2.4	V
Low Voltage Reset	V_{LVR}	-	1.6	1.8	2.0	V
Low Voltage Protect	V_{LVP}	-	0.9 V		V_{LVR}	V

15.3 AC Characteristics

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CPU Op. Frequency	F_{CPU}	RC/Crystal, V_{DD} = 3.0V	0.5	4	-	MHz
Frequency Deviation by Voltage Drop for RC Oscillator	$\frac{\Delta f}{f}$	$\frac{f(3.0V) - f(2.4V)}{f(3.0V)}$	-	2	4	%
POR duration	T_{POR}	F_{OSC} = 4 MHz	5	10	20	mS

16 Revision History

Revision	Page	Descriptions	Date
V0.10		Original	
V0.20		Modify the P3.0, P3.1 description and add the DP0.	
V0.30		Add P3.0~P3.6	
V0.70		Modify the P0 I/O description	
V0.80		Deleted data pointer, added LVP, modified LVD and interrupt.	
V0.90		Modified Feature, Pad Description, SFR table, Interrupt vector, IRQ, Divider, Timer 0 ~ Timer 1, Port 0 ~ Port 2; Deleted Divider 1, Timer 2, melody relation functions, X32I/O.	
V0.91		Added Timer 2 and TEST pin; Modified features, Pad Description, RAM size, SFR table, Interrupt vector, IRQ, Timer 0 ~ Timer 2, Port 1 ~ Port 2.	
V0.92		Modify Timer 0 from 8-bit to 16-bit.	
V0.93		Modify WDT time selector, RESOK function as mask option.	
V0.94		Revise the error of interrupt circuit diagram on page 7. Modify the read value of port 0 in output mode from “external pad” to “output buffer”.	
V0.95		Modify the Reset OK function: Must write #$90 into the register at program start.	
V0.96		Modify the LVD voltage and I/O drive/sink current	
V1.11		Modify feature, reset vector table and DC characteristics.	
V2.00		Update document format.	2011/11/09

Note:

Here are customer's requirements:

(before 2007/3/14)

1. Increasing Port 1:3 source current to 10mA, sink current remaining unchanged.
2. Having internal reset circuit requiring no external components but can be OR-ed to external circuitry if required.
3. DC operation to be 2.2V @ 4MHz (is 2.4V at present). Note upper limit can be < 5.5V
4. Change X32I to Schmitt input pin. Change X32O to input/output pin.
5. Combining AGND & GND and AVDD & VDD to be single GND and VDD pins. Why are 4 supply connections needed? This would save us cost by eliminating 2 bonds on every single remote.
6. Costing of RAM increased by 64 bytes, 128 bytes or 256 bytes.
7. Any implications of above for development tools e.g. ICE, Flash, etc.
8. All the above adds no extra pins to the IC and, if item 5 can be implemented, we'd save pins. Note implementation of items 2 & 4 will also save on external component cost.

(2007/3/14)

1. Supply voltage: in the spec, the operation voltage is marked as 1.8V to 3.6V, however the specification also notes that the ceramic oscillator at 4MHz requires 2.1V - which voltage is correct?
2. Pad count - maintaining the current pad count (i.e. 36 pads) only allows port 3 to be 7 bits (you have 4 bits assigned to 3 pads - pads 33-36).
3. Timer Registers - we need to keep all three timers (TIMER0, TIMER1, TIMER2) - in fact, a fourth timer would be desirable.
4. Port sink currents - all ports should sink 6mA - note that it is important that they all sink the same current.
5. IRO - P1.3 - should source 10mA
6. Reset OK function - please remove/disable.
7. Remove the interrupt function from Port 2 - we'd prefer to have the new port, Port 3 with the wake-up interrupts (maskable).
8. Keep the DIV0 and DIV1 registers to drive the associated Port 3 output.

(2007/3/16)

1. Timers - we don't want to change any of the timers - currently, you have updated Timer0 to be an 8 bit timer - we would prefer that you revert this back to 16 bit as in the MLC041.
2. RESOK (Reset OK) - we would like to see this function removed - in fact, we don't want to make use of this nor the watchdog timers.
3. Page 19: "5. Added Port 3.0 ~ Port 3.7 for GPIO, Port 3.6 can be the clock source of timer." - port 3.7 does not exist... should be power 3.0 to Port 3.6.

Compare the major difference with MLC041

Added:

1. Low Voltage Detector in 1.9V.
2. Low Voltage Protector in 0.9V to V_{LVR} (Low voltage reset voltage). In LVP state, oscillator is stopped by logic circuit; oscillator will start again when $V_{DD} > V_{LVR}$.
3. Reset OK function, this function is mask option.
4. Port 3.0 ~ Port 3.6 with interrupt function. Interrupt function setting is individual.
5. Added Port 3.0 ~ Port 3.6 for GPIO, Port 3.6 can be the clock source of timer.

Deleted:

1. NMI selects function.
2. Divider 0 and Divider 1 control SFR and interrupt function.
3. AGND, AV_{DD}, SPK1, SPK2, TEST and 32K Crystal Pad (X32I / X32O).
4. F_{CPU} selector.
5. CH1, CH2, CH3 three DAC buffer and control SFR
6. Voice / Tone control SFR

Modify:

1. Add RAM from 256 Bytes to 320 Bytes.
2. Modify Memory Map, Extended share memory from 0x0000h~0x007FH to 0x0000h~0x00BFh.
3. Move all SFR to zero page (0x00C0H ~ 0x00FFH) and modify the addresses of SFR.
4. Modify the interrupt vector (Port 0 and Port 3 share the “Port” interrupt vector)
5. Interrupt vector table: Delete NMI, Divider 0 and Divider 1. Modify Port 0 to Port.
6. IRQ: Delete Divider 0 and Divider 1. Added LVD. Modify Port 0 to Port.
7. Divider is only used to generate clock to Timer and WDT.
8. Power saving controls SFR: Delete X32 relation function (because there is no X32 pad).
9. Release halt mode SFR: Delete Divider 0, Divider 1. Modify Port 0 to Port.
10. Port 0.0 ~ 0.7 and **Port 3.0~ 3.6** with interrupt function. Interrupt function setting is individual.
11. Port 1 multi-function selector. Keep Port 1.3, P1.6 and P1.7 can be timer 0, timer 1 and timer 2 carry out. Delete Port1.4 and P1.5 timer serial input.
12. Timer 0: Modify clock source; Delete Shift control and serial input through P1.4 and P1.5; Keep carry out with P1.3.
13. Timer 1: Modify clock source; Delete Shift control and serial input through /P1.4; Keep carry out with P1.6.
14. Timer 2: Modify clock source; Keep carry out with P1.7.
15. Delete I/O weak input pull high resistor (keep 50K Ω pull-high).
16. Change Port 0, P1.4~P1.7, Port 2 and Port 3 **drive** current from 1.5mA to 3.0mA.
17. Change P1.0~P1.3 drive current from 1.5mA to 10.0mA.
18. Change Port 0, Port 1, Port 2 and Port 3 **sink** current from 9.0mA to 6.0mA.
19. Change WDT time to 4 steps: 65.5ms, 131ms, 262ms and 524ms.