

The MA28140 Packet Telecommand Decoder (PTD) is a single-chip implementation of the core part of a telecommand decoder, manufactured using CMOS-SOS high performance, radiation hard, 1.5µm technology. The PTD is a full implementation of and fully compliant with the packet telecommand standard ESA PSS-04-107 and the telecommand decoder specification ESA PSS-04-151, these being derived from the corresponding CCSDS standards.

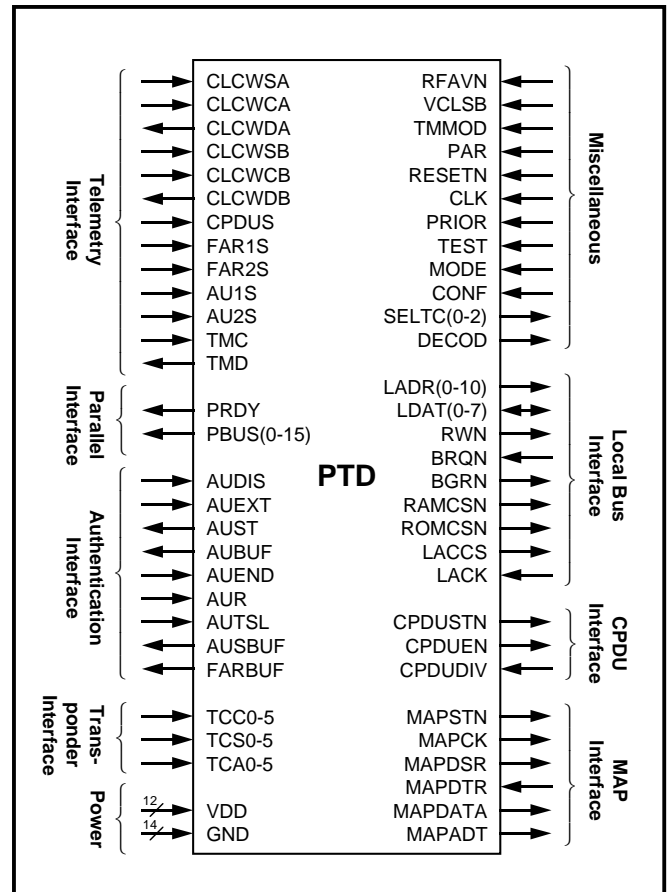
The PTD, which handles 6 NRZ TC input channels, processes the following layers:

- Coding Layer
- Transfer Layer
- Segmentation Layer
- Authentication Layer
- Command Pulse Distribution

Some of these layers have a telemetry reporting mechanism. The processed TC segment can be transferred to the application either serially or in parallel.

**FEATURES**

- Single Chip Implementation of all TC Decoder Core Functions
- Built-in Authentication Unit
- Built-in Command Pulse Distribution Unit Core Logic
- Radiation Hard to 1MRads (Si)
- High SEU Immunity, Latch-up Free
- CMOS-SOS Technology
- Conforms to CCSDS Standards
- 6 NRZ TC Input Channels
- 50Kbps Bit Rate
- Low Power Consumption
- Single 5V Supply
- -55 to +125°C Operation



Pin connections

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**REFERENCES**

1. "Packet Telecommand Standard" ESA PSS-04-107, Issue 2, April 92.
2. "Telecommand Decoder Specification" ESA PSS-04-151, Issue 1, September 93.

**1. INTRODUCTION**

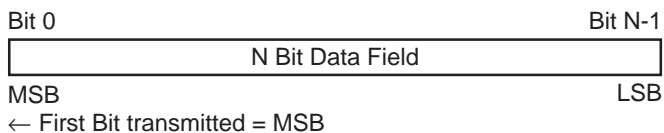
This document is the data sheet of the "Packet Telecommand Decoder", henceforth called the PTD.

The PTD is compatible with the ESA PSS-04-107 standard directly derived from the CCSDS recommendations. This standard is described in references 1 and 2. The data sheet is based on both documents for the description of the protocol. Nevertheless, it was impossible to include the whole reference documents in the data sheet, thus some specific points of the protocol or some descriptions of the recommended hardware implementation have not been included. The reader may find these points in the applicable documents.

**CONVENTION**

In this document the two conventions described in references 1 and 2 apply:

1. The first bit in the field to be transmitted (i.e. the most left justified bit when drawing a figure) is defined to be Bit 0. When the field is used to express a binary value, the Most Significant Bit (MSB) shall be the first transmitted bit of the field (i.e. Bit 0).



Note: Some of the external interfaces have parallel busses (LADR, LDAT, PBUS, SELTC) which have the opposite bit order specified, i.e. Bit 0 is The Least Significant Bit.

2. An 8-bit word (a byte) is called an OCTET.

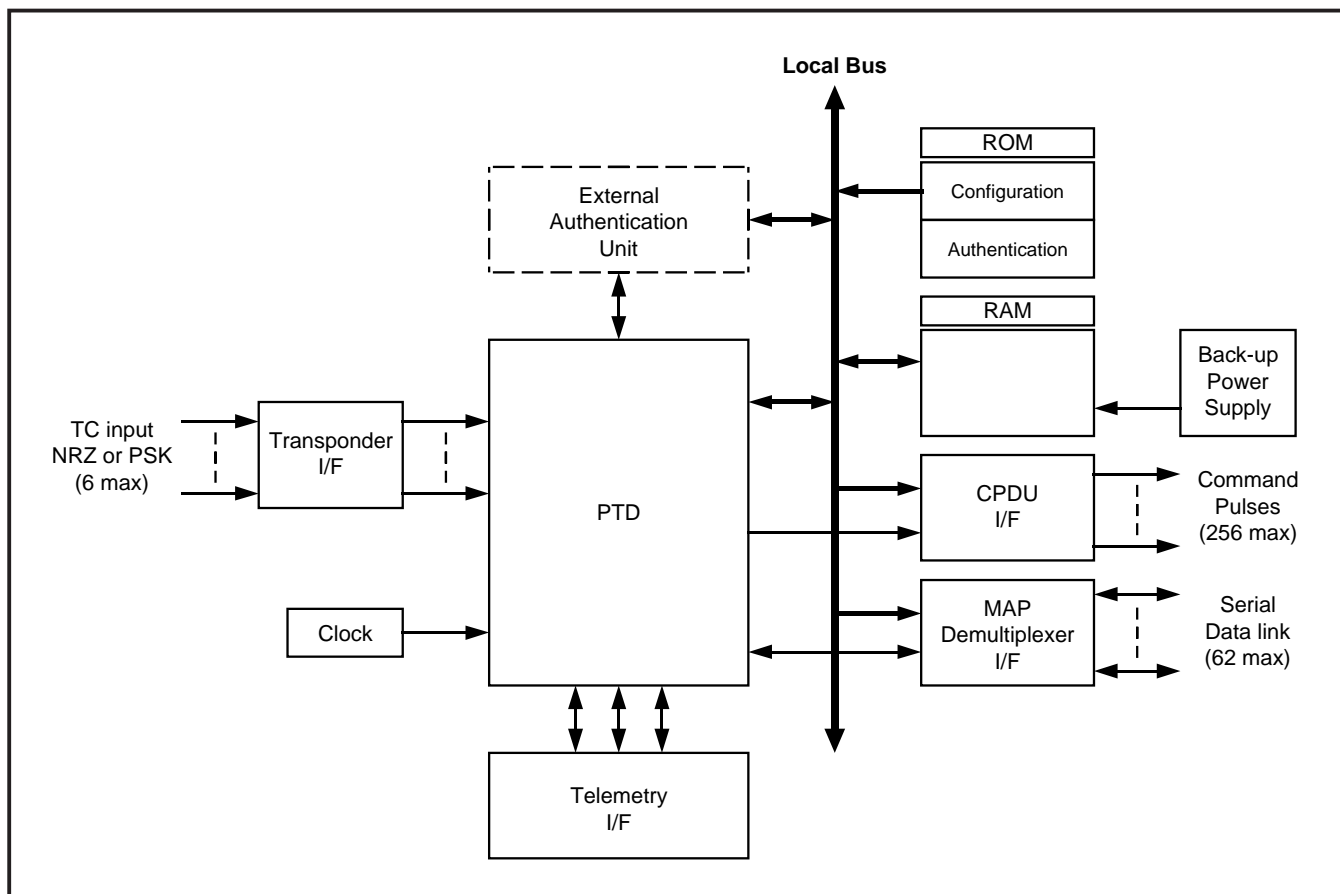


Figure 1: Block Diagram of a TC Decoder Subsystem

## 2. TC DECODER SUBSYSTEM OVERVIEW

An ESA/CCSDS Telecommand Decoder subsystem including the PTD and fulfilling the receiving-end functions established in the Packet Telecommand Standard (ref 1) is shown in Figure 1.

The PTD requires the following additional hardware to fulfil the requirements of the Telecommand Decoder Specification (ref 2):

- Transponder I/F including demodulators for PSK TC inputs.
- Telemetry I/F. The telemetry reporting signals can be directly connected to a Virtual Channel Multiplexer (ref 3).
- Command Pulse Distribution Unit I/F. This function performs decoding of commands present on the local bus and power amplification. The PTD ASIC associated with the CPDU I/F can manage 256 pulse outputs.
- MAP demultiplexer I/F. This interface is composed of a demultiplexer to provide the TC segment data to various Data Management System interfaces. The demultiplexer is controlled by the MAP data present on the Local Bus. The PTD ASIC can manage 62 different serial data interfaces (63 if AU is disabled).
- Memories. There are 2 different memories:
  - RAM (2Kx8) used to store the received TC data and protocol variables (programme authentication key for instance) and eventually to store the TC segment available for further processing by the Data Management System. If this memory is used to store the recovery LAC counter (Authentication function), it must be a non-volatile memory.
  - ROM (1Kx8) divided in two parts:
    - Configuration part, used to provide the Mission Specific Data.
    - Authentication part, used to provide the fixed Authentication key.
- External Authentication Unit (optional). Although an AU is implemented in the PTD, it is also possible to use an external AU if the mission requires a different authentication algorithm. This external unit accesses the RAM in order to authenticate a TC segment.

### 3. PTD ARCHITECTURAL OVERVIEW

Figure 2 describes the PTD functional architecture which features 7 major blocks described below. Figure 3 shows the CCSDS protocol layer architecture. The PTD deals with the Coding Layer, the Transfer Layer, the Authentication Layer, the Segmentation Layer and a part of the Packetisation Layer of the CCSDS protocol.

#### CODING LAYER BLOCK

The coding layer block multiplexes the 6 physical TC channel inputs and fulfils the coding layer function described in section 5 of ref.1.

The main tasks performed by the PTD at this level are:

- Start sequence detection and selection of the first active TC input.
- Codeblock error detection and correction.
- Valid codeblock transfer to the above layer.
- Generation of part of the FAR and CLCW status.

#### TRANSFER LAYER BLOCK

This level is concerned with the processing of the frames received from the coding layer and fulfils the transfer layer function described in section 6 of ref.1.

At this level, the PTD performs the following tasks:

- Clean frame validation.
- Legal frame validation.
- Frame analysis report mechanism.
- Reporting word (16 bit CLCW and part of 32 bit FAR) generation.

#### AUTHENTICATION UNIT BLOCK

This block (which is optional and can be disabled permanently or during flight) is concerned with the segment data protection, it enables the spacecraft to authenticate the received data. The authentication concept is the "plain text with appended signature" approach, described in Section 8 of ref. 2.

In the PTD architecture this function is implemented on chip. However, a specific interface allows authentication to be performed externally - if another coding algorithm is to be used, the on-chip block can be disabled and an external authentication system can be used.

The block generates a reporting word (Authentication Status = 80 bits) and part of the 32 bit FAR.

#### SEGMENTATION LAYER BLOCK

This block implements only some of the segmentation layer functions described in section 7 of ref.1. Its purpose is to manage the back-end buffer shared with the FARM-1 block of the transfer layer and to implement the MAP interface in order to demultiplex (with external hardware) the segments dedicated to the different spacecraft applications.

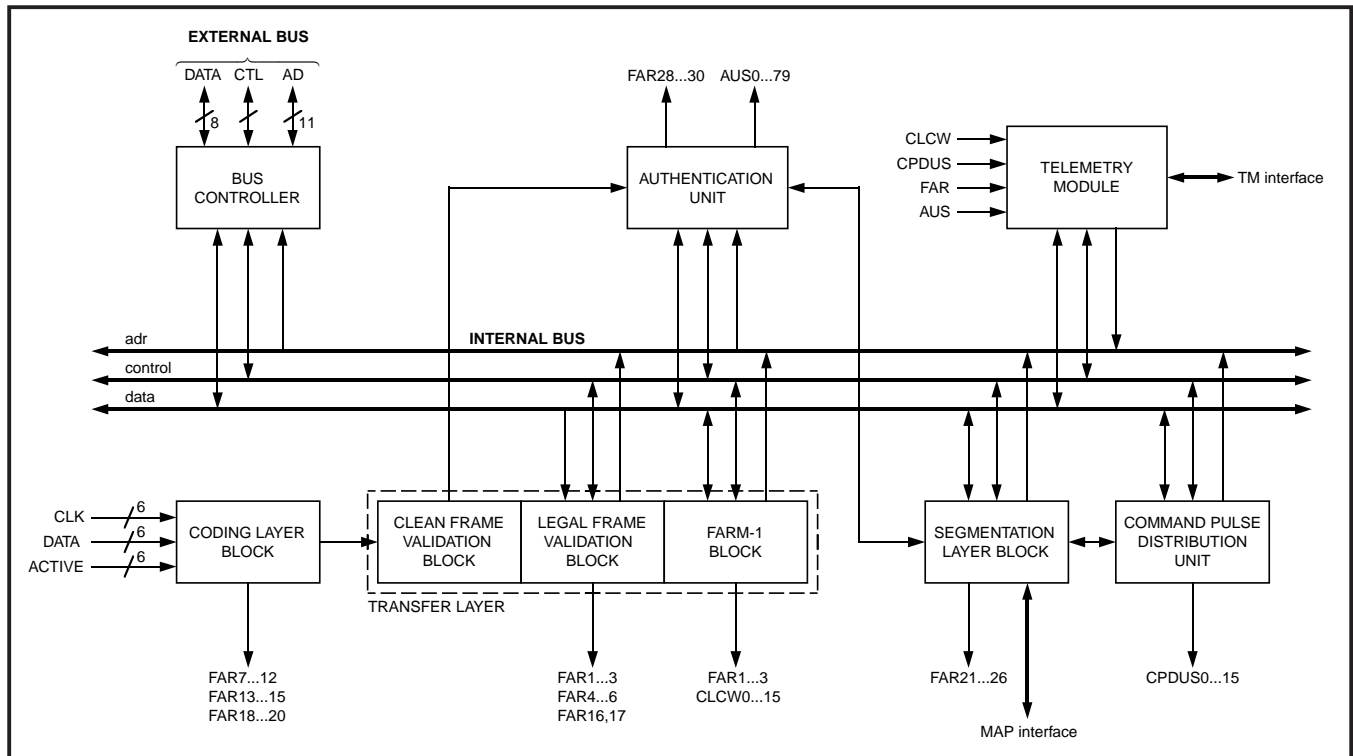


Figure 2: PTD Internal Architecture

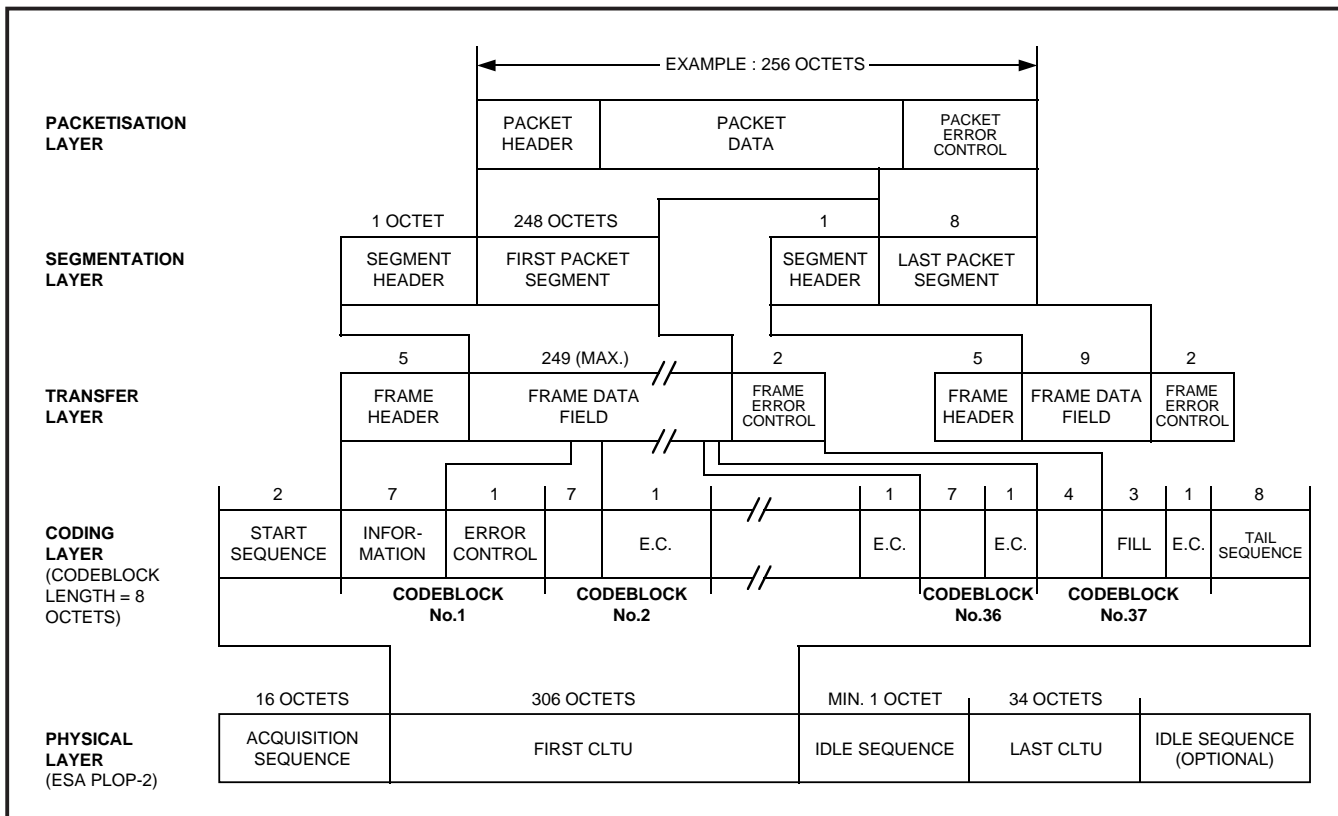


Figure 3: CCSDS Protocol Layer Architecture

**COMMAND PULSE DISTRIBUTION UNIT**

The CPDU is integrated into the PTD ensuring higher reliability for this critical function (direct telecommand for spacecraft reconfiguration) than if implemented in an external chip. The critical commands executed by the CPDU are received in specific packets. The CPDU responds to the MAP identifier 0, and to a mission dependent application process identifier (stored in ROM). No segmentation is accepted, the commands must be contained in an unsegmented package. The unit generates a reporting word (CPDU Status = 16 bits).

**BUS CONTROLLER**

This block is the interface between external memories and on chip modules. Its different functions are:

- address decoding.
- internal and external bus access arbitration.

**TELEMETRY MODULE**

This block is the interface with the telemetry subsystem. It manages the data report storage using double buffered registers.

4. PTD FUNCTIONAL DESCRIPTION

4.1 CODING LAYER

Overview of the Layer

The coding layer provides the forward error correction capability and synchronisation services used by the Transfer layer. Each Transfer Frame is encoded/embedded in one CLTU (Command Link Transmission Unit), which is the protocol-data unit of the coding layer. At the receiving end of the Coding Layer, a “dirty” symbol stream (plus control information on whether the physical channel is active or inactive) is received from the layer below. Searching for the Start Sequence, the coding layer finds the beginning of a CLTU and decodes the TC Codeblocks. As long as no errors are detected, or errors are detected and corrected, the coding layer passes “clean” octets of data to the Transfer layer. Should any codeblock contain an uncorrectable error, this Codeblock is abandoned and considered as Tail Sequence, no further data is passed to the layer above and the Coding Layer returns to a Start Sequence searching mode until it detects one. The coding layer also generates part of the CLCW and FAR status.

The PTD can handle up to 6 TC input interfaces, the data bit rate on these inputs should not exceed 50 Kbits per second when using the Authentication Unit. If the Authentication unit is not used the symbol rate could exceed 200kBits/sec (not guaranteed).

Standard Data Structures Within the Layer

A CLTU is made up of three distinct protocol data elements:

- one 16-bit Start Sequence,
- one or more TC Codeblocks of a fixed length of 8 octets to encode the protocol data unit from the layer above,
- one Tail Sequence of length equal to that of the TC Codeblock, i.e. 8 octets.

Start Sequence	First Codeblock	.....	Last Codeblock	Tail Sequence
16 Bits	Variable Number of Codeblocks			8 Octets

The Start Sequence marks the beginning of the TC Codeblock field within a CLTU. It consists of a 16-bit synchronisation pattern represented in hexadecimal as EB90, where the first transmitted octet is EB.

The TC Codeblock field consists of one or more TC Codeblocks. The codeblock length of received data is fixed and set to 8 octets (information field: 7 octets).

	P0 (MSB)	P6	P7 (LSB)
Information Field	Error Control Field 7 parity bits		Filler Bit
7 Octets	1 Octet		

The Tail Sequence marks the end of the TC Codeblock Field within a CLTU. The length of the Tail Sequence is that of a TC Codeblock. Reference 1 specifies that its pattern should be alternating “zeros” and “ones”, ending with a “one” (55 .... 55 in hexadecimal), but any double error codeblock, or single error codeblock with filler bit equal to 1 will be interpreted as Tail Sequence by the PTD.

Synchronization and TC Input Selection

Synchronization is performed by searching for the Start Sequence simultaneously on all active TC inputs. The Start Sequence detection allows one bit error anywhere in the 16-bit pattern. Furthermore due to NRZ coding ambiguity on the incoming bit stream, it is possible to detect the inverted Start Sequence pattern in order to choose between positive or negative representation for further NRZ data processing. If an inverted Start Sequence is detected, the following bit stream is inverted until the Tail Sequence is encountered.

Two different modes to perform the TC channel selection are supported, selectable with the PRIOR configuration input:

Standard Mode (PRIOR = 0), in which all TC inputs TC0 to TC5 have the same priority, and the search for a Start Sequence is performed on all active TC channels simultaneously.

Priority Mode (PRIOR = 1), in which two inputs are assigned an absolute priority.

**Note:** This mode is not compliant with Ref. 1, and is intended for applications with specific requirements on unconditional access to the TC decoder. If this mode is used, a thorough analysis of potential failure modes and the built-in timeout mechanisms is recommended.

Standard Mode

The TC input selection locks the selection multiplexer on the first TC channel where the Start Sequence is found. The selection mechanism is restarted once a Tail Sequence or a codeblock rejection has been detected. Furthermore, as a protection mechanism in case of RF receiver breakdown, a timeout mechanism is provided; if the TC channel clock is not detected during a certain time, the TC selection mechanism is reactivated in order not to remain latched on a Channel without a clock signal.

The timeout value between two successive edges of the TC channel clock is: 3932160

tCK < TC clock timeout < 4587520 tCK, with tCK being the system clock period. With a

system clock frequency fCK of 4MHz this equals 0.98s <TC clock timeout < 1.15s.

**Priority Mode**

In this mode two inputs have priority, according to the following rule: TC0 > TC1 > TC2 = TC3 = TC4 = TC5. When neither the TC0 input nor the TC1 input is active, the selection between the inputs TC2 to TC5 is performed as in the Standard Mode.

As soon as the TC active signal of TC0 is asserted, this TC input is selected, and the 5 other channels are inhibited. In case another input was already selected and receiving data, it is abandoned. The TC0 input remains selected until one of the following events:

- a1: its TC active signal becomes inactive, or
- b1: its bit clock has not been received for a period equal to the TC clock timeout, or
- c1: no Start Sequence has been detected for a period equal to the TC active timeout, or
- d1: a Tail Sequence or a codeblock rejection has occurred.

Upon events (a1) and (d1), the selection logic returns to the search state. Upon events (b1) and (c1), the TC0 input is ignored (i.e. considered inactive) until the event (a1) occurs.

When the TC0 input is inactive (including the case of a timeout as described above), as soon as the TC active signal of TC1 is asserted, this TC input is selected, and the lower priority inputs TC2 to TC5 are inhibited. In case any of these inputs was already selected and receiving data, it is abandoned. The TCI input remains selected until one of the following events:

- a2: its TC active signal, becomes inactive, or
- b2: its bit clock has not been received for a period equal to the TC clack timeout, or
- c2: no Start Sequence has been detected for a period equal to the TC active timeout, or
- d2: a Tail Sequence or a codeblock rejection has occurred, or
- e2: the TCO active signal is asserted.

Upon events (a2) and (d2), the selection logic returns to the search state. Upon events (b2) and (c2), the selection logic ignores the TC1 input until event (a2) occurs. Upon event (e2) the TCI input is inhibited and the TC0 input is selected as previously described.

The TC clock timeout value between two successive edges of the TC channel clock is:  $3932160 t_{CK} < \text{TC clock timeout} < 4587520 t_{CK}$ . With a system clock frequency  $f_{CK}$  of 4 MHz this equals  $0.98s < \text{TC clock timeout} < 1.15s$ .

The TC active timeout value between two successive Start Sequence patterns being detected is  $334233600 t_{CK} < \text{TC active timeout} < 335399960 t_{CK}$ . With a system clock frequency  $f_{CK}$  of 4MHz this equals  $83.5s < \text{TC active timeout} < 83.9s$ .

**Codeblock Decoding**

Codeblock decoding is performed for each received codeblock. At the sending end, a systematic block coding procedure processing 56 bits per Codeblock and generating 7 parity check bits per Codeblock is used. The parity check bits are then complemented and placed into the codeblocks: P0 (MSB) through P6 are located in the first seven bits (MSBs) of the last octet of the codeblock. The last bit of the last octet, P7 (LSB), is a filler bit appended to complete the 8-bit Error Control Field. This Filler Bit should normally be a zero, except for the Tail Sequence. The code is a (63,56) modified Bose-Chaudhuri-Hocquenghem (BCH), based on the following polynomial generator:  $g(x)=x^7+x^6+x^2+1$ . A single error correction & double error detection mode is provided by using this code.

The following table describes the Decoding Strategy of the codeblocks:

ERRORS DETECTED	FILLER BIT VALUE	DECISION
no errors	ignored	codeblock accepted
even number of errors	ignored	codeblock rejected
odd number of errors with a binary syndrome value equal to all zeros	ignored	codeblock rejected
odd number of errors with a binary syndrome value different from all zeros	0	codeblock accepted correction of a single error
odd number of errors with a binary syndrome value different from all zeros	1	codeblock rejected

**CLTU Management**

CLTU decoding consists of the states and events summarized in the following table and state diagram:

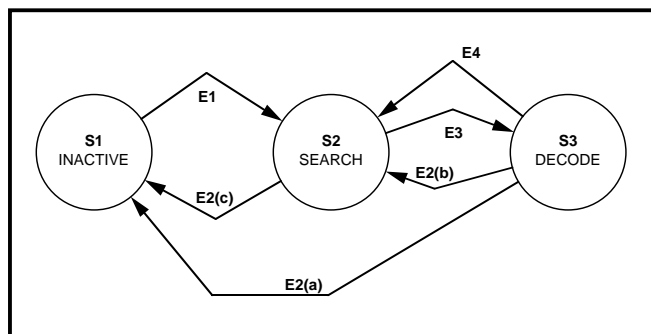


Figure 4: CLTU Decoder State Diagram

## MA28140

State Number	State Name	State Definition
S1	INACTIVE	All telecommand channels are inactive (no bit lock is achieved) or no bit modulation is detected.
S2	SEARCH	Incoming bit stream is searched, bit by bit, for the Start Sequence pattern.
S3	DECODE	Codeblocks, which are either free of error or which can be corrected, are received and decoded, and their information octets are transferred to the layer above

Event Number	Event Name	Event Definition
E1	CHANNEL ACTIVATION	Bit modulation is detected and bit lock is achieved: telecommand bit stream is present
E2 (a) (c) (b)	CHANNEL DEACTIVATION CLTU ERROR	Deactivation of the TC Active Signal  More than 37 codeblocks accepted in the CLTU or Timeout on the TC Clock signal or Activity on a channel having higher priority in priority mode
E3	START SEQUENCE FOUND	The Start Sequence pattern has been detected, signalling the beginning of the first codeblock of the CLTU
E4	CODEBLOCK REJECTION	A codeblock is found uncorrectable (erroneous codeblock or tail sequence). No information octet from this codeblock is transferred to the layer above

Codeblock transfer is performed in a serial way to the above layer (Transfer layer). Two indication signals are provided to the above layer - one indicating the whole frame duration, the other asserted each time a 7 octets block is being transferred.

The following rules apply to the data transfer between the Coding Layer and the Transfer Layer:

- When the first Candidate Codeblock is affected by an event E4 or by an event E2, the CLTU is abandoned. No Candidate Frame is transferred to the Transfer Layer.
- When the first Candidate Codeblock is found to be error free, or if it contained one error which has been corrected, its information octets (i.e. 7 octets) are transferred to the Transfer Layer. The decoding of the CLTU continues until one of the following events occurs:

1- when an event E4 (codeblock rejection) occurs for any of the 37 possible Candidate Codeblocks the decoder returns to the search state S2 with the following actions:

- The codeblock is abandoned
- No information from that codeblock is transferred to the layer above
- The Coding Layer indicates to the Transfer Layer the end of transfer of the Candidate Frame.

2- when an event E2 (channel deactivation) occurs the decoder returns to the inactive state (for the channel) with the following actions:

- The CLTU is aborted,
- The CLTU is reported as abandoned,
- A signal is sent to the Transfer Layer to indicate that the entire block of octets making up the Candidate Frame must be erased.

3- When an event E2(b) (CLTU error) occurs, the decoder returns to the search state with the following actions:

- The CLTU is aborted,
- The CLTU is reported as abandoned,
- A signal is sent to the Transfer Layer to indicate that the entire block of octets making up the Candidate Frame must be erased.

A CLTU error occurs in the following cases:

- More than 37 codeblocks have been accepted in the CLTU,
- A timeout on the TC clock signal occurs,
- Activity on a channel having higher priority is detected in priority mode.

The DECOD output is activated when the CLTU decoder state is S3.



## 4.2 TRANSFER LAYER

### Overview of the Layer

The Transfer Layer implements the following sublayers:

- The Frame Error Control Sublayer which ensures that only “clean” frames are transferred to the sublayer above by using a CRC error syndrome verification.
- The Frame Header Sublayer verifies the conformity of the relevant frame header fields by using the Legal Frame Validation process before passing the frame to the FARM1.
- The “Frame Acceptance and Reporting Mechanism One” or FARM1 ensures that frames are processed in the correct sequence.

There are three types of TC transfer frames:

- two types for the Sequence-Controlled Service: AD and BC frames
- one type for the Expedited Service: BD frames

The Sequence-Controlled Service is used for normal spacecraft communications. It concerns essentially TC Transfer Frames carrying TC segments: the AD frames. To configure the AD machine, special control frames are used called BC frames.

The Expedited Service is used for recovery in the absence of the telemetry downlink or during unexpected situations. It is only concerned with TC transfer frames carrying TC segments: the BD frames.

### Standard Data Structures Within the Layer

The major fields of the TC Transfer Frame are shown below:

5 octets	1 to 249 octets	2 octets
Frame Header	Frame Data Field	Frame Error Control Field

### Frame Header

The structure of the frame header is given below:

2 octets		1 octet		1 octet	1 octet			
version number	bypass flag	control command flag	reserved field A	spacecraft ID	virtual channel ID	reserved field B	frame length	frame sequence number
2	1	1	2	10	6	2	8	8

A description of the fields of the frame header is given below:

- Version number, Reserved field A and Reserved field B should always be 00 (ref 1).
- Bypass flag and control command flags. Their values are given in the next table:

Bypass Flag	Control Command Flag	Interpretation
0	0	AD frames
0	1	ILLEGAL
1	0	BD frames
1	1	BC frames

- Spacecraft identifier. This field provides the identification of the spacecraft being commanded.

- Virtual channel identifier. It is used as a spacecraft sub-identifier. It can provide an identification of the spacecraft telecommand chain selected for operating the spacecraft.

- Frame length. This field specifies the number of octets contained within the entire TC transfer frame:  
Field Value = (Total number of octets) - 1

- Frame sequence number. This number is denoted as N(S). It is set to different values:
  - for AD frames it should be set to the Transmitter Frame Sequence Number and it is compared to the Receiver Frame Sequence Number V(R) stored in the PTD, to control the transfer of a sequence of frames (see the FARM-1 process)
  - for BC and BD frames it should be set to all zeros.

Except for the bypass and control command flags, the values of the first three header octets are programmed in the external ROM.

In the abbreviations AD, BD and BC, A stands for Acceptance check of N(S), B stands for Bypass of A, C stands for Control and D stands for Data. AC is an illegal combination because Control Commands cannot reliably use a transfer service which they are meant to modify.

### Frame Data Field

The frame data field is of variable length from a minimum of 1 octet to a maximum of 249 octets. When the frame is a data frame (type AD or BD), it contains a TC segment. When the frame is a BC frame, this field can contain 2 control commands to configure the FARM-1 process:

- the UNLOCK command. The FARM-1 has a built in mechanism which will go into a Lockout state whenever it receives a type-AD frame containing a frame sequence number N(S) outside the limits of the FARM-1 Sliding Window. The UNLOCK command provides a mechanism to reset the Lockout condition. The UNLOCK command is encoded as a single octet with the value: 00000000.

- The SET V(R) command. The SET V(R) command allows V(R) to be preset to any desired value. The SET V(R) command is encoded as three octets with the values:

10000010      00000000      XXXXXXXX

The value to be set into V(R) is stored in the third octet.

### Frame Error Field

The frame error field is a mandatory 16-bit field which occupies the two trailing octets of the TC Transfer Frame. It is a cyclic redundant code (CRC) generated with the polynomial  $X^{16} + X^{12} + X^5 + 1$  with the shift register being initialised to all ones before processing each frame (refer to ref 2 for a complete description of this field). The CRC is only used for error detection by the frame and not for error correction.

**Standard Procedures Within the Layer**

**The Clean Frame Validation Process**

On receiving a new frame, the Clean Frame Validation process performs the following tasks:

- the number of octets in the frame is checked to be greater than 7 octets,
- the transfer frame is assumed to be a version 1 frame,
- the frame length field is checked to be compliant with the real number of octets of the frame,
- the number of fill octets is verified to be minimum zero and maximum six,
- the fill octets are removed,
- the CRC error syndrome verification is carried out.

All candidate frames passing all the preceding validation checks are declared clean and transferred immediately to the Legal Frame Validation process. Frames failing any of the preceding tests are declared dirty and are erased.

**The Legal Frame Validation Process**

On receiving a clean frame, the Legal Frame Validation process performs the following validation checks:

- the version number is checked to be as defined in the ROM,
- the reserved fields A and B are checked to be as defined in the ROM,
- the value of the spacecraft ID is checked to be as defined in the ROM,
- the value of the Virtual Channel ID is checked to be as defined in the ROM and by the VCLSB input,
- the Bypass and Control Command flags must combine legally,
- the BC frames must contain a valid control command (either UNLOCK or SET V(R)),
- for a BC or BD frame the Frame Sequence Number field must be set to all zeros.

The LSB of the VC ID is indirectly defined from a dedicated pin VCLSB; it allows easy configuring of a pair of redundant TC decoders.

- VCLSB = 1: The VC ID LSB read from the ROM is inverted.
- VCLSB = 0: The VC ID LSB read from the ROM is not inverted.

All candidate frames passing all the preceding validation checks are declared legal and transferred immediately to the FARM-1 process. Frames failing any of the preceding tests are declared illegal and erased.

**The FARM-1 Process**

**THE FARM-1 VARIABLES**

The Frame Acceptance and Reporting mechanism (FARM-1) is described by a finite state machine represented by the FARM-1 state table. The FARM-1 maintains a set of variables which are described below:

• The State. This may be one of the following:

- Open (S1)
- Wait (S2)
- Lockout (S3)

This variable represents the state of the FARM-1 automaton. In Open State, the FARM-1 accepts frames and passes them to the above layer. In Wait State, there is no buffer space available in which to place any further received data of type AD. The protocol leaves the Wait State upon receipt of a buffer release signal from the Higher Layer. Lockout is entered if the protocol machine detects an error. It is a safe state in that no user data (AD frames) will be accepted or transferred to the Higher Layer. The only accepted data frames are the BD frames, but even in this case the protocol machine remains in lockout state. The protocol machine leaves the Lockout State upon receipt of an UNLOCK control command.

• The Lockout Flag. This is set to 1 whenever the protocol is in the Lockout State.

• The Wait Flag. This is set to 1 whenever the protocol is in Wait State.

• The Retransmit Flag. This is set to 1 whenever the protocol machine knows that an AD frame has been lost in transmission or has been discarded because there was no buffer space available. This flag is reset to 0 upon the successful receipt of a frame with  $N(S)=V(R)$ , the receipt of a SET V(R) control command (unless in Lockout State) or receipt of an UNLOCK control command.

• FARM B counter. This is incremented whenever a valid BD or BC frame arrives. This counter is a 2 bit wraparound counter.

• Receiver Frame Sequence Number V(R). This records the value of N(S) expected to be seen in the next AD frame.

• The buffer management variable. The PTD maintains a flag indicating the number of the back end buffer. The AUBUF output pin provides the value of this flag (the back end and front end buffers are represented in Figure 6). The number of the TC channel on which the data stored in the back-end buffer has been received is provided on the output pins (SELTC2-0).

• FARM Sliding window variables. The purpose of these are to protect FARM-1 against the unauthorised transfer of a sequence of frames such that the Frame Sequence Number N(S) of one or more of these frames will exceed the current value of the V(R) counter. The FARM Sliding Window concept applies only to AD frames.

The FARM Sliding Window is defined in terms of two variables:

- the width of the positive part referred to as PW
- the width of the negative part referred to as NW

The FARM Positive window area starts with V(R) and extends PW frames in the positive direction. The FARM Negative window starts at V(R) - 1 and extends NW frames in the negative direction.

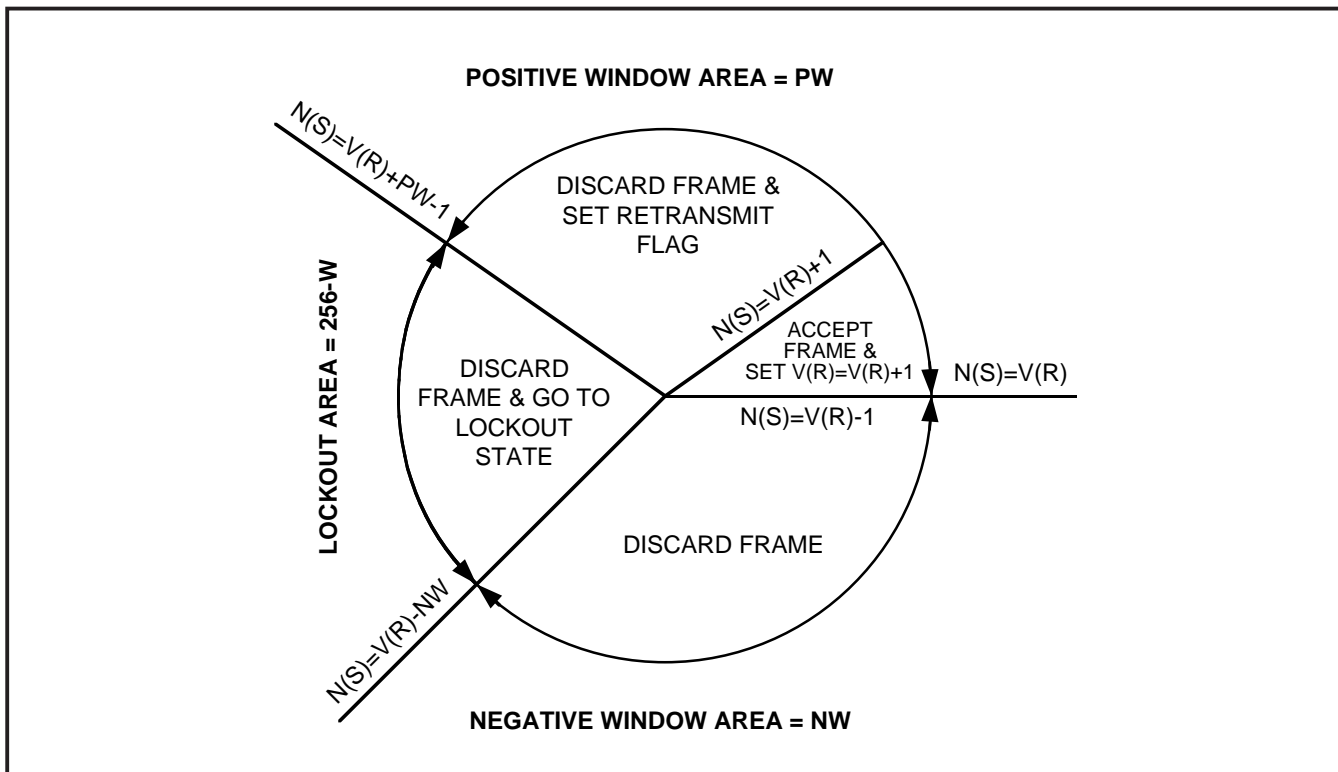


Figure 5: The FARM Sliding Window Concept

A Frame Sequence Number  $N(S)$  falls outside the FARM Sliding Window i.e. in the Lockout Area when:

$$\begin{matrix} N(S) > V(R) + PW - 1 \\ N(S) < V(R) - NW \end{matrix}$$

In this case, the Lockout flag is set.

When  $N(S)$  falls inside the FARM Sliding Window, one of the following three cases can occur:

- First case

$$N(S) = V(R)$$

The frame is accepted

- Second Case

$$\begin{matrix} N(S) > V(R) \text{ and} \\ N(S) \leq V(R) + PW - 1 \end{matrix}$$

The frame is in the positive window and does not contain the expected Frame Sequence Number. The Frame is discarded and the retransmit Flag is set.

- Third Case

$$\begin{matrix} N(S) < V(R) \text{ and} \\ N(S) \geq V(R) - NW \end{matrix}$$

The frame is in the negative window and is discarded without any other action being taken.

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## THE FARM-1 PROCESS DESCRIPTION

At the user end of the FARM-1 process the TC segments are delivered as a buffer of accepted data. No distinction is made between a TC segment delivered by means of an AD frame and one delivered by a BD frame. However, the management of the common FARM-1 back end buffer is affected as follows:

**• BD Frames:**

When a frame of this type is accepted by the FARM-1, the TC segment it contains shall be placed in the back end buffer of the FARM-1 even if this buffer still contains data (partially read or not) in which case this data will be erased, an abort signal sent to the Segment Layer to signal the erasure and the new data signalled as arrived. This implies an Event E10.

**• AD frames:**

When a frame of this type is accepted by the FARM-1, the TC segment it contains is placed in the back end buffer of the FARM-1 only when the buffer is available (empty). If the buffer still contains data, the newly arrived frame is discarded (erased) as shown by the FARM-1 state table (Event E2 in table 1).

The definitions used in the FARM-1 State Table are listed below:

• “Valid frame arrives” means that the Legal Frame Validation Sublayer has placed a legal frame in the front-end buffer. If the frame is a data frame (AD or BD) and if the FARM-1 accepts it, the back end buffer is allocated for the data.

• “Accept” for an AD frame is subject to a buffer available signal. When no back end buffer is available (Event E2) the frame is discarded. The data is then made available for the Authentication Layer, or the Segmentation Layer if Authentication is disabled.

• “Accept” for a BD frame means that the TC segment is placed in the back end buffer even when this buffer still contains data, in which case this previous data is erased (event E10). The Wait concept does not apply to BD frames. The data is available for the Authentication Layer, or the Segmentation Layer if Authentication is disabled.

State Name	OPEN	WAIT	LOCKOUT
Main Feature of State	Normal state to accept frames	Wait Flag is on	Lockout Flag is on
State Number	(S1)	S(2)	S(3)

Event	Conditions		Event Number	OPEN	WAIT	LOCKOUT
Valid AD frame arrives	N(S)=V(R)	A buffer is available for this frame	E1	Accept frame, V(R):=V(R)+1R etransmit Flag:=0  (S1)	Not applicable	Discard  (S3)
	N(S)=V(R)	No buffer is available for this frame	E2	Discard, Retransmit Flag:=1, Wait Flag:=1  (S2)	Discard  (S2)	Discard  (S3)
	N(S)>V(R) and N(S)≤V(R) i.e. inside part of sliding window and N(S)<	+PW-1 positive window and >V(R)	E3	Discard, Retransmit Flag:=1  (S1)	Discard  (S2)	Discard  (S3)

**Table 1: The FARM-1 State Table**

Event Conditions		Event Number	OPEN	WAIT	LOCKOUT
(Cont') Valid AD frame arrives	$N(S) < V(R)$ and $N(S) \geq V(R) - NW$ i.e. inside negative part of sliding window	E4	Discard  (S1)	Discard  (S2)	Discard  (S3)
	$N(S) > V(R) + PW - 1$ and $N(S) < V(R) - NW$ i.e. outside sliding window	E5	Discard  Lockout Flag:=1  (S3)	Discard  Lockout Flag:=1  (S3)	Discard    (S3)
Valid BD frame arrives*		E6	Accept, Increment FARM-B Counter  (S1)	Accept, Increment FARM-B Counter  (S2)	Accept, Increment FARM-B Counter  (S3)
Valid Unlock BC frame arrives		E7	Increment FARM-B Counter, Retransmit Flag:=0  (S1)	Increment FARM-B Counter, Retransmit Flag:=0, Wait Flag:=0  (S1)	Increment FARM-B Counter, Retransmit Flag:=0, Wait Flag:=0, Lockout Flag:=0  (S1)
Valid Set $V(R)$ to $V^*(R)$ BC frame arrives		E8	Increment FARM-B Counter, Retransmit Flag:=0 $V(R) := V^*(R)$  (S1)	Increment FARM-B Counter, Retransmit Flag:=0 Wait Flag:=0 $V(R) := V^*(R)$  (S1)	Increment FARM-B Counter,   (S3)
Invalid frame arrives		E9	Discard  (S1)	Discard  (S1)	Discard  (S3)
Buffer release signal		E10	Ignore  (S1)	Wait Flag:=0  (S1)	Wait Flag:=0  (S3)
CLCW report time		E11	Report value of: $V(R)$ , Lockout Flag, Wait Flag, Retransmit Flag, FARM-B Counter  (S1)	Report value of: $V(R)$ , Lockout Flag, Wait Flag, Retransmit Flag, FARM-B Counter  (S2)	Report value of: $V(R)$ , Lockout Flag, Wait Flag, Retransmit Flag, FARM-B Counter  (S3)

\* Note: Event E6 implies that Event E10 also occurs. When in state S2, an event E6 will lead to state S1.

Table 1: The FARM-1 State Table (continued)

**Buffer Management**

Once the data is validated (Clean, Legal and Frame Validation processes passed), it is transferred from the front-end buffer to the back-end buffer for use by the segmentation layer. Only one back-end buffer is managed by the PTD. This mechanism is depicted in figure 6 below:

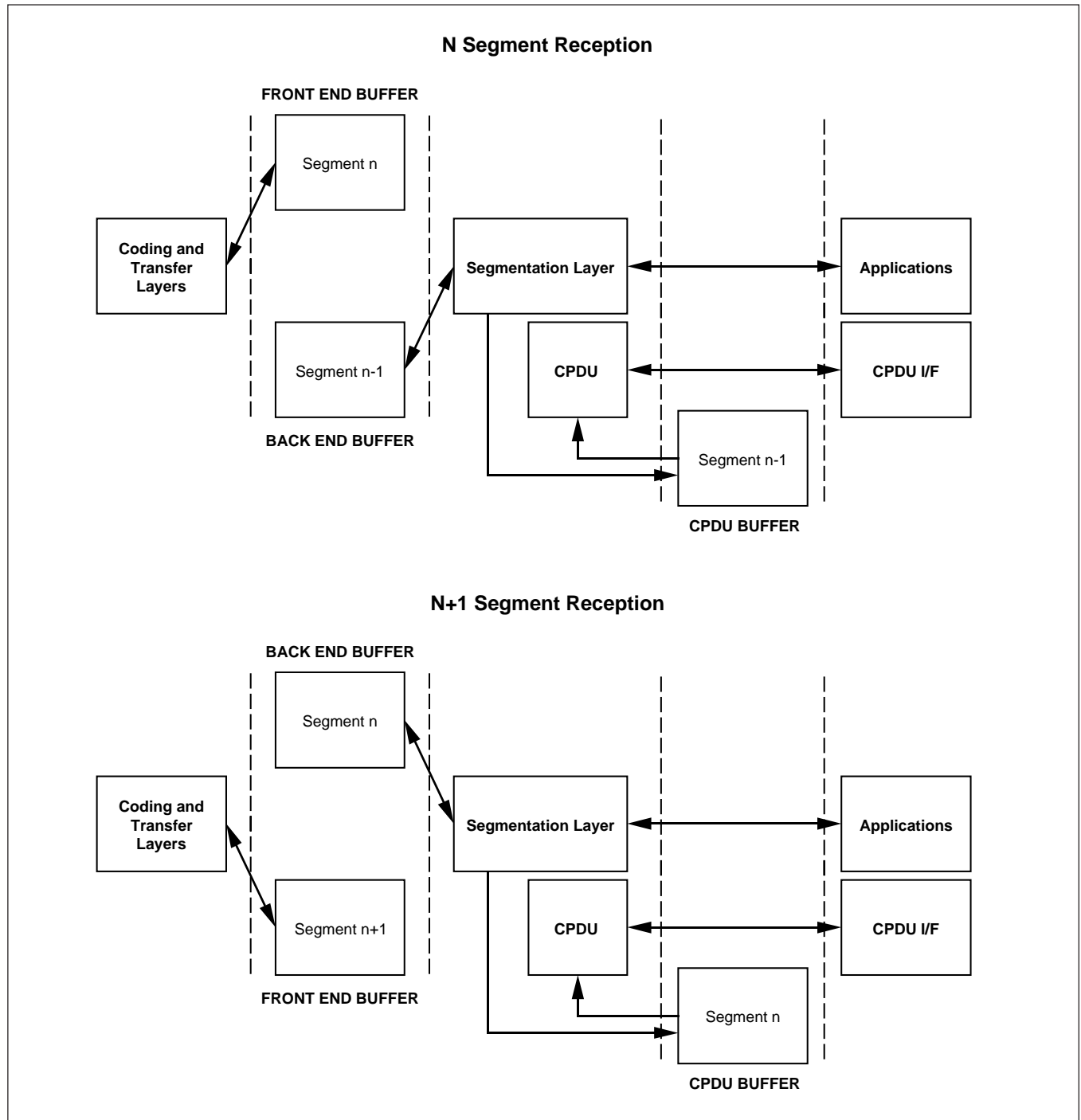


Figure 6: Buffer Management

### 4.3 AUTHENTICATION LAYER

#### Structure of the Authenticated Segments

The TC segment is the protocol data unit of the Segmentation Layer. The general format of an authenticated TC Segment is specified in Section 10 of ref.1. The particular format of an authenticated TC segment for the PTD is the following:

(a) The length of the signature field of the Authentication Tail is 5 octets.

(b) The length of the Authentication Tail is 9 octets (5 octets for the signature + 4 octets for the LAC); the maximum length of the TC Segment is 249 octets (Segment Header (1 octet) + Segment Data Field (239 octets) + Authentication Tail (9 octets)), and its minimum length 10 octets (Segment Header (1 octet) + Authentication Tail (9 octets)).

SEGMENT HEADER		SEGMENT DATA FIELD	SEGMENT TRAILER (optional)
Sequence Flags 2 bits	MAP Identifier 6 bits	variable	9 octets
<-----1 octet ----->		<----- from 9 to 248 octets ----->	

The segment trailer is optional and has a fixed length of 9 octets. The following table summarizes the management of the Segment Trailer.

Type of Authentication	Type of Frame	Segment Trailer
Internal AU	Authenticated frame	segment trailer (9 octets length)
	Not authenticated frame	no segment trailer
External AU	Authenticated frame	segment trailer (9 octets length) if AuTsl=0, no segment trailer if AuTsl=1
	Not authenticated frame	no segment trailer
AU disable	All	no segment trailer

The selection of MAPs that are deemed to carry authenticated TC segments takes into account the possibility to associate MAP IDs in pairs when packet re-assembly is required. Therefore, authenticated MAPs are selected by pairs, using the 5 LSBs of the MAP identifier field of the Segment Header. The selection mechanism is such that it will point at the last pair of MAP identifiers (counting upwards from MAP 0) that carries authenticated segments. The value identifying this particular pair of identifiers is called the Authenticated MAP ID Pointer and is stored in ROM.

For example, selecting MAP 4 (i.e. Authenticated MAP ID Pointer = 4) means that the first 5 pairs of MAPs (i.e. MAP 0 and 32, MAP 1 and 33, MAP 2 and 34, MAP 3 and 35, MAP 4 and 36) are expected to carry authenticated TC segments.

#### Overview of the Layer

This optional layer is implemented on-chip but a connection to an external Authentication Unit is also implemented in case another implementation is desired. The choice of the AU is done by means of a dedicated configuration input AUEXT:

- AUEXT = 1: the internal AU is disabled and the external AU is used,
- AUEXT = 0: the internal AU is used and the external AU is disabled.

MAP 63 is reserved for AU configuration commands when authentication is disabled. It is possible to bypass this layer (when no authentication is required) by means of a dedicated configuration input AUDIS. In this case, segments are passed directly to the segmentation layer. The values of the AUDIS pin are:

- AUDIS = 1: the internal or external AU is disabled,
- AUDIS = 0: the internal or external AU is enabled.

When the AU is disabled, the TC segment does not have an AU tail (the last nine octets are not deleted), the Authenticated MAP ID Pointer has no meaning and MAP 63 is considered as a standard MAP (the data is output on MAP number 63 without removing the AU tail).

An 80 bit length status, AUS, is generated by this block and fetched by the telemetry system in order to send it back to the ground segment.

#### The Authentication Processor

The authentication method specified in references 1 and 2 consists of generating a 40-bit digital signature using a transformation under a secret key applied to the TC Segment. This authentication signature is appended to the TC segment and guarantees to the recipient that the TC Segment is authentic with respect to its sender and its contents.

An incoming TC Segment is authenticated by performing the same transformation made by the transmitting end, and by comparing the received signature with the onboard-generated one. A functional diagram of the Authentication Processor is shown below. There are four main parts:

- the Hashing Function;
- the Hard Knapsack;
- the Deletion Box;
- the Signature Comparator.

They are described in the next four subsections. Not apparent on the functional diagram of Figure 7 is the organisation of the secret Authentication Keys stored in the Authentication Processor. This is described in the section on AU Control Commands on page 18.

THE HASHING FUNCTION

One purpose of the Hashing Function is to compress the variable amount of data bits constituted by the extended message *x* into a pre-signature *P* of fixed length (60 bits). The device realising the Hashing Function is a 60-bit linear feedback shift register (LFSR), as shown in Figure 8. The 60 feedback coefficients *C*<sub>0</sub>, *C*<sub>1</sub>,.....,*C*<sub>59</sub> are part of the Authentication Key.

The LFSR is initialised to the 60-bit value *P*' = 1000....000 (where Bit *P*<sub>0</sub> = 1) before the process of each authenticated TC Segment begins. *P* will be the value in the LFSR after the last bit of the variable-length extended message *x* has been shifted in. The extended message *x* (*x* = [*m*,*l*,*z*]) consists of the following data elements, placed one after the other in that order:

- the received message *m*, i.e., the TC Segment (variable from 1 to 240 octets) without the Authentication Tail;
- the received LAC value *l*, i.e., 4 octets (2 bits of LAC ID, plus 30 bits of LAC Count);
- three octets of virtual fill *z*, consisting of 24 zeros.

The purpose of the 24 bits of virtual fill is to ensure that the Hashing Function is provided with a minimum of data bits. The 24 bits of virtual fill *z* are generated by the PTD. Note that since *m* (the TC Segment) cannot be equal to zero, the total length of an authenticated TC Segment (i.e., [*m*,*l*,*s*]) cannot be smaller than 10 octets (Segment Header (1 octet) + Authentication tail (9 octets)). Anything smaller than 10 octets is rejected as being too short.

THE HARD KNAPSACK

The purpose of the Hard Knapsack is to ensure that it is not possible to deduce the presignature *P* from the signature *S*. The Hard Knapsack is based on the concept of the modular knapsack. It consists of 60 weights (numbered from *W*<sub>0</sub> to *W*<sub>59</sub>, each weight being 48 bits long) and is defined by the following transformation:

$$S' = (\sum_{j=0}^{j=59} P_j W_j) \text{ mod } 2^{48}$$

where the bits *P*<sub>*j*</sub> of the presignature *P* select the corresponding weights *W*<sub>*j*</sub> of the knapsack.

The result is the 48-bit knapsack sum *S*'. The most significant bit of the sum is called *S*'<sub>0</sub>.

THE DELETION BOX

The Deletion Box deletes the 8 least significant bits of the 48-bit knapsack sum *S*', i.e., bits *S*'<sub>40</sub> through *S*'<sub>47</sub>. The result is the 40-bit authentication signature *S* (numbered from Bit 0 to Bit 39, as for signature *s*).

THE SIGNATURE COMPARATOR

The Signature Comparator compares the received 40-bit signature *s* with the onboard generated 40-bit signature *S*.

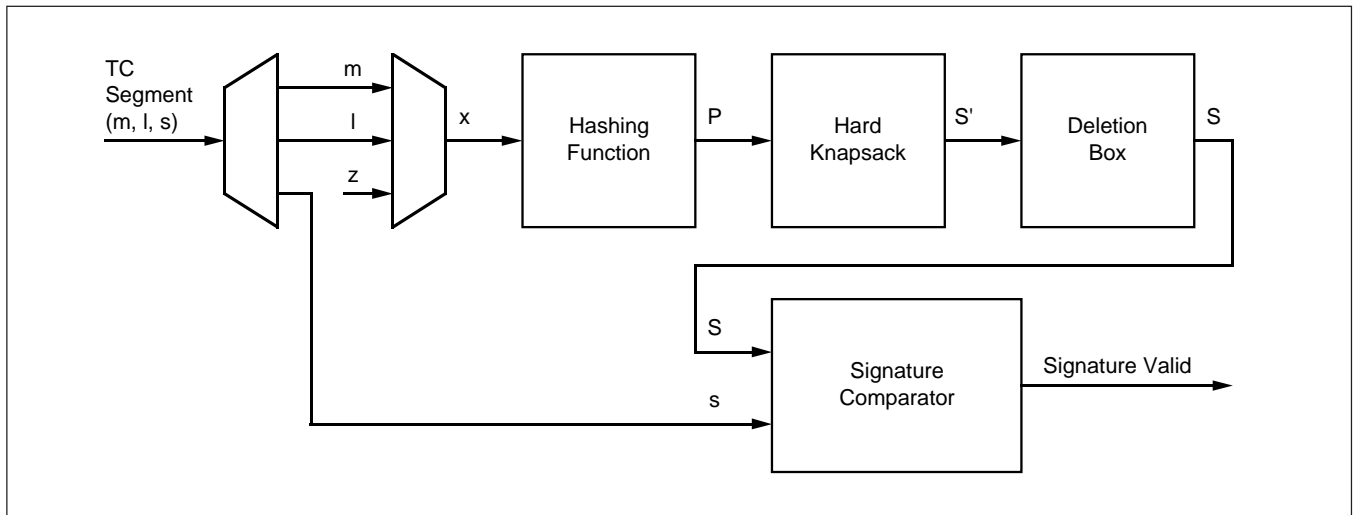


Figure 7: Functional Diagram of the Authentication Processor



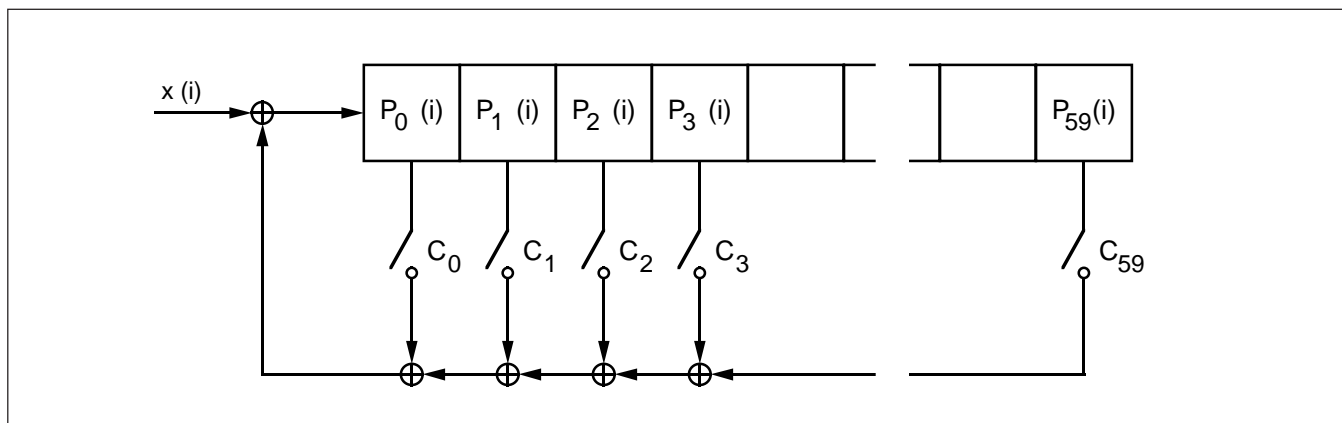


Figure 8: Realisation of the Hashing Function

### THE AUTHENTICATION KEY

The Authentication Key consists of:

60 x 48-bit Hard Knapsack Weights = 2880 bits = 360 octets

60 x 1-bit Hashing Function coefficients = 60 bits = 8 octets

Full Authentication Key = 2940 bits = 368 octets

The system includes two such 2940-bit keys:

- a fixed, mission-unique Authentication Key, called the Fixed Key;
- an in-flight programmable Authentication Key, called the Programmable Key.

#### (a) Fixed Key

The Fixed Key is required for start-up and emergency (recovery) operations. The Fixed Key is stored in the external ROM as part of the Mission-Specific Data.

#### (b) Programmable Key

The Programmable Key is required for all normal operations. The contents of the Programmable Key reside in the RAM where it can be modified by means of Authentication Control Commands specifically defined for that purpose. The format of these Change Programmable Key Block Control Commands, which are specified in the section on AU Control Commands (page 18), allows any 5-octet block to be modified starting at any of the 368 octet boundaries.

### The Supervisor

The Supervisor consists of four main parts:

- the Logical Authentication Channel (LAC) Registers;
- the Final Authorisation Function;
- the Control Command Processor;
- the Deletion Function.

They are briefly described in the next four subsections.

### THE LAC COUNTERS

A LAC Counter is basically a 30-bit counter which is used to associate every TC segment with an authentication sequence number. The purpose of this number is to protect the system against attacks by ensuring that identical TC segments will not have the same signature except at very large intervals of time. The LAC counter is incremented by one every time a TC segment is successfully authenticated (and only then). The LAC counter value used for authenticating each TC segment is uplinked with each signature.

Three LAC Registers are provided:

- one Principal LAC register (LAC ID = 00);
- one Auxiliary LAC register (LAC ID = 01);
- one Recovery LAC register (LAC ID = 10).

Bits 0 and 1 of the LAC are fixed in order to select the LAC Register to be used for the final authorisation of a TC Segment. For what concerns the 30 bits of LAC Count (Bits 2 through 31, where the LSB is Bit 31), they are implemented as follows:

- The Principal and Auxiliary LAC counters have 30 bits.
- The Recovery LAC counter has 8 bits (the LSBs 24-31) whereas the remaining 22 bits (2-23) are permanently set to 1.

### THE FINAL AUTHORISATION FUNCTION

When the received signature  $s$  of a TC Segment compares with the onboard-generated signature  $S$ , the contents of the received LAC Count field is compared with the contents of the indicated LAC Register. If both contents are found equal, there are two cases:

- The TC Segment was transferred on a MAP to be authenticated with a MAP ID lower or equal to the MAP ID pointer. In this case, the TC Segment is authorised for transfer to the Segmentation Layer.

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- The TC Segment was transferred on MAP 63 (i.e., MAP 111111), which is dedicated to the transfer of Authentication Control Commands. In this case, the Control Command Processor is authorised to further process the TC Segment, which will never be transferred to the Segmentation Layer.

In both cases, the contents of the indicated LAC Register is incremented by one.

### THE CONTROL COMMAND PROCESSOR

The function of the Control Command Processor is to execute the special TC Segments called Authentication Control Commands after being authorised by the Final Authorisation Function. The formats of the various Authentication Control Commands are specified in the section on AU Control Commands next. Any TC Segment not conforming to the specified formats (i.e., both in length and in contents) are rejected and reported as not executable.

### THE DELETION FUNCTION

The Deletion Function deletes the Authentication Tail of all TC Segments authorised by the Final Authorisation Function. The complete authentication process is meant to be transparent to an observer placed at the receiving end of the Segmentation Layer.

### AU Control Commands

It is necessary to differentiate TC Segments containing the Authentication Control Commands required to reconfigure the AU. This is done by allocating the TC Segment Header contents "all ones" to these particular segments, i.e.:

- Sequence Flags set to 11 (Unsegmented)
- MAP ID set to 111111 (MAP63)

TC Segments containing the Authentication Control Commands shall always be authenticated. The formats of the Authentication Control Commands are organised in three groups as follows:

- One octet of TC Segment Header for all three groups.
- One octet following the Segment Header to specify the Control Command Identifier
- Zero, four or eight octets of Control Command Data Field, depending on the group.

Table 2 gives the complete list of Authentication Control Commands, with Group numbers, Control Command IDs and Command Names. Table 3 shows the format of the TC Segment for each Group, complete with Authentication Tail. Each Control Command is specified in the next subsections.

### DUMMY CONTROL COMMAND

The purpose of this command is to serve as NOP (No Operation) for testing purposes. After being authenticated, this Control Command will have no effect. However, since the AU has authenticated the Dummy Segment, the contents of the LAC Register used during the authorisation process have been incremented and a telemetry report prepared accordingly.

### SELECT KEY CONTROL COMMANDS

#### (a) Select Fixed Key

The AU selects the Fixed Key prior to authenticating the TC Segment:

- If authentication is successful, the Fixed Key remains selected.
- If authentication is unsuccessful, the key previously in use remains selected.

#### (b) Select Programmable Key

The AU selects the Programmable Key for authentication of the TC Segment:

- If authentication is successful, the Programmable Key remains selected.
- If authentication is unsuccessful, the key previously in use remains selected.

### LOAD FIXED KEY IN PROGRAMMABLE KEY MEMORY CONTROL COMMAND

This command reloads the Fixed Key set in the Programmable Key memory with a single command instruction. The key used for authenticating the TC Segment containing the Control Command will be whatever key was selected in the AU at the time the command was transmitted.

### SET NEW LAC COUNT VALUE CONTROL COMMAND

The purpose of this Control Command is to set the value of one of the three programmable LAC Counters: Principal, Auxiliary or Recovery with LAC Identifiers 00, 01 and 10 respectively. If the LAC Identifier is set to 11, the command is not executed and reported as not executable. As soon as the TC Segment is authorised by the authentication process, the specified LAC Count value is forced into the selected LAC Register. Note that the 22 MSBs of the 30-bit Recovery LAC Register are permanently set to all ones, therefore those same bits in a Set New Recovery LAC Count Value Control Command are ignored by the AU. The key used for authenticating the TC Segment containing the Control Command will be whatever key was selected in the AU at the time the command was transmitted.

GROUP	CONTROL COMMAND IDENTIFIER (8 BITS)	COMMAND NAME
GROUP 1	0000 0000	DUMMY
	0000 0101	SELECT FIXED KEY
	0000 0110	SELECT PROGRAMMABLE KEY
	0000 0111	LOAD FIXED KEY IN PROGRAMMABLE KEY MEMORY
GROUP 2	0000 1001	SET NEW LAC COUNT VALUE
GROUP 3	0000 1010	CHANGE PROGRAMMABLE KEY BLOCK A
	0000 1011	CHANGE PROGRAMMABLE KEY BLOCK B

Table 2: List of Authentication Control Commands

1 octet	1 octet	9 octets
Segment Header	Control Command Identifier	Authentication Tail
11111111	00000***	LAC+Signature

Group 1 Control Command, 11 Octets

1 octet	1 octet	4 octets		9 octets
Segment Header	Control Command Identifier	LAC value to be set		Authentication Tail
11111111	00001001	LAC ID 2 bits	LAC Count 30 bits	LAC + Signature

Group 2 Control Command, 15 Octets

1 octet	1 octet	1 octet	7 octets	9 octets
Segment Header	Control Command Identifier	Start Address of new 40 bit Keyblock	Key specific pattern to be encoded	Authentication Tail
11111111	0000101*			LAC+Signature

Group 3 Control Command, 19 Octets

Table 3: Formats of Authentication Control Commands (Full TC Segment)

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## CHANGE PROGRAMMABLE KEY BLOCK CONTROL COMMANDS A AND B

Two such Control Commands are provided to cover the full size of the Programmable Key:

- Command A concerns the first 256 octet boundaries.
- Command B concerns the last 112 octet boundaries.

It is possible to load a 5-octet (40 bits) block starting from any of the 368 octet boundaries. Any transmission using the unused boundaries of Command B (from 113 to 255) is ignored and reported as non-executable. The key used for authenticating the TC Segment containing one of these Control Commands will be whatever key was selected in the AU at the time each Control Command was received. Once the TC Segment has been authorized by the authentication process, the TC Segment, minus the 40-bit signature *s* (i.e. [m,l]) is complemented and passed once more through the

signature-building process, i.e. through the Authentication Processor. The 24 bits of virtual fill *z* are inserted as before, i.e., they are not complemented, but remain all zeros. The result of the process is a 40-bit pseudo-signature which, instead of being sent to the Signature Comparator, is loaded in the Programmable Key memory, starting at the octet location indicated by the start address field, as follows:

- Bits 32 through 39 of pseudo-signature at the indicated octet location;
- Bits 24 through 31 of pseudo-signature at the next location (start address + 1);
- And so on, until Bits 0 through 7 are loaded at location start address + 4.

Any arbitrary procedure can be used for changing the key, starting from any of the 368 octet boundaries.

RAM Mapping	Address provided in the Control command (decimal)		
Bank A	200	000	40 <b>W0 (40 to 47)</b> 47
	201	001	32 <b>W0 (32 to 39)</b> 39
	202	002	24 <b>W0 (24 to 31)</b> 31
	203	003	16 <b>W0 (16 to 23)</b> 23
	204	004	8 <b>W0 (8 to 15)</b> 15
	205	005	0 <b>W0 (0 to 7)</b> 7
	206	006	40 <b>W1 (40 to 47)</b> 47
	207	007	32 <b>W1 (32 to 39)</b> 39
	2FF	255	16 <b>W42 (16 to 23)</b> 23
	Bank B	300	000
367		103	0 <b>W59 (0 to 7)</b> 7
368		104	59 <b>C (59 to 56)</b> 56
369		105	55 <b>C (55 to 48)</b> 48
36A		106	47 <b>C (47 to 40)</b> 40
36B		107	39 <b>C (39 to 32)</b> 32
36C		108	31 <b>C (31 to 24)</b> 24
36D		109	23 <b>C (23 to 16)</b> 16
36E		110	15 <b>C (15 to 8)</b> 8
36F		111	7 <b>C (7 to 0)</b> 0

Note: Bit 0 is the MSB

Figure 9: Organisation of the Programmable Key Memory

## 4.4 SEGMENTATION LAYER

### Overview of the Layer

The segmentation layer provides the means to distribute several distinct streams of variable-length data units (e.g. the TC packets) to different applications by providing a number of service access points called the Multiple Access Points (MAPs). The data flow on each stream can be controlled by the receiving application using handshake control.

A TC segment consists of three distinct protocol data elements:

- an 8-bit segment header, the purpose of which is to identify the MAP connection and flag the sequential position of the segment relative to the complete TC Packet,
- a segment data field, of maximum length 248 octets, which contains all or a portion of a TC Packet,
- the 9-octet Segment Trailer specific to authenticated segments is removed by the authentication layer.

### Standard Data Structures Within the Layer

The structure of the TC segment is given below:

SEGMENT HEADER		SEGMENT DATA FIELD
Sequence Flags 2 bits	MAP Identifier 6 bits	
		variable

<----- 1 octet -----><- from 0 to 248 octets ->

### Segment Header

The Segment Header is the first octet (octet 0) of the TC segment structure. The Segment Header is divided into two major fields as follows:

- Sequence Flags (bits 0 & 1): this field is used by the segmentation protocol to indicate the sequential position of the segment relative to the complete data unit (e.g. the TC Packet). The flags are interpreted as follows:

Bit 0 (MSB)	Bit 1	Interpretation
0	1	First segment
0	0	Continuation segment
1	0	Last segment
1	1	Unsegmented

When the flags are set to 11 this means that the TC Segment Data Field contains an entire TC Packet. Except for the CPDU described in section 4.5, these flags are ignored by the PTD.

- Multiplexed Access Point (MAP) Identifier: this 6-bit field enables up to 64 MAP connection addresses to be associated with a single Virtual Channel. The PTD supports MAP 1 to 63 as externally available MAPs. MAP 0 is dedicated to the CPDU. MAP 63, when AU is enabled, is reserved for AU commands; when the AU is disabled, MAP 63 is processed by the segment layer like a standard MAP (see section 4.3).

### Segment Data Field

The segment data field may vary from 0 to 248 octets maximum. When the optional Segment Trailer is used, the maximum length of the segment data field will be reduced by 9 octets.

### Standard Procedures Within the Layer

The following segmentation layer functions are implemented in the PTD:

- the back-end buffer for the accepted TC segment. The back-end buffer is shared between the Transfer Layer and the Segmentation Layer.
- the MAP interface.

Upon reception of a new segment the Segment Layer performs the following operations:

- Checks whether the segment is authenticated or not.
- Starts the AU process if the segment is authenticated and if the AU is not disabled. The Segment Layer waits for the completion of the AU process (internal or external). A security mechanism is implemented, in case of AU locking mechanism the user can stop the AU process by activating the AU disable signal. In this case, the segment layer stops waiting for the AU completion process and the content of the back end buffer is lost.
- Checks if the frame is a CPDU command (MAP 0). In this case, the CPDU layer is activated and no data is output on the MAP interface.
- Checks if the frame is an AU command (MAP 63) and the AU is not disabled. In this case no data is output on the MAP interface.
- For a MAP 1 to 62 and for MAP 63 if the AU is disabled, the data is provided in serial or in parallel via the MAP interface. The MAP output frequency for serial MAP is selectable by reading a value associated with each MAP in the external ROM (see section 5.2).

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## 4.5 COMMAND PULSE DISTRIBUTION UNIT

### General Requirements

The CPDU is a simple unit that is solely accessible from ground. The aim of this unit is to generate pulses to drive certain actuators (e.g. relays). The CPDU is identified by the Application Process Identifier placed in the TC Packet Header. The Application Identifier of the CPDU is programmable in ROM at addresses 006 and 007.

### Functional Description

The CPDU receives TC segments, each segment containing a complete TC Packet. TC segments having a MAP equal to zero are carrying CPDU commands. It must be noted that if the internal AU is enabled, MAP0 segments are always authenticated. When a new segment carrying CPDU commands has arrived, two cases are possible:

- the CPDU is still executing previous CPDU commands. In this case, the incoming TC segment is ignored, whether it was transferred in an AD or BD transfer frame.

- the CPDU is idle. The incoming TC segment is copied from the back end buffer to the CPDU buffer for checking and execution by the CPDU.

An important point must be noted: there is no packetisation layer abort command associated with the CPDU. Once it has accepted a TC Packet, the CPDU cannot release it until all command instructions specified in that packet have been executed.

The CPDU performs first the clean validation process which verifies the complete packet (CRC, packet length, segmentation flags). If the clean validation process is successful, the CPDU performs the legal validation process, which checks the content of the Packet Headers. The result of the two previous verifications is reported in the 16 bits CPDU status. For a dirty or illegal CPDU Packet, the CPDU buffer is erased. The execution of the CPDU commands is possible only if all the verifications succeed.

### Checking the CPDU-Specific TC Packet

The CPDU Packet format is shown below:

PACKET HEADER (48 bits)						PACKET DATA FIELD (variable)			
PACKET IDENTIFICATION				PACKET SEQUENCE CONTROL		PACKET LENGTH	DATA FIELD HEADER	APPLICATION DATA	PACKET ERROR CONTROL
version number	type	data field header flag	application process ID	Sequence Flags	Packet Name or Sequence Count				
3	1	1	11	2	14	16	variable	variable	16
16				16					

A short description of the fields of the CPDU Packet is given below:

- version number: 3-bit field occupying the 3 MSBs of the packet header. To be compliant with ref.1, these 3 bits should be 000.

- type bit: this bit identifies if the Packet is telemetry type (type bit = 0) or telecommand type (type bit = 1). To be compliant with ref 1, this bit should be set to 1.

- data field header flag: this indicates the presence (data field header flag = 1) or absence (data field header flag = 0) of a data field header within the packet data field. To be compliant with ref 1, this bit should be set to 0.

- application process identifier: this field identifies the particular process to which the CPDU Packet is sent.

- sequence flags: this two-bit field indicates if the packet is a first, last or intermediate component of a higher layer data structure. For CPDU Packets, these two bits shall be equal to 11.

- packet sequence count: this 14-bit field allows a particular TC Packet to be identified with respect to others occurring within a telecommand session. This field is reported in the CPDU status for clean and legal CPDU packets.

- packet length: this field specifies the number of octets contained within the packet data field, by indicating the number of octets in data field minus 1.

- packet data field: this field contains the CPDU commands and the CRC for packet error control.

The CPDU Packet is checked in two steps: the clean validation process and the legal validation process. The clean verification process performs the following tests:

- correct CRC (last two octets of the Packet contain a 16-bit CRC calculated using the same algorithm as used for the TC transfer frame, see section on transfer frame) to verify that there is no error in the Packet.

- the TC Segment Segmentation Flags (in Segment Header) are equal to 11.

- the CPDU Packet length is checked to be an even number of octets, greater than or equal to 10 octets and less than or equal to 248 octets:  $10 \text{ octets} \leq \text{TC Packet length} = \text{even number of octets} \leq 248 \text{ octets}$ . The CPDU Packet length is read from Packet Header octets 5 and 6.

- consistency between the actual number of octets making up the CPDU Packet and the Packet length field. To achieve this, the Packet Header octet 5 is checked to be zero and the Packet Header octet 6 is checked to be consistent with the effective packet length.

At this level, if the packet is found to be error-free, it is declared clean and the process continues. Otherwise, the complete CPDU packet is erased.

The legal verification process performs the following tests on the Packet Header (see ref 1, Section 8):

- the first octet of the Packet Header (version number & type bit & data fields header flag & 3 MSBs of Application Process Identifier) is compared with the value programmed in ROM at address 006.

- the second octet (8 LSBs of Application Process Identifier) is compared with the value programmed in ROM at address 007.

- in the third octet (sequence flags & 6 MSBs of packet name or sequence count), only the sequence flags field is checked by the PTD to be equal to 11. The packet name or sequence count is not verified, it is only reported in the CPDU status.

- the fourth octet (8 LSBs of packet name or sequence count) is not tested since the packet name or sequence count is not verified. It is only reported in the CPDU Status.

If the above check succeeds, the TC Packet is declared legal and its Application Data (command instructions) read out and executed as described in the next subsection. If the check fails, the Packet is erased.

## Processing the Application Data

The CPDU receives a segment from the segment layer and stores it for further processing in the CPDU buffer provided in RAM. At the same time, the clean process is performed. This segment duplication is necessary due to delayed command execution. The duration of the transfer is equal to:

$$T_d = N_b * T_{acc}$$

where  $N_b$  is the number of octets of the TC segment (including AU tail), and  $T_{acc}$  is the duration of three RAM accesses Read - Write - Read (the last read is used for computing the CRC with data effectively stored in RAM).  $T_{acc}$  can be estimated to  $20 * T_{ck}$  (5  $\mu$ s for a clock frequency of 4 MHz).

The application data of the CPDU packet should consist of at least one command instruction in the form of one double octet, or several of such double-octet command instructions, up to the maximum capacity.

Each double octet should be formatted as follows:

- first octet: specifies one of 256 Command Pulse outputs. The command distribution shall be made by an external demultiplexer (256 possible command pulse outputs).

- Second octet: specifies the duration of the Command Pulse to be issued on the specified output as follows:

- the 5 MSBs are ignored by the CPDU,

- the 3 LSBs specify the duration of the Command Pulse, which is equal to about  $2^X$  multiplied by D where X is the value of the 3 LSBs and

$D = 40960$  clock periods for CPDUDIV=0,

$D = 8192$  clock periods for CPDUDIV=1.

(see section 5.5 for exact figures.)

When there is more than one command instruction in the CPDU Packet, each instruction is executed one after the other in the same sequence as in the packet.

The maximum capacity of the CPDU packet is:

- 248 octets corresponding to 120 command instructions if the Internal or External Authentication Unit is disabled (AUDIS=1) or if the External Authentication Unit is enabled (AUEXT=1 and AUDIS=0) and AUTSL=1.

- 238 octets corresponding to 115 command instructions if the Internal Authentication Unit is enabled (AUEXT=0 and AUDIS=0) or if the External Authentication Unit is enabled (AUEXT=1 and AUDIS=0) and AUTSL=0.

For the calibrated pulses being output on the CPDUEN pin, the pulse amplification shall be made by external hardware. The CPDU provides a 16 bit status, CPDUS, that can be fetched by the telemetry system. The different fields of the CPDU status are detailed later.

4.6 TELEMETRY REPORTING

General Description

Telemetry reporting is essential to the normal operation of the telecommand data communication system.

Data Reports are not modified during telemetry readout. In particular they are not affected by the arrival of new report data. If the telemetry interface sampling rate is slower than the rate at which new data reports are generated, a double register mechanism ensures that the complete data report is read out.

CLCW Status Report

The Command Link Control Word (CLCW) is a standard reporting data structure of the Packet Telecommand System. It is a four-octet word generated by the spacecraft, the PTD generating only the 2 least significant octets of this CLCW which are described hereafter.

Bits	Value	Meaning
0 (MSB)	0	No RF Available
1		No Bit Lock
2		Lock Out
3		Wait
4		Retransmit
5,6		FARM B Counter
7		Report Type
8 - 15 (LSB)		Report Value

Each CLCW field is specified in the next paragraphs:

- No RF Available. This field is dedicated to the Physical Layer, i.e. the RF Transponders. When this field is 1, the RF physical connection is not available through any of the spacecraft transponders. When it is 0, the RF connection is available through at least one of the spacecraft transponders. This information is provided to the PTD by an input pin called RFAVN.
- No Bit Lock. This field is dedicated to the Physical layers, and monitors the presence of the spacecraft demodulation. When this field is 1, all the TC Active Signals (0 to 5) are zero at the PTD input pins. When it is 0, at least one of the TC Active signals is set to 1.
- Lockout Flag. If 1, this field indicates that the FARM- 1 is in the Lockout state.
- Wait Flag. If 1, this field indicates that the FARM- 1 is in a Wait state.
- Retransmit Flag. If 1, this field indicates that an AD frame has been lost in transmission or has been discarded because there was no buffer space available.
- FARM B counter. This 2 bit field contains a wraparound up-counter (modulo 4) of each TC frame of type BC or BD declared valid by the Legal Frame Validation process, and therefore acceptable by the FARM-1.
- Report Type. In the PTD it is always 0 in accordance with reference 1.

- Report Value. This field is maintained by the FARM-1 and contains the next expected frame sequence number V(R).

The first bit to be read in serial mode is Bit 0 (MSB). The interface for reading the CLCW status is specified in section 5.3.

CPDU Status Report

The CPDU Status report consists of 16 bits of status data formatted as follows:

Bits	Value	Meaning
0,1	00	Cold Start
	01	Last TC Packet accepted legal
	10	Last TC Packet accepted clean, but erased as not legal
	11	Last TC Packet erased as not clean
2 - 15 (LSB)	all 1 all other values	Cold Start Packet Sequence Count (or Name) of last legal CPDU Packet

The first bit to be read out in serial mode is Bit 0 (MSB). Legal and Clean concepts are defined previously. The telemetry interface used to read out the CPDU Status Report is fully described in section 5.3.

AU Status Report

The AU Status Report consists of 80 bits (i.e. 10 octets) of status data formatted as follows:

Bits	Value	Meaning
0,1	00	Permanently set to 00
2 - 31		Current value of the contents of the Principal LAC counter. The LSB of the LAC counter value is in bit 31
32,33	01	Permanently set to 01
34 - 63		Current value of the contents of the auxiliary LAC counter. The LSB of the LAC counter value is in bit 63
64	0000000	Key in use by AU: 0 fixed key in use 1 Programmable key in use
65 - 71		Permanently set to 0 (reserved for future use)
72 - 79 (LSB)	0000000	Current value of the 8 LSBs of the recovery LAC counter. The LSB of the LAC counter value is in bit 79.

The first bit to be read in serial mode is bit 0 (MSB). The AU Status report is implemented by using a double register mechanism located in the external RAM. In the case of external AU, the external AU can write the AU Status in RAM. The number of the buffer is given by the AUS pin and the toggling mechanism of the AU Status buffer is locked by the PTD when the signal AUST ( External AU Start) is high. The telemetry interface used to read the AU status report is described in section 5.3.



## Frame Analysis Report

The FAR is required for proper testing and check-out of the TC Decoder. The FAR consists of 32 bits of survey data formatted as follows:

BITS	VALUE	MEANING
0 (MSB)	0	STATUS OF SURVEY DATA New survey data (or Cold Start)
	1	Old survey data
1,2,3		FRAME ANALYSIS Note: The report of the lowest rank (i.e. of lowest 3-bit value) has precedence in case of conflicting states.
	000	Abandoned CLTU (see Note 1)
	001	Frame declared dirty
	010	Frame declared illegal for one reason
	011	Frame declared illegal for multiple reasons
	100	Frame (AD) discarded because of LOCKOUT
	101	Frame (AD) discarded because of WAIT
	110	Frame (AD) discarded because of N(S) or V(R)
	111	Frame (AD, BD or BC) Accepted by FARM-1
	4,5,6	
000		No illegal report (or Cold Start)
001		Error in fixed fields (Version & Reserved)
010		Illegal combination (AC) of Bypass & Control Command Flags
011		Wrong Spacecraft ID
100		Wrong VC ID (because of Bits 0 to 4 of ID)
101		Wrong VC ID (because of Bit 5 of ID)
110		N(S) of BC or BD frame not set to all 0
111		Wrong BC frame data format (not executable)
7 - 12		xxxxxx
13,14,15	xxx	COUNT OF SINGLE-ERROR CORRECTIONS PER CLTU Straight 3-bit binary count, saturates at maximum value, no roll over. (Cold Start value:000)
16,17		LEGAL FRAME QUALIFIER (4 STATES)
	00	AD frame
	01	No report on legal frame (or Cold Start)
	10	BD frame
18,19,20		SELECTED CHANNEL INPUT (MAXIMUM CAPABILITY : 6 INPUTS)
	xxx	(Cold Start value : 111)
21 - 26	xxxxxx	LAST MAP ADDRESSED (64 MAPS) (Cold Start value : 111111)
27	0	RESERVED BY ESA (set to 0)
28,29,30		AUTHENTICATION PROCESS ANALYSIS
	000	No authentication report (or Cold Start)
		AUTHORISED SEGMENT QUALIFIER
	001	Authorised data segment
	010	Authorised (and executable) Authentication Control Command
	011	Authorised dummy segment received

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<b>BITS</b>	<b>VALUE</b>	<b>MEANING</b>
		<b>REJECTED SEGMENT QUALIFIER</b>
	100	Error in Signature
	101	Error in LAC
	110	Wrong format (not executable) of authorised Authentication Control Command (includes Segment Header)
	111	Wrong length of TC Segment prior to being authenticated (authorised), i.e. length shorter than 10 octets
31 (LSB)	0	set to 0

A few specific points need to be detailed:

Note 1: The abandoned CLTU state (000) is used to indicate:

- the Cold Start
- a first TC codeblock of CLTU was abandoned (erased) because of event 4 or event 2
- an event E2(a) channel deactivation occurs (see section 4.1)
- an event E2(b) CLTU error occurs (see section 4.1)

In the case of an Abandoned CLTU the Legal/Illegal Frame Qualifier (bits 4, 5, 6) is set to 000 and the Legal Frame Qualifier (bits 16, 17) is set to No Report on Legal Frame (01).

Note 2: The rejected segment qualifier in the Authentication process analysis has the following prioritisation:

- 111 Too short TC segment has the highest precedence, followed by
- 100 Error in Signature, followed by
- 101 Error in LAC, followed by
- 110 Wrong format of AU command or segmentation flags.

The FAR is sampled and read by a telemetry interface described in section 5.3.

## 5. PTD INTERFACES

### 5.1 PHYSICAL CHANNEL INTERFACE

Each TC channel consists of 3 input lines:

- TCC<sub>i</sub>: symbol clock input
- TCS<sub>i</sub>: symbol stream input (NRZ-L)
- TCA<sub>i</sub>: channel active indication input

The maximum symbol rate with guaranteed operation (using the internal AU) on these channels is 50 kbps. For higher frequency, an incomplete AU process may occur resulting in wrong signature calculation and thus rejected frames. Without AU the symbol rate could be 200 kbps (not guaranteed). At higher frequency, incorrect processing may occur due to insufficient time to perform memory accesses. The interface is composed of 6 TC channels. Figure 10 below gives the timing associated with one of these 6 channels. For unused channels, the TCA<sub>i</sub> signal should be connected to V<sub>SS</sub>, and the TCC<sub>i</sub> and TCS<sub>i</sub> signals to V<sub>DD</sub>.

The DECOD output is activated when the CLTU decoder state machine is in the decode state (see section 4.1). This output goes high following the detection of a start sequence, and goes low following a codeblock rejection or CLTU error.

### 5.2 MAP INTERFACE

The MAP interface allows the PTD to provide the on-board applications with the TC segments stored in the back-end buffer in the RAM. It is possible to transfer full TC segments (including segment header and packet segment) with various lengths, from 1 octet to 249 octets. The first data output is the TC segment header. It is possible for an application to use either a serial or parallel interface to read this TC data. The choice between serial or parallel interface is made with the configuration input pin PAR as follows:

- PAR = 1; the parallel MAP interface is used (section 5.4)
- PAR = 0; the serial MAP interface is used

The serial MAP interface consists of 5 signals.

- MAPDSR, data set ready output,
- MAPDTR, data terminal ready input,
- MAPCK, MAP clock output,
- MAPDATA, segment data output,
- MAPADT, aborted data transfer output.

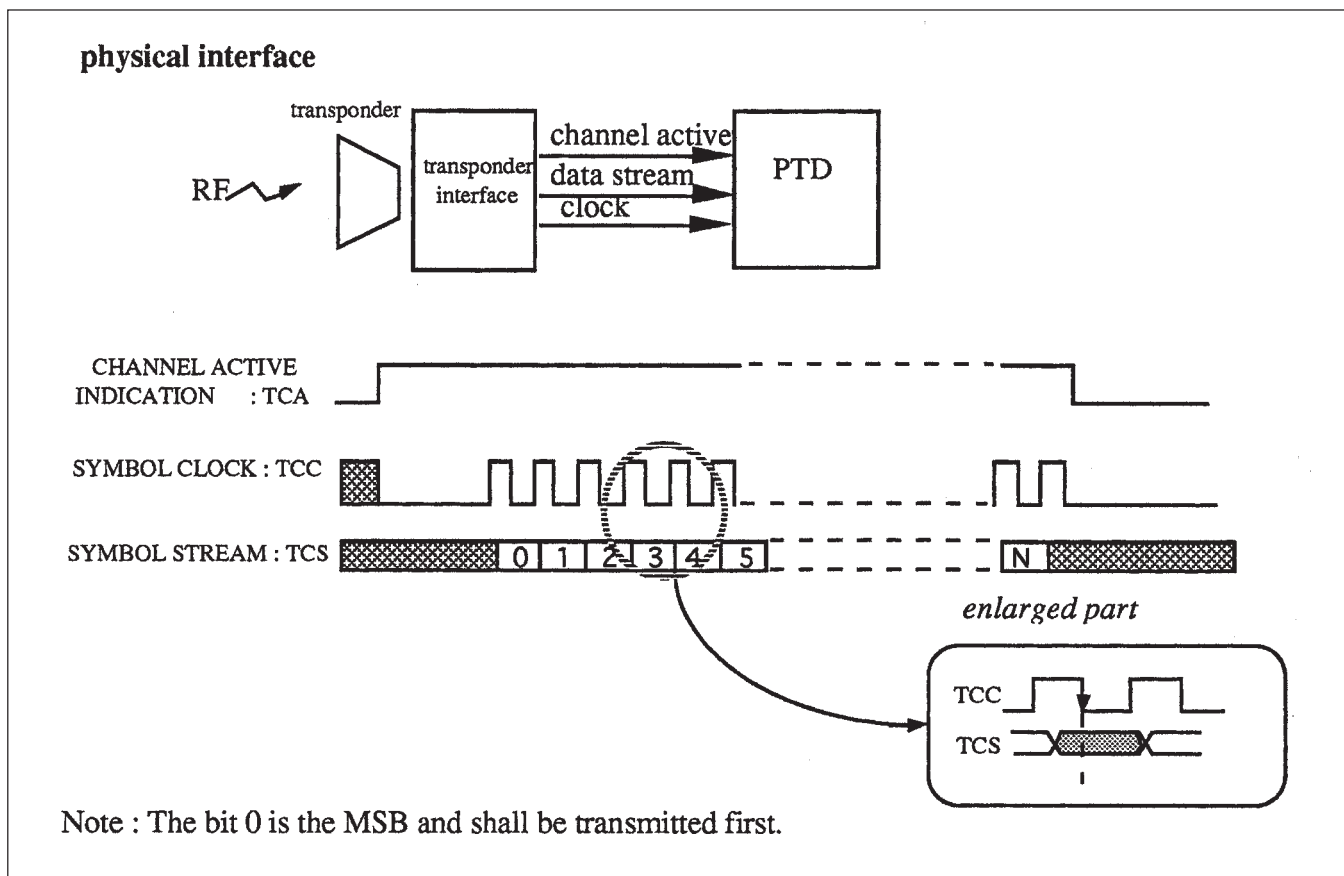


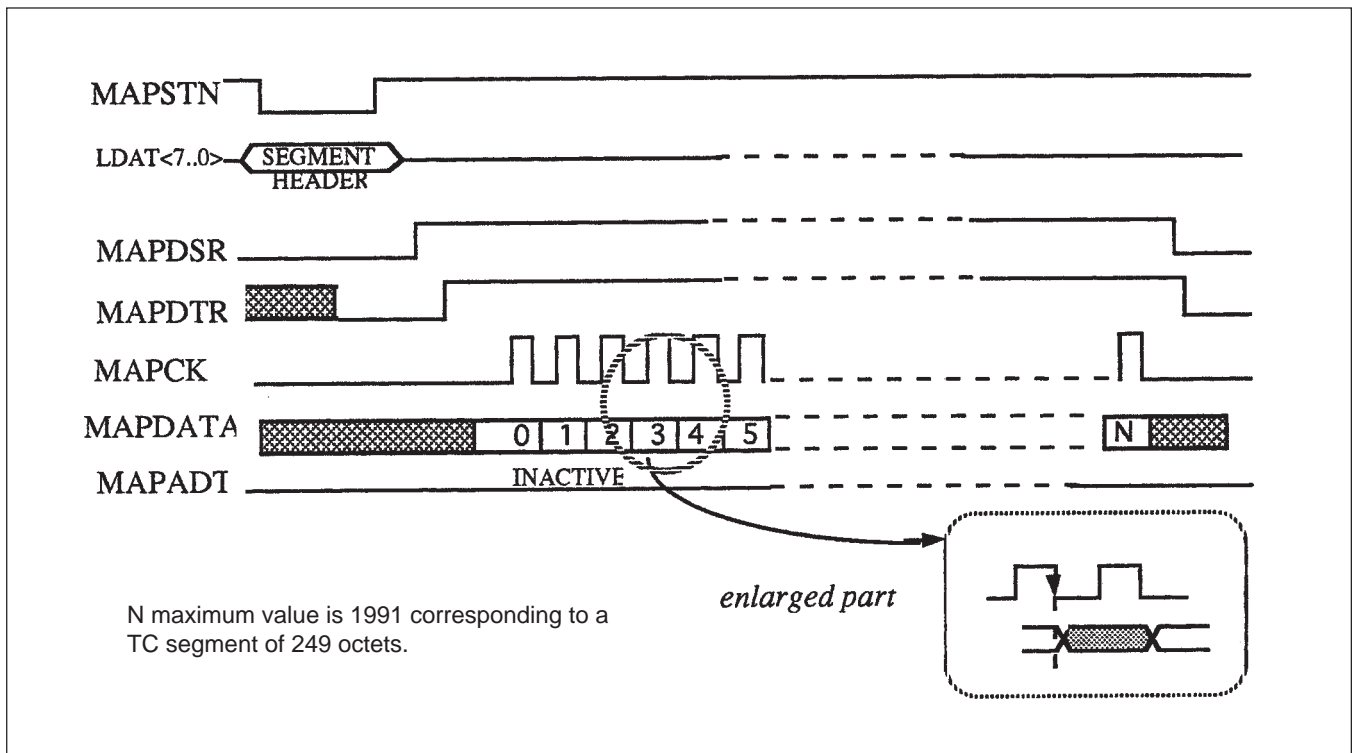
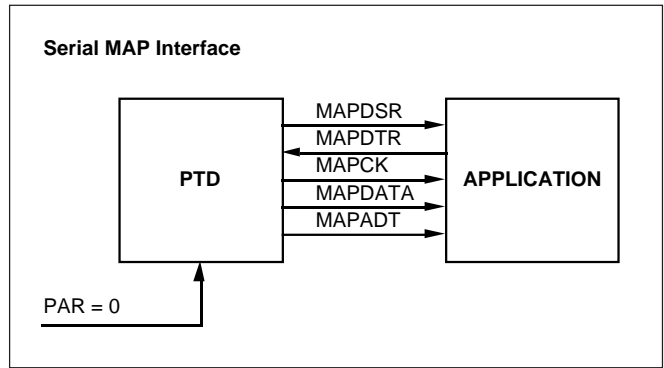
Figure 10: TC Channel Input Timing

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In addition, the MAP interface provides the output signal MAPSTN, in order to save the MAP identifier present on the local data bus (LDAT<7..0>) in an external latch. This MAP identifier is used to demultiplex the segment data toward the selected application. The MAPSTN signal can be controlled by the LACK signal. MAPDSR has no effect when MAPDTR output is deasserted.

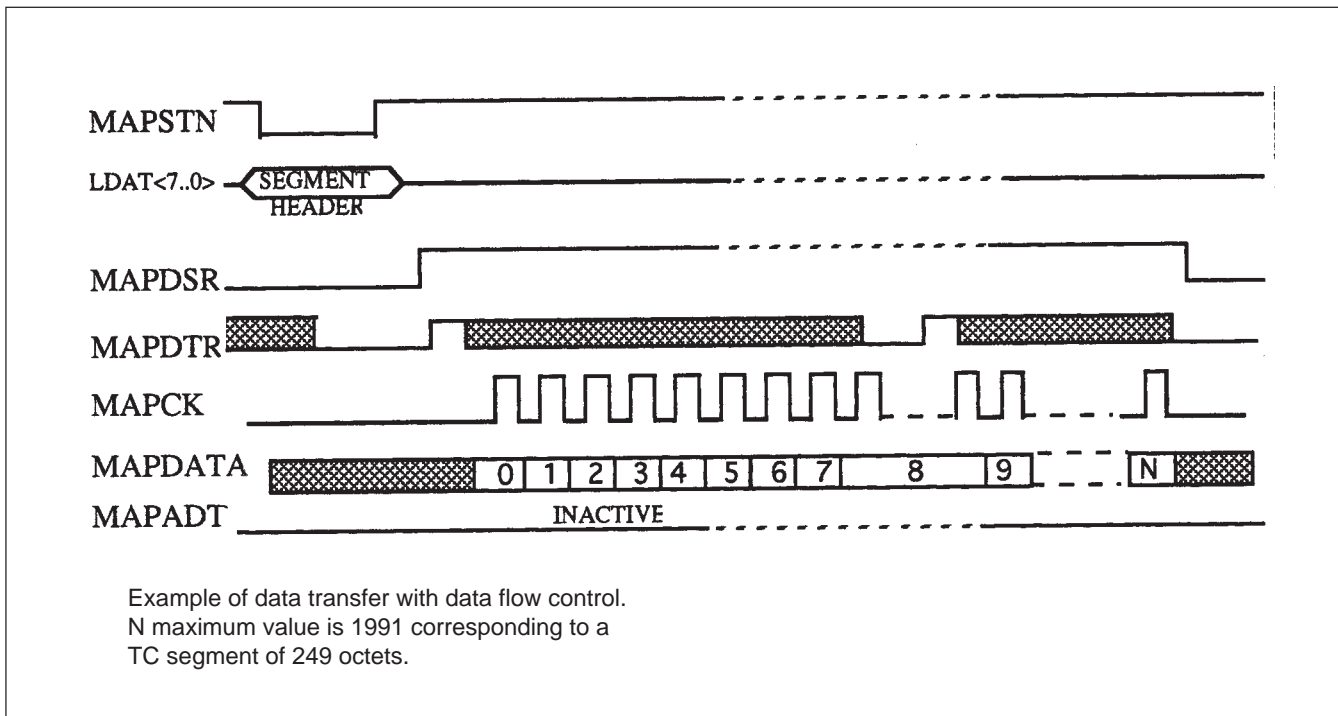
The output frequency for each MAP is programmable and is defined in ROM. For MAP number n, the address of the value X defining the MAP frequency is (hex) 100+n. The MAP output frequency is given by  $F = f_{ck} / [2^X]$ , (X is coded on the 4 LSBs and its value varies from 1 to 13; for other values, the output frequency is  $F = f_{ck} / 2$ ). For example for a PTD clock frequency of 4 MHz, setting the ROM value to 4 will generate a MAP frequency of 250 kHz. With a system clock frequency fck of 4 MHz, the MAPCK frequency can vary from 488 Hz (X=13) to 2 MHz (X=1). The use of a too low MAP frequency compared to the TC clock frequency may lead to the activation of the WAIT flag if the MAP output of a previous frame is not finished when a new segment arrives. As a rule of thumb, in order to avoid the Wait flag being asserted, the MAP frequency should be at least the TC input bit rate multiplied by 10 when fully variable segment size (by 2 if fixed length).

Figure 11 describes the serial interface in three different transfer situations.

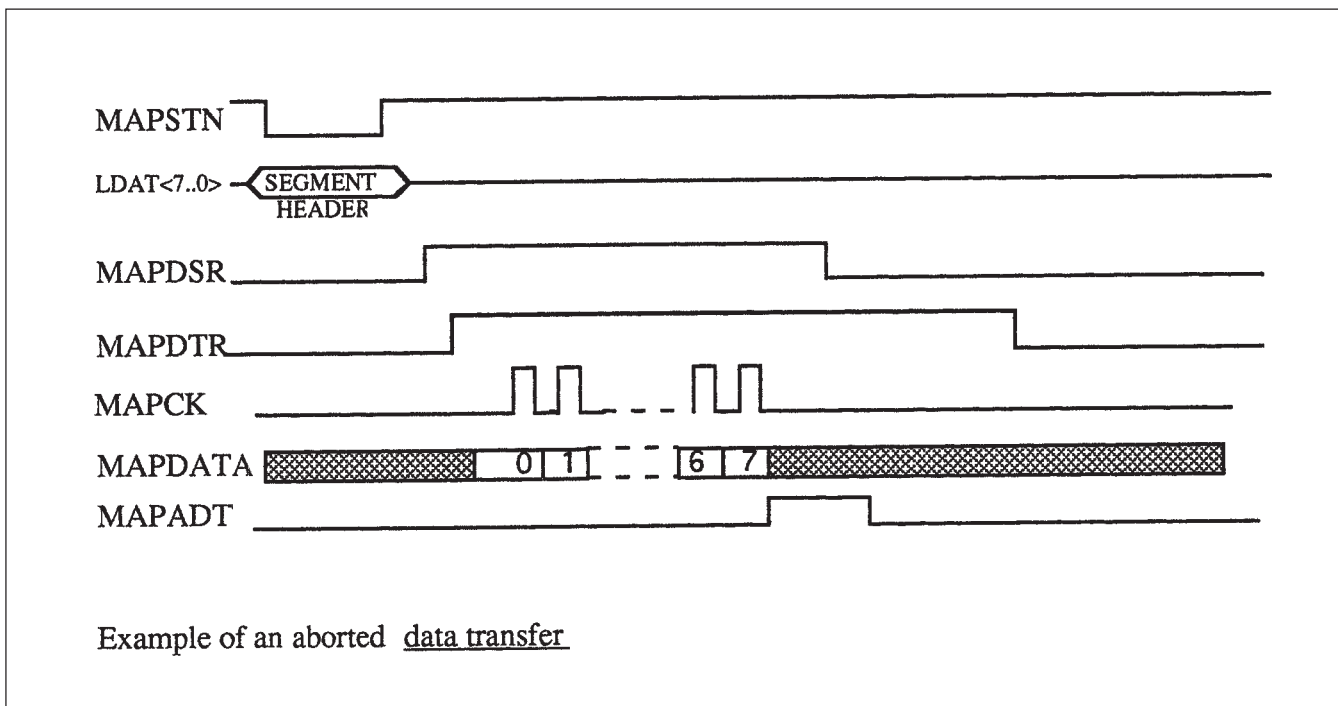


Note: The bit 0 is the MSB and shall be transmitted first.

Figure 11: Serial MAP Interface



Note: For each MAPDTR pulse one octet is transferred.



Note: The MAPADT signal is asserted on octet boundaries of the MAP data being transferred.

Figure 11: Serial MAP Interface (continued)

5.3 TELEMETRY INTERFACE

The Telemetry interface allows four different reporting words to be retrieved.

- the Command Link Control Word (CLCW),
- the Command Pulse Distribution Unit Status (CPDUS),
- the Frame Analysis Report (FAR),
- the Authentication Unit Status (AUS).

It is possible for an application to use either a serial or parallel interface to read these reports. The selection between serial or parallel interface is made with the configuration input pin PAR as follows:

- PAR = 1; the parallel TM interface is used
- PAR = 0; the serial TM interface is used

The parallel interface is described in section 5.4. The parallel interface is useful for integrating subsystems comprising both the TC decoder and a processor, without cross-coupling after the TC decoders. The CLCW has its own serial telemetry interface which is redundant in serial mode.

The other three reports (CPDUS, FAR, AUS) can be fetched through a common serial interface (clock and data lines) using two or five different sample signals. The selection between using two or five sample signals is made with the configuration input pin TMMOD as follows:

- TMMOD = 0; the status (CPDUS, FAR, AUS) reports are fetched with 5 sample signals.

- TMMOD = 1; the status (CPDUS, FAR, AUS) reports are fetched with 2 sample signals.

Both interfaces use the same TMC and TMD signals. When the parallel interface is selected it is not possible to use the TM (and MAP) serial interface, except for the CLCWB interface which can be used in a serial mode even if the PAR signal is set to 1. The protocol for the serial interface is fully compliant with section 4.3 of TTC-B-01 (serial 16 bit digital channel).

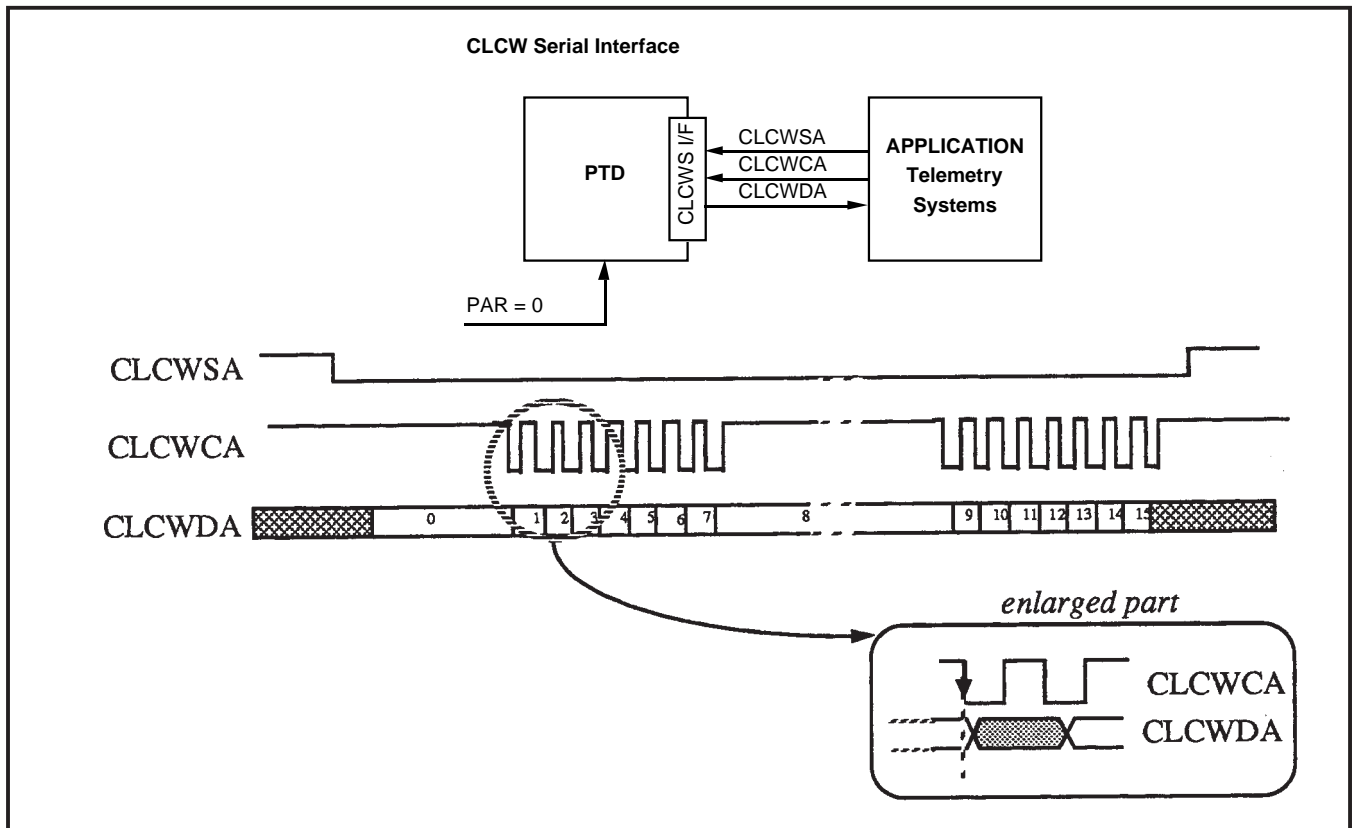
Serial CLCW Interface

The 16 bit Command Link Control Word (CLCW) can be retrieved through this interface. The serial CLCW interface is redundant in order to allow two separate redundant TM encoders to be connected to each TC decoder. Figure 12 shows the serial CLCW telemetry interface. The serial interface is implemented with 3 signal lines:

- CLCWSA: status sample input,
- CLCWCA: status clock input,
- CLCWDA: status data output.

The redundant serial CLCW interface is identical with the nominal serial CLCW interface using the 3 signals:

- CLCWSB: status sample input,
- CLCWCB: status clock input,
- CLCWDB: status data output.



Note: The 0 bit is the MSB and is transmitted first.

Figure 12: Serial CLCW Telemetry Interface

The sample signal CLCWSA should be activated only once to fetch the entire CLCW word. The serial CLCW interface has been designed to allow the VCM device specified in reference 3 to automatically retrieve the CLCWs without any additional components being required. If one of the CLCW interfaces is not used, the following signals CLCWSx and CLCWCx should be connected to  $V_{DD}$ . Activating the CLCWCA (CLCWCB) signal when CLCWSA (or CLCW SB) is deasserted, will generate invalid data output on CLCWDA (or CLCWDB).

**CPDU Status Report Interface in 5 Samples Mode**

The 16 bit Command Pulse Distribution Unit Status report can be retrieved through this interface. It is possible for an application to use either a serial or a parallel interface to read out this status report. The serial or parallel mode is selected with the PAR configuration pin of the PTD (see section 5.4). The serial interface in 5 samples mode uses 3 signal lines:

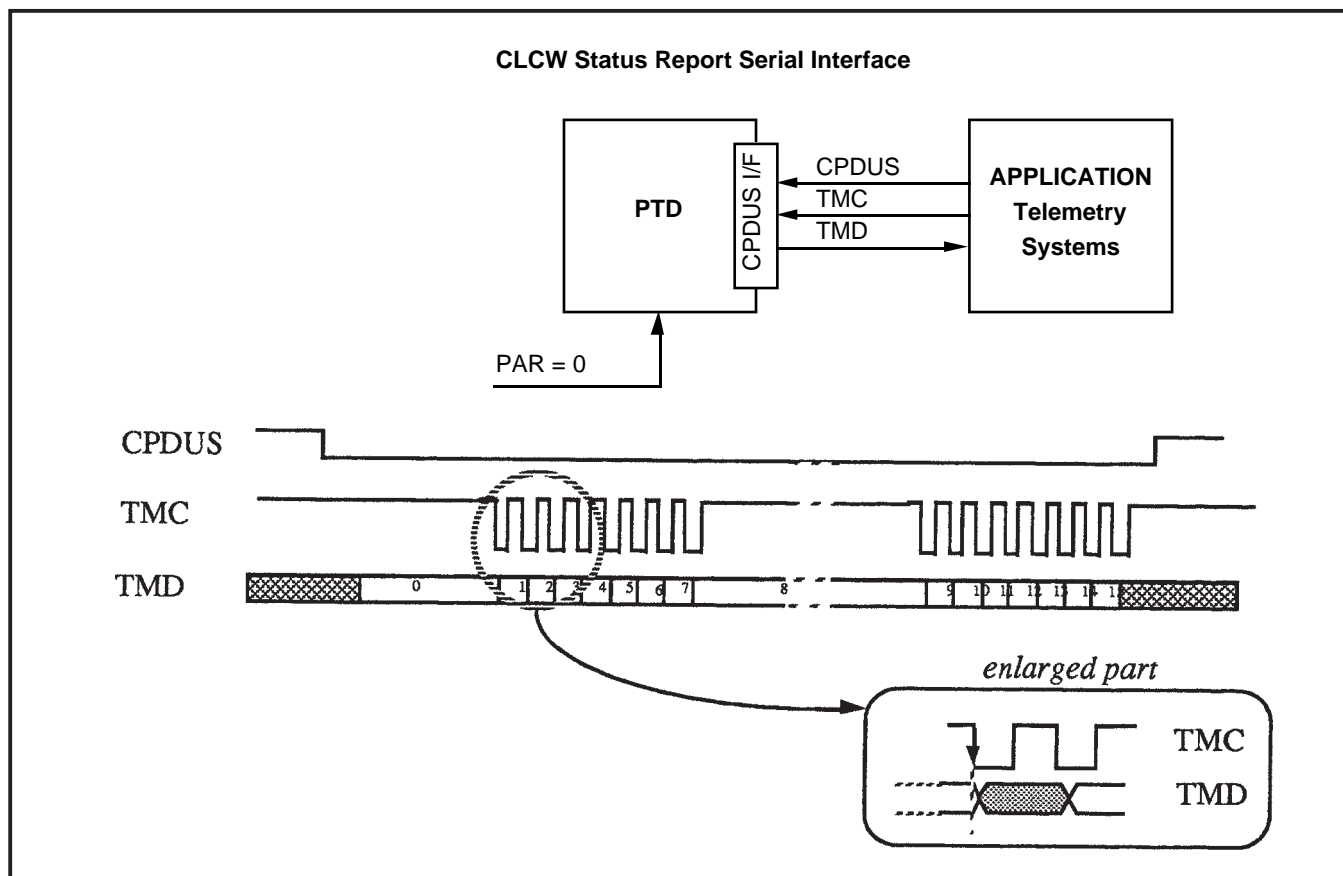
- CPDUS: status sample input.
- TMC: status clock input, is also used for FAR and AUS.
- TMD: status data output, is also used for FAR and AUS.

The sample signal CPDUS needs to be activated only once to fetch the entire CPDUS word. CPDUS, FAR1S, FAR2S, AUS1S and AU2S cannot be asserted simultaneously. If CPDUS, FAR1S, FAR2S, AUS1S and AU2S are not asserted, activating the TMC signal will generate invalid data on the TMD output. If the CPDU status report interface is not used, the CPDUS signal should be connected to  $V_{DD}$ . Figure 13 below describes the CPDU telemetry serial interface.

**Serial FAR Status Report Interface in 5 Samples Mode**

The 32 bit Frame Analysis Report can be retrieved through this interface. It is possible for an application to use either a serial or a parallel interface to read out this status report. The serial or parallel mode is selected with the PAR configuration pin of the PTD (see section 5.4). The serial interface in 5 samples mode uses 4 signal lines:

- FAR1S: first status sample input,
- FAR2S: second status sample input,
- TMC: status clock input, is also used for CPDUS and AUS,
- TMD: status data output, is also used for CPDUS and AUS.



Note: The 0 bit is the MSB and is transmitted first.

Figure 13: CPDU Telemetry Serial Interface

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The sample signals FAR1S and FAR2S should be asserted to fetch the 32 bits of FAR. CPDUS, FAR1S, FAR2S, AUS1S and AU2S cannot be asserted simultaneously. If CPDUS, FAR1S, FAR2S, AUS1S and AU2S are not asserted, activating the TMC signal will generate invalid data on the TMD output. If the FAR status report interface is not used, the FAR1S and FAR2S signals should be connected to  $V_{DD}$ .

Figure 14 describes the FAR telemetry serial interface.

## Serial AU Status Interface in 5 Samples Mode

The 80 bit Authentication Unit Status report can be retrieved through this interface. It is possible for an application to use either a serial or a parallel interface to read out this status report. The serial or parallel mode is selected with the PAR configuration pin of the PTD (see section 5.4). The serial interface in 5 samples mode is implemented with 4 signal lines:

- AU1S: first status sample input,
- AU2S: second status sample input,
- TMC: status clock input, is also used for CPDUS and FAR.
- TMD: status data output, is also used for CPDUS and FAR.

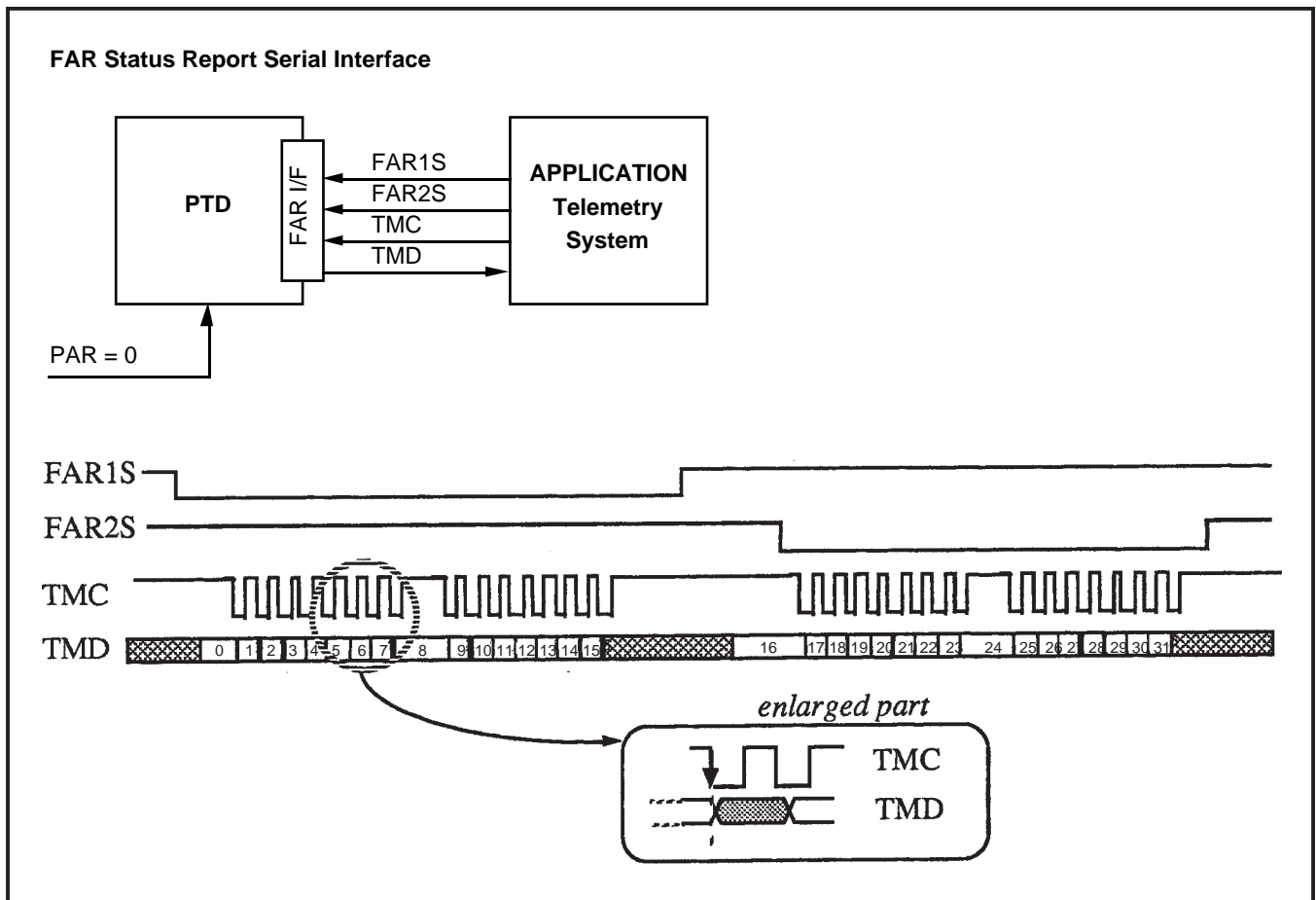
When AU1S is asserted, the pointer for reading out data with AU2S is reset to the second octet of the report. The sample signals AU1S and AU2S should be asserted as described in Figure 15 to fetch the 80 bits of AUS report. CPDUS, FAR1S, FAR2S, AUS1S and AU2S cannot be asserted simultaneously. If CPDUS, FAR1S, FAR2S, AUS1S and AU2S are not asserted, activating the TMC signal will generate invalid data on the TMD output. If the AU status report interface is not used, the AU1S and AU2S signals should be connected to  $V_{DD}$ .

Figure 15 describes the AUS telemetry serial interface.

## Serial CPDU, FAR, AU Status Interface in 2 Samples Mode

The 16 bit Command Pulse Distribution Unit status report, the 32 bit Frame Analysis report and the 80 bit Authentication Unit status report can be retrieved through this interface. The serial interface in 2 samples mode is implemented with 4 signal lines:

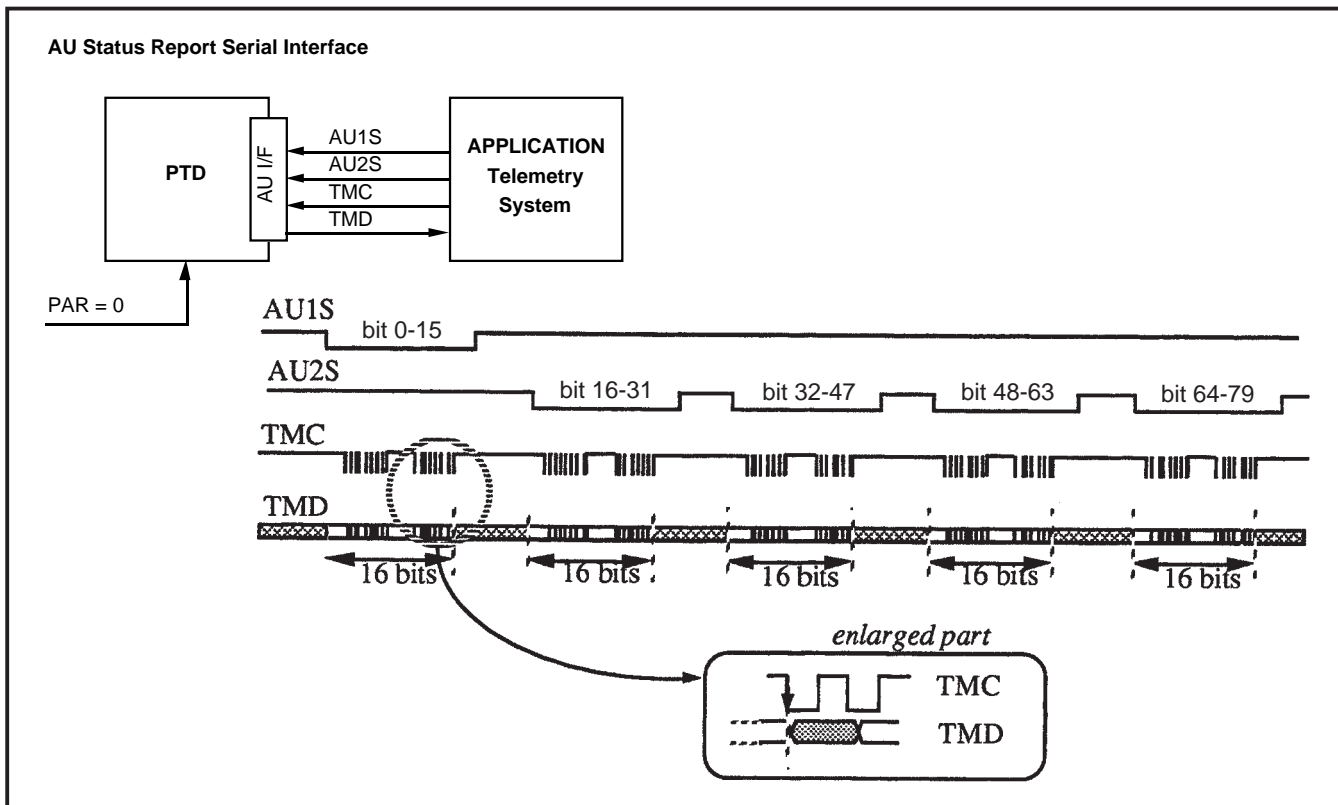
- CPDUS: first status sample input,
- FAR1S: second status sample input,
- TMC: status clock input,
- TMD: status data output.



Note: The 0 bit is the MSB and is transmitted first.

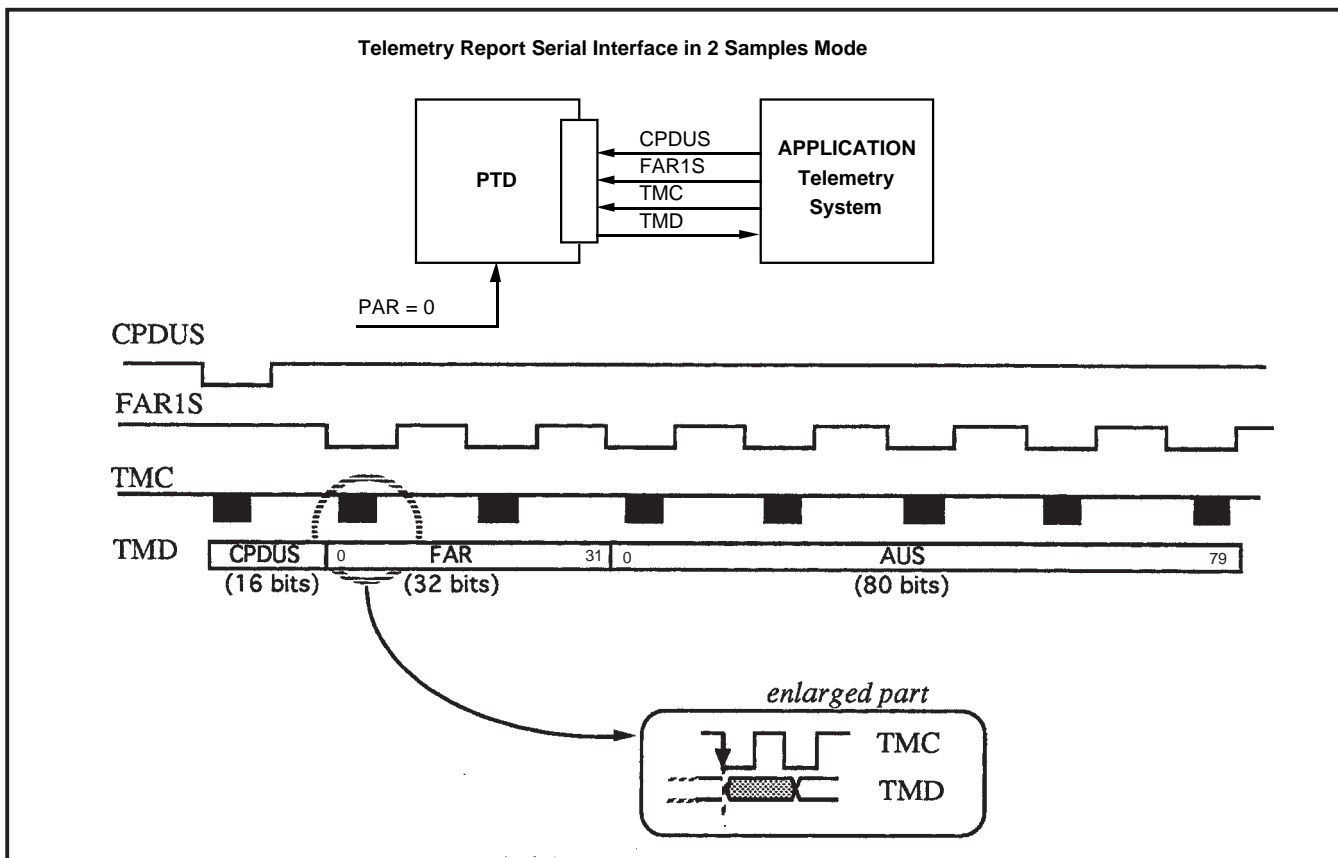
Figure 14: FAR Telemetry Serial Interface





Note: The 0 bit is the MSB and is transmitted first.

Figure 15: AUS Telemetry Serial Interface



Note: The 0 bit is the MSB and is transmitted first.

Figure 16: Telemetry Serial Interface in 2 Sample Mode

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When CPDUS is asserted, the pointer for reading out data with FAR1S is reset to the first octet of the FAR. The samples CPDUS and FAR1S should be activated as described in Figure 16 to fetch the 128 bits of status words. The first 16 bits are those of the CPDU status word, to be acquired by asserting the CPDUS signal line. The next 32 bits are those of the FAR status word, to be acquired by signalling on the FAR1S signal line (2 x 16 bits). The last 80 bits are those of the AU status word, to be acquired by additional assertions (5 x 16 bits) of the FAR1S signal line. It is possible to read out only the first 48 bits (CPDU and FAR), e.g. if the AU is not used.

FAR1S, AU1S and AU2S do not have any impact in this mode, but should be connected to V<sub>DD</sub>.

## 5.4 PARALLEL INTERFACE

A parallel interface is provided on the PTD to access the TC segment and the four reporting words: CLCW, CPDUS, FAR and AUS. The parallel mode is selected with the PAR configuration pin of the PTD (the parallel mode is selected when PAR is set to 1). The parallel interface is implemented with the following signals:

- PCSN: parallel bus chip select input,
- PAD<2..0>: parallel address bus (input),
- PRDY: data validation output,
- PBUS<15..0>: parallel data bus (output),
- MAPDSR: MAP data set ready output,
- MAPADT: MAP aborted data transfer output.

The PCSN, PAD2, PAD1 and PAD0 signal lines use respectively the CPDUS, FAR1S, FAR2S and AU1S input pins of the serial interface. The application acquires the TC segment and the four reporting words by read cycles. The addressing of these words is as follows:

PAD2	PAD1	PAD0	read word
0	0	0	MAP segment
0	0	1	CPDU status
0	1	0	CLCW status
0	1	1	MAP status
1	0	0	FAR1 status
1	0	1	FAR2 status
1	1	0	AU1 status
1	1	1	AU2 status

When the AU1 status is read, the pointer for reading out data with AU2S is reset. The MAP TC segment is read as described in Figure 17.

A TC segment is read by consecutive accesses to <000>. Data read when MAPDSR is not asserted is not valid. The TC segment data octet of even rank is output on the 8 MSB of PBUS (the first octet is 00 and therefore even). The TC segment data octet of odd rank is output on the 8 LSB of PBUS. In the case of a TC segment with an odd number of octets, the last 16 bits word output on PBUS contains the last TC segment data octet on the 8 MSB and a non significant

octet (all bits set to 0) on the 8 LSB. For example, if the TC segment to be output is (hexadecimal) AABBCC, the first word read is AABB and the second one is CC00.

After a PCSN assertion, the PRDY output is activated when the data is available on the PBUS output. The PRDY is released when the PCSN signal is deasserted. The PRDY signal will not be asserted if PCSN is asserted and PAD = 000 (MAP segment read) when MAPDSR is inactive. When PCSN is deasserted the PBUS bus is tristated. The MAP status word can be read at any time. The access to this word is identical to the telemetry status word accesses as described in Figure 18. It contains the following information:

- PBUS<0>: MAPDSR information (identical to MAP data set ready signal line).
- PBUS<1>: ODD/EVEN segment length information (Odd: 1, Even: 0).
- PBUS<15..2>: not used (value : 00000000000000).

NOTE: only TC segments appearing on MAP 1 to 62 and on MAP 63 when AU is disabled, can be read out using this parallel interface. MAP 0 is not affected by this parallel interface since it is directly connected to the CPDU. The telemetry status word is read as described in Figure 18.

The CLCW status word is read using one read cycle where PAD = 010.

The CPDU status word is read using one read cycle where PAD = 001.

The FAR status words are read with two read cycles:

- One read cycle with PAD = 100 for the first 16 bits (FAR1)
- One read cycle with PAD = 101 for the last 16 bits (FAR2).

The AU status words are read using five read cycles:

- One read cycle with PAD = 110 for the first 16 bits (AU1)
- Four read cycles with PAD = 111 for the last 64 bits (AU2): bits 16-31, bits 32-47, bits 48-63 and bits 64-79.

When the AU1 Status report is read, the pointer for reading out data with AU2 is reset to the second octet of the AU report. The Status of Survey bit is set when FAR2 is read. The following pins have no influence in parallel mode:

- MAPDTR (should be connected to V<sub>SS</sub>),
- CLCWSA, CLCWCA (should be connected to V<sub>DD</sub>),
- AU2S (should be connected to V<sub>DD</sub>),
- TMC (should be connected to V<sub>DD</sub>),
- TMMOD (should be connected to V<sub>SS</sub>),

The reports and TC segments cannot be read out in an arbitrary order. The following constraints apply: A FAR2 read out shall not be separated from the previous FAR1 read out by AU1 or AU2 read out. An AU2 read out shall not be separated from a previous AU1 or a previous AU2 read out by FAR1 or FAR2 read out.

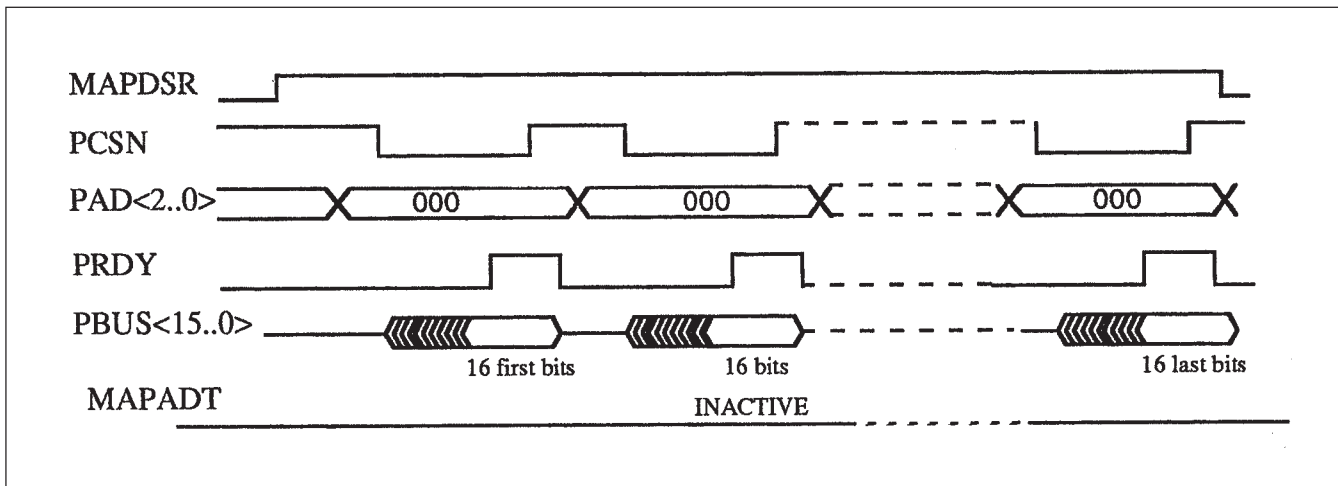


Figure 17: Parallel MAP Interface

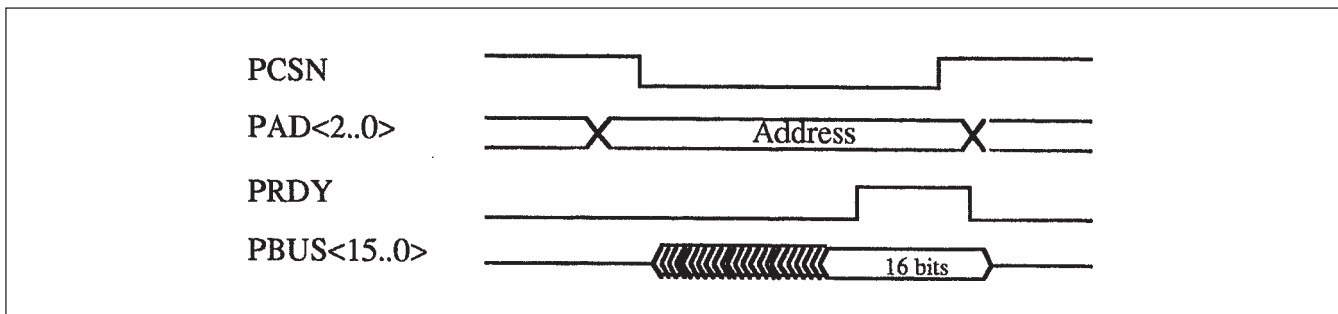


Figure 18: Parallel Telemetry Read Cycle

**5.5 CPDU INTERFACE**

This interface consists of 3 signal lines:

- CPDUSTN: CPDU address strobe output,
- CPDUEN: CPDU enable output,
- CPDUDIV: CPDU frequency divider input.

The CPDU interface provides the output signal CPDUSTN in order to save the CPDU physical channel identifier present on the local data bus LDAT<7..0> in an external latch (no specific LADR address is associated with this data). This CPDU identifier is used to demultiplex the command pulse toward the selected CPDU output. The CPDUSTN signal can be controlled by the LACK input. The CPDUEN signal is representative of the command pulse as far as duration is concerned. The pulse amplification should be made after demultiplexing with external circuitry. The CPDUDIV signal allows division of the pulse length specified in ref 2 by a factor of 5, in order to get a better accuracy. Alternatively, this allows the PTD to be used with a 1MHz clock frequency, instead of a 4 MHz clock.

For a 4 MHz clock, the duration D is 10.24 ms if CPDUDIV=0 and 2.048 ms if CPDUDIV=1. The maximum duration (=128xD) is about 1.31 s if CPDUDIV=0, and 262 ms if CPDUDIV=1. The delay between the time at which the packet has been declared Legal and the execution of the command instruction (rising edge of CPDUEN) can be any value between 0.5 D and 1.5 D. The duration between two instructions placed one after the other in the same CPDU packet (from falling edge to rising edge of CPDUEN) corresponds to about D.

COMMAND	PULSE LENGTH (CLOCKS) (CPUDIV=0)	PULSE LENGTH (CLOCKS) (CPUDIV= 1)
000	40961	8193
001	81921	16385
010	163841	32769
011	327681	65537
100	655361	131073
101	1310721	262145
110	2621441	524289
111	5242881	1048577

Table 4: CPDU Pulse Lengths

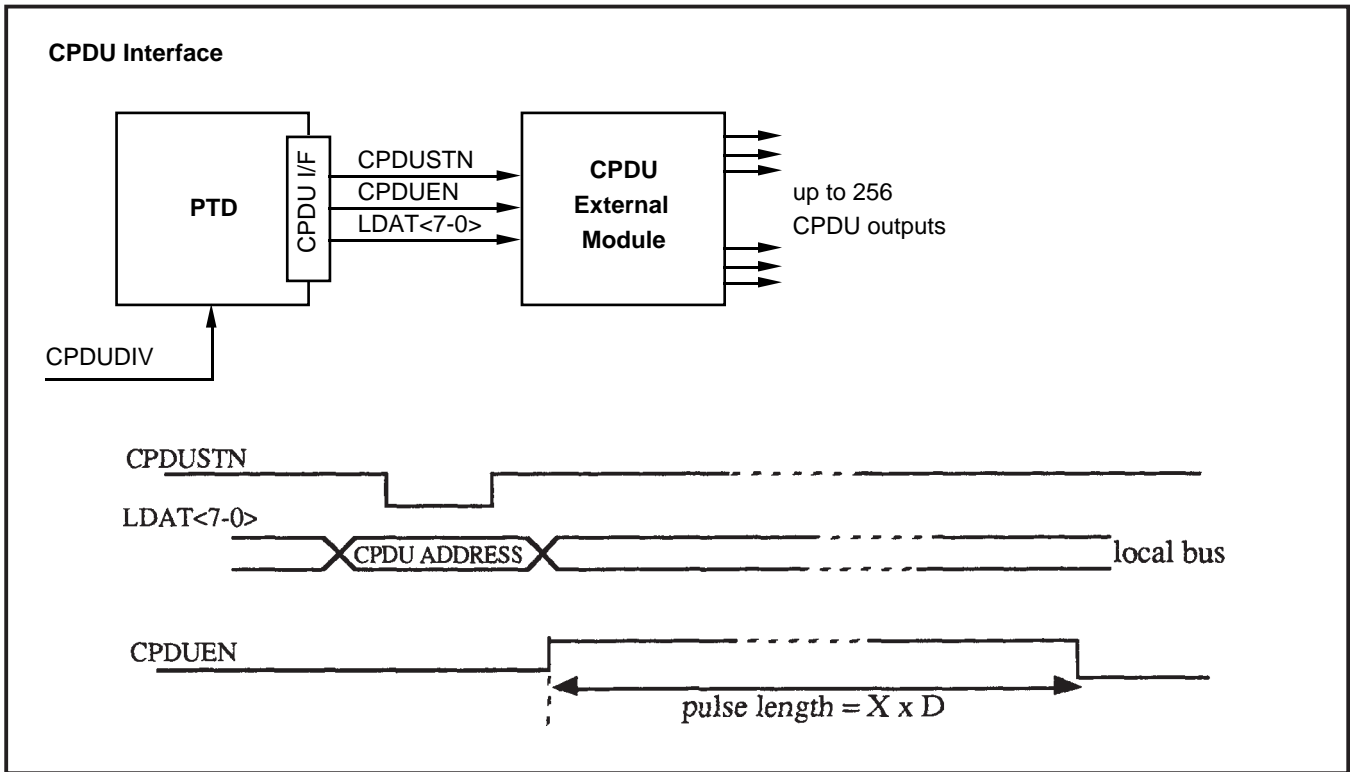


Figure 19: CPDU Interface

5.6 LOCAL BUS INTERFACE

This interface is used to access the external memory map. It consists of the following signals:

- LADR<10..0>: address bus (output),
- LDAT<7..0>: data bus (input/output),
- RWN: read write output,
- LACK: memory acknowledge input,
- RAMCSN: RAM chip select output,
- ROMCSN: ROM chip select output,
- LACCS: chip select output asserted for recovery LAC counter access.

The Local bus cycle is started by asserting the RWN and CSN signals and activating the LADR signal. It is ended by asserting LACK signal. If extended access times are not required, LACK can be permanently asserted. This interface provides a bus fault timer which is enabled when CSN signals are active and reset when LACK signal is active. If a reset doesn't occur within a minimum of 32 Tck (8 us for a 4 MHz clock frequency) and a maximum of 64 Tck (16 us for a 4 MHz clock frequency), the current Local bus cycle is aborted by forcing CSN inactive. The functional timings corresponding to the local bus interface are given in section 8.2.

5.7 MEMORIES

The PTD manages two types of memory:

- RAM to temporarily store the received TC data and all protocol variables (counter values, programmable key, ...). The RAM is organized in 2K words of 8 bits. In the case when it is used to store the eight bits of the recovery LAC counter, it should be non volatile.
- ROM (1Kx8) to store the mission specific data and the fixed Authentication key.

In order to allow the use of slow memories, an acknowledge signal (LACK) is used to indicate when the memory access is completed.

In order to save the 8 LSBs of recovery LAC counter in a device different from the RAM, two different chip select signals (RAMCSN and LACCS) are provided for the recovery LAC counter access. Two different modes are provided to manage the LAC counter select signals, these modes are selectable with a configuration pin called AUTSL as follows:

- AUTSL = 1: The recovery LAC counter is stored in RAM. The PTD asserts the RAMCSN signal when it performs the recovery LAC counter access.
- AUTSL = 0: The recovery LAC counter is stored in a device different from the RAM. The PTD asserts the LACCS signal when it performs the recovery LAC counter access. This non volatile memory could be for example an EEPROM for low radiation requirements or relays for radiation hardened recovery LACs.

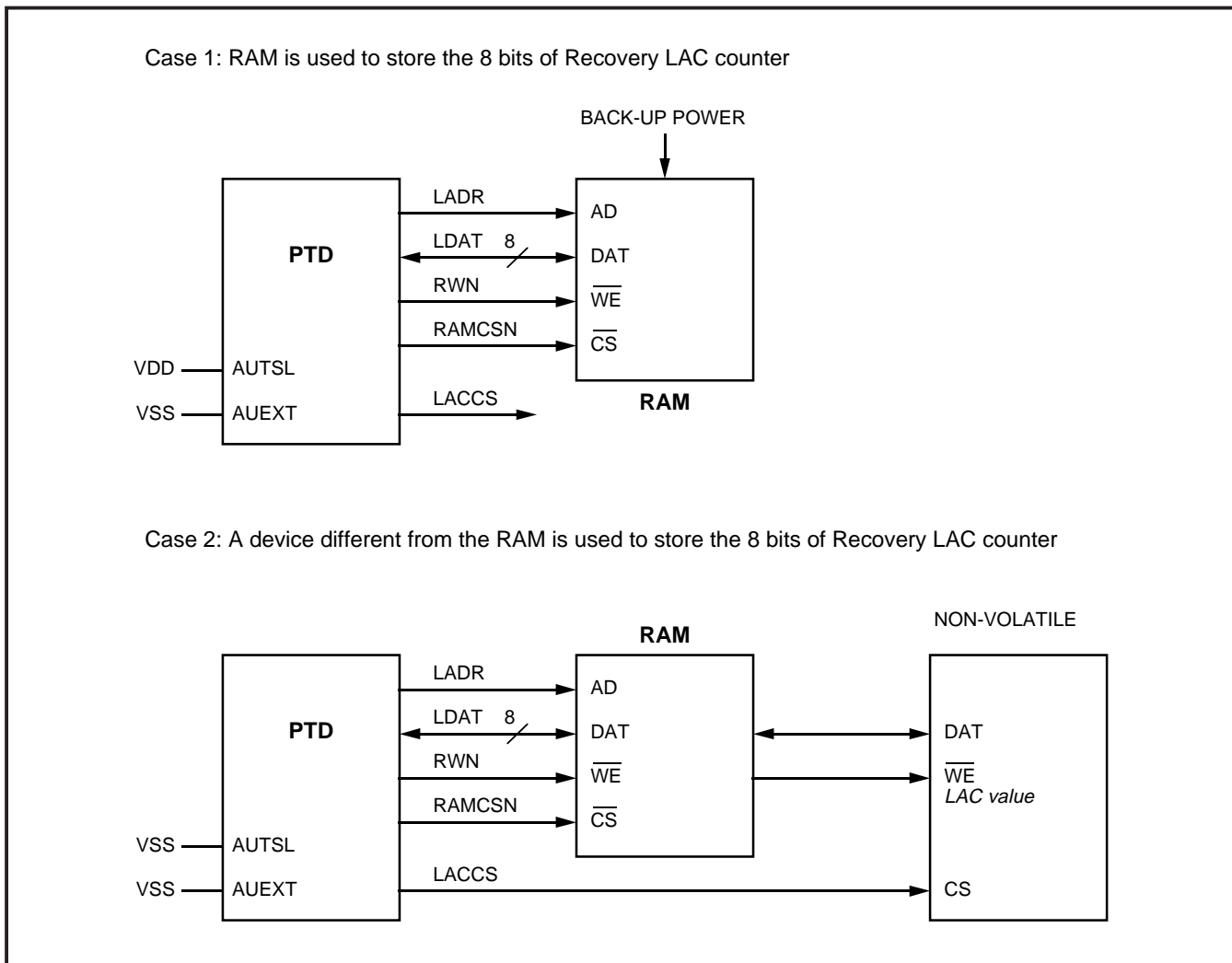


Figure 20: Recovery LAC Value Storage

A diagram of two possible implementations is given in Figure 20.

The RAM mapping is organized in such a way that the PTD is able to use the following external RAM buffers:

- two buffers working in a flip-flop mode between transfer and segmentation layer, respectively called Front End and Back End buffer.
- one buffer used by the CPDU interface

The buffer management is described in section 4.2. The memory mapping is defined in tables 5 and 6.

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<b>RAM</b>	<b>Start Address</b>	<b>End Address</b>
Buffer0-(front end/back end) (see note 1)	000	0FF
Buffer1-(back end/front end) (see note 1)	100	1FF
Programmable key - Knapsack	200	367
Programmable key - Hashing	368	36F
Internal use (reserved)	370	373
Free	374	3FF
8 LSB of Recovery LAC	400	400
Internal use (reserved)	401	401
Auxiliary LAC Counter - octet 4 LSB	402	402
Auxiliary LAC Counter - octet 3	403	403
Auxiliary LAC Counter - octet 2	404	404
Auxiliary LAC Counter - octet 1 MSB	405	405
Principal LAC Counter - octet 4 LSB	406	406
Principal LAC Counter - octet 3	407	407
Principal LAC Counter - octet 2	408	408
Principal LAC Counter - octet 1 MSB	409	409
Free	40A	40F
AUS octet 10 - buffer 0	410	410
AUS octet 9 - buffer 0	411	411
AUS octet 8 - buffer 0	412	412
AUS octet 7 - buffer 0	413	413
AUS octet 6 - buffer 0	414	414
AUS octet 5 - buffer 0	415	415
AUS octet 4 - buffer 0	416	416
AUS octet 3 - buffer 0	417	417
AUS octet 2 - buffer 0	418	418
AUS octet 1 - buffer 0	419	419
FAR octet 4 - buffer 0	41A	41A
FAR octet 3 - buffer 0	41B	41B
FAR octet 2 - buffer 0	41C	41C
FAR octet 1 - buffer 0	41D	41D
Free	41E	42F
AUS octet 10 - buffer 1	430	430
AUS octet 9 - buffer 1	431	431
AUS octet 8 - buffer 1	432	432
AUS octet 7 - buffer 1	433	433
AUS octet 6 - buffer 1	434	434
AUS octet 5 - buffer 1	435	435
AUS octet 4 - buffer 1	436	436
AUS octet 3 - buffer 1	437	437
AUS octet 2 - buffer 1	438	438
AUS octet 1 - buffer 1	439	439
FAR octet 4 - buffer 1	43A	43A
FAR octet 3 - buffer 1	43B	43B
FAR octet 2 - buffer 1	43C	43C
FAR octet 1 - buffer 1	43D	43D
Free	43E	5FF
CPDU buffer (see note 2)	600	6FF
Free	700	7FF

Note 1: The addresses 000 and 100 contain the buffer length (X) and the first word of the frame are stored at address X and 100+X respectively; the last word is stored at address 001 and 101 respectively.

Note 2: The address 600 contains the CPDU buffer length (X) and the first word of the frame is stored at address 600+X, the last word is stored at address 601.

*Table 5: RAM Mapping*

ROM	Start Address	End Address
Frame Header octet 1 (see note 3)	000	000
Frame Header octet 2 (see note 3)	001	001
Frame Header octet 3 (see note 3)	002	002
FARM PW' = PW - 1 (see note 4)	003	003
FARM NW' = 256 - NW (see note 4)	004	004
Authenticated MAP ID pointer (see note 5)	005	005
CPDU Packet Header octet 1 and 2 (see note 6)	006	007
Free	008	0FF
MAP frequency table defined in section 5.2	100	13F
Free	140	1FF
Fixed key - Knapsack (see note 7)	200	367
Fixed key - Hashing (see note 8)	368	36F
Free	370	3FF

Note 3: These 3 octets contain all the fields of the Frame Header including reserved bits and version bits. Bypass and Control flags (in Frame Header octet 1) form the only field that is not a fixed value: the value of these 2 bits in ROM has no influence on the PTD operation (default value = 00).

Note 4: In order to facilitate the implementation of the FARM Sliding Window Concept in the PTD, the values stored in the ROM are not PW and NW but:

- PW' = PW - 1
- NW' = 256 - NW

The PW' and NW' numbers can be any value between 0 and 255.

Note 5: Bits 7 and 6 are not used.

Note 6: These 2 octets contain all the field of the Packet Header including version and type bits.

Note 7: The Knapsack key mapping is given in Figure 9. Address 200 contains the least significant octet of the first Knapsack coefficient W0. Address 201 contains octet 1 of the first Knapsack coefficient W0, (see example below).

Note 8: The Hashing key mapping is given in Figure 9. Address 368 contains the 4 LSBs of the Hashing key stored at the right of the memory octet in the reverse order. Address 369 contains the 8 following bits in the reverse order. **Caution:** if the Hashing key is read bit by bit starting from the MSB, the memory must be filled from right to left, (see example below).

Table 6: ROM Mapping

## Example

An example of ROM programming is given here for a fictitious spacecraft.

Note: In the following example 16# indicates hexadecimal, 10# indicates decimal, 2# indicates binary.

The value of the spacecraft ID is : 16#301  
The value of the virtual channel ID is : 16#20  
The value of the Application Process ID is : 16#456  
For the FARM-1 process, the values of PW and NW are : 10#100 and 10#100  
The Authentication MAP ID Pointer is : 16#15  
For the CPDU, the Application Process Identifier is : 16#456

Frame Header octet 1 contains the following fields:

Version number : 2#00 in accordance with ref 1  
Bypass flag : 0 or 1 (no influence): 0 for example  
Control Command flag : 0 or 1 (no influence): 0 for example  
Reserved field A : 2#00 in accordance with ref 1  
Spacecraft ID (2 MSBs) : 2#11

The value of the ROM at address 000 is: 16#03

Frame Header octet 2 contains the following field:

Spacecraft ID (8 LSBs) : 2#00000001

The value of the ROM at address 001 is: 16#01

Frame Header octet 3 contains the following fields:

Virtual Channel ID : 2#100000  
Reserved field B : 2#00 in accordance with ref 1

The value of the ROM at address 002 is: 16#80

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The calculation of PW' gives:  $PW' = PW - 1 = 100 - 1 = 99 \rightarrow 16\#63$

The value of the ROM at address 003 is: 16#63

The calculation of NW' gives:  $NW' = 256 - NW = 256 - 100 = 156 \rightarrow 16\#9C$

The value of the ROM at address 004 is: 16#9B

The authenticated MAP ID is 5 bits long. The 5 LSBs of the ROM value @ address 05 correspond to the authenticated MAP ID, the 3 MSBs can be either 0 or 1 (0 for example).

The value of the ROM at address 005 is: 16#15

CPDU Packet Header octet 1 contains the following fields:

Version number : 2#000 in accordance with ref 1  
 Type : 1 for CPDU  
 Data Fields Header flag : 0 for CPDU  
 Application Process ID (3 MSBs) : 2#100

The value of the ROM at address 006 is: 16#14

CPDU Packet Header octet 2 contains the following field:

Application Process ID (8 LSBs) : 2#01010110

The value of the ROM at address 007 is: 16#56

The ROM will be programmed as follows:

Address	Data
000	03
001	01
002	80
003	63
004	9C
005	15
006	14
007	56

## Knapsack and Hashing Key

If the Knapsack key is (example from ref.2 appendix B2)

W0 : 00 01 02 03 04 05

W1 : 06 07 08 09 0A 0B

W59 : 62 63 64 65 66 67

And if the Hashing Key is : C0...C59 A A A A A A A A A A  
 MSB

The ROM will be programmed as follows:

Address	Data
200	05
201	04
202	03
203	02
204	01
205	00
206	0B
207	0A
etc	etc
367	62
368	05
369	55
370	55
etc	55
36E	55
36F	55



## 5.8 EXTERNAL AUTHENTICATION INTERFACE

This interface is provided to connect the PTD with an external Authentication Unit. The PTD allows the external AU to access the data buffer (described in section 5.7) of the RAM in order to process a TC segment which is to be authenticated. The interface is composed of the following signals:

- AUDIS: (input) This signal functions as for the internal AU, disabling the authentication unit.
- AUEXT: (input) This signal indicates the use of an external authentication unit.
- AUST: (output) This signal indicates that a TC frame has been received and must be authenticated. In this case, AUST is activated a few clock periods after the deactivation of the DECOD output indicating the end of the tail sequence of the frame.
- AUBUF: (output) This signal indicates to the external AU which RAM buffer is the back-end buffer containing the TC segment to be authenticated.
- BRQN: (input) This signal is the bus request to read or write the buffer from the external AU. It is activated for each external access to memory.
- BGRN: (output) This signal is the acknowledge of the PTD to BRQN; the PTD will then tristate its signals connected to the RAM (RAMCSN, ROMCSN, LACCS, RWN, LADR and LDAT). The LACK input has no effect when BGRN output is asserted.
- AUEND: (input) AU result validation. This signal indicates the end of the external authentication process and validates the AUR signal.
- AUR: (input) AU result signal. This signal indicates that the received TC frame is authorized or non authorized at the rising edge of AUEND.
- AUTSL: (input) AU tail length select signal. This signal allows definition of the length of the AU tail as follows:
  - AUTSL = 0: The length of the AU tail shall be 9 octets. In this case the 9 last octets of the segment authenticated by the external AU will be deleted by the PTD before transferring the segment to the application.
  - AUTSL = 1: The length of the AU tail shall be 0 octets. In this case all octets of the segment authenticated by the external AU shall be transferred to the application.
- AUSBUF: (output) This signal indicates which AU Status buffer the external AU must update.
- FARBUF: (output) This signal indicates which FAR status buffer the external AU must update (the external AU shall update only the bits 28 through 30 of the FAR status).

The external AU process starts upon receipt of the rising edge of the AUST signal, which is asserted by the PTD until the AUEND input is asserted indicating that the external AU process is finished. The result of the external authentication is given by the AUR signal (set to 1 for a valid authentication). The total duration of the external AU process plus the duration of the MAP output (if it exists) must be smaller than the duration of the next frame to arrive, measured from the start of the frame to the end of the last valid codeblock. A longer duration may lead to a rise of the FARMB WAIT flag. The result must be given to the PTD before the end of the last valid codeblock of the next frame to arrive, so as not to lock the back-end/front-end buffer toggling mechanism, and the FAR buffer management of the next frame.

The external AU can also write the AUS status in the local RAM, in the buffer number given by the AUSBUF output. The PTD locks the toggling mechanism of the AU status buffer while AUST is high in order to prevent data corruption. The external AU can also write bits 28 to 30 of the FAR status by writing the fourth octet of the FAR status in the local RAM, in the buffer number indicated by the FARBUF output. A similar mechanism locks the toggling of the FAR buffer when the AUST output is high. The AUS and FAR buffer update can start when the PTD activates the AUST output and shall be completed when the application asserts the AUEND signal. The local memory interface provides a bus arbiter fault timer. This timer is enabled when BGRN signal is active and reset when BRQN signal is inactive. If a reset does not occur within a minimum of 32 Tck and a maximum of 64 Tck (8 to 16  $\mu$ s at 4 MHz), the BGRN signal is forced to inactive state. The functional timings corresponding to this interface are given in section 8.2.

## 6. STATE AFTER RESET

Asserting the RESETN signal asynchronously forces the local bus interface to avoid bus contention. The master clock should be started before RESETN deassertion. After 2 master clock cycles, the PTD is in a stable state and all its outputs take their cold start value. Deasserting the RESETN signal starts the initialisation phase. After this phase, the PTD registers are initialised.

### PTD Outputs After the Assertion of RESETN Input

- LADR<10..0>	→ 000
- LDAT<7..0>	→ ZZ
- RWN	→ 1
- RAMCSN	→ 1
- ROMCSN	→ 1
- LACCS	→ 0
- all other outputs	at unknown state

### PTD Outputs After the Reset Sequence

- LADR<10..0>	→ 000
- LDAT<7..0>	→ ZZ
- RWN	→ 1
- BGRN	→ 1
- RAMCSN	→ 1
- ROMCSN	→ 1
- LACCS	→ 0
- MAPSTN	→ 1
- MAPCK	→ 0
- MAPDSR	→ 0
- MAPDATA	→ 0
- MAPADT	→ 0
- CPDUSTN	→ 1
- CPDUEN	→ 0
- CLCWDA	→ 0
- TMD	→ 0
- CLCWDB	→ 0
- PRDY	→ 0
- PBUS<15..0>	→ ZZZZ
- AUST	→ 0
- AUBUF	→ 1
- AUSBUF	→ 0
- FARBUF	→ 0 after Reset, 1 after initialization (FAR write)
- SELTC<2..0>	→ 111
- DECOD	→ 0

### PTD Outputs After the Initialisation Phase

#### CODING LAYER:

The coding layer is ready to receive a frame after the reset.

#### TRANSFER LAYER:

The transfer layer initialisation state after reset is the following:

- FARM-1 state : lockout
- FARMB counter : 11
- V(R) counter : 00000000

The cold start value of the CLCW (2 octets) is X000 (where X can be hexadecimal 2, 6, A or E).

The value of the MSB (No RF available) depends on the value of the RFAVN pin. The value of the second MSB (No Bit Lock) depends on the activation of the Tca signals (see section 4.6).

#### AUTHENTICATION LAYER:

The cold start initialisation state for the AU layer can be summarized as follows if AUDis = 0 and AUExt = 0:

- Key in use : fixed key
- Contents of programmable key : undefined
- Contents of Principal and Auxiliary LAC Registers : all ones
- Contents of the Recovery LAC counter : unchanged by the PTD

The cold start value of the AU Status (10 octets) takes the following value if AUDis = 0 and AUExt = 0:

3FFFFFFF 7FFFFFFF 00XX in hexadecimal

The value of the last octet corresponds to that of the 8 LSBs of the recovery LAC, which should be maintained even in the event of loss of power. Thus, this value shall be defined during the system implementation.

**SEGMENT LAYER:**

The segment layer is ready to receive a new segment. The MAP outputs are inactive. The cold start value of the FAR (4 octets) is the following: 00007FE0 in hexadecimal.

**CPDU LAYER:**

The CPDU layer is ready to receive a new CPDU. The CPDUEN output is inactive. The cold start value of the CPDU status (2 octets) is: 3FFF in hexadecimal.

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## 7. SIGNAL DESCRIPTION

In this pin description, first the name of the pin is given, then its type (input (I) or output (O)), and then a brief description.

Total input pins	: 47
Total output pins	: 51
Total I/O pins	: 8
Total number of Input, Output and I/O pins	: 106

Note: Bit numbering convention: for busses, the bit number 0 is considered as the Least Significant Bit (LSB). For strobe signals, it is indicated in the text if they are active on low or high level.

### Transponder Interface

TCC0-TCC5	I	Symbol Clock signals. These signals are only recognised while Channel Active Indication input is asserted. These signals can be asynchronous.
TCS0-TCS5	I	Symbol Stream signals. The data should be valid at the falling edge of the TCCi signals. These signals can be asynchronous w.r.t. system clock, but not w.r.t. symbol clock signals.
TCA0-TCA5	I	Channel Active Indication signals. These signals serve as enable signals for the Symbol Stream signals. Active high. These signals can be asynchronous.

### Local Bus Interface

LADR<10..0>	O	Local Address Bus . This bus is unidirectional and is tristated when the BGRN signal is asserted. LADR<0> is the LSB.
LDAT<7..0>	I/O	Data Bus - This 8 bit data bus is driven as outputs during write cycles and as inputs during read cycles. This bus is tristated when the BGRN signal is asserted. LDAT<0> is the LSB.
RWN	O	Read/Write signal. This signal indicates the direction of the data transfer on the Local Bus and is tristated when the BGRN signal is asserted. RWN = 1: read mode. RWN = 0: write mode.
LACK	I	Memory acknowledge signal. This signal allows wait state cycles to be inserted for memory (RAM, ROM or LAC) read and write access and for CPDUSTN and MAPSTN outputs. LACK=0 inserts wait states. LACK can be permanently connected to 1 when no wait states are required. This signal can be asynchronous. Active high.
BRQN	I	Bus request signal. This signal is asserted by an external unit to request the Local Bus (external Authentication Unit for instance). Active low. This signal can be asynchronous.
BGRN	O	Bus grant signal. This signal is asserted to allow an external unit to use the Local Bus. Active low.
RAMCSN	O	Ram chip select signal. This signal is asserted during RAM access and is tristated when the BGRN signal is asserted. It is affected by the LACK input. Active low.
ROMCSN	O	Configuration Rom chip select signal. This signal is asserted during Configuration Rom access and is tristated when the BGRN signal is asserted. It is affected by the LACK input. Active low.
LACCS	O	Non volatile memory select signal. This signal is asserted during recovery LAC counter access and is tristated when BGRN signal is asserted. It is affected by the LACK input. Active high.

### Map Interface

MAPSTN	O	MAP address strobe signal. This signal allows the MAP Demultiplexer circuitry to latch the MAP identifier present on the local data bus. It is affected by the LACK input. Active low.
MAPCK	O	MAP clockout signal. This signal is only activated when both MAPDSR and MAPDTR signals are active.
MAPDSR	O	MAP data set ready signal. This output indicates that a TC segment is available for transfer. Active high.
MAPDTR	I	MAP data terminal ready signal. This signal indicates that the receiving device is ready to clock in the segment data in serial mode or a segment data sample in parallel mode. Active high. This signal can be asynchronous.
MAPDATA	O	MAP segment data serial line. The segment data is clocked out on the falling edge of the MAPCK signal.
MAPADT	O	MAP abort data transfer signal. This output is asserted when the PTD has aborted the transfer of a TC segment. Active high.

**CPDU Interface**

CPDUSTN	O	CPDU address strobe signal. This signal allows the CPDU interface to latch the CPDU output address present on the local data bus LDAT<7..0>. It is affected by the LACK input. Active low.
CPDUEN	O	CPDU enable signal. This signal provides the command pulse with the appropriate duration. Active high.
CPDUDIV	I	CPDU clock division selection input. CPDUDIV = 0: the CPDU base clock (corresponding to D) is the system clock CLK divided by 40960. CPDUDIV = 1: the CPDU base clock (corresponding to D) is the system clock CLK divided by 8192.

**CLCW Interface**

CLCWSA	I	Nominal CLCW status sample. This signal indicates that the CLCW status is sampled by the telemetry interface. Active low. This signal can be asynchronous
CLCWCA	I	Nominal CLCW status clockout signal. This signal is provided to the PTD when CLCWSA signal is active. This signal can be asynchronous
CLCWDA	O	Nominal CLCW status data line (serial mode). The data is provided either on the falling edge of CLCWSA or on the falling edge of CLCWCA.
CLCWSB	I	Redundant CLCW status sample. Active low. This signal can be asynchronous
CLCWCB	I	Redundant CLCW status clockout signal. This signal can be asynchronous
CLCWDB	O	Redundant CLCW status data line (serial mode). The data is provided on the falling edge of CLCWSB or on the falling edge of CLCWCB.

**Telemetry Interface**

CPDUS/PCSN	I	CPDU status report sample. This signal indicates that the CPDU status report is sampled by the telemetry interface in serial mode. Active low. This signal has the function parallel bus chip select (PCSN) in parallel mode. This signal can be asynchronous
FAR1S/PAD2	I	FAR status report first sample. This signal indicates that the first 16 bits of FAR are sampled in serial mode. Active low. This signal has the function bit 2 of parallel address bus (PAD2) in parallel mode. This signal can be asynchronous
FAR2S/PAD1	I	FAR status report second sample. This signal indicates that the last 16 bits of FAR are sampled in serial mode. Active low. This signal has the function bit 1 of parallel address bus (PAD1) in parallel mode. This signal can be asynchronous
AU1S/PAD0	I	AUS status report first sample. This signal indicates that the first 16 bits of AUS are sampled in serial mode. Active low. This signal has the function bit 0 of parallel address bus (PAD0) in parallel mode. This signal can be asynchronous.
AU2S	I	AUS status report second sample. This signal is used to read out the last 4 bits of the AU status report by asserting it four times. Active low. This signal can be asynchronous.
TMC	I	Common status clockout line used for CPDU, FAR and AUS (serial mode). This signal can be asynchronous.
TMD	O	Common status data line for CPDU, FAR and AUS (serial mode). The data is provided on the falling edge of CPDUS, FAR1S, FAR2S, AU1S or AU2S, or after the falling edge of TMC.

**Parallel Interface**

PRDY	O	Parallel interface control line. This output is asserted when the data selected by PAD<2...0> is available in parallel mode. Active low.
PBUS<15..0>	O	Parallel interface data bus PBUS<15..0> (PBUS0 being the LSB). PBUS tristate is controlled by the PCSN input. When PCSN is deasserted PBUS is tristated.

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### External Authentication Unit Interface

AUDIS	I	Internal AU disable signal. This signal allows bypassing of the internal or external authentication unit. The internal and external AU are disabled when AUDIS is high. This signal can be asynchronous
AUEXT	I	External AU select signal. This signal indicates the use of an external authentication unit. The PTD uses the external AU when AUEXT is high and the internal AU when AUEXT is low. This signal can be asynchronous
AUST	O	AU start signal. This signal indicates that a TC frame is received and must be authenticated. It remains active as long as the external AU is working; it is deasserted after the activation of the AUEND input. Active high.
AUBUF	O	Buffer indication signal. This signal indicates which back-end buffer contains the TC segment to be authenticated. AUBUF=0: buffer 0 is used AUBUF=1: buffer 1 is used.
AUEND	I	AU result validation signal. This signal validates the authentication process result given on pin AUR, and indicates the end of the authentication process. This signal can be asynchronous
AUR	I	AU result signal. This signal indicates that the received TC frame is authorized or not authorized. AUR=0 indicates a bad authentication result, AUR=1 indicates a valid authentication. This signal can be asynchronous.
AUTSL	I	AU tail length select signal. This signal indicates the length of the tail for segments authenticated with the external AU. - AUTSL = 0: the length of the AU tail is 9 octets - AUTSL = 1: the length of the AU tail is 0 octets. If the internal AU is selected (AUEXT = 0), this signal defines the implementation of the Recovery LAC counter: - AUTSL = 0: the Recovery LAC counter is stored outside the RAM - AUTSL = 1: the Recovery LAC counter is stored in the RAM.
AUSBUF	O	AU Status buffer. This output indicates which AU status buffer that the external AU should update. - AUSBUF = 0: AU status buffer 0 - AUSBUF = 1: AU status buffer 1.
FARBUF	O	FAR buffer. This output indicates which FAR status buffer that the external AU should update. - FARBUF = 0: FAR status buffer 0 - FARBUF = 1: FAR status buffer 1.

### Miscellaneous

RFAVN	I	Incoming signal from physical layer, used to generate CLCW report. Active low. Asynchronous.
VCLSB	I	Virtual Channel Identifier LSB (static input). This bit enables differentiation between nominal and redundant decoder, even when using the same Configuration ROM for both decoders. - VCLSB = 1: The 'VC ID' LSB read from the ROM is inverted - VCLSB = 0: The 'VC ID' LSB read from the ROM is not inverted.
SELTC<2..0>	O	Selected TC channel signals. These outputs indicate the last selected TC channel on which the data present in the back-end buffer was received, it does not concern the CLTUs being input. SELTC<0> is the LSB.
DECOD	O	Decode state signal. This signal indicates that the PTD is in the Decode state (active for all bits after the start sequence until and including the tail sequence); it can be used for a scrambler.
TMMOD	I	TM mode signal. This static signal allows selection of the telemetry serial mode. - TMMOD = 0: the status (CPDUS, FAR, AUS) words are fetched with 5 samples - TMMOD = 1: the status (CPDUS, FAR, AUS) words are fetched with 2 samples.
RESETN	I	Reset signal. This signal allows the initialization of the PTD. Active low.
PAR	I	Parallel or serial interface selecting pin. This static input allows selection of the parallel or serial interface for MAP data and TM data. - PAR = 1: parallel mode is selected - PAR = 0: serial mode is selected.
MODE	I	Reserved pin. This static input shall be connected to ground.
CONF	I	Reserved pin. This static input shall be connected to ground.
PRIOR	I	Priority mode configuration pin. When this static input is set to 1, the priority mode (TC channels selection) is selected.
TEST	I	Test pin for production test only. This static input shall be connected to ground in functional mode.
CLK	I	System Clock signal.
VDD	I	+5V (12 pins).
VSS	I	Ground (14 pins).

## 8. ELECTRICAL CHARACTERISTICS AND RATINGS

### 8.1 DC PARAMETERS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	$V_{DD}+0.3$	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

**Note:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 7: Absolute Maximum Ratings**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{DD}$	Supply Voltage	-	4.5	5.0	5.5	V
$V_{IHC}$	CMOS input high voltage	-	$0.8 V_{DD}$	-	$V_{DD}$	V
$V_{ILC}$	CMOS input low voltage	-	$V_{SS}$	-	$0.2 V_{DD}$	V
$V_{IHT}$	TTL input high voltage	-	2	-	-	V
$V_{ILT}$	TTL input low voltage	-	-	-	0.8	V
$V_{OH}$	Output high voltage	$I_{OH} = -3.2mA$	$0.9 V_{DD}$	-	-	V
$V_{OL}$	Output high voltage	$I_{OL} = 5.0mA$	-	-	$0.1 V_{DD}$	V
$I_{PDL}$	Input Pull-down current	$V_{DD} = 5.5V, V_{IN} = V_{SS}$	-30	-	30	$\mu A$
$I_{PDH}$	Input Pull-down current	$V_{DD} = 5.5V, V_{IN} = V_{DD}$	-30	-	150	$\mu A$
$I_{PUL}$	Input Pull-up current	$V_{DD} = 5.5V, V_{IN} = V_{SS}$	-150	-	30	$\mu A$
$I_{PUH}$	Input Pull-up current	$V_{DD} = 5.5V, V_{IN} = V_{DD}$	-30	-	30	$\mu A$
$I_L$	Input leakage current	$V_{DD} = 5.5V, V_{IN} = V_{SS}$ or $V_{DD}$	-10	-	10	$\mu A$
$I_{OZL}$	Output leakage current	$V_{DD} = 5.5V, V_{OUT} = V_{SS}$	-50	-	50	$\mu A$
$I_{OZH}$	Output leakage current	$V_{DD} = 5.5V, V_{OUT} = V_{DD}$	-50	-	50	$\mu A$
$I_{OPDL}$	Output Pull-down current	$V_{DD} = 5.5V, V_{IN} = V_{SS}$	-50	-	50	$\mu A$
$I_{OPDH}$	Output Pull-down current	$V_{DD} = 5.5V, V_{IN} = V_{DD}$	-50	-	150	$\mu A$
$I_{DD1}$	Static Power supply Current	$V_{DD} = 5.5V$	-	0.5	20	mA
$I_{DD2}$	Dynamic Power supply Current	$f = 4MHz, V_{DD} = 5.5V$	-	20	40	mA

- Notes: 1.  $V_{DD} = 5V \pm 10\%$  over full temperature range.  
 2. Total dose radiation not exceeding  $10^5$  Rads(Si).  
 3. Mil-Std-883, method 5005, subgroups 1, 2, 3.  
 4. All outputs are suitable for TTL/CMOS drive.  
 5. Electro-Static Discharge protection is provided for all pins.  
 6. Internal pull-up or pull-down resistors should not be relied upon for proper operation and/or termination of input levels under all operating conditions without prior consultation with Dynex Semiconductor.  
 7. Input and output leakage measurements are guaranteed but not tested at  $-55^\circ C$ .

**Table 8: DC Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$C_{IN}$	Input Capacitance	$V_I = 0V$	-	3	5	pF
$C_{OUT}$	Output Capacitance	$V_{IO} = 0V$	-	5	7	pF

NOTE 1:  $T_A = 25^\circ C$  and  $f = 1MHz$ . Data obtained by characterisation or analysis; not routinely measured.

**Table 9: Capacitance**

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## 8.2 AC CHARACTERISTICS

Symbol	Parameter	Conditions
$F_T$	Functionality	$V_{DD} = 4.5 - 5.5V$ , $FREQ = 4MHz$ $V_{IL} = V_{SS}$ , $V_{IH} = V_{DD}$ , $V_{OL} = V_{OH} = V_{DD}/2$ Temp. = $-55^{\circ}C$ to $+125^{\circ}C$ , GPS Pattern Set MIL-STD-883 5005 subgroups 7, 8A, 8B

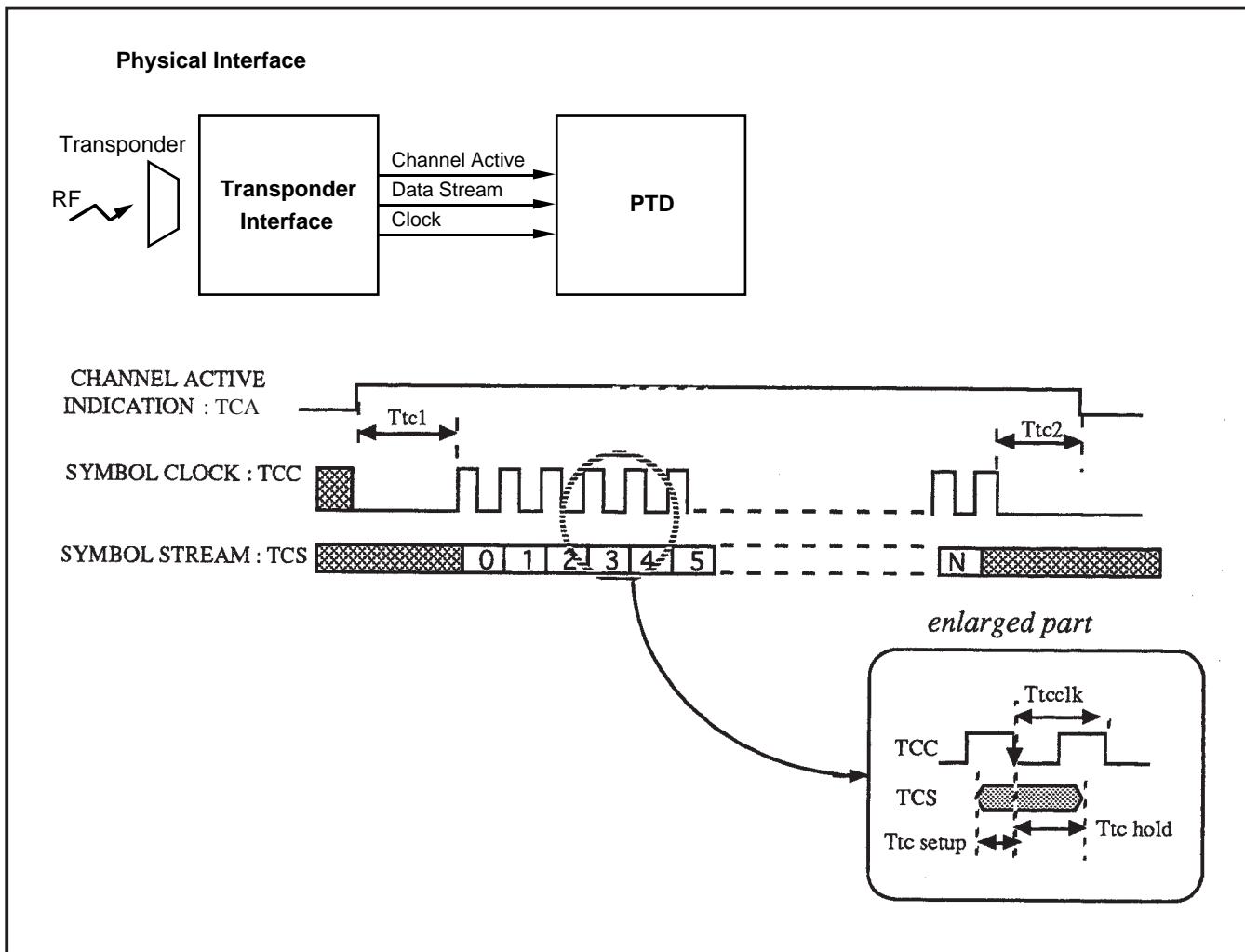
**Table 10: Functionality**

Symbol	Parameter	Min.	Typ.	Max.	Units
Fck	Clock frequency	-	-	4	MHz
Tck	Clock period	-	1/Fck	-	-
Tcl	Clock low pulse width	100	-	-	ns
Tch	Clock high pulse width	100	-	-	ns

- NOTES.
1.  $T_{CK}$  will be used as a reference for the timings.
  2. For timings specified as a number of clock cycles, it should be noted that there is a variance of  $\pm 10ns$  caused by the hold time (for inputs only) and different delays for rising and falling signals.
  3. It should be noted that a half clock cycle can mean either the longer or shorter time for a clock not having a duty cycle of 50%.
  4.  $V_{DD} = 5V \pm 10\%$  over full temperature range.
  5. Total dose radiation not exceeding  $10^5$  Rads (sec).
  6. Input pulse =  $V_{SS}$  to 4V.
  7. Measurement reference level = 1.5V.
  8. Output load 1 TTL gate and  $C_L = 50pF$ .
  9. Tables 11-25 contain Mil-Std-883, method 5005, subgroups 9, 10, 11.

**Table 11: Clock Timings**



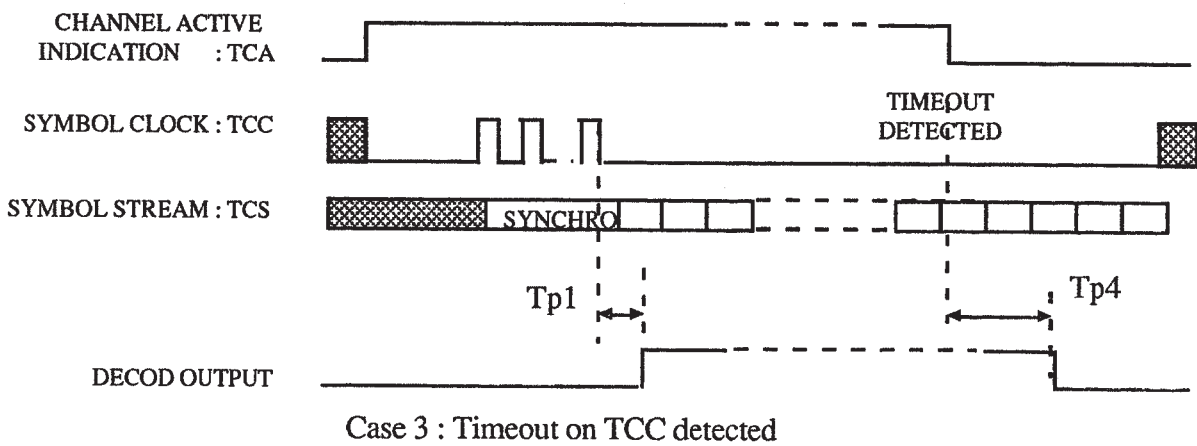
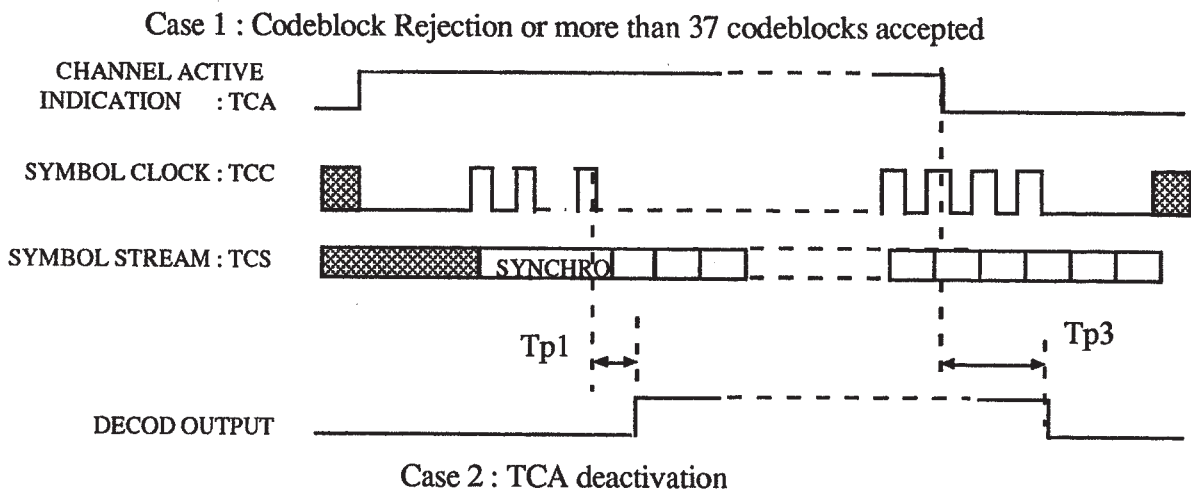
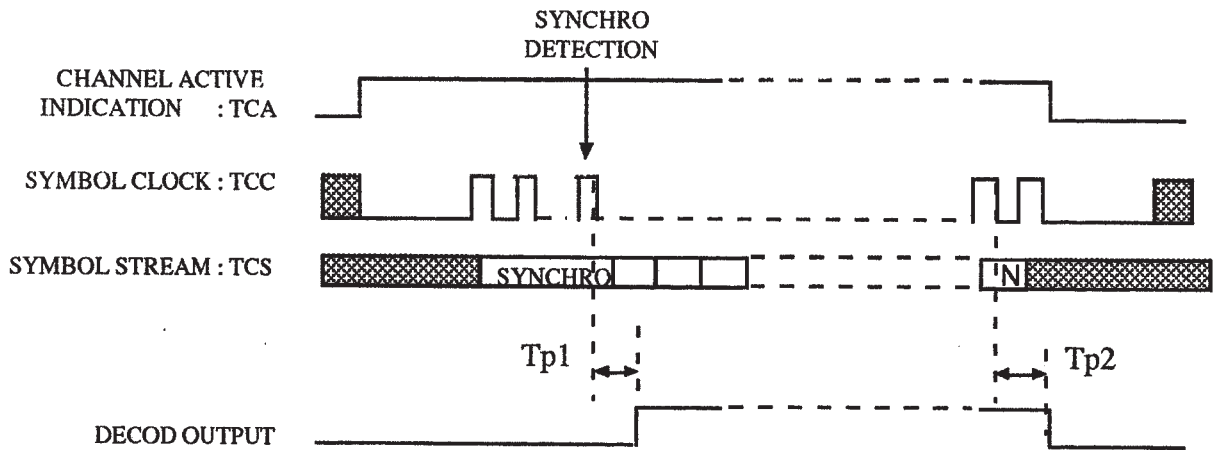


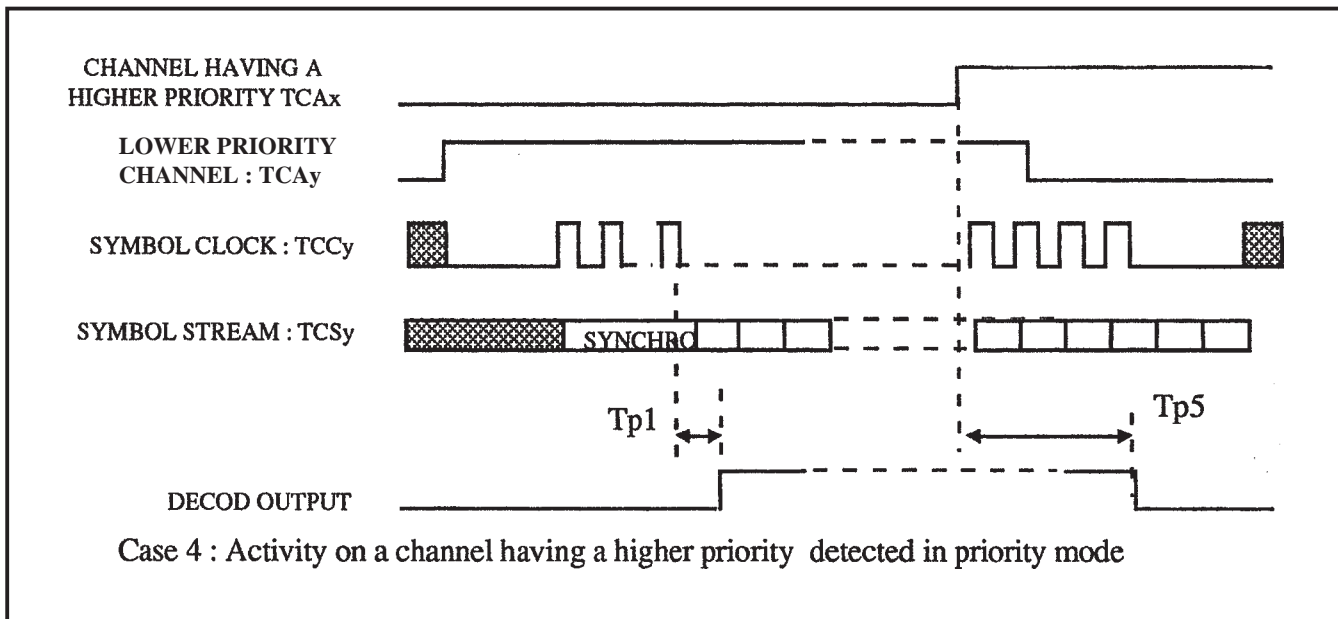
TIMING	Description	min	typ	max
Ttc1 *	TCA high to first TCC rising	4 Tck		
Ttc2 *	Last TCC falling to TCA low	4 Tck		
Ttcclk	TCC period	20 μs		
Ttc setup	TCS setup to TCC falling	0 ns		
Ttc hold	TCS hold after TCC falling	4 Tck		

\* NOTE: if the required timing is not fulfilled on Ttc1 and Ttc2, there is a risk of loss of the first or last bits.

Table 12: Physical Interface Timings

### Decod Output

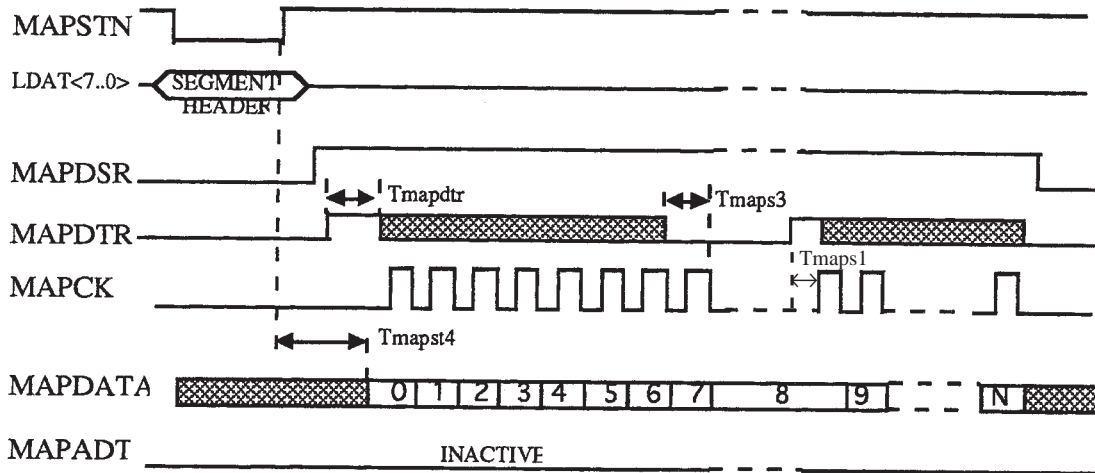
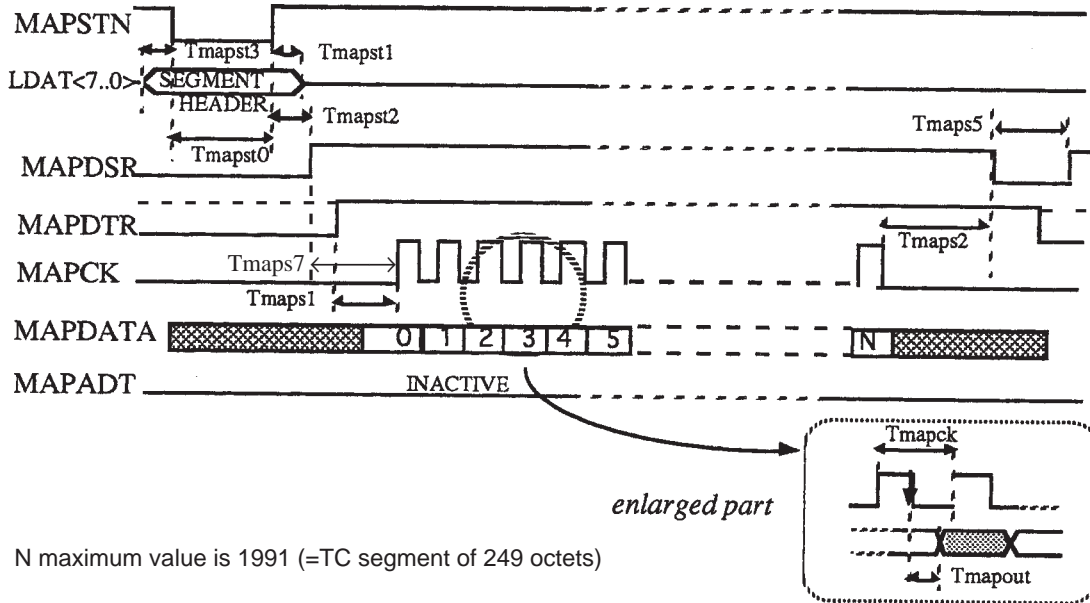
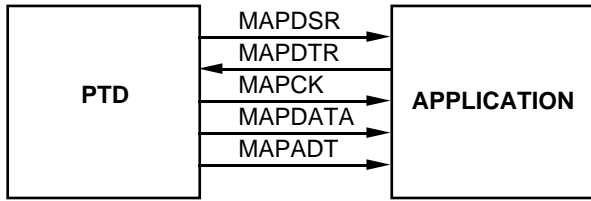




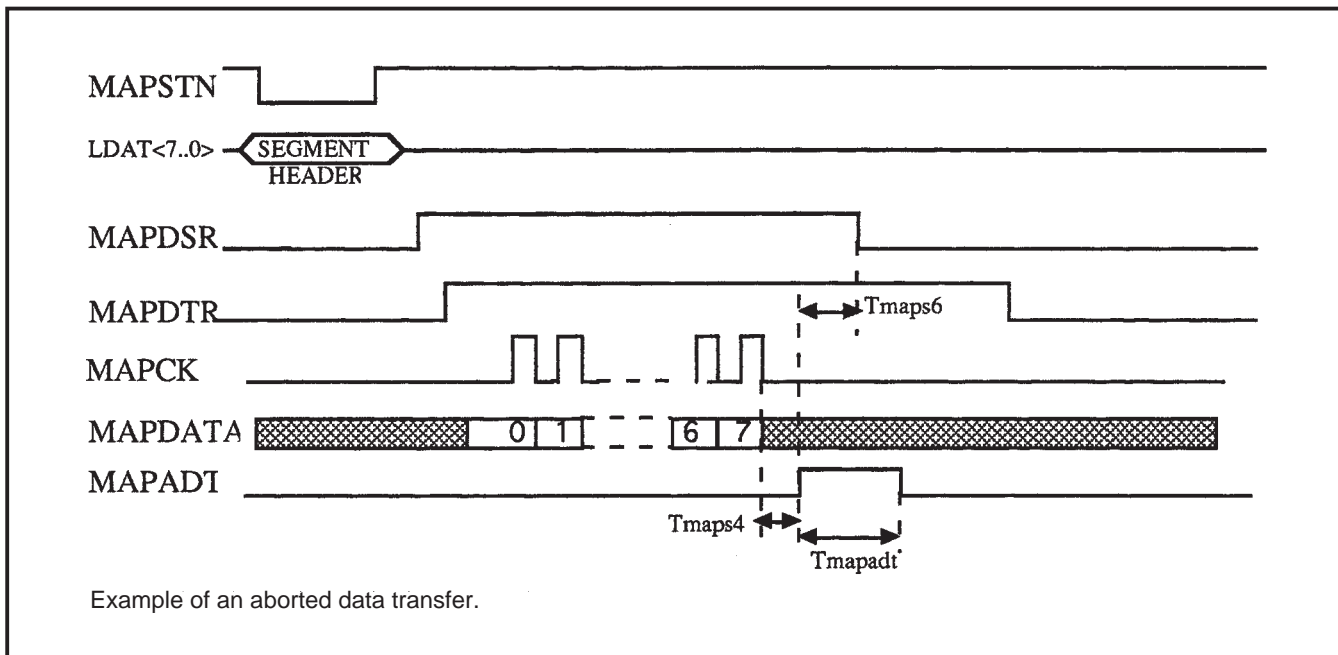
Timing	Description	Min	Typ	Max
Tp1	TCC falling of the last synchro bit to DECOD rising			3 Tck
Tp2	TCC falling of the last bit of the rejected codeblock or of the last bit of codeblock number 38 to DECOD falling			3 Tck
Tp3	TCA deactivated to DECOD falling			3 Tck
Tp4	Timeout on TCC detected to DECOD falling			3 Tck
Tp5	TCA rising on the channel with higher priority to DECOD falling			3 Tck

Table 13: DECOD Output Timings

Serial MAP Interface



Example of data transfer with data flow control  
 for each MAPDTR pulse one octet is being transferred  
 N maximum value is 1991 (=TC segment of 249 octets)



Timing	Description	Min	Typ	Max
Tmapst0 (1) (3)	MAPSTN low pulse width		1 Tck	
Tmapst1	LDAT hold after MAPSTN rising	0.5 Tck		
Tmapst2	MAPST rising to MADSR rising	2 Tck		1 Tmapck + 2 Tck
Tmapst3	LDAT setup to MAPSTN falling	0.5 Tck		
Tmapst4	MAPSTN rising to MAPDATA valid	2 Tck		1 Tmapck + 2 Tck
Tmaps1	MAPDTR high to MAPCK rising	0.5 Tmapck		1.5 Tmapck + 1 Tck
Tmaps2 (3)	MAPCK falling to MAPDSR falling		1 Tmapck	
Tmaps3	MAPDTR setup to MAPCK falling	2 Tck		
Tmapck (2)	MAPCK period	2 Tck		[2 <sup>13</sup> ] Tck
Tmapout	MAPCK falling to MAPDATA valid	-5 ns		10 ns
Tmapdtr	MAPDTR high pulse width	2 Tck		
Tmapadt (3)	MAPADT high pulse width		2 Tmapck	
Tmaps4 (3)	MAPCK falling to MAPADT rising		1 Tmapck	
Tmaps5	MAPDSR falling to MAPDSR rising	56 Tck		
Tmaps6 (3)	MAPADT rising to MAPDSR falling		1 Tmapck	
Tmaps7 (4)	MAPDSR rising to MAPCK rising	0.5 Tmapck		1.5 Tmapck

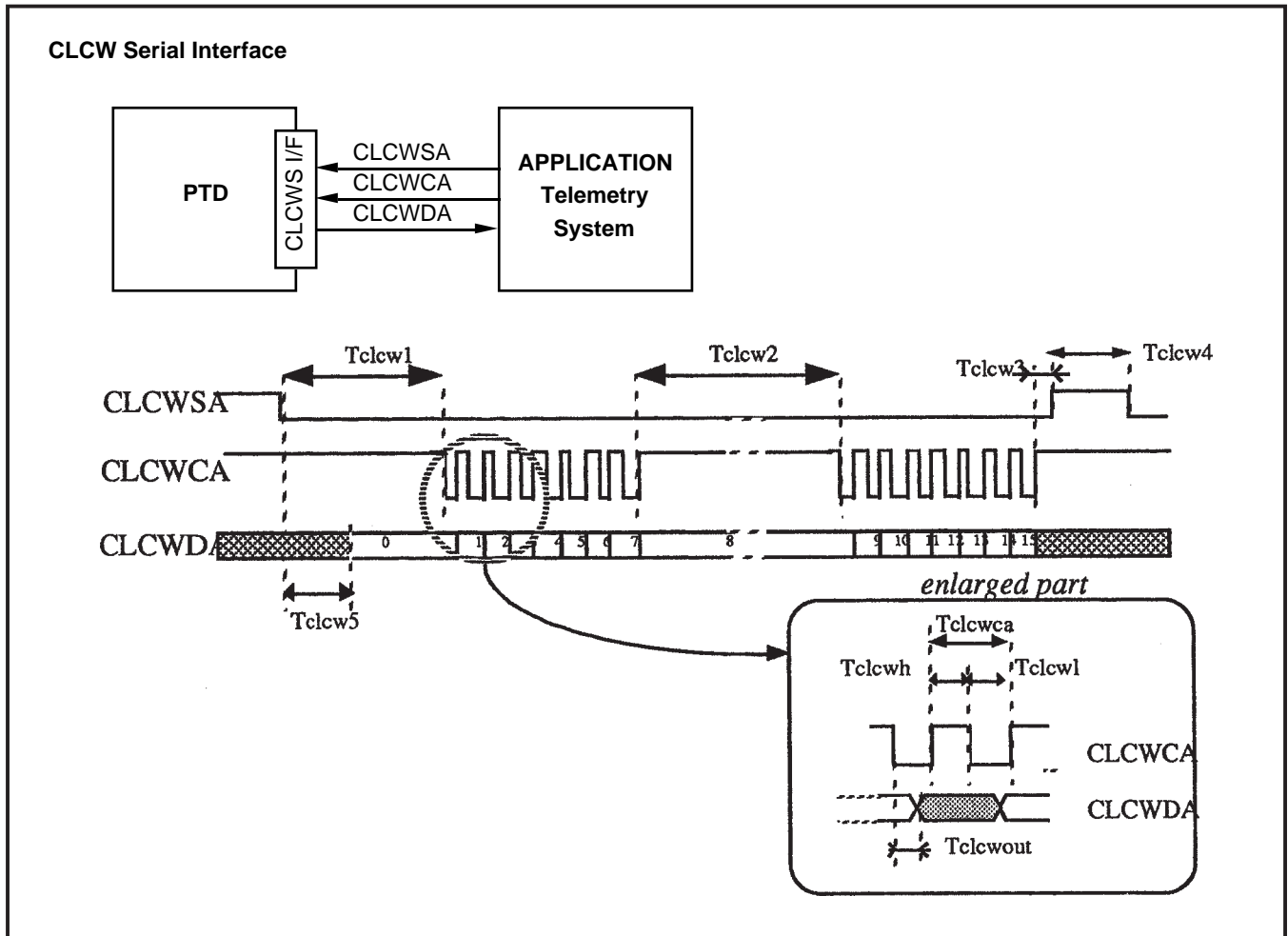
Note (1): This timing is specified with no wait state configuration (LACK permanently asserted). The asserting of this signal is identical with the asserting of the RAMCSN signal in a write cycle.

Note (2): Tmapck period is programmable as defined in section 5.2.

Note (3): These timings are exact with a variance of -10ns to +10ns.

Note (4): This timing is for a data transfer with MAPDTR permanently asserted.

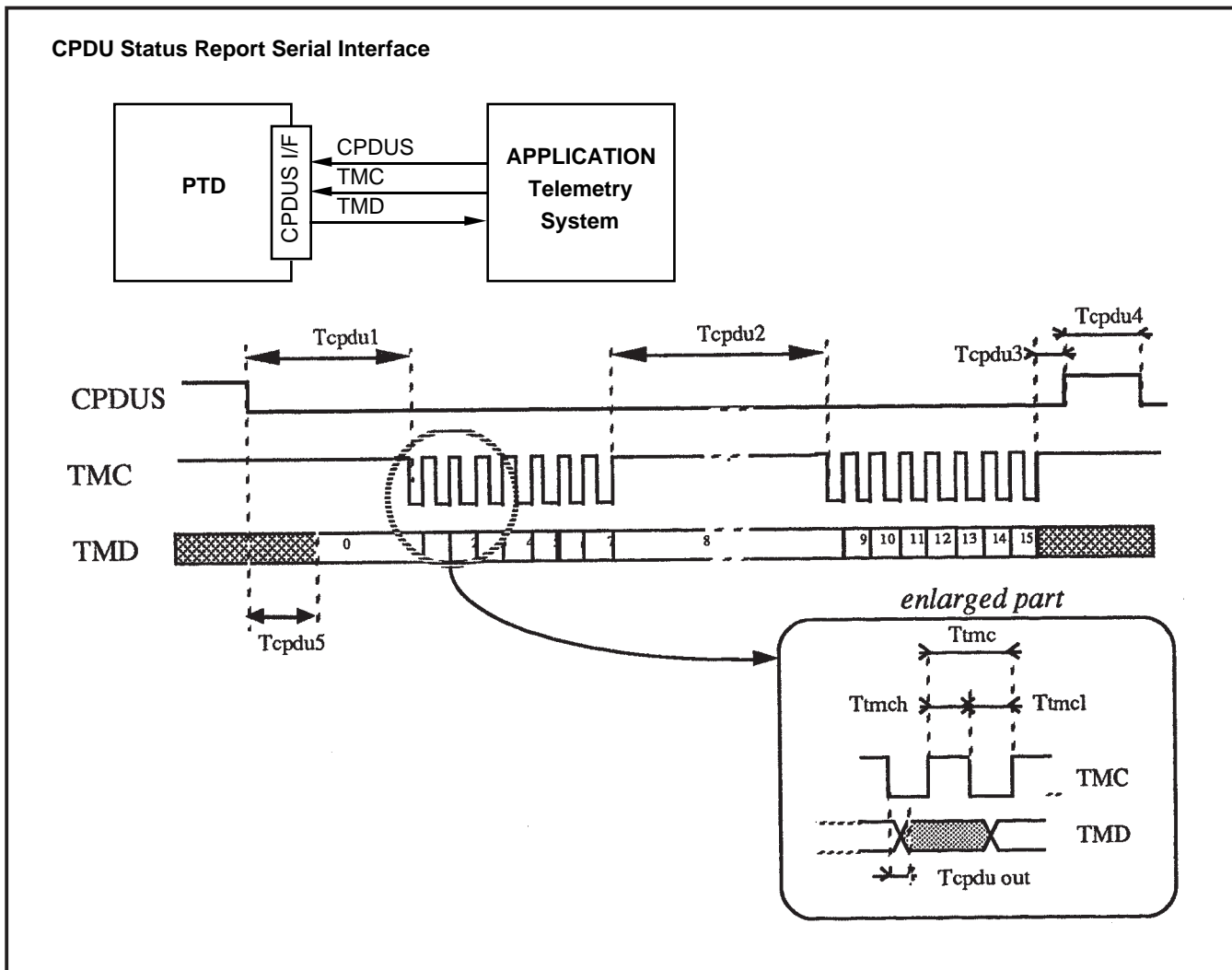
Table 14: Serial MAP Interface Timings



Timing	Description	Min	Typ	Max
Tclw1	CLCWSA falling to CLCWCA falling	5 Tck		
Tclw2	CLCWCA high pulse width between octets	2 Tck		
Tclw3	CLCWCA setup to CLCWSA	0 ns		
Tclw4	CLCWSA high pulse width	3 Tck		
Tclw5	CLCWSA falling to CLCWDA valid (bit 0)	4 Tck		
Tclcwh	CLCWCA high pulse width	Tck		
Tclcwl	CLCWCA low pulse width	Tck		
Tclcwca	CLCWCA period	4 Tck		
Tclcwout	CLCWCA falling to CLCWDA valid	1 Tck		2 Tck

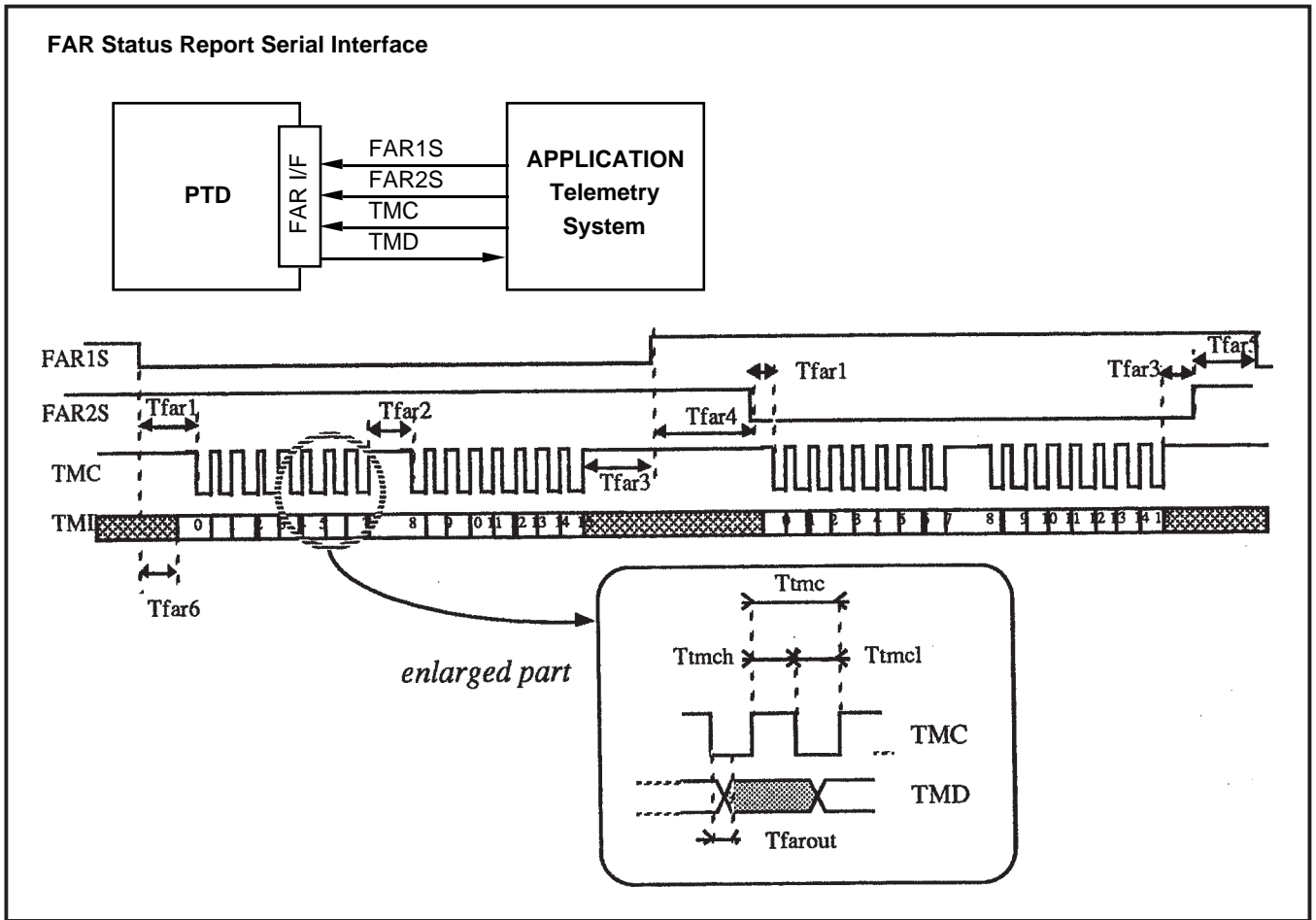
Note: The same timings apply for the redundant CLCW status telemetry interface, which is composed of CLCW SB, CLCW CB, CLCW DB signals.

Table 15: CLCW Serial Interface Timings



Timing	Description	Min	Typ	Max
Tcpdu1	CPDUS falling to TMC falling	6 Tck		
Tcpdu2	TMC high pulse width between octets	2 Tck		
Tcpdu3	TMC setup to CPDUS	0 ns		
Tcpdu4	CPDUS high pulse width	3 Tck		
Tcpdu5	CPDUS falling to TMD valid (bit 0)	5 Tck		
Ttmch	TMC high pulse width	Tck		
Ttmcl	TMC low pulse width	Tck		
Ttmc	TMC period	4 Tck		
Tcpduout	TMC falling to TMD valid	1 Tck		2 Tck

Table 16: CPDUS Serial Interface Timings



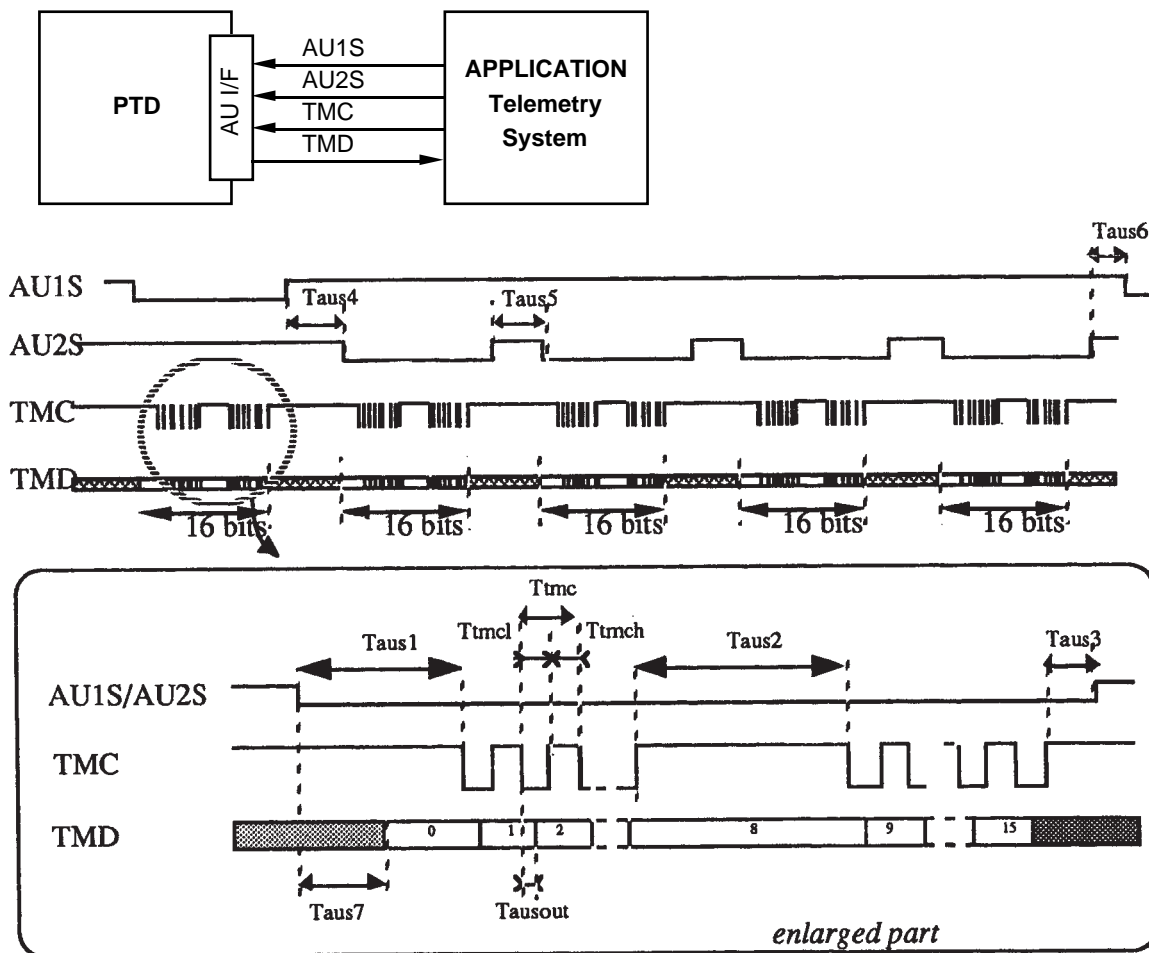
Timing	Description	Min	Typ	Max
Tfar1 (1)	FARS falling to TMC falling	16 Tck		
Tfar2	TMC high pulse width between octets	2 Tck		
Tfar3	TMC setup to FARS	0 ns		
Tfar4	FAR1S rising to FAR2S falling	2 Tck		
Tfar5	FAR2S rising to FAR1S falling	4 Tck		
Tfar6 (1)	FARS falling to TMD valid (bit 0)	15 Tck		
Tmch	TMC high pulse width	Tck		
Tmcl	TMC low pulse width	Tck		
Tmc	TMC period	4 Tck		
Tfarout	TMC falling to TMD valid	1 Tck		2 Tck

Note (1): These timings are guaranteed when there is no request for the local bus through the BRQN input. In addition when using slow memories, the local memory accesses may be delayed by using the LACK input of duration  $d_L$  (defined by the user). In this case Tfar1 and Tfar6 become  $Tfar1+2d_L$  and  $Tfar6+2d_L$ .

Table 17: FAR Status Report Serial Interface Timings



**AU Status Report Serial Interface**

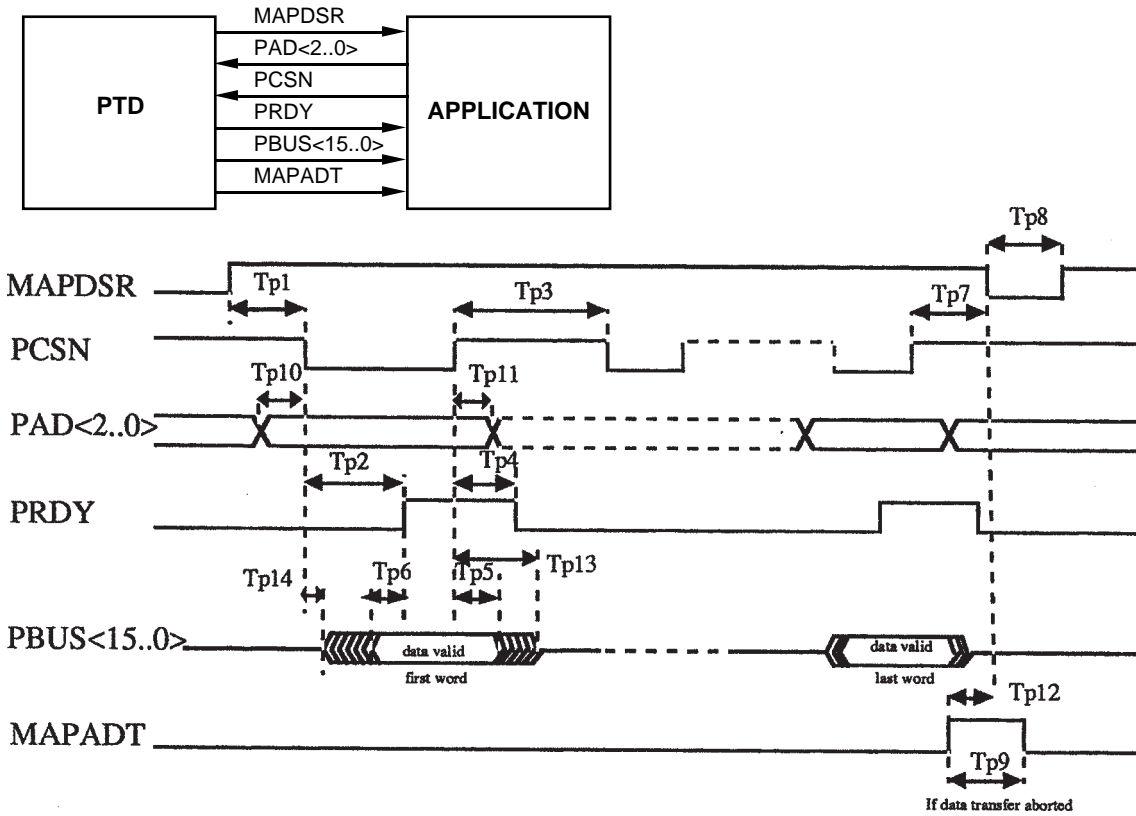


Timing	Description	Min	Typ	Max
Taus1 (1)	AUS falling to TMC falling	16 Tck		
Taus2	TMC high pulse width between octets	2 Tck		
Taus3	TMC setup to AUS	0 ns		
Taus4	AU1S rising to AU2S falling	2 Tck		
Taus5	AU2S rising to AU2S falling	2 Tck		
Taus6	AU2S rising to AU1S falling	4 Tck		
Taus7 (1)	AUS falling to TMD valid (bit 0)	15 Tck		
Ttmch	TMC high pulse width	Tck		
Ttmcl	TMC low pulse width	Tck		
Ttmc	TMC period	4 Tck		
Tausout	TMC falling to TMD valid	1 Tck		2 Tck

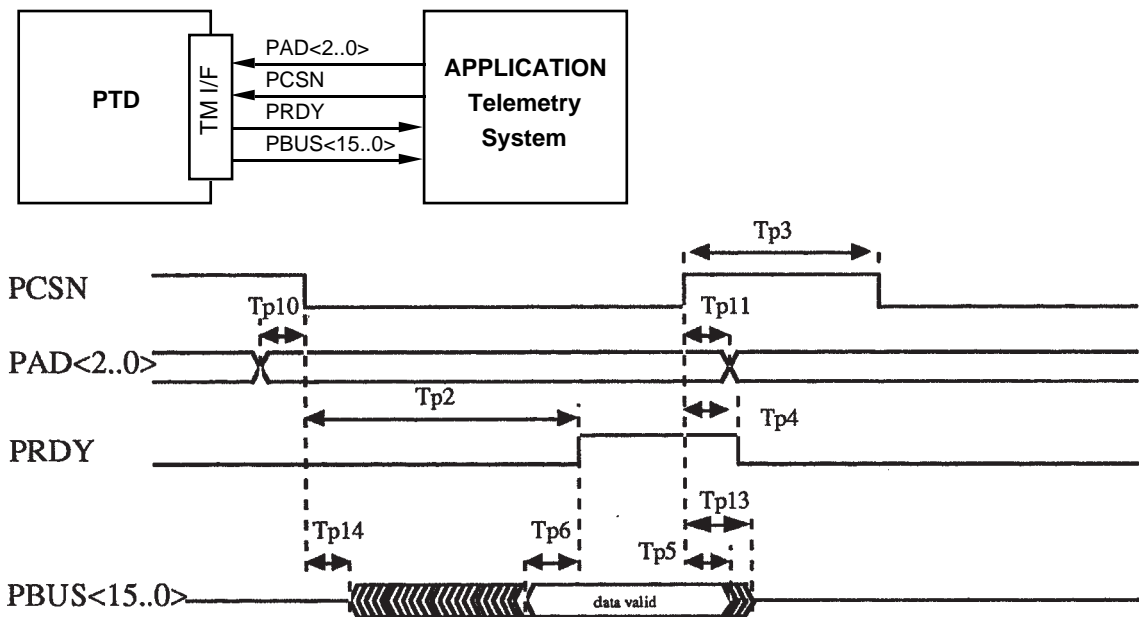
Note (1): These timings are guaranteed when there is no request for the local bus through the BRQN input. In addition when using slow memories, the local memory accesses may be delayed by using the LACK input of duration  $d_L$  (defined by the user). In this case Taus1 and Taus6 become Taus1+2 $d_L$  and Taus7+2 $d_L$ .

**Table 18: AU Status Report Serial Interface Timings**

Parallel MAP Interface



Status Report Telemetry Parallel Interface

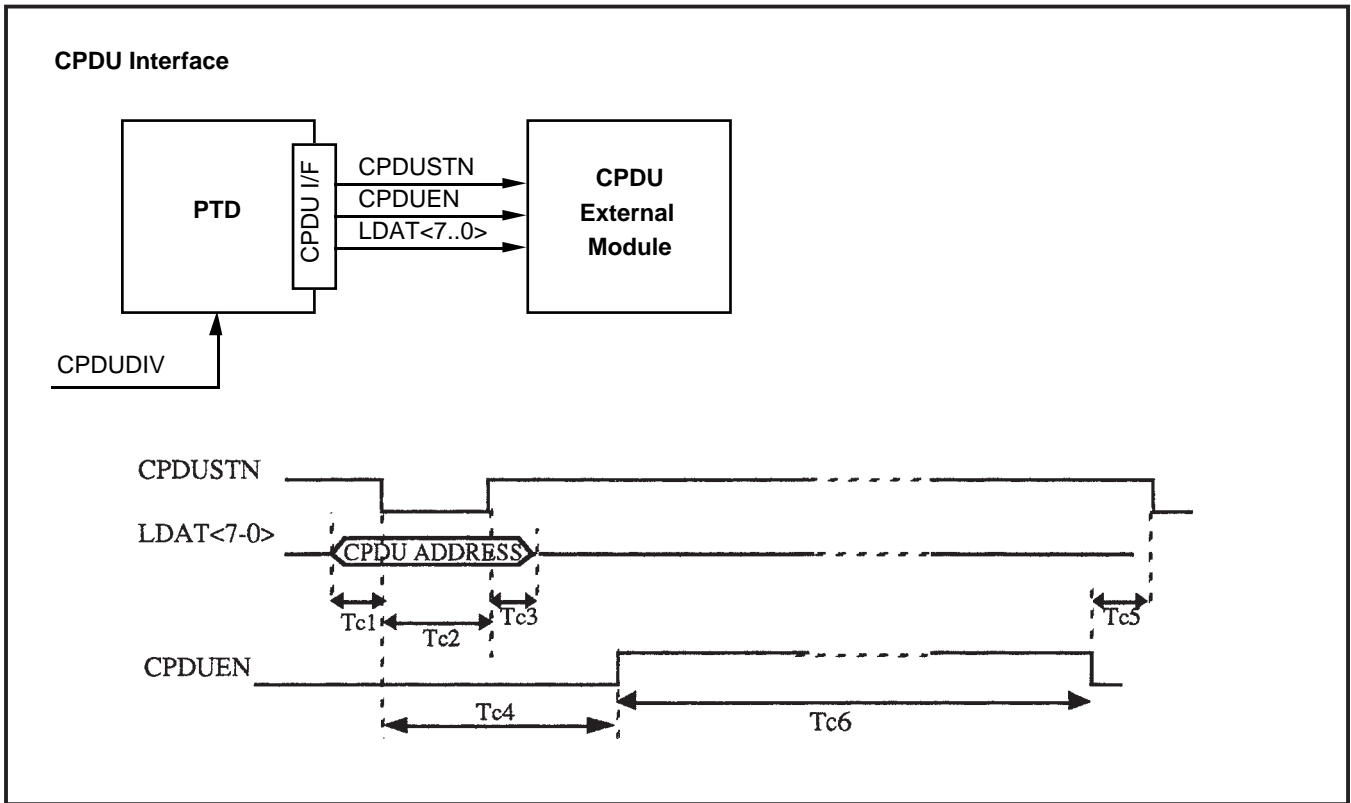


Timing	Description	Min	Typ	Max
Tp1	MAPDSR rising to PCSN falling	0 ns		
Tp2 (1)	PCSN falling to PRDY rising - for MAP word (1) - for CLCW word - for CPDU status word - for AU and FAR status word (1)	2 Tck		17 Tck 5 Tck 7 Tck 13 Tck
Tp3	PCSN high width	Tck		
Tp4	PCSN rising to PRDY falling			39 ns
Tp5	PBUS hold after PCSN rising	0 ns		
Tp6	PBUS valid before PRDY	Tck		
Tp7	PCSN rising to MAPDSR falling	3 Tck		4 Tck
Tp8	MAPDSR low pulse width	40 Tck		
Tp9 (2)	MAPADT high pulse width		2 Tck	
Tp10	PAD setup to PCSN falling	Tck		
Tp11	PAD hold after PCSN rising	Tck		
Tp12 (2)	MAPADT rising to MAPDSR falling		Tck	
Tp13	PCSN rising to PBUS tristate			31 ns
Tp14	PCSN falling to PBUS asserted	0 ns		55 ns

Note (1): These timings are guaranteed when there is no request for the local bus through the BRQN input. In addition when using slow memories, the local memory accesses may be delayed by using the LACK input, two extra delays shall be added to Tp2.

Note (2): These timings are exact with a variance of -10ns to +10ns.

**Table 19: Parallel MAP Interface Timings**

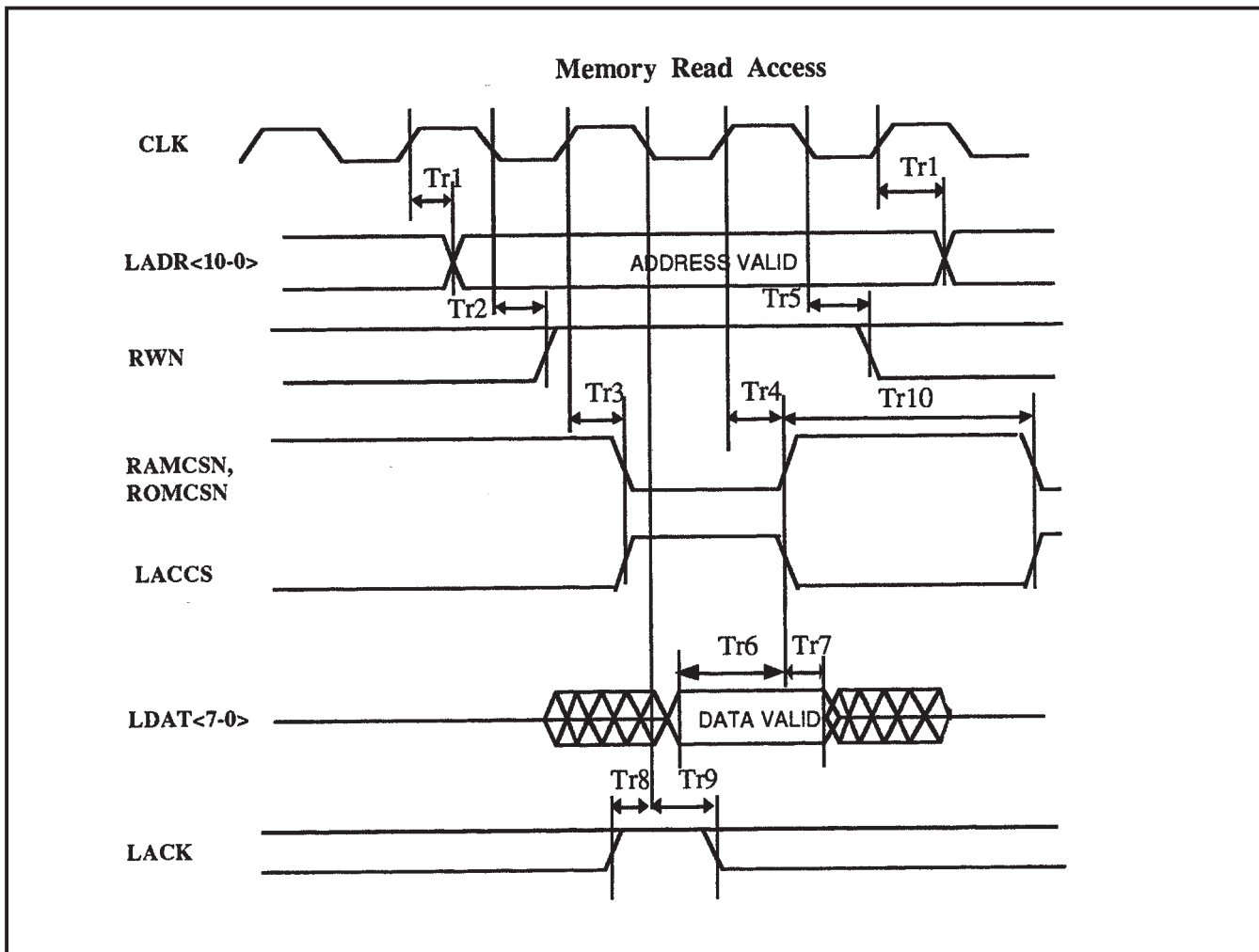


Timing	Description	Min	Typ	Max
Tc1	LDAT setup to CPDUSTN falling	0.5 Tck		
Tc2 (1) (2)	CPDUSTN low pulse width		1 Tck	
Tc3	LDAT hold after CPDUSTN rising	0.5 Tck		
Tc4	CPDUSTN falling to CPDUEN rising			D/2 - 3 Tck
Tc5 (2)	CPDUEN falling to CPDUSTN falling		D/2 + 1 Tck	
Tc6	CPDUEN high pulse width	D + Tck	$[2^X] \times D + Tck$	128D + Tck
D (1)	CPDUDIV = 0		40960 Tck	
D (1)	CPDUDIV = 1		8192 Tck	

Note (1): This timing is specified with no wait state configuration (LACK permanently asserted). The asserting of this signal is identical with the asserting of the RAMCSN signal in a write cycle.

Note (2): These timings are exact with a variance of -10ns to +10ns.

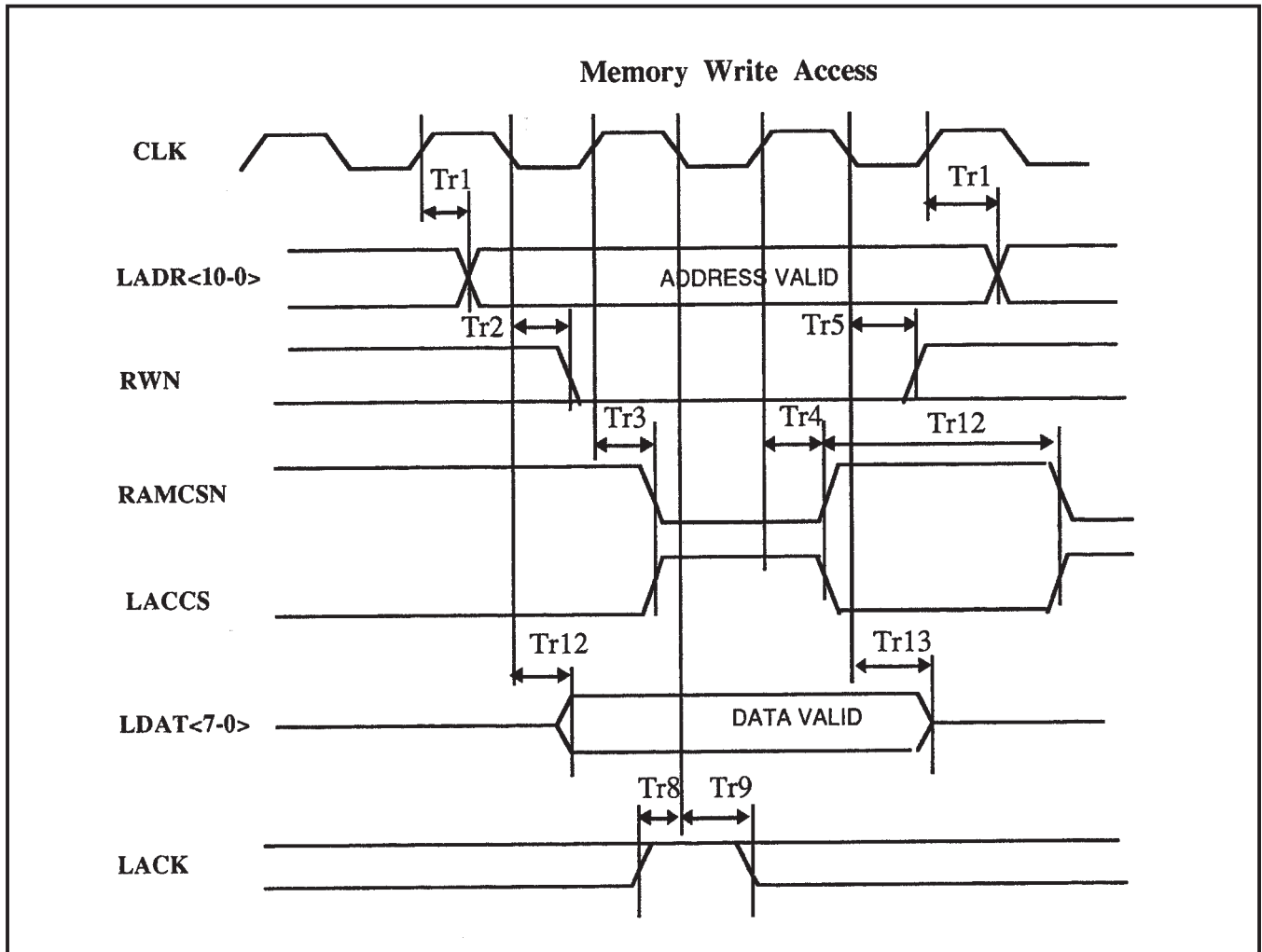
Table 20: CPDU Interface Timings



Timing	Description	Min	Typ	Max
Tr1	CLK rising to LADR valid	0 ns		150 ns
Tr2	CLK falling to RWN valid	0 ns		57 ns
Tr3	CLK rising to CSN asserted	0 ns		67 ns
Tr4	CLK rising to CSN deasserted	0 ns		68 ns
Tr5	CLK falling to RWN invalid	0 ns		57 ns
Tr6	LDAT setup to CSN deasserted	100 ns		
Tr7	LDAT hold after CSN deasserted	0 ns		
Tr8 (1)	LACK setup to CLK falling	20 ns		
Tr9 (1)	LACK hold after CLK falling	20 ns		
Tr10	CSN pulse width deasserted	2 Tck		

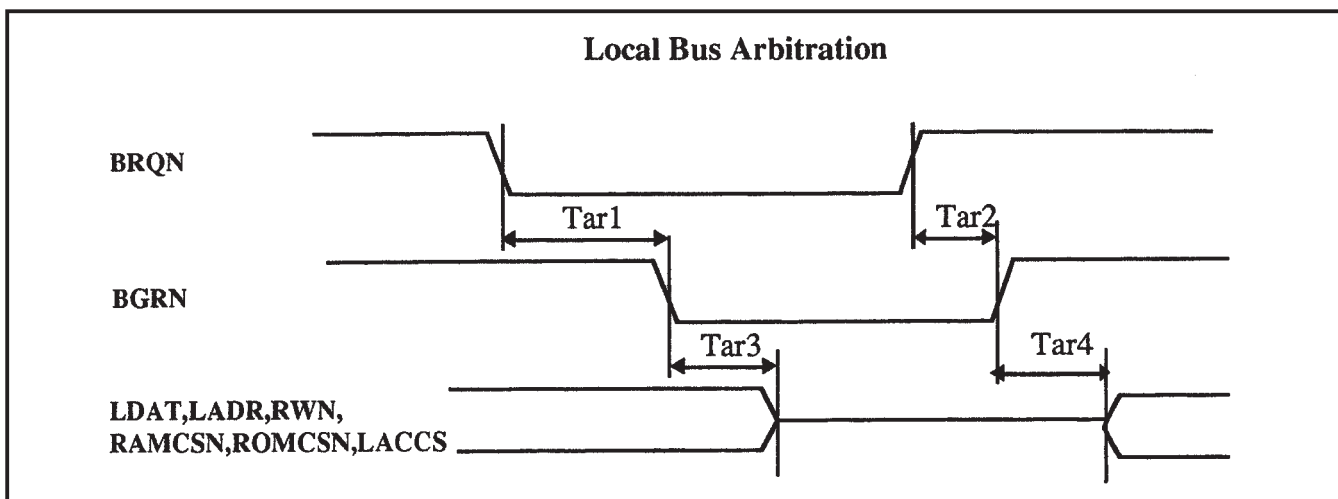
Note (1): Violation will lead to uncertainty about the number of wait states inserted.

Table 21: Memory Read Timings



Timing	Description	Min	Typ	Max
Tr12	CLK falling to LDAT valid	0 ns		62 ns
Tr13	CLK falling to LDAT hi-Z	0 ns		40 ns

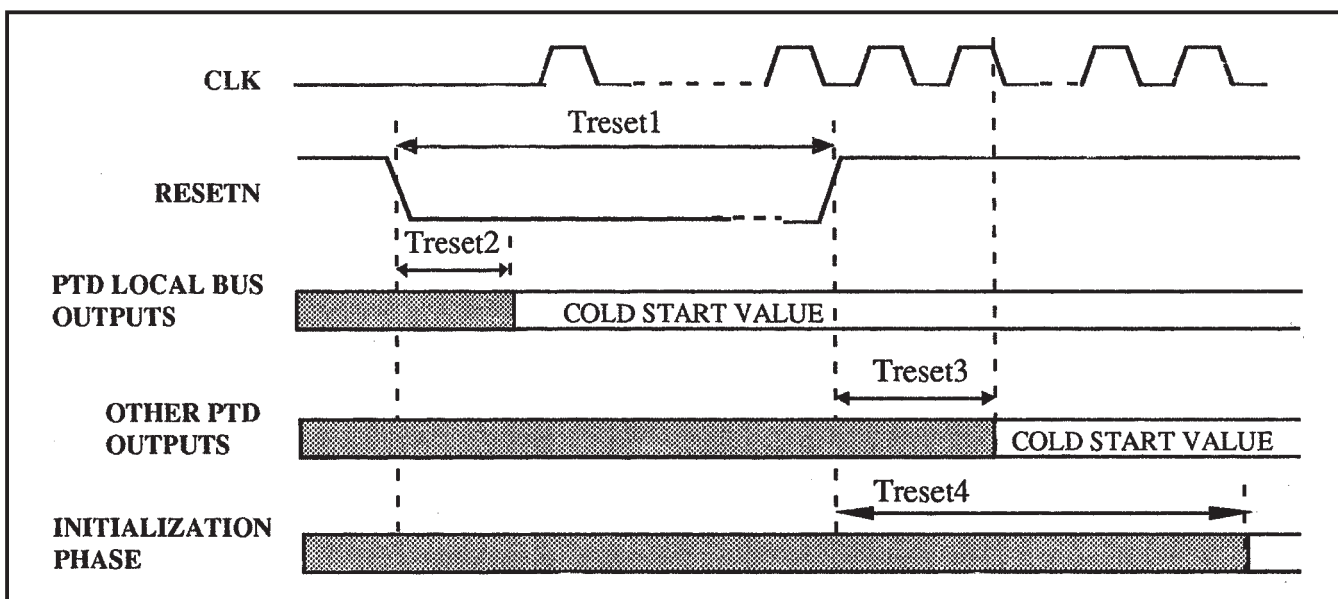
Table 22: Memory Write Timings



Timing	Description	Min	Typ	Max
Tar1 (1)	BRQN falling to BGRN falling	1.5 Tck		2.5 Tck
Tar2	BRQN rising to BGRN rising	1.5 Tck		2.5 Tck
Tar3	BGRN falling to Local Bus hi-Z			20 ns
Tar4	BGRN rising to Local Bus driven			20 ns

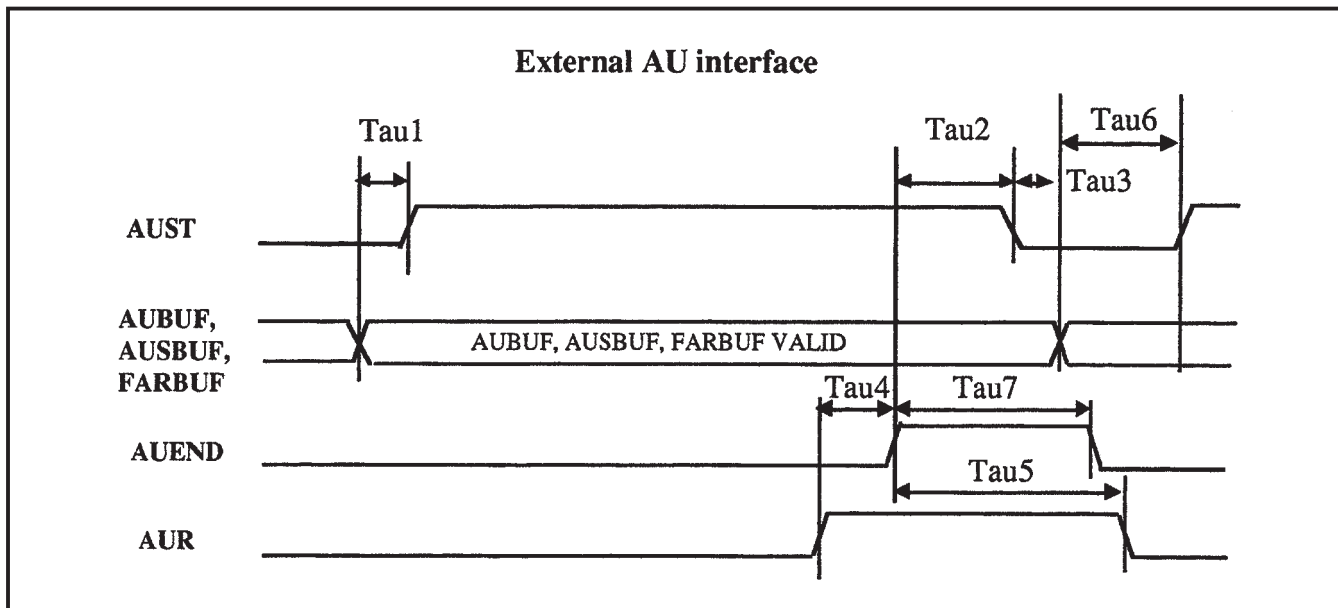
Note (1): This timing is dependent on the activity on the local bus. It is defined here for the case when the PTD does not use the local bus.

Table 23: Local Bus Arbitration Timings



Timing	Description	Min	Typ	Max
Treset1	ResetN low pulse width	5 Tck		
Treset2	ResetN asserted to local bus outputs at cold start values (0, 1; Z)			60 ns
Treset3	ResetN deasserted to PTD outputs at cold start values (0, 1; Z)			2 Tck
Treset4	ResetN deasserted to end of initialisation phase: PTD functional			200 Tck

Table 24: Reset Timings



Note: In order to use the external authentication unit, the AUDIS and AUEX signals should be set to 0 and 1 respectively.

Timing	Description	Min	Typ	Max
Tau1	AUBUF or AUSBUF or FARBUF setup to AUST rising	2 Tck		
Tau2	AUEND rising to AUST falling	2 Tck		3 Tck
Tau3	AUBUF or AUSBUF or FARBUF hold after AUST	0 ns		
Tau4	AUR setup to AUEND rising	2 Tck		
Tau5	AUR hold after AUEND rising	2 Tck		
Tau6	AUST pulse width deasserted	2 Tck		
Tau7	AUEND pulse width asserted	2 Tck		

Table 25: External AU Interface Timings

Subgroup	Definition
1	Static characteristics specified in Table 8 at +25°C
2	Static characteristics specified in Table 8 at +125°C
3	Static characteristics specified in Table 8 at -55°C
7	Functional characteristics specified in Table 10 at +25°C
8A	Functional characteristics specified in Table 10 at +125°C
8B	Functional characteristics specified in Table 10 at -55°C
9	Switching characteristics specified in Tables 11 to 25 at +25°C
10	Switching characteristics specified in Tables 11 to 25 at +125°C
11	Switching characteristics specified in Tables 11 to 25 at -55°C

Table 26: Definition of Subgroups

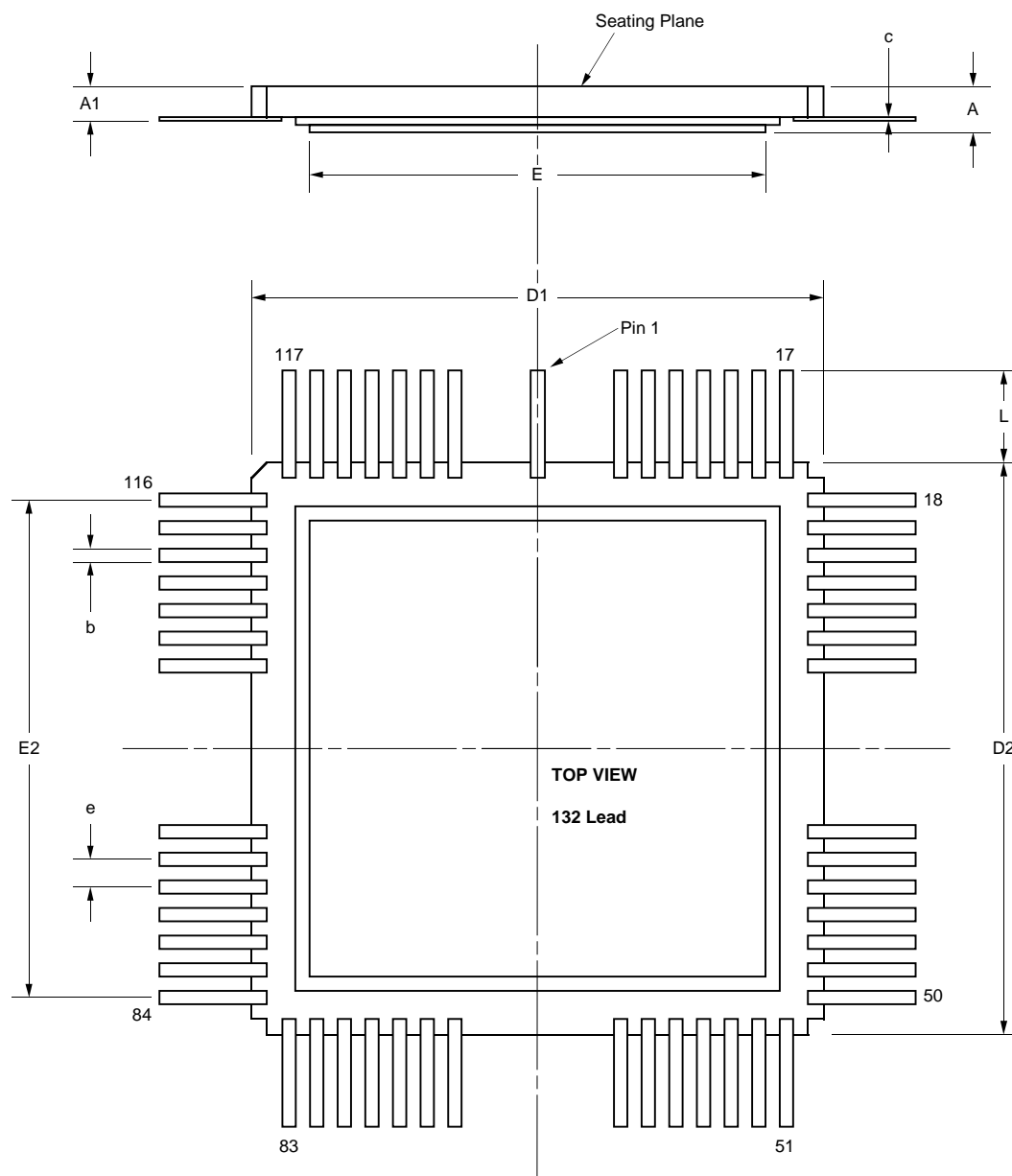


9. PACKAGE DETAILS

9.1 DIMENSIONS

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.59	-	-	0.102
A1	1.37	-	1.88	0.054	-	0.074
b	0.23	-	0.33	0.009	-	0.013
c	0.10	-	0.18	0.004	-	0.007
D1, D2	-	-	24.38	-	-	0.960
E	-	-	18.11	-	-	0.713
E2	-	20.32	-	-	0.800	-
e	-	0.63	-	-	0.025	-
L	6.35	-	7.11	0.250	-	0.280

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## 9.2 PIN ASSIGNMENT

The “type” field gives the type of buffer used in the PTD:

- CMOS                for CMOS input
- TTL                for TTL input
- 3STA                for tri-state output
- TTL/CMOS        for TTL/CMOS output
- TTL + 3STA        for a bidirectional TTL input associated with a tri-state output

The “buffer” field gives the name of the GPS MA9000a buffer used in the PTD:

- CMOSIP            for input CMOS buffer
- TTLIP             for input TTL buffer
- BOP                for TTL/CMOS output buffer
- TRIOUT            for output tristate buffer
- CSCHMITT        for input CMOS buffer with Schmitt trigger

The “pu/pd” field indicates if an internal pull up or pull down is present in the buffer.

Note: Internal pull-up or pull-down resistors should not be relied upon for proper operation and/or termination of input levels under all operating conditions without prior consultation with GPS.

### Transponder Interface

signal	pin	I/O	type	pu/pd	buffer	comments
TCC0	82	I	CMOS	PU	CSCHMITT	Symbol Clock signal
TCC1	79	I	CMOS	PU	CSCHMITT	" " "
TCC2	75	I	CMOS	PU	CSCHMITT	" " "
TCC3	72	I	CMOS	PU	CSCHMITT	" " "
TCC4	68	I	CMOS	PU	CSCHMITT	" " "
TCC5	65	I	CMOS	PU	CSCHMITT	" " "
TCS0	81	I	CMOS	PU	CSCHMITT	Symbol Stream signal
TCS1	78	I	CMOS	PU	CSCHMITT	" " "
TCS2	74	I	CMOS	PU	CSCHMITT	" " "
TCS3	71	I	CMOS	PU	CSCHMITT	" " "
TCS4	67	I	CMOS	PU	CSCHMITT	" " "
TCS5	64	I	CMOS	PU	CSCHMITT	" " "
TCA0	80	I	CMOS	PD	CSCHMITT	Channel Active Indication
TCA1	77	I	CMOS	PD	CSCHMITT	" " "
TCA2	73	I	CMOS	PD	CSCHMITT	" " "
TCA3	70	I	CMOS	PD	CSCHMITT	" " "
TCA4	66	I	CMOS	PD	CSCHMITT	" " "
TCA5	63	I	CMOS	PD	CSCHMITT	" " "

## Local Bus Interface

signal	pin	I/O	type	pu/pd	buffer	comments
LADR<0>	5	O	3STA		TRIOUT	Address bus
LADR<1>	4	O	3STA		TRIOUT	" "
LADR<2>	3	O	3STA		TRIOUT	" "
LADR<3>	2	O	3STA		TRIOUT	" "
LADR<4>	1	O	3STA		TRIOUT	" "
LADR<5>	132	O	3STA		TRIOUT	" "
LADR<6>	130	O	3STA		TRIOUT	" "
LADR<7>	129	O	3STA		TRIOUT	" "
LADR<8>	128	O	3STA		TRIOUT	" "
LADR<9>	127	O	3STA		TRIOUT	" "
LADR<10>	126	O	3STA		TRIOUT	" "
LDAT<0>	16	I/O	TTL+3STA	PD	TTLIP+TRIOUT	Data bus
LDAT<1>	15	I/O	TTL+3STA	PD	TTLIP+TRIOUT	" "
LDAT<2>	14	I/O	TTL+3STA	PD	TTLIP+TRIOUT	" "
LDAT<3>	13	I/O	TTL+3STA	PD	TTLIP+TRIOUT	" "
LDAT<4>	11	I/O	TTL+3STA	PD	TTLIP+TRIOUT	" "
LDAT<5>	10	I/O	TTL+3STA	PD	TTLIP+TRIOUT	" "
LDAT<6>	9	I/O	TTL+3STA	PD	TTLIP+TRIOUT	" "
LDAT<7>	8	I/O	TTL+3STA	PD	TTLIP+TRIOUT	" "
RWN	119	O	3STA		TRIOUT	Read/Write
BRQN	116	I	CMOS	PU	CMOSIP	Bus Request
BGRN	125	O	TTL/CMOS		BOP	Bus Grant
RAMCSN	120	O	3STA		TRIOUT	Chip Select RAM
ROMCSN	121	O	3STA		TRIOUT	Chip Select ROM
LACCS	122	O	3STA		TRIOUT	Recovery LAC access
LACK	115	I	CMOS	PU	CSCHMITT	Acknowledge

## Map Interface

signal	pin	I/O	type	pu/pd	buffer	comments
MAPSTN	22	O	TTL/CMOS		BOP	MAP strobe
MAPCK	25	O	TTL/CMOS		BOP	MAP clockout
MAPDSR	26	O	TTL/CMOS		BOP	MAP data set ready
MAPDTR	36	I	CMOS	PU	CSCHMITT	MAP data term. ready
MAPDATA	28	O	TTL/CMOS		BOP	MAP serial data
MAPADT	23	O	TTL/CMOS		BOP	MAP abort data

## CPDU Interface

signal	pin	I/O	type	pu/pd	buffer	comments
CPDUSTN	29	O	TTL/CMOS		BOP	Strobe signal
CPDUEN	30	O	TTL/CMOS		BOP	Pulse output
CPDUDIV	54	I	CMOS	PD	CMOSIP	Clock dividing

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### Telemetry Interface

signal	pin	I/O	type	pu/pd	buffer	comments
CLCWSA	47	I	CMOS	PU	CSCHMITT	CLCW status sample
CLCWCA	46	I	CMOS	PU	CSCHMITT	CLCW status clkout
CLCWDA	32	O	TTL/CMOS		BOP	CLCW status data
CLCWSB	45	I	CMOS	PU	CSCHMITT	Redundant CLCW
CLCWCB	44	I	CMOS	PU	CSCHMITT	Redundant CLCW
CLCWDB	31	O	TTL/CMOS		BOP	Redundant CLCW
CPDUS	43	I	CMOS	PU	CSCHMITT	CPDU status sample
FAR1S	42	I	CMOS	PU	CSCHMITT	FAR status first sample
FAR2S	40	I	CMOS	PU	CSCHMITT	FAR status last sample
AU1S	39	I	CMOS	PU	CSCHMITT	AU status first sample
AU2S	38	I	CMOS	PU	CSCHMITT	AU status second sample
TMC	37	I	CMOS	PU	CSCHMITT	CPDU/FAR/AU status clk
TMD	33	O	TTL/CMOS		BOP	CPDU/FAR/AU status data

### Parallel Interface

signal	pin	I/O	type	pu/pd	buffer	comments
PRDY	86	O	TTL/CMOS		BOP	Parallel interface control line
PBUS<0>	106	O	3STA		TRIOUT	Parallel interface data bus
PBUS<1>	105	O	3STA		TRIOUT	Parallel interface data bus
PBUS<2>	104	O	3STA		TRIOUT	Parallel interface data bus
PBUS<3>	103	O	3STA		TRIOUT	Parallel interface data bus
PBUS<4>	101	O	3STA		TRIOUT	Parallel interface data bus
PBUS<5>	100	O	3STA		TRIOUT	Parallel interface data bus
PBUS<6>	99	O	3STA		TRIOUT	Parallel interface data bus
PBUS<7>	98	O	3STA		TRIOUT	Parallel interface data bus
PBUS<8>	96	O	3STA		TRIOUT	Parallel interface data bus
PBUS<9>	95	O	3STA		TRIOUT	Parallel interface data bus
PBUS<10>	94	O	3STA		TRIOUT	Parallel interface data bus
PBUS<11>	93	O	3STA		TRIOUT	Parallel interface data bus
PBUS<12>	91	O	3STA		TRIOUT	Parallel interface data bus
PBUS<13>	90	O	3STA		TRIOUT	Parallel interface data bus
PBUS<14>	89	O	3STA		TRIOUT	Parallel interface data bus
PBUS<15>	88	O	3STA		TRIOUT	Parallel interface data bus

### Authentication Interface

signal	pin	I/O	type	pu/pd	buffer	comments
AUDIS	109	I	CMOS	PU	CMOSIP	Internal AU bypass signal
AUEXT	113	I	CMOS	PD	CMOSIP	External AU selection
AUST	84	O	TTL/CMOS		BOP	AU Start signal
AUBUF	85	O	TTL/CMOS		BOP	AU buffer signal
AUEND	112	I	CMOS	PD	CMOSIP	AU end validation signal
AUR	111	I	CMOS	PD	CMOSIP	AU result signal
AUTSL	110	I	CMOS	PU	CMOSIP	AU tail length select
AUSBUF	50	O	TTL/CMOS		BOP	AU Status Buffer
FARBUF	49	O	TTL/CMOS		BOP	FAR buffer

## Miscellaneous

signal	pin	I/O	type	pu/pd	buffer	comments
RFAVN	61	I	CMOS	PU	CSCHMITT	Physical interface status
VCLSB	60	I	CMOS	PD	CMOSIP	VCI <sub>d</sub> differentiation
TMMOD	58	I	CMOS	PD	CMOSIP	TM mode select
PAR	51	I	CMOS	PD	CMOSIP	Parallel/serial selection
RESETN	52	I	CMOS	PU	CSCHMITT	Reset
CLK	53	I	CMOS	PU	CSCHMITT	Clock
PRIOR	59	I	CMOS	PD	CMOSIP	Priority mode
TEST	114	I	CMOS	PD	CMOSIP	To be connected to VSS
MODE	57	I	CMOS	PD	CMOSIP	To be connected to VSS
CONF	56	I	CMOS	PD	CMOSIP	To be connected to VSS
SELTC<0>	21	O	TTL/CMOS		BOP	Selected Channel
SELTC<1>	20	O	TTL/CMOS		BOP	Selected Channel
SELTC<2>	19	O	TTL/CMOS		BOP	Selected Channel
DECOD	27	O	TTL/CMOS		BOP	Decode state

## Power Supply

signal	pin	I/O	type	pu/pd	buffer	comments
VDD	6					VDD power supply
VDD	12					VDD power supply
VDD	18					VDD power supply
VDD	35					VDD power supply
VDD	48					VDD power supply
VDD	62					VDD power supply
VDD	76					VDD power supply
VDD	87					VDD power supply
VDD	97					VDD power supply
VDD	107					VDD power supply
VDD	117					VDD power supply
VDD	124					VDD power supply
VSS	7					VSS power supply
VSS	17					VSS power supply
VSS	24					VSS power supply
VSS	34					VSS power supply
VSS	41					VSS power supply
VSS	55					VSS power supply
VSS	69					VSS power supply
VSS	83					VSS power supply
VSS	92					VSS power supply
VSS	102					VSS power supply
VSS	108					VSS power supply
VSS	118					VSS power supply
VSS	123					VSS power supply
VSS	131					VSS power supply

10. RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 method 1019 Ionizing Radiation (total dose) test.

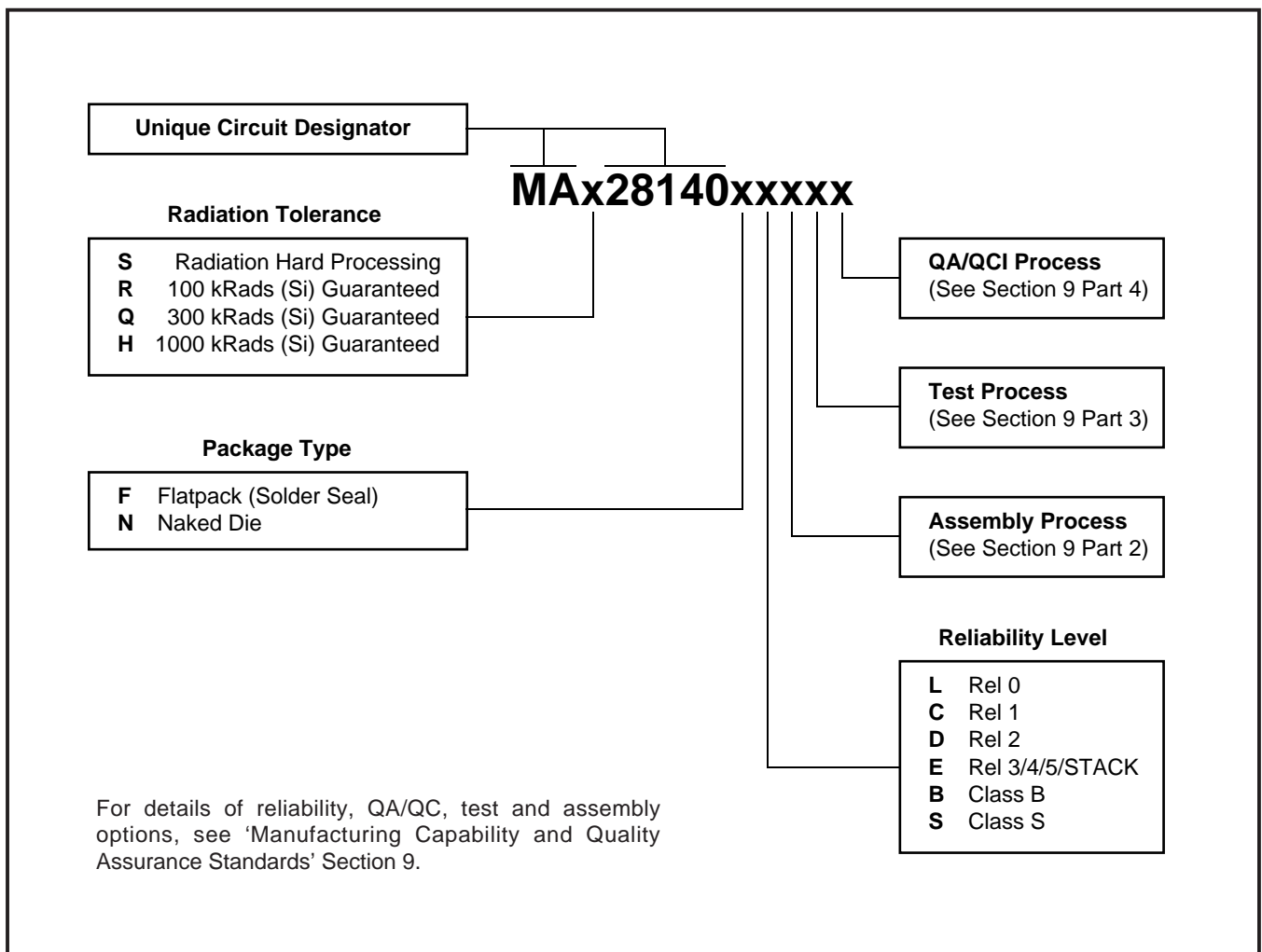
Total Dose (Function to specification)*	1x10 <sup>5</sup> Rad(Si)
Transient Upset (Stored data loss)	5x10 <sup>10</sup> Rad(Si)/sec
Transient Upset (Survivability)	>1x10 <sup>12</sup> Rad(Si)/sec
Neutron Hardness (Function to specification)	>1x10 <sup>15</sup> n/cm <sup>2</sup>
Single Event Upset**	<1x10 <sup>-11</sup> Errors/bit day
Latch Up	Not possible

\* Other total dose radiation levels available on request

\*\* Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 27: Radiation Hardness Parameters

11. ORDERING INFORMATION



## 12. SYNONYMS

AD	Accepted Data Frame (accepted by the FARM)	NRZ(-L)	Non Return to Zero (Level)
ASIC	Application Specific Integrated Circuit	N(S)	Frame Sequence Number of a transmitted TC Frame
AU(S)	Authentication Unit (Status)	NW	Negative Window
BC	Bypass Control Frame	PLOP	Physical Layer Operation Procedure
BD	Bypass Data Frame	PSK	Phase Shift Keying
CCSDS	Consultative Committee for Space Data Systems	PSS	Procedures, Specification and Standards
CLCW	Command Link Control Word	PTD	Packet Telecommand Decoder
CLTU	Command Link Transmission Unit	PW	Positive Window
CPDU(S)	Command Pulse Distribution Unit (Status)	RAM	Random Access Memory
CRC	Cyclic Redundant Code	RF	Radio Frequency
ESA	European Space Agency	ROM	Read Only Memory
FAR	Frame Analysis Report	EEPROM	Electrically Erasable Programmable ROM
FARM	Frame Acceptance and Reporting Mechanism	SEU	Single Event Upset
GPS	GEC Plessey Semiconductors	SOS	Silicon On Sapphire
ID	Identifier	TC	Telecommand
LAC	Logical Authentication Channel	TM	Telemetry
LFSR	Linear Feedback Shift Register	VC	Virtual Channel
LSB	Least Significant Bit	VCM	Virtual Channel Multiplexer
MAP	Multiplexed Access Point	V(R)	The next expected TC frame sequence number
MSB	Most Significant Bit	W	FARM Sliding Window Width (variable of the FARM)
NOP	No Operation		

## 13. APPLICATIONS

### Note 1: Failure/Problem Description

The CPDU I/F generates continuously false output signals in the event that "External Authentication" and "0 octet AU Trailers" are used (i.e. AUDIS='0', AUEXT='1' and AUTSL='1'). This malfunction is particularly critical for applications using the CPDU I/F for its intended purpose to handle emergency situations.

After generating a first sequence or correct output signals, the state machine driving the CPDU I/F will get caught in a never-ending loop of states and continue to generate false (pseudo-random) output signals until the PTD is reset by RESTN='0' or AUDIS='1'. No other command will stop the erroneous outputs of the CPDU I/F.

Recommended action by users

The following combination of signal states must not be used : AUDIS='0', AUEXT='1' and AUTSL='1'. This can be ensured by either hardwiring on the PCB or appropriate SW provisions. All users are strongly advised to validate the functionality of the CPDU I/F operation for their choice of operation modes.



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