GEC PLESSEY
SEMICONDUCTORS

APRIL 1995
PRELIMINARY INFORMATION
DS3577-3.4

MA2909/11

RADIATION HARD MICROPROGRAM SEQUENCER

The MA2909/11 Microprogram Sequencer is fully compatible with the industry standard 2909A and 2911A components, and forms part of the GPS 2900 Series of devices. The series offers a building block approach to microcomputer and controller design, with each device in the range being expandable to permit efficient emulation of any microcode machine.

The devices have tristate outputs and have an internal address register, with all internal registers changing state on LOW to HIGH clock transition.

The 4-bit slice can cascade to any number of microwords. Branch input for N-way branches is supported. Additional features include:

- 4-bit cascadable microprogram counter.
- 4 x 4 file with stack counter supporting nesting microsubroutines.
- Zero input for returning to the zero microcode word.
- Individual OR input for each bit for branching to higher microinstructions (2909 only).

The 2909 is a 4-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two 2909s may be interconnected to generate an 8-bit address (256 words), and three may be used to generate a 12-bit address (4K words).

The 2909 can select an address from any of four sources:

1) A set of external direct inputs (D);

2) External data from the R inputs, stored in an internal register;

3) A four-word push/pop stack; or

4) A program counter register (which usually contains the last address plus one).

The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.

The 2911 is an identical circuit to the 2909 except the four OR inputs are removed and the D and R inputs are tied together.

FEATURES

- Fully Compatible with Industry Standard 2909A and 2911A Components
- Radiation Hard CMOS SOS Technology
- High SEU Immunity
- High Speed / Low Power
- Fully TTL Compatible

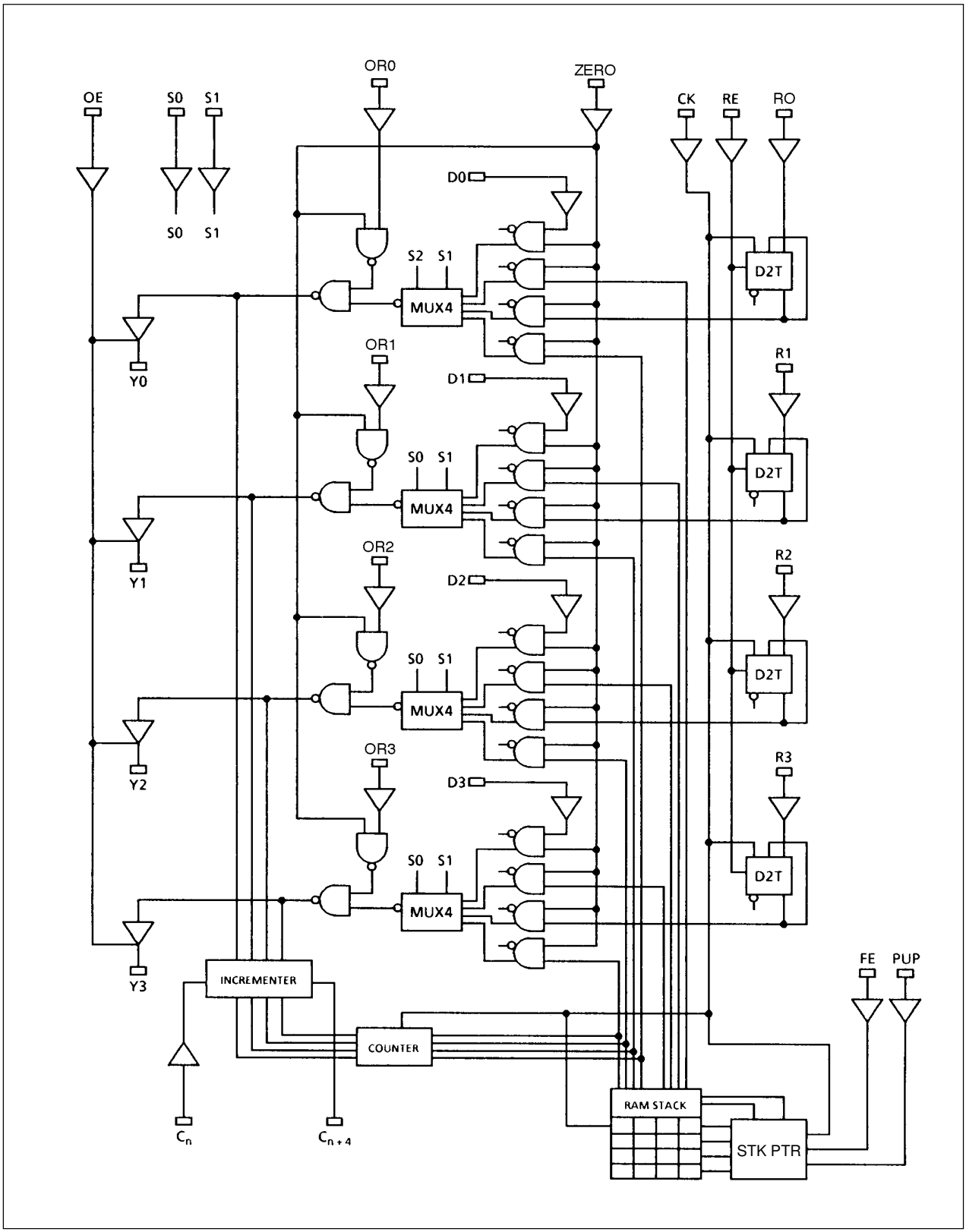


Figure 1: Microprogram Sequencer Block Diagram

The 2909/2911 are CMOS SOS microprogram sequencers intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256 words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in figure 1.

The device contains a four input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S0 and S1 inputs.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The address register is available at the multiplexer as a source for the next microinstruction address The direct input is a 4-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the 2911 the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The 2909/2911 contains a microprogram counter (µPC) that is composed of a 4-bit incrementer followed by a 4bit register. The incrementer has carry-in (C_n) and carry-out (C_n + 4) such that cascading to larger word lengths is straight forward. The µPC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y + 1 ➔ µPC). Thus sequential microinstructions can be executed. If this least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprgram register is loaded with the same Y word on the next clock cycle (Y ➔ µPC). Thus, the same microinstruction can be executed any number of times by using the 4x4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the PUSH operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage - the next microinstruction address following the subroutine jump which initiated the PUSH.

If the file enable input is LOW and the push/pop control is LOW, a POP operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer regardless of any other input.

The stack pointer linkage is such that any combination of push, pop or stack references can be achieved. One microinstruction subroutine can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the four outputs to the binary zero state. When the ZERO input is LOW all Y outputs are LOW regardless of any other inputs (except OE). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

The 2909/2911 feature three-state Y outputs. These can be particularly useful in designs requiring external equipment to provide automatic checkout of the microprocessor. The internal control can be placed in the high impedance state and preprogrammed.

MULTIPLEXER SELECT CODES

Table 1 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Table 1 also shows the truth table for the output control and for the control of the push/pop stack. Table 2 shows in detail the effect of S_0, S_1, FE and PUP on the 2909. These four signals define the address that apears on the Y outputs and what the state of all the internal registers will be following the clock LOW-to-HIGH edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain R_a through R_d.

OR1	ZERO	OE	Y1
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0S_1

H = High, L = Low, Z = High Impedance

Table 1a: Output Control

FE	ZERO	PUSH-POP stack change
H	X	No change
L	H	Increment stack pointer, then push current PC on to STK0
L	L	Pop stack (decrement stack pointer)

H = High, L = Low, X = Irrelevant

Table 1b: Synchronous Stack Control

S_1	S_2	Source for Y outputs	Symbol
L	L	Microprogram counter	µPC
L	H	Address/Holding register	AR
H	L	Push-Pop stack	STKO
H	H	Direct inputs	D_1

Table 1c: Address Selection

Cycle	S1	S0	FE	PUP	µPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	Comment	Principal Use
N	L	L	L	L	J	K	R_a	R_b	R_c	R_d	J	Pop Stack	End Loop
N + 1		-			J + 1	K	R_b	R_c	R_d	R_a	-		
N	L	L	L	H	J	K	R_a	R_b	R_c	R_d	J	Push µPC	Set-up Loop
N + 1		-			J + 1	K	J	R_a	R_b	R_c	-		
N	L	L	H	X	J	K	R_a	R_b	R_c	R_d	J	Continue	Continue
N + 1		-			J + 1	K	R_a	R_b	R_c	R_d	-		
N	L	H	L	L	J	K	R_a	R_b	R_c	R_d	K	Pop Stack;	End Loop
N + 1		-			K + 1	K	R_b	R_c	R_d	R_a	-	Use AR for Address	
N	L	H	L	H	J	K	R_a	R_b	R_c	R_d	K	Push µPC;	JSR AR
N + 1		-			K + 1	K	J	R_a	R_b	R_c	-	Jump to Address in AR	
N	L	H	H	X	J	K	R_a	R_b	R_c	R_d	K	Jump to Address in AR	JMP AR
N + 1		-			K + 1	K	R_a	R_b	R_c	R_d	-		
N	H	L	L	L	J	K	R_a	R_b	R_c	R_d	R_a	Jump to Address in	RTS
N + 1		-			R_a + 1	K	R_b	R_c	R_d	R_a	-	STK0; Pop Stack	
N	H	L	L	H	J	K	R_a	R_b	R_c	R_d	R_a	Jump to Address in	
N + 1		-			R_a + 1	K	J	R_a	R_b	R_c	-	STK0; Push µPC	
N	H	L	H	X	J	K	R_a	R_b	R_c	R_d	R_a	Jump to Address in	Stack Ref
N + 1		-			R_a + 1	K	R_a	R_b	R_c	R_d	-	STK0	(Loop)
N	H	H	L	L	J	K	R_a	R_b	R_c	R_d	D	Pop Stack;	End Loop
N + 1		-			D + 1	K	R_b	R_c	R_d	R_a	-	Jump to Address on D	
N	H	H	L	H	J	K	R_a	R_b	R_c	R_d	D	Jump to Address on D;	JSR D
N + 1		-			D + 1	K	J	R_a	R_b	R_c	-	Push µPC	
N	H	H	H	X	J	K	R_a	R_b	R_c	R_d	D	Jump to Address on D	JMP D
N + 1		-			D + 1	K	R_a	R_b	R_c	R_d	-		

1 = High, 0 = Low, X = Irrelevant, Assume C_n = High

Note: STK0 is the location addressed by the stack pointer

Table 2: Output and Internal Next-Cycle Register States for 2909/2911

Table 3 (Page 5) illustrates the execution of a subroutine using the 2909. The configuration of Figure 2 is assumed. The instruction being executed at any given time is the one contained in the microword register (µWR). The contents of the µWR also control (indirectly, perhaps) the four signals S0, S1, FE, and PUP. The starting address of the subroutine is applied to the D inputs of the 2909 at the appropriate time.

In the column on the left is the sequence of microinstructions to be executed. At address J+2, the sequence control portion of the microinstruction contains the command “Jump to subroutine at A”.

At the time T_2, this instruction is in the µWR, and the 2909 inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the µWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the µWR. On the next clock transition, I(A) is loaded into the µWR for execution, and the return address J + 3 is pushed on to the stack. The return instruction is executed at T_5. Table 4 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
2909 inputs (from µWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	FE	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	µPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	J + 4	J + 5		
	STK0	-	-	-	J + 3	J + 3	J + 3	-	-		
	STK1	-	-	-	-	-	-	-	-		
	STK2	-	-	-	-	-	-	-	-		
	STK3	-	-	-	-	-	-	-	-		
2909 Output	Y	J + 1	J + 2	A	A + 1	A + 2	J + 3	J + 4	J + 5		
ROM Output	(Y)	I(J + 1)	JSR A	I(A)	I(A + 1)	RTS	I(J + 3)	I(J + 4)	I(J + 5)		
Contents of µWR (instruction being executed)	µWR	I(J)	I(J + 1)	JSR A	I(A)	I(A + 1)	RTS	I(J + 3)	I(J + 4)		

Table 3: Subroutine Execution

CONTROL MEMORY

Execute Cycle	Microprogram	
	Address	**Sequencer Instruction**
	J - 1	-
T_0	J	-
T_1	J + 1	-
T_2	J + 2	JSR A
T_6	J + 3	-
T_7	J + 4	-
	-	-
	-	-
	-	-
	-	-
	-	-
T_3	A	I(A)
T_4	A + 1	-
T_5	A + 2	RTS
	-	-
	-	-
	-	-
	-	-
	-	-
	-	-

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
2909 inputs (from µWR)	S_1, S_0	0	0	3	0	0	2	0	0	2	0
	FE	H	H	L	H	H	L	H	H	L	H
	PUP	X	X	H	X	X	L	X	X	L	X
	D	X	X	A	X	X	X	X	X	X	X
Internal Registers	µPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	B + 1	A + 4	A + 5	J + 4
	STK0	-	-	-	J + 3	J + 3	J + 3	A + 3	J + 3	J + 3	-
	STK1	-	-	-	-	-	-	J + 3	-	-	-
	STK2	-	-	-	-	-	-	-	-	-	-
	STK3	-	-	-	-	-	-	-	-	-	-
2909 Output	Y	J + 1	J + 2	A	A + 1	A + 2	B	A+ 3	A + 4	J + 3	J + 4
ROM Output	(Y)	I(J + 1)	JSR A	I(A)	I(A + 1)	JSR B	RTS	I(A + 3)	RTS	I(J + 3)	I(J + 4)
Contents of µWR (instruction being executed)	µWR	I(J)	I(J + 1)	JSR A	I(A)	I(A + 1)	JRS B	RTS	I(A + 3)	RTS	I(J + 3)

Table 4: Two Nested Subroutines

CONTROL MEMORY

Execute Cycle	Microprogram	
	Address	**Sequencer Instruction**
	J - 1	-
T_0	J	-
T_1	J + 1	-
T_2	J + 2	JSR A
T_9	J + 3	-
	-	-
	-	-
	-	-
	-	-
T_3	A	-
T_4	A + 1	-
T_5	A + 2	JSR B
T_7	A + 3	-
T_8	A + 4	RTS
	-	-
	-	-
	-	-
	-	-
T_6	B	RTS
	-	-

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-	20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Table 5: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Subgroup	Definition
1	Static characteristics specified in Table 7 at +25°C
2	Static characteristics specified in Table 7 at +125°C
3	Static characteristics specified in Table 7 at -55°C
7	Functional characteristics at +25°C
8a	Functional characteristics at +125°C
8b	Functional characteristics at -55°C
9	Switching characteristics specified in Tables 8, 9 and 10 at +25°C
10	Switching characteristics specified in Tables 8, 9 and 10 at +125°C
11	Switching characteristics specified in Tables 8, 9 and 10 at -55°C

Table 6: Definition of Subgroups

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{OH}	Output high voltage	V_{DD} = Min., I_{OH} = -2.6mA, V_{IN} = V_{IH} or V_{IL}	V_{DD} -0.5	-	V
V_{OL}	Output low voltage	V_{DD} = Max., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}	-	0.5	V
V_{IH}	Input high level (Note 1)	Guaranteed input logical high voltage for all inputs	V_{DD}/2	-	V
V_{IL}	Input low level (Note 1)	Guaranteed input logical low voltage for all inputs	-	0.8	V
I_{IH}	Input high current	V_{IN} = V_{DD} (Note 3)	-	10	µA
I_{IL}	Input low current	V_{IN} = V_{SS} (Note 3)	-	-10	µA
I_{OZH}	Tristate high current	V_O = V_{DD} (Note 3)	-	50	µA
I_{OZL}	Tristate low current	V_O = V_{SS} (Note 3)	-	-50	µA
I_{DD}	Power supply current		-	10	mA

NOTES:
Mil-Std-883, Method 5005, Subgroups 1, 2, 3.
1. These input levels provide no guaranteed noise immunity and should only be static tested in a noise-free environment.
2. V_{DD} = 5V ±10%, over full operating temperature range.
3. Guaranteed but not tested at low temperatures.

Table 7: DC Operating Characteristics

Time	
Minimum clock low time	15
Minimum clock high time	15

Table 8: Cycle Time and Clock Charcteristics

From input	Y	$C_n + 4$
D_1	35	40
S_0, S_1	30	35
OR_I	20	30
C_n	-	25
ZERO	35	40
OE LOW (enable) (Note 2)	25	-
OE HIGH (disable) (Note 3)	25	-
Clock: S_1S_0 = LH	40	45
Clock: S_1S_0 = LL	40	45
Clock: S_1S_0 = HL	50	45

Notes:
1. CL < 50pF
2. RL ≥ 680Ω
3. RL ≥ 680Ω, measured 0.5V change in output level

Table 9: Maximum Combinational Propogation Delays

From input	Set-up time	Hold Time
RE	10	10
R_I	10	7
PUP	20	5
FE	20	10
C_n	15	5
D_I	20	0
OR_I	20	0
S_0, S_1	20	0
ZERO	25	0

Table 10: Guaranteed Set-up and Hold Times (all in ns)

All times in ns across full voltage and temperature range.
MIL-STD-883, method 5005, subgroups 9, 10 and 11.

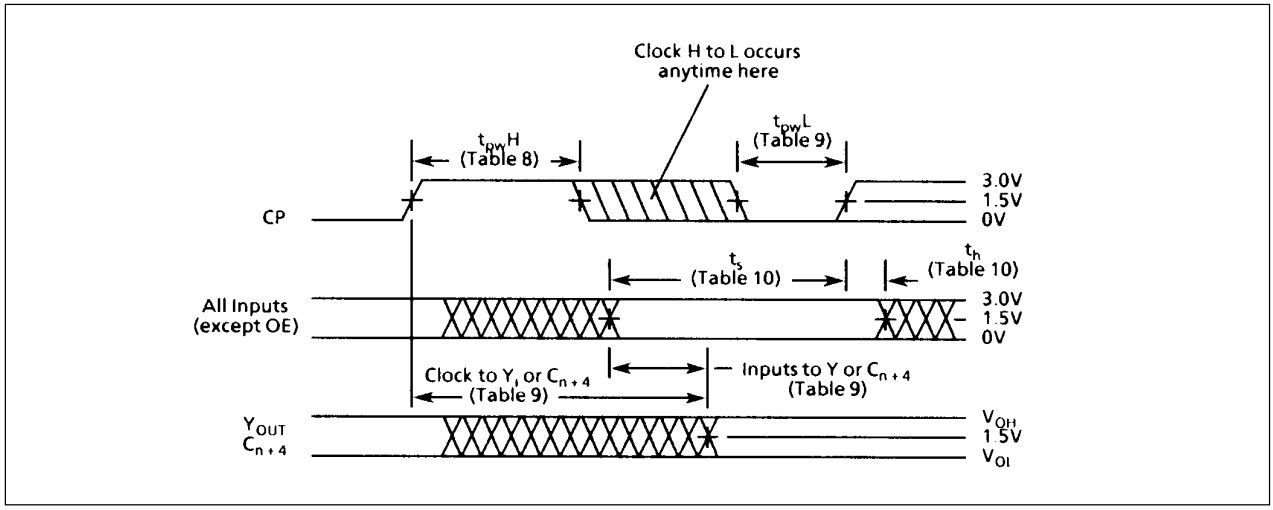


Figure 2

PACKAGE OUTLINES

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	36.02	-	-	1.418
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG404

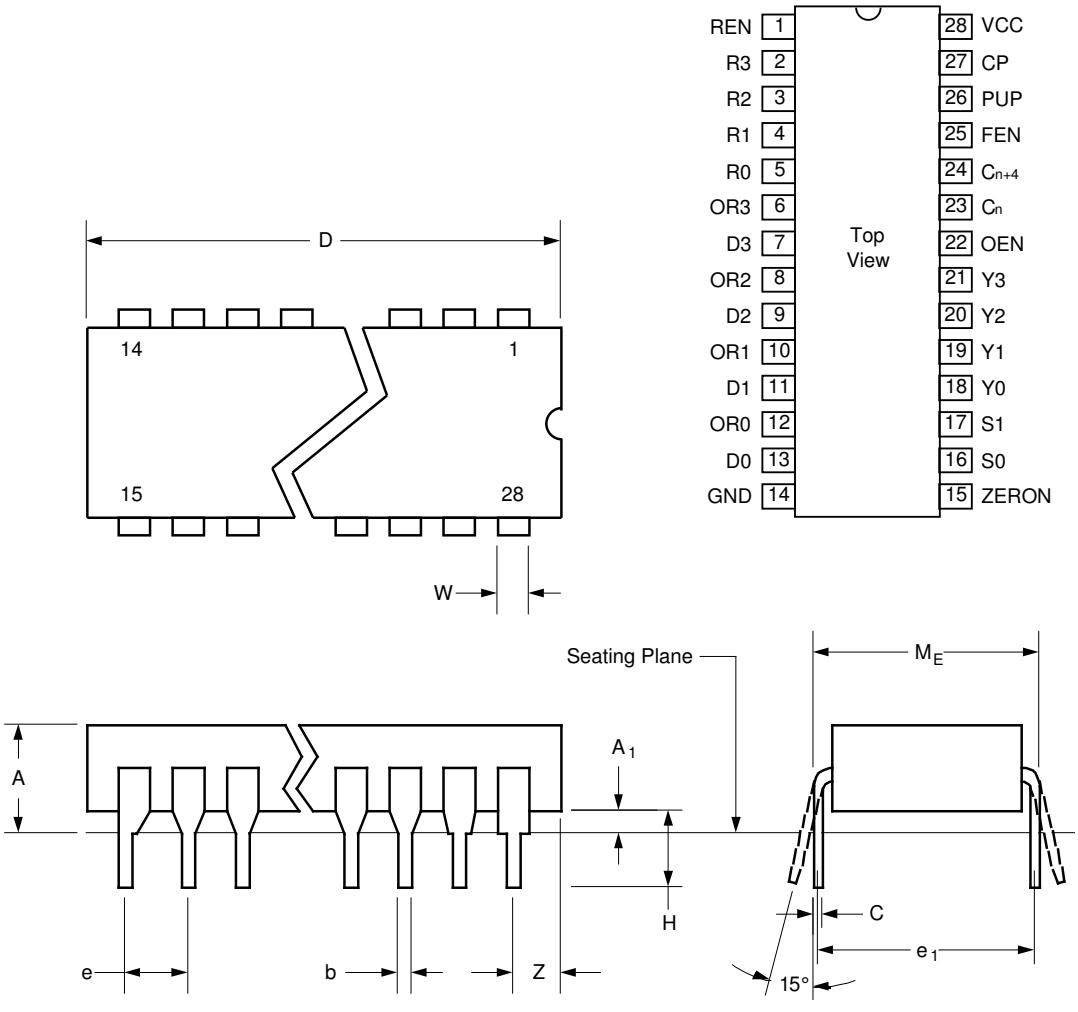


Figure 3: 28-Lead Ceramic DIL (Solder Seal) - Package Style C

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.97	-	-	0.117
b	0.381	-	0.482	0.015	-	0.019
c	0.076	-	0.152	0.003	-	0.006
D	18.08	-	18.49	0.712	-	0.728
E	12.50	-	12.9	0.492	-	0.508
E2	9.45	-	9.85	0.372	-	0.388
e	1.143	-	1.40	0.045	-	0.055
L	8.00	-	9.27	0.315	-	0.365
Q	0.66	-	-	0.026	-	-
S	-	-	1.14	-	-	0.045

XG543

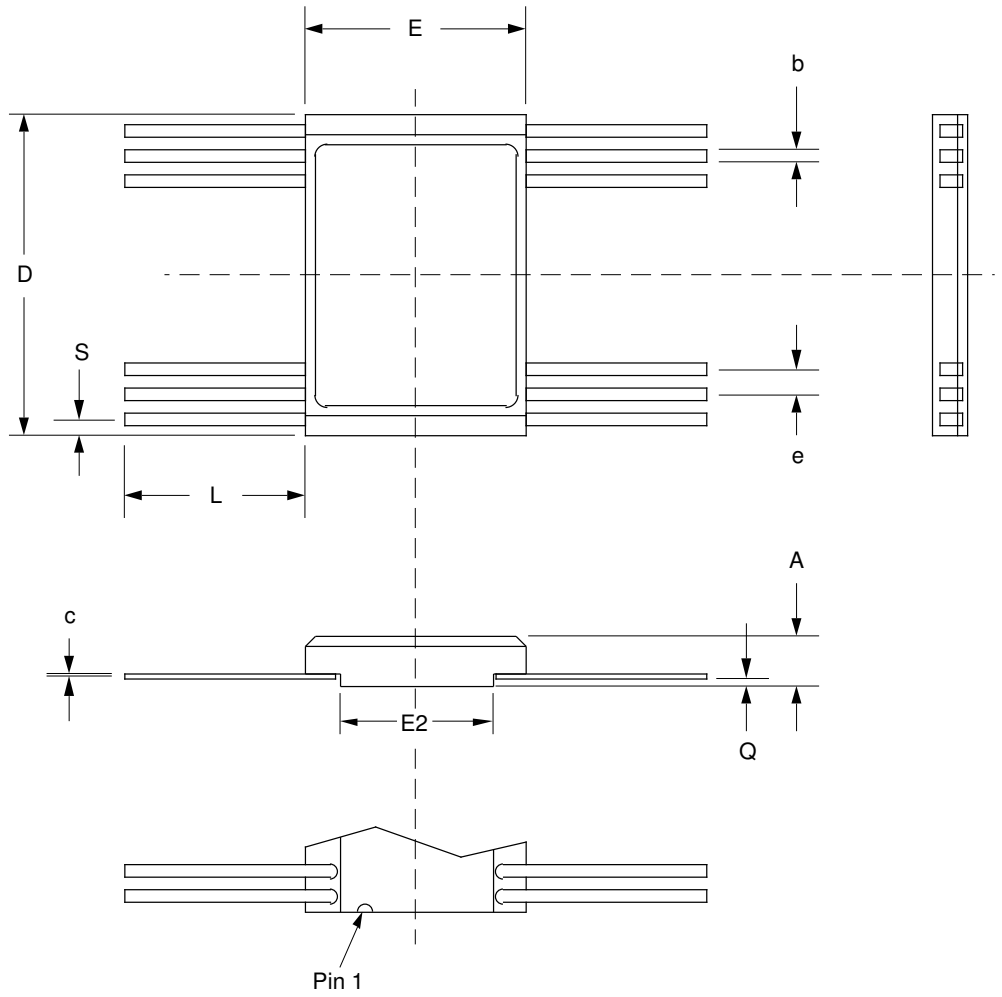


Figure 3: 28-Lead Dual Flatpack (Solder Seal) - Package Style C

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

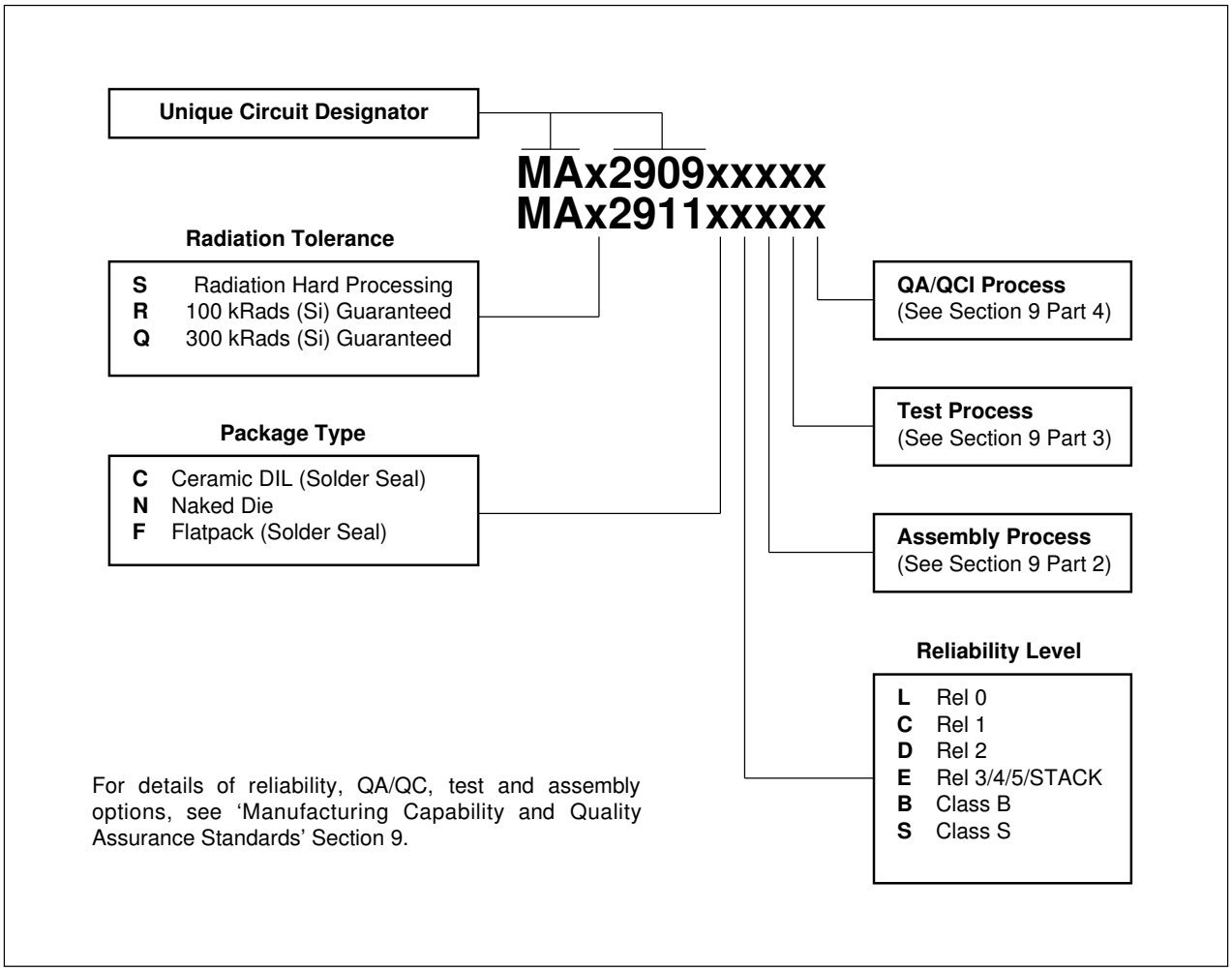
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 11: Radiation Hardness Parameters

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

GEC PLESSEY
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 Publication No. DS3577-3.3 March 1995

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