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GEC PLESSEY
SEMICONDUCTORS

AUGUST 1993
ADVANCE DATA
DS3832-2.1

MA3864

RADIATION HARD 8192 x 8 BIT MASK-PROGRAMMABLE ROM

The MA3864 64k Mask Programmable ROM is configured as 8192x8 bits and manufactured using CMOS-SOS high performance, radiation hard, 1.5µm technology.

The design has full static operation with no clock or timing strobe required. Address input buffers are deselected when chip select is in the HIGH state.

Programming is performed during fabrication by customising the penultimate layer of the process. Programming data may be supplied in EPROM or as a data file in the standard INTEL Hex format.

Operation Mode	*E	G	I/O	Power
Read Output Disable	L L	L H	D OUT High Z	
Standby	H X	X X	High Z X	ISB 2

*E is a mask programmed NAND function of E1,E2,E3,E4 and their inverses.

Figure 1: Truth Table

FEATURES

- 1.5µm CMOS-SOS Technology
- Latch-up Free
- Fast Access Time 60ns Typical
- Total Dose 10^6 Rad(Si)
- Transient Upset >10^{11} Rad(Si)/sec
- SEU 4.3 x 10^{-11} Errors/bitday
- Single 5V Supply
- Three State Output
- Low Standby Current 100µA Typical
- -55°C to +125°C Operation
- All Inputs and Outputs Fully TTL or CMOS Compatible
- Fully Static Operation
- Programmable at Via Level for Fast Turnaround
- 4 Mask Programmable Chip Selects

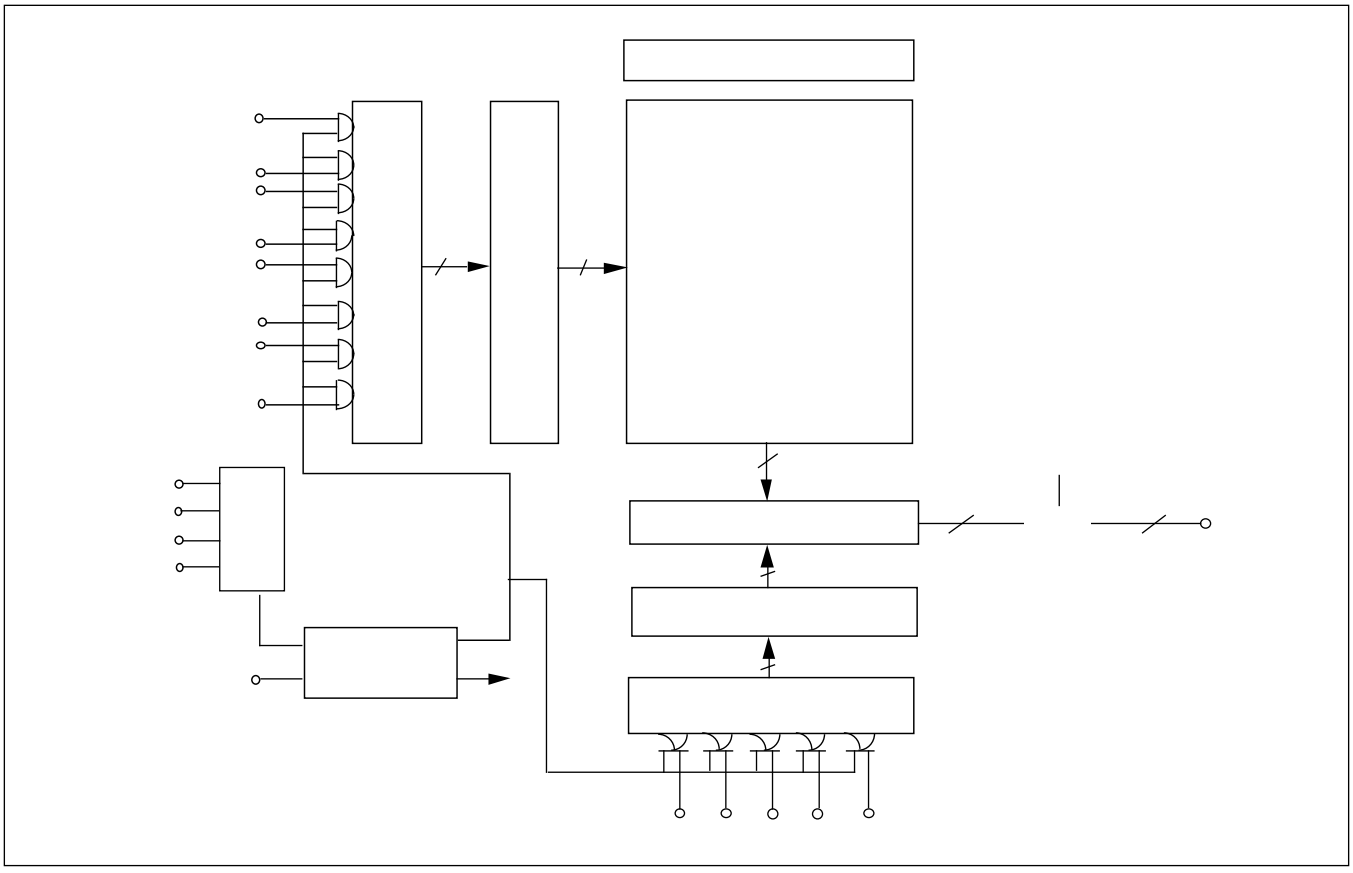


Figure 2: Block Diagram

SIGNAL DEFINITIONS

A0-12
Address input pins which select a particular eight bit word within the memory array.

Q0-7
Data output pins

E1, E2, E3, E4
Are mask programmed, to the customer's specification, to form the active LOW chip select function (E). E is driven by a 4-input NAND gate which has E1,E2,E3,E4 or their inverses as it's inputs. Unused NAND gate I/Ps will be tied high internally. When chip select (E) is low, a read is activated. When it is at a high level it defaults the ROM to a precharge condition and holds the data output drivers in a high impedance state.

G
Output Enable which when at a high level holds the data output drivers in a high impedance state. When at a low level, data output driver state is defined by CS. If this signal is not used it must be connected to VSS.

CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.5	7.0	V
V_I	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functlonal operation of the device at these condltions, or at any other condition above those indicated in the operations section of this specification, is not implied Exposure to absolute maxlmum rating conditions for extended periods may affect device reliability.

Figure 3: Absolute Maximum Ratings

Notes for Table 4:
Characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10% (characteristics at higher radiation levels available on request). GROUP A SUBGROUPS 1, 2, 3.

Symbol	Parameter	Conditions (Option)	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Logical '1' Input Voltage	- (TTL) (CMOS)	2.0 0.8 V_{DD}	- -	V_{DD} V_{DD}	V V
V_{IL}	Logical '0' Input Voltage	- (TTL) (CMOS)	V_{SS} V_{SS}	- -	0.8 0.2 V_{DD}	V V
V_{OH1}	Logical '1' Output Voltage	I_{OH1} = -4mA	2.4	-	-	V
V_{OH2}	Logical '1' Output Voltage	I_{OH2} = -3mA	V_{DD} -0.5	-	-	V
V_{OL}	Logical '0' Output Voltage	I_{OL} = 8mA	-	-	0.4	V
I_{LI}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} all inputs	-	-	±10	µA
I_{LO}	Output Leakage Current	Chip disabled, V_{OUT} = V_{DD} or V_{SS}	-	-	±10	µA
I_{SB1}	Selected Static Current (CMOS)	All inputs = V_{DD} -0.2V except CS = V_{SS} +0.2V	-	0.1	2	mA
I_{DD}	Dynamic Operating Current (CMOS)	f_{RC} = 1MHz, all inputs switching, V_{IH} = V_{DD} -0.2V	-	3	10	mA
I_{SB2}	Standby Supply Current	CS = V_{DD} -0.2V	-	0.1	2	mA

Figure 4: Electrical Characteristics

AC CHARACTERISTICS

Conditions of Test for Table 5:
1. Input pulse = V_{SS} to 4.5V.
2. Times measurement reference level = 1.5V.
3. Input Rise and Fall times ≤5ns.
4. Output load 1TTL gate and CL = 60pF.
5. Transition is measured at ±500mV from steady state (T_{ELQX}, T_{EHQZ}, T_{GHQZ}).
6. These parameters are sampled and not 100% tested (T_{ELQX}, T_{EHQZ}, T_{GHQZ}).

Characteristics apply to pre-radiation at T_A = -55°C to +125°C with V_{DD} = 5V±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10%. GROUP A SUBGROUPS 9, 10, 11.

Symbol	Parameter	Min	Max	Units
T_{AVAX}	Read Cycle Time	60	-	ns
T_{AVQV}	Address Access Time	-	60	ns
$*T_{ELQV}$	Chip Select Access Time	-	60	ns
T_{GLQV}	Output Enable to Output Valid	-	15	ns
T_{AXQX}	Output Hold Time for Address Access	15	-	ns
$*T_{ELQX}$	Chip Select Low to Outputs Active	-	30	ns
$*T_{EHQZ}$	Chip Select High to Outputs Hi-Z	-	30	ns
T_{GHQZ}	Output Enable High to Output Hi-Z	-	10	ns
T_{ELEH}	Chip Select Pulse Width	60	-	ns

*These functions refer to the action of the internal chip select, E. The timings given are relative to the last of the pins; E1, E2, E3 and E4 to change which causes the specified transitions of E.

Figure 5: Read Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Figure 6: Capacitance

Symbol	Parameter	Conditions
F_T	Basic Functionality	V_{DD} = 4.5V - 5.5V, FREQ = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55°C to +125°C, GPS PATTERN SET GROUP A SUBGROUPS 7, 8A, 8B

Figure 7: Functionality

Subgroup	Definition
1	Static characteristics specified in Table 4 at +25°C
2	Static characteristics specified in Table 4 at +125°C
3	Static characteristics specified in Table 4 at -55°C
7	Functional characteristics specified in Table 7 at +25°C
8A	Functional characteristics specified in Table 7 at +125°C
8B	Functional characteristics specified in Table 7 at -55°C
9	Switching characteristics specified in Table 5 at +25°C
10	Switching characteristics specified in Table 5 at +125°C
11	Switching characteristics specified in Table 5 at -55°C

Figure 8: Definition of Subgroups

TIMING DIAGRAMS

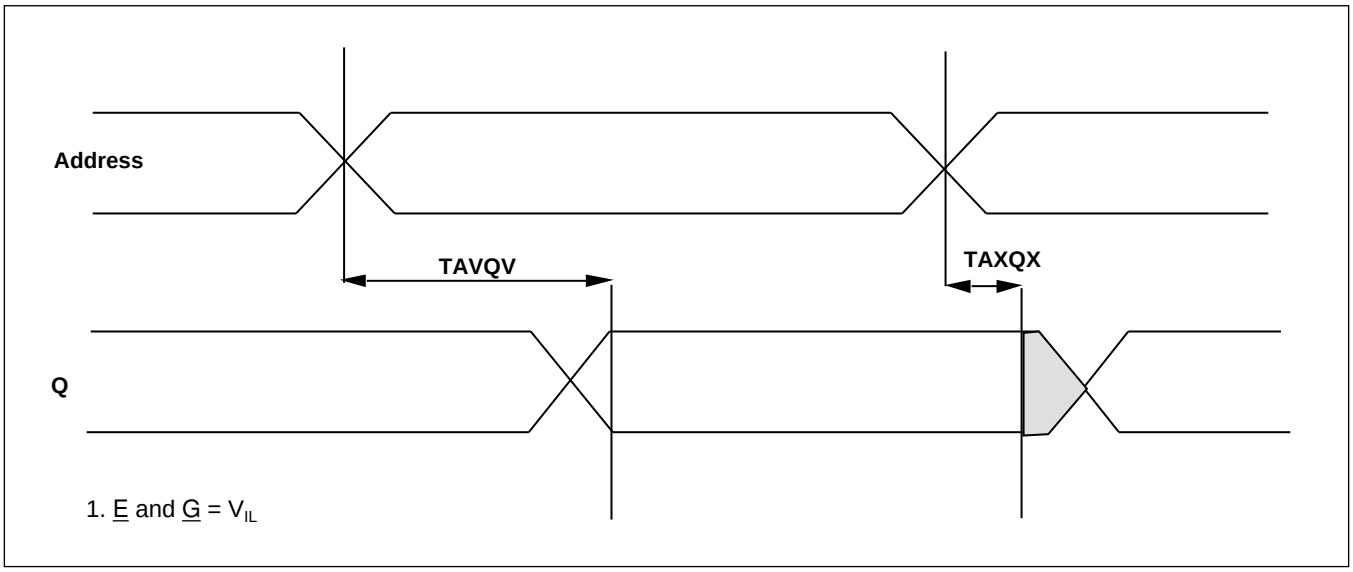


Figure 9: Address Controlled Read Cycle

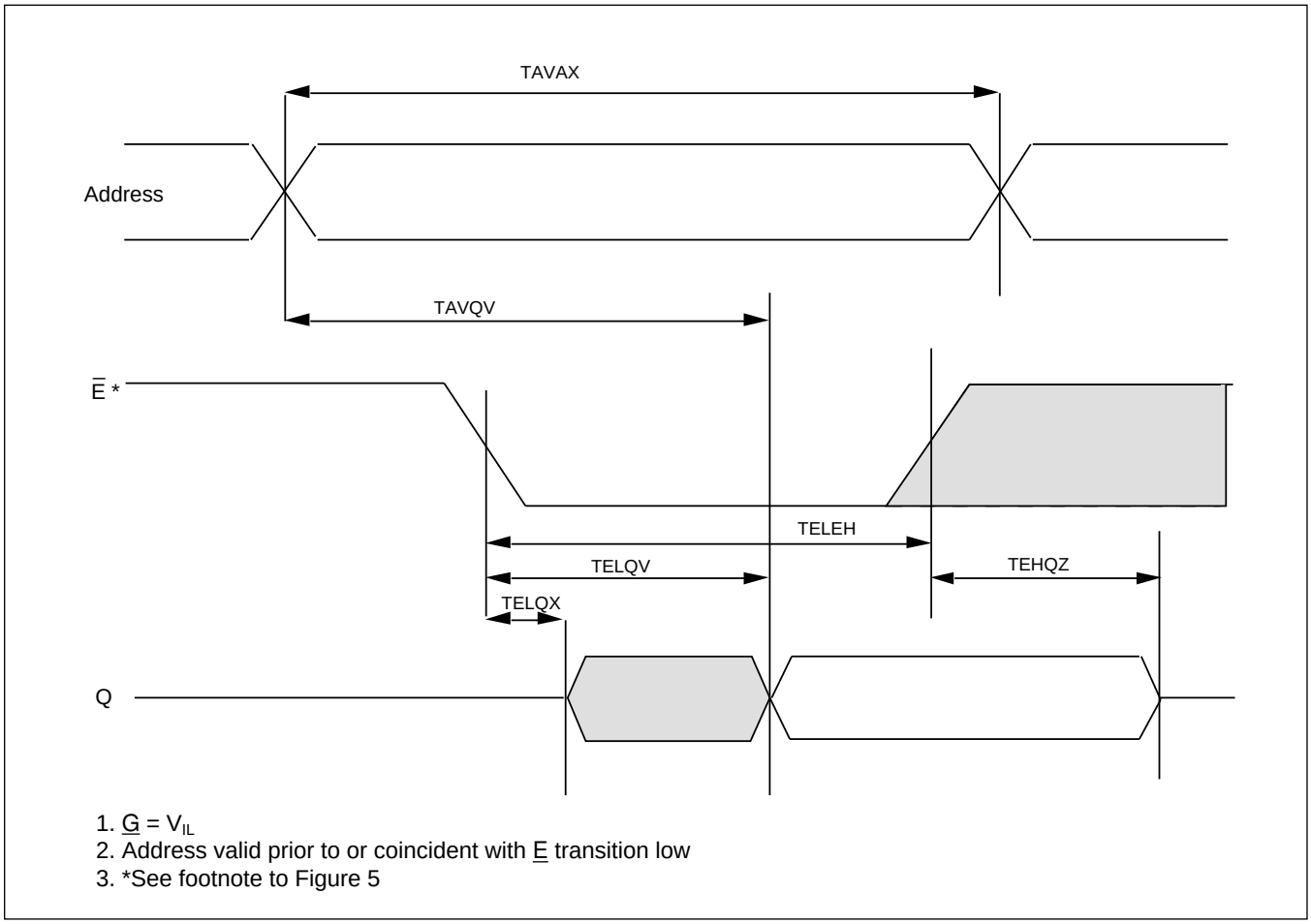


Figure 10: Chip Select Controlled Read Cycle

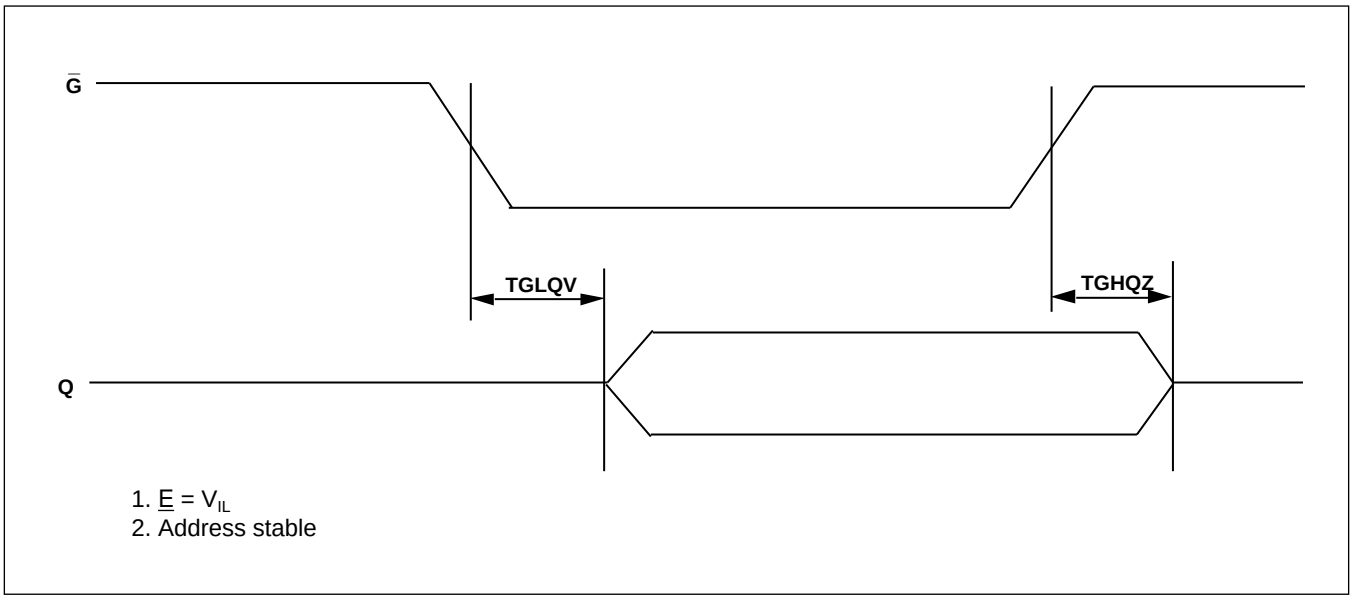
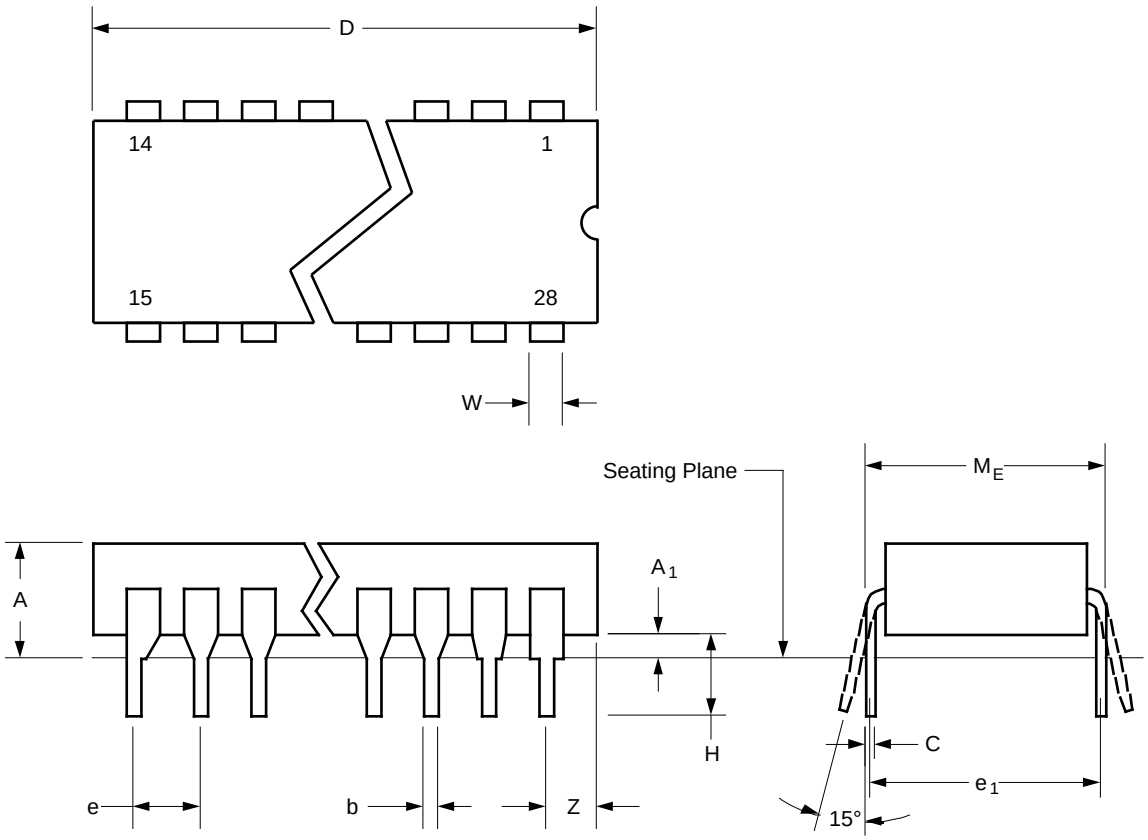


Figure 11: Output Enable Operation

OUTLINES AND PIN ASSIGNMENTS



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	36.02	-	-	1.418
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG404

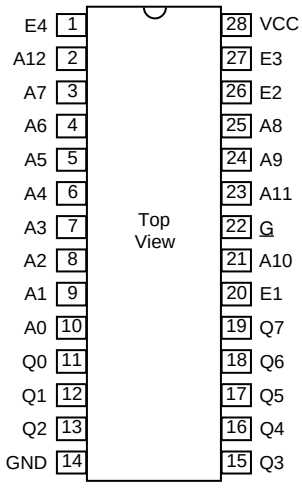
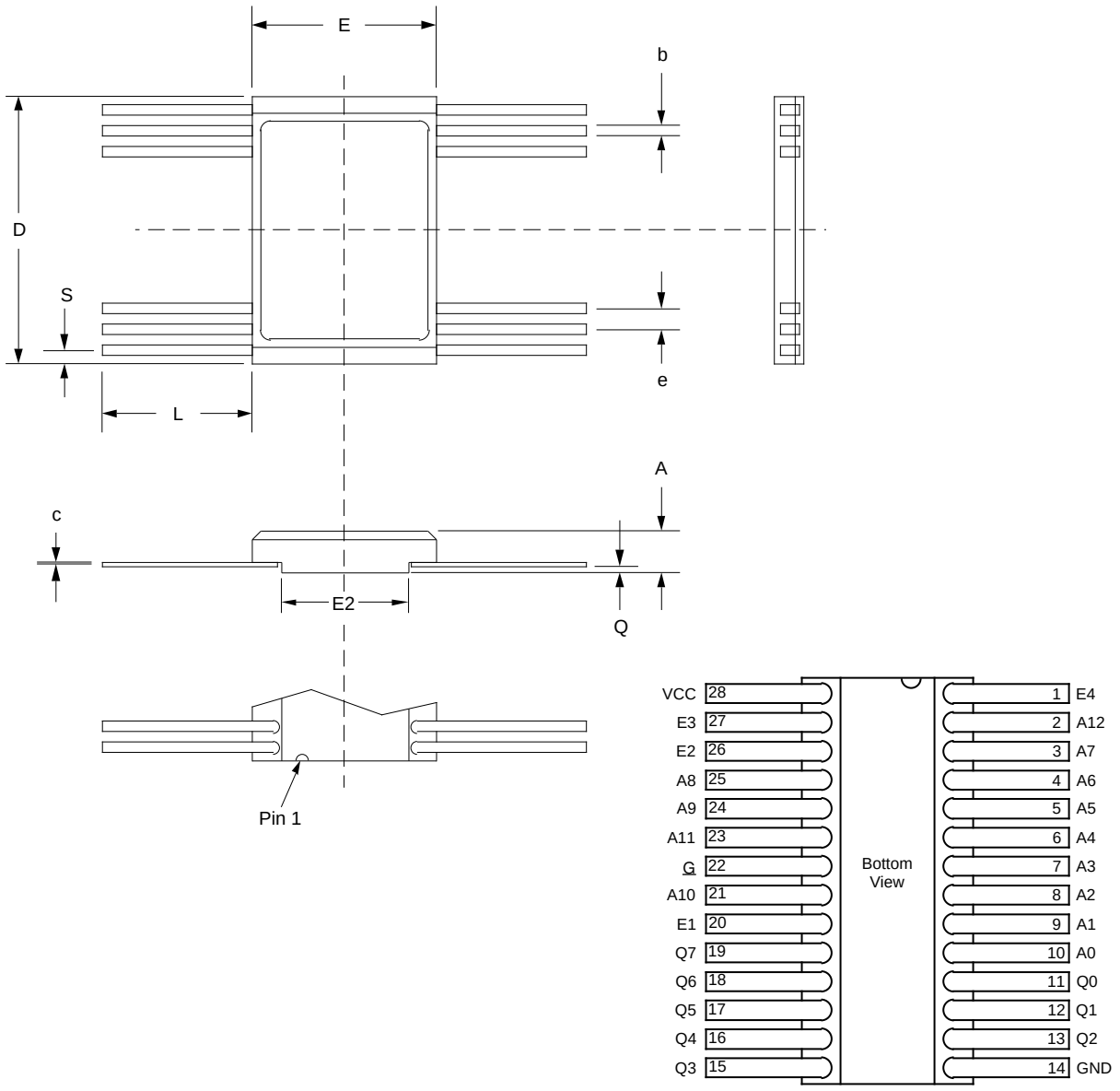


Figure 12: 28-Lead Ceramic DIL (Solder Seal) - Package Style C



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.97	-	-	0.117
b	0.381	-	0.482	0.015	-	0.019
c	0.076	-	0.152	0.003	-	0.006
D	18.08	-	18.49	0.712	-	0.728
E	12.50	-	12.9	0.492	-	0.508
E2	9.45	-	9.85	0.372	-	0.388
e	1.143	-	1.40	0.045	-	0.055
L	8.00	-	9.27	0.315	-	0.365
Q	0.66	-	-	0.026	-	-
S	-	-	1.14	-	-	0.045

XG543

Figure 13: 28-Lead Ceramic Flatpack (Solder Seal) - Package Style F

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

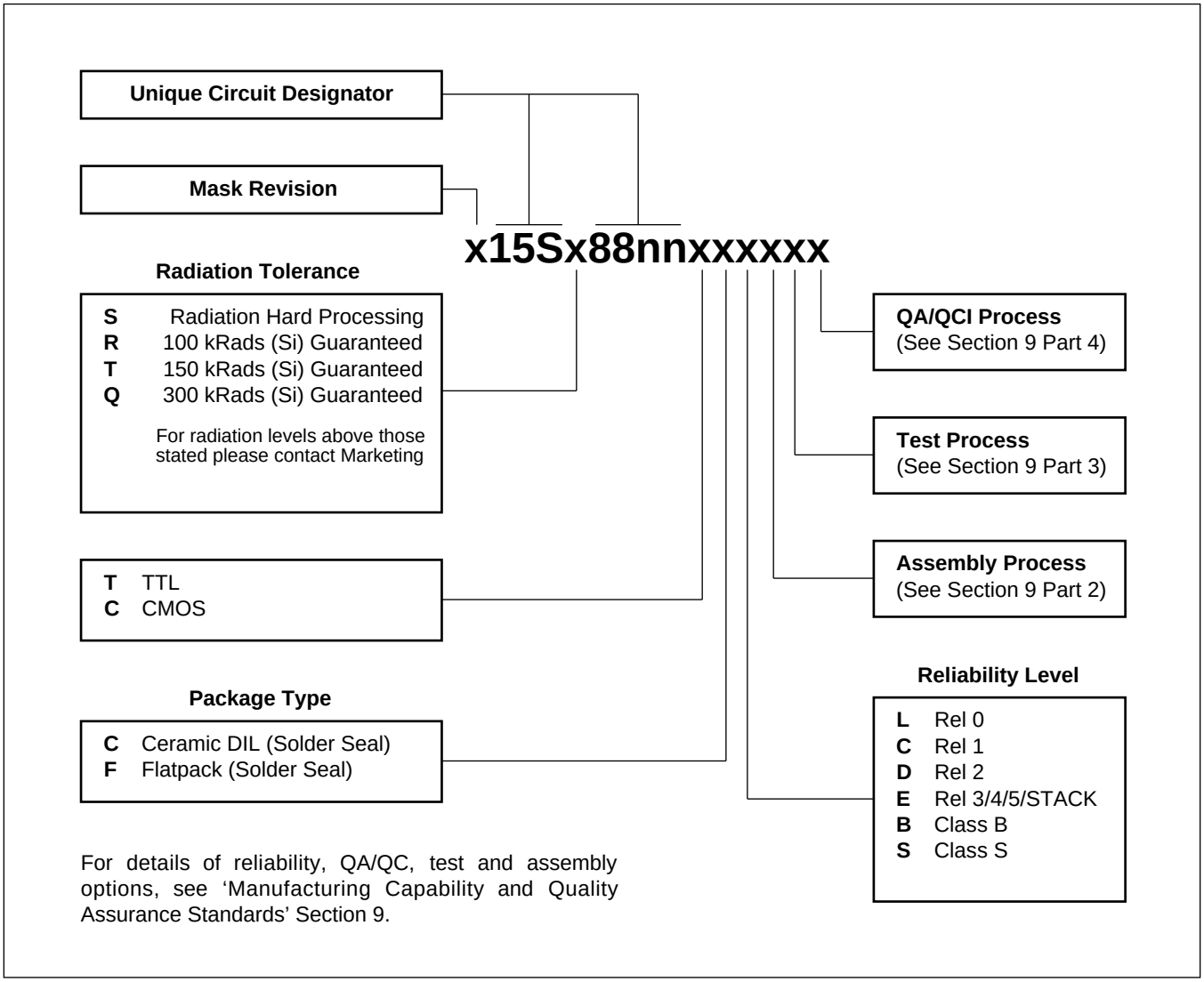
The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Basic function)	$1x10^5$ Rad(Si)
Total Dose (Function to specification)	$1x10^6$ Rad(Si)
Transient Upset	$>10^{11}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$4.3x10^{-11}$ errors/bitday
Latch-up	Not possible

Figure 14: Typical Radiation Hardness Parameters

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

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 Publication No. DS3832-2.1 August 1993