40V Synchronous Buck Controller with 2ch CC/CV

❖ GENERAL DESCRIPTION

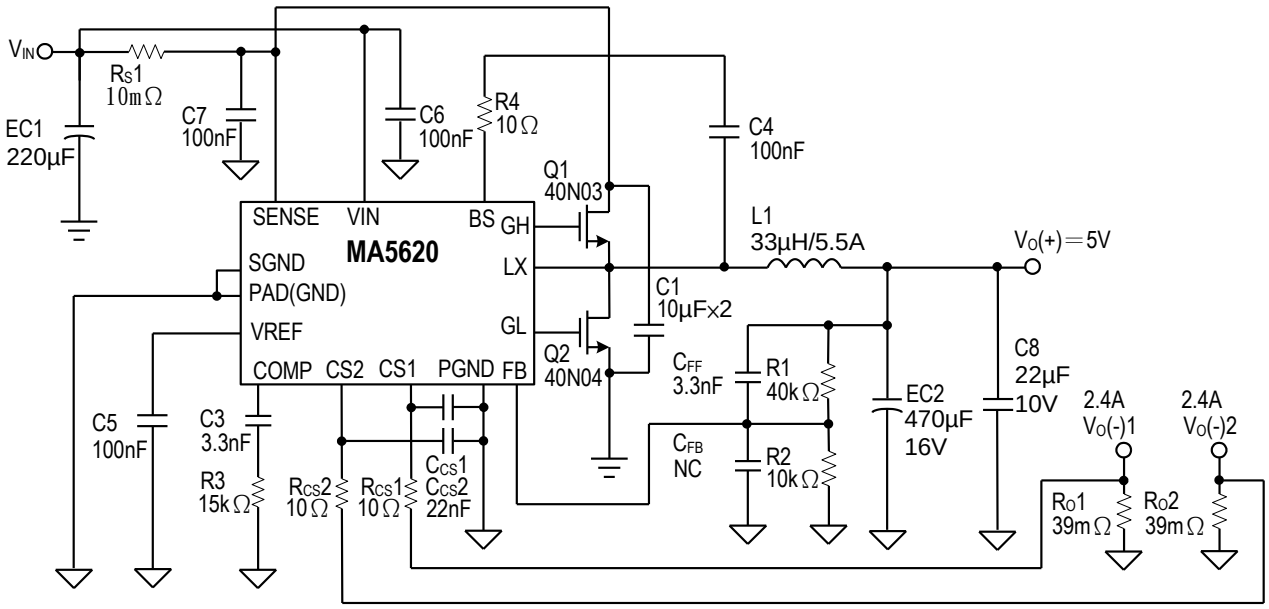
The MA5620 is a synchronous buck controller. The device need externals high-side and external low-side power MOSFETs, and provides higher than 5A continuous load current and a wide input voltage from 8V to 40V. Current mode control provides fast transient response and cycle-by-cycle current limit.

An internal soft-start prevents inrush current at turn-on, this device available in small TDFN-12L (3x3) package, provides a very compact solution with minimal external components.

❖ FEATURES

- Wide 8V～40V Operating Input Range.
- Externals high-side / low-side Power MOSFET Switches.
- Output Adjustable : V_{FB} (1.00V±2%).
- Up to 97% Efficiency.
- Internal Soft-Start and Fixed 160KHz Frequency.
- Duty on ratio : 0% to 91% PWM control.
- Cycle-by-Cycle Current Limit（or called Over Current Protection, OCP）
- Thermal Shutdown Protection（or called Over Temperature Protection, OTP）
- Input Under／Over Voltage Lockout.（UVLO／OVLO）
- FB Over Voltage Protection.（OVP）

❖ APPLICATION CIRCUIT

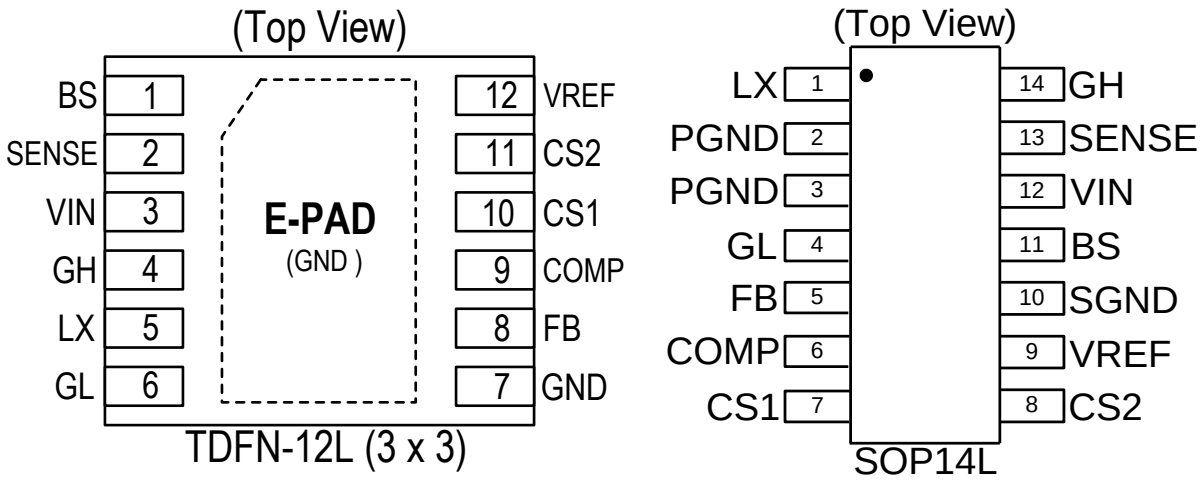


$V_{OUT} = V_{FB} \times (1 + R1 / R2)$, V_{FB} = 1.0V, R2 suggest 1K～30KΩ.

$I_{CS} = V_{CS} / R_O = 0.105V / 39m\Omega = 2.6923A$

❖ PIN ASSIGNMENT

The packages of MA5620 are TDFN-12L (3x3) and SOP14L; the pin assignment is given by:



Name	Description
BS	Boot-Strap pin. It supplies high-side gate driver. Decouple this pin to LX pin with 0.1uf ceramic CAP (e.g. X5R) and a low resistance Resistor (4.7～24Ω .)
SENSE	Power Input and Current Limit SENSE pin. Bypass SENSE (of High-side $_N$MOS) to Ground (of Low-side $_N$MOS) with high capacitance ceramic MLCC (e.g. X5R) to eliminate noise, and bypass MA5620 SENSE-pin to pin7-GND (TDFN-12L) or pin2-PGND (SOP14L) with a 0.1uf～1uf ceramic MLCC. (e.g. X5R.). Ensure a very large SENSE area for High-side $_N$MOS cooling.
VIN	Power Input pin. Bypass VIN to Ground (of low-side Power MOSFET) with a suitably high capacitance E-CAP to eliminate noise, and bypass MA5620 pin3-VIN to pin7-GND (TDFN-12L) or pin12-VIN to pin2-PGND (SOP14L) with a 0.1uf ceramic MLCC (e.g. X5R.) Connect a high power package (1206 at least), precision resistor (±1% at least) from this pin to SENSE-pin, and a large VIN area for resistor cooling is necessary
GH	Gate driver for external high-side $_N$MOS.
LX	Switching node and Switching sense pin.
GL	Gate driver for external Low-side $_N$MOS.
SGND GND	Signal Ground, Output CAP Ground, FB Ground and COMP Ground.
FB	Negative feedback Input pin. FB senses the output voltage to regulate voltage. Drive FB with a resistive voltage divider from the output voltage, and connect a C_{FF} (X5R, 3.3nf to 22nf) as a feed-forward CAP from FB to output. If output voltage is higher than 12V or multiple output voltage steps (like USB PD or QC2.0/3.0/4.0), a C_{FB} (X5R, 1nf to 10nf) as a feed-backward CAP from FB to GND is necessary.
COMP	Negative feedback compensation Node. Connect a series RC network from COMP-pin to pin7-GND (TDFN-12L) or to pin10-SGND (SOP14L.)
CS1	The Current Sense 1st channel pin.
CS2	The Current Sense 2nd channel pin.
VREF	Internal Reference Regulator pin. Connect an MLCC 0.1uf～1uf to GND.
PGND	Pre-driver Ground, not Power Ground. (Only in SOP14L package)
E-PAD	Exposed pad. Connect to GND. (Only in TDFN-12L package)