MA600

High-Accuracy, <0.6° (<0.1°) INL, High-Bandwidth, Configurable Digital Magnetic Angle Sensor

DESCRIPTION

The MA600 is a precision, high-bandwidth magnetic angle sensor that detects the absolute angular position of a permanent magnet, typically a diametrically magnetized cylinder on a rotating shaft. Integrated with a precision tunnel magnetoresistance (TMR) sensor, the MA600 achieves high-bandwidth and high accuracy (INL), making it an ideal solution for position control and robotics.

The MA600 supports a wide range of magnetic field strengths and spatial configurations. End-of-shaft (on-axis) and side-shaft (off-axis) mounting configurations are supported.

On-chip non-volatile memory (NVM) provides storage for configuration parameters, including the reference zero-angle position, ABZ/UVW/PWM settings.

The MA600 is factory-calibrated to achieve an error (INL) below 0.6° across its operating temperature range. Furthermore, a final system calibration is available through a 32-point user configurable correction table. The resulting error (INL) after user calibration can be smaller than 0.1°.

Communication with the MA600 can be done via the serial peripheral interface (SPI) and synchronous serial interface (SSI).

The MA600 is available in a small QFN-16 (3mmx3mm) package.

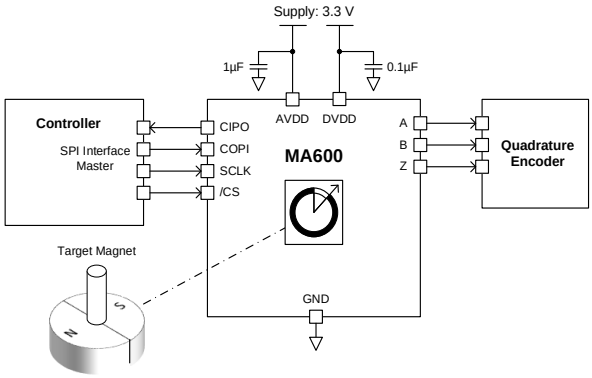
FEATURES

- <0.6° Error (INL)
- <0.1° Error (INL) After User Calibration with On-Chip 32-Point Lookup Table
- Configurable 12-Bit to 15-Bit Absolute Angle Encoder
- High Bandwidth (e.g. 12kHz at 12.5-Bit Resolution)
- No Latency
- Wide 10mT to >100mT Magnetic Field Range
- Serial Peripheral Interface (SPI) for Digital Angle Readout and Chip Configuration
- Synchronous Serial Interface (SSI) for Digital Angle Readout
- Incremental ABZ Quadrature Encoder Interface with Configurable Pulses per Turn (1 to 4096)
- Incremental UVW Encoder Output
- Pulse-Width Modulation (PWM) Absolute Output
- Multi-Turn or Speed Output Option
- 3.3V Supply
- 7.5mA Quiescent Current (I_{AVDD} + I_{DVDD})
- -40°C to +125°C Operating Temperature
- Available in a Small QFN-16 (3mmx3mm) Package

APPLICATIONS

- Robotics
- Multi-Turn Encoders
- Position Control
- Speed Control

TYPICAL APPLICATION



Digital Filter Window FW[3:0]	Noise-Free Resolution (bits)	Latency Cancellation at Constant Speed	Bandwidth (kHz)
0	12.3	No	17
5 (default)	12.5	Yes	12
6	13	Yes	5.8
7	13.5	Yes	2.7
8	14	Yes	1.3
9	14.3	Yes	0.63
10	14.6	Yes	0.31
11	14.8	Yes	0.15
12	15	Yes	0.075

Configurable Filter Window to Optimize Resolution vs. Bandwidth (BW)

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MA600GQE-0000	QFN-16 (3mmx3mm)	*See Below*	1
MA600GQE-xxxx**			

* For Tape & Reel, add suffix -Z (e.g.: MA600GQE-xxxx-Z).

** “-xxxx” is the configuration code identifier for the register settings. The first four digits of the suffix (“-xxxx”) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number for the non-default function option. “-0000” is the factory default code.

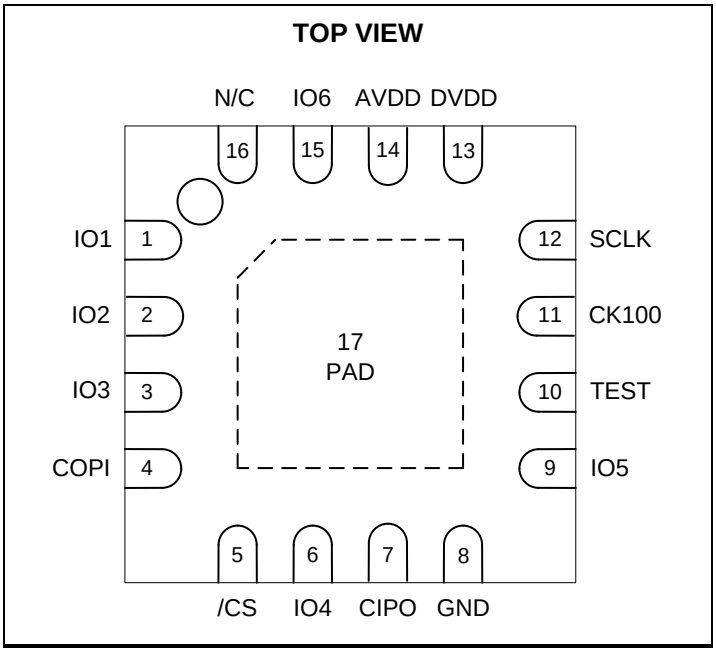
TOP MARKING

CBFY

LLLL

CBF: MPS product code of MA600GQE-xxxx
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-16 (3mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	IO1	**Digital I/O 1.** The IO1 pin is bidirectional and configured as push-pull by default. (1) Float IO1 if not used.
2	IO2	**Digital I/O 2.** The IO2 pin is bidirectional and configured as push-pull by default. (1) Float IO2 if not used.
3	IO3	**Digital I/O 3.** The IO3 pin is bidirectional and configured as push-pull by default. (1) Float IO3 if not used.
4	COPI	**SPI data in.** The COPI pin is pulled down internally. (2) Connect COPI to GND if not used.
5	/CS	**SPI chip selection.** The /CS pin is pulled up internally. (2) Connect /CS to DVDD if not used.
6	IO4	**Digital I/O 4.** The IO4 pin is bidirectional and configured as push-pull by default. (1) Float IO4 if not used.
7	CIPO	**SPI data out.** The CIPO pin is configured as push-pull when the serial peripheral interface (SPI) is active. CIPO is configured as pull-down when the SPI is idle. (2) Float CIPO if not used.
8	GND	**Supply ground.**
9	IO5	**Digital I/O 5.** The IO5 pin is bidirectional and configured as push-pull by default. (1) Float IO5 if not used.
10	TEST	**Test.** Connect the TEST pin to GND.
11	CK100	**Clock output reference for speed calculation.** Float the CK100 pin if not used.
12	SCLK	**SPI clock.** The SCLK pin is pulled down internally. (2) Connect SCLK to GND if not used.
13	DVDD	**Digital supply 3.3V.** Bypass the DVDD pin to GND with a low, 0.1µF ESR capacitor. See the Electrical Mounting and Power Supply Decoupling section on page 13 for details on the layout reference.
14	AVDD	**Analog supply 3.3V.** Bypass the AVDD pin to GND with a 1µF low ESR capacitor. See the Electrical Mounting and Power Supply Decoupling section on page 13 for details on the layout reference.
15	IO6	**Digital I/O 6.** The IO6 pin is bidirectional and configured as push-pull by default. (1) Float IO6 if not used.
16	NC	**No connection.**
17	E-PAD	**E-pad.** No connection. Float the EPAD pin.

Notes:

1) Can be configured as open drain with the OD615 and OD243 parameters.
2) Can be configured to high impedance with the SPULLIN and TRISTATE parameters.

ABSOLUTE MAXIMUM RATINGS (3)

Supply voltage (V_{AVDD}, V_{DVDD}) .....-0.5V to +4.6V
Input pin voltage (V_I) .....-0.5V to +6V
Output pin voltage (V_O) .....-0.5V to +6V
Continuous power dissipation (T_A = 25°C) (4)
..... 2W
Lead temperature .....260°C
Operating temperature..... -40°C to +125°C
Maximum magnetic field 200mT

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM).....±2kV

Recommended Operating Conditions (5)

V_{AVDD}, V_{DVDD} .....3V to 3.6V
Operating junction temp (T_J).... -40°C to +125°C

Notes:

3) Exceeding these ratings may damage the device.
4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) The device is not guaranteed to function outside of its operating conditions.

ELECTRICAL CHARACTERISTICS

V_{AVDD} = V_{DVDD} = 3.3V, T_A = -40°C to +125°C, typical values at T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Recommended Operating Conditions						
Supply voltage	V_{AVDD}		3	3.3	3.6	V
	V_{DVDD}		3	3.3	3.6	V
V_{DD} under-voltage lockout (UVLO) threshold	V_{DD_UVLO}	V_{DD} rising, V_{AVDD} = V_{DVDD}			2.9	V
V_{DD} UVLO hysteresis	$V_{DD\_UVLO\_HYS}$	V_{AVDD} = V_{DVDD}	60			mV
Supply current	I_{AVDD} + I_{DVDD}	T_A = 25°C	5.5	7.5	9.5	mA
Supply current drift		T_A = -40°C to +125°C		0.006		mA/°C
Digital I/O						
Input high voltage	V_{IH}		2.5		5.5	V
Input low voltage	V_{IL}		-0.3		+0.8	V
Push-Pull Option						
Output low voltage	V_{OL_PP}	I_{OL} = 12mA			0.4	V
Output high voltage	V_{OH_PP}	I_{OH} = 12mA	2.4			V
Pull-up resistor	R_{PU}	V_I = GND		80		kΩ
Pull-down resistor	R_{PD}	V_I = DVDD		30		kΩ
Rising edge slew rate	T_R	C_{LOAD} = 50pF		0.7		V/ns
Falling edge slew rate	T_F	C_{LOAD} = 50pF		0.7		V/ns
Open-Drain Option						
Output low voltage	V_{OL_OD}	I_{OL} = 12mA			0.4	V
Output high voltage (6)	V_{OH_OD}	Supplied by external pull-up resistor			5.5	V
Open-drain leakage current				100		nA

GENERAL CHARACTERISTICS

V_{AVDD} = V_{DVDD} = 3.3V, 20mT < B < 80mT, T_A = -40°C to +125°C, typical values at T_A = 25°C and B = 45mT, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating temperature	T_{OP}		-40		+125	°C
Applied magnetic field	B	Optimal linearity	20		80	mT
		Functional	10		150	
Absolute Output (Serial)						
Resolution (6)		±3σ noise deviation	12		15	bit
Noise RMS (6)			0.002		0.015	deg
Refresh rate	$f_{REFRESH}$	T_A = 25°C	780	800	820	kHz
Oscillator drift		T_A = -40 to +85°C		-30		ppm/°C
		T_A = 85 to 125°C		-100		ppm/°C
Data output length				16		bit
Response Time						
Start-up time (6)		FW = 0, T_A = 25°C			250	µs
Latency (added time beyond refresh time) (6)	L	FW = 0		32		µs
		FW = 5 to 12	-0.5		+0.5	µs
Filter cutoff frequency	f_{CUTOFF}	FW = 0		17		kHz
Accuracy						
Integral non-linearity (6)	INL	T_A = 25°C, B = 45mT		0.2	0.6	deg
		After user calibration with on-chip 32-point lookup table, T_A = 25°C		0.06	0.1	deg
Output Drift						
Temperature induced drift (6)		T_A = -40 to +85°C		0.0015	0.0045	deg/°C
		T_A = 85 to 125°C		0.005	0.02	deg/°C
Magnetic field induced (6)		T_A = 25°C		0.004	0.007	deg/mT
Voltage supply induced (6)		B = 45mT, T_A = 25°C		0.1	0.3	deg/V
Functional Test Mode						
Functional test accuracy				2		deg
Absolute Output (PWM)						
Pulse-width modulation (PWM) frequency	f_{PWM}	PWMF = 0, T_A = 25°C	243	250	257	Hz
		PWMF = 1, T_A = 25°C	0.975	1	1.025	kHz
PWM resolution				12		bit
Incremental Output (ABZ)						
ABZ update rate		T_A = 25°C	12	12.8		MHz
Edges per turn resolution		Configurable	4		16384	
Pulses per channel per turn	PPT + 1	Configurable	1		4096	
Differential non-linearity	DNL			1.7		%
Overall ABZ jitter (3σ)		PPT = 511, speed = 1krpm		0.06		deg
		PPT = 2047, speed = 10krpm		0.02		deg

GENERAL CHARACTERISTICS *(continued)*

V_{AVDD} = V_{DVDD} = 3.3V, 20mT < B < 80mT, T_A = -40°C to +125°C, typical values at T_A = 25°C and B = 45mT unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Incremental Output (UVW)						
Cycle per turn	NPP + 1	Configurable	1		8	
UVW jitter (3σ)		NPP = 0, speed = 5krpm		0.4		deg
Speed Output						
Speed scale	S_{SPEED}	f_{CK100} = 100kHz		5.722		rpm/LSB
CK100 clock frequency		T_A = 25°C	98	100	102	kHz

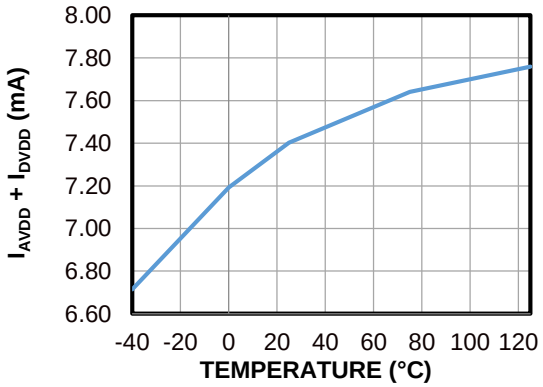
Note:

6) Guaranteed by design and characterization.

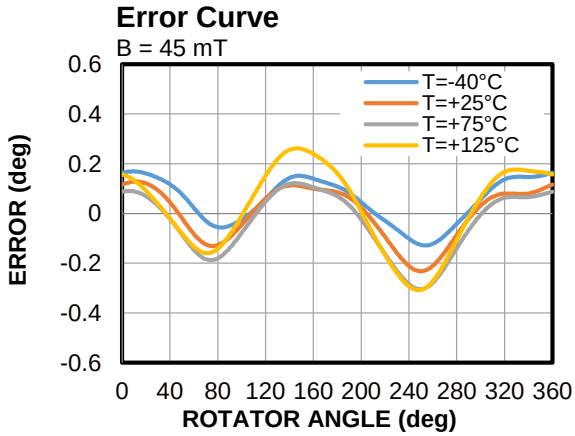
TYPICAL CHARACTERISTICS

V_{AVDD} = V_{DVDD} = 3.3V, 20mT < B < 80mT, T_A = 25°C, unless otherwise noted.

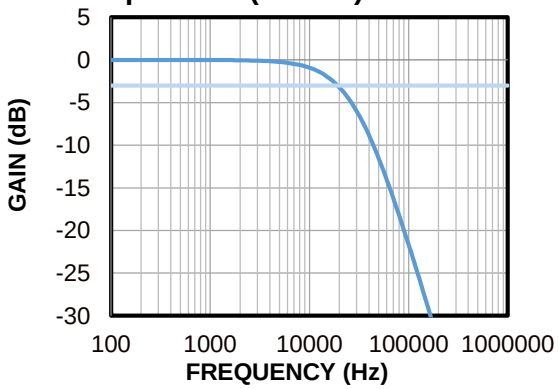
Supply Current



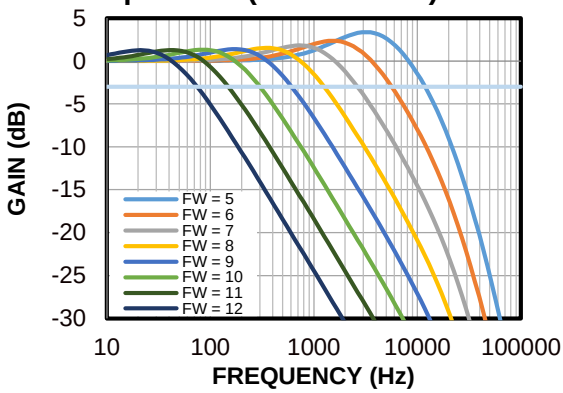
Error Curve



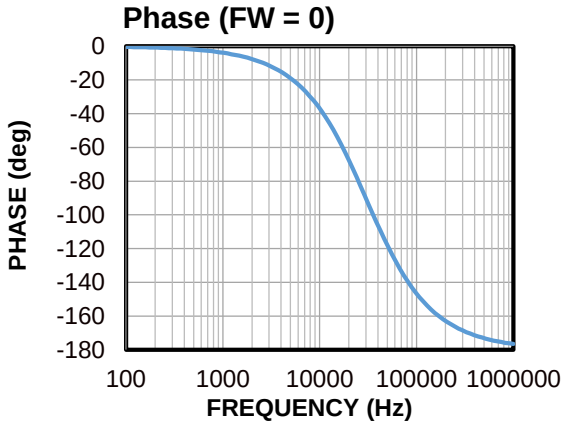
Spectrum (FW = 0)



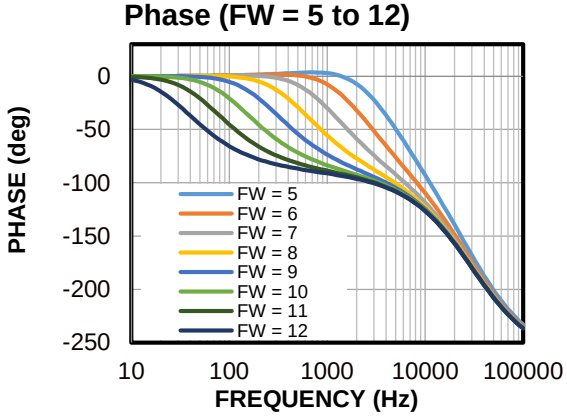
Spectrum (FW = 5 to 12)



Phase (FW = 0)



Phase (FW = 5 to 12)

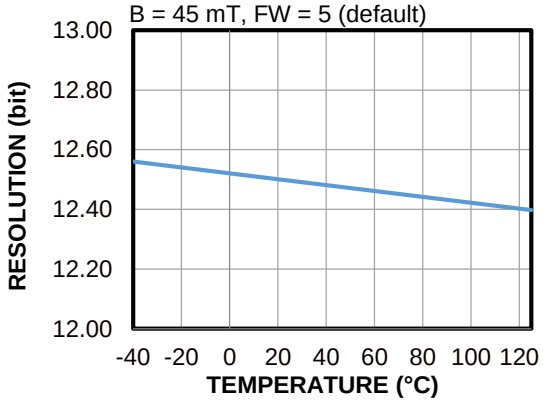


TYPICAL CHARACTERISTICS *(continued)*

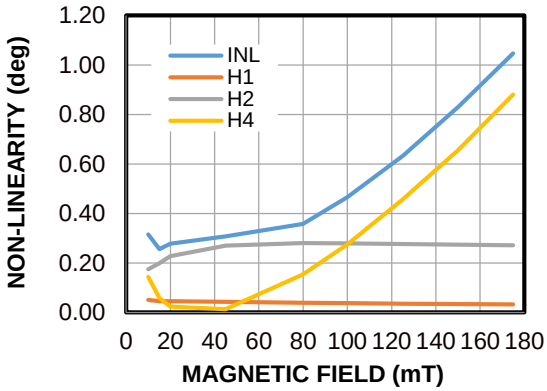
V_{AVDD} = V_{DVDD} = 3.3V, 20mT < B < 80mT, T_A = 25°C, unless otherwise noted.

Resolution Over-Temperature

B = 45 mT, FW = 5 (default)

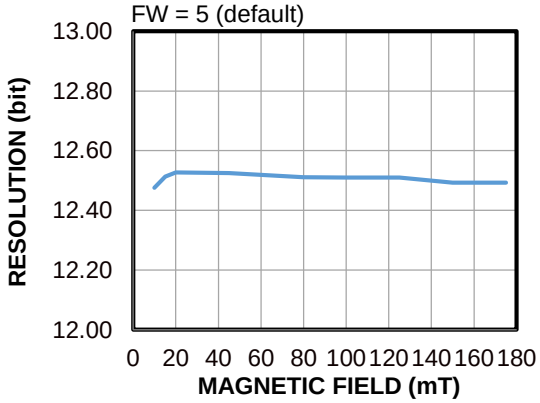


INL and Harmonics vs. Magnetic Field



Resolution vs. Magnetic Field

FW = 5 (default)



FUNCTIONAL BLOCK DIAGRAM

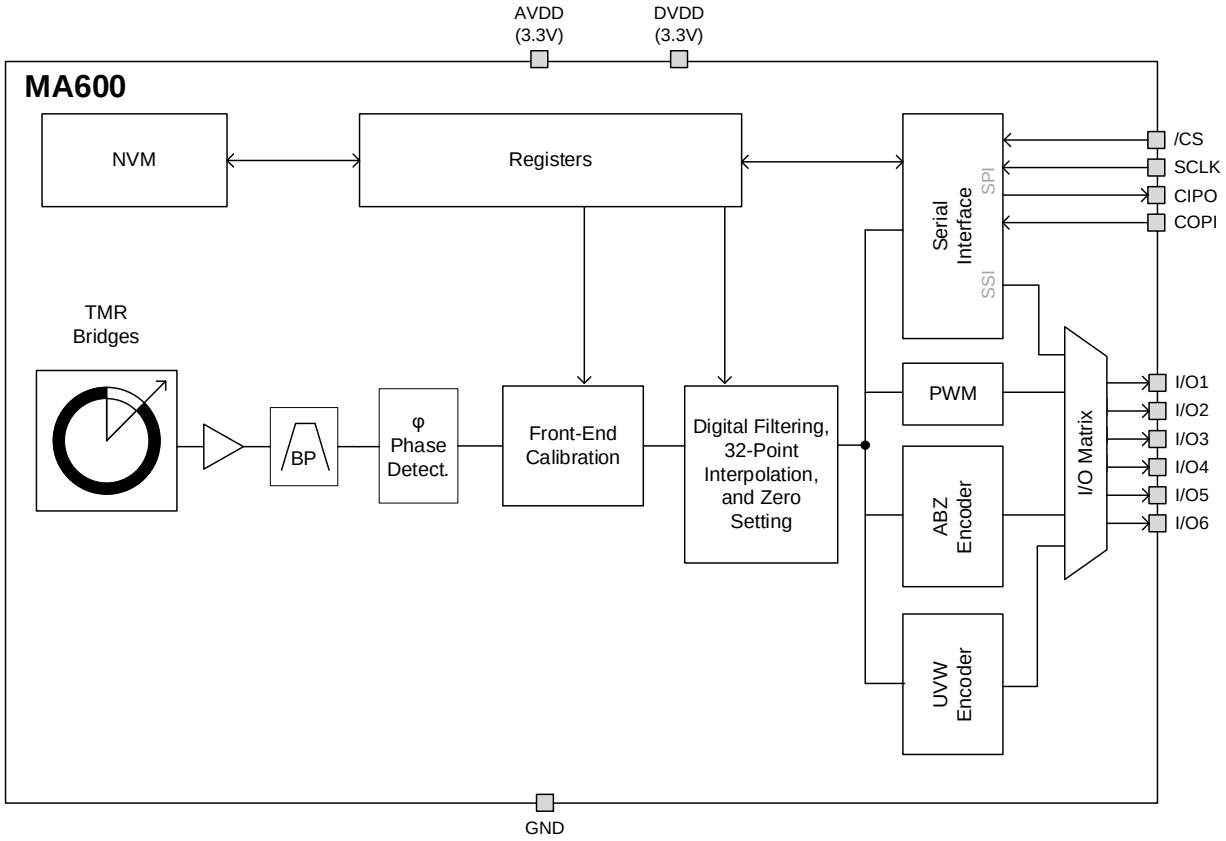


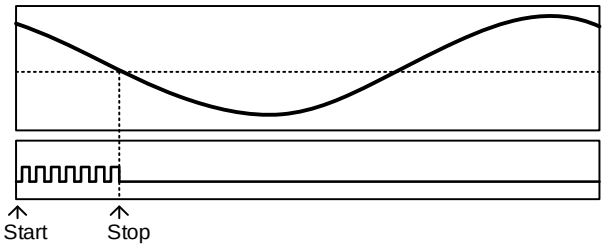
Figure 1: Functional Block Diagram

OPERATION

Sensor Front End

The magnetic field is detected with the tunneling magnetoresistance (TMR) bridges located in the center of the package. The angle is measured using the Spinaxis™ method, which directly digitizes the direction of the field without complex arctangent computation or feedback loop-based circuits (interpolators).

The Spinaxis™ method is based on phase detection, and this method generates a sinusoidal signal with a phase that represents the angle of the magnetic field. The angle is then obtained by a time-to-digital converter, which measures the time between the zero crossing of the sinusoidal signal and the edge of a constant waveform (see Figure 2). The time-to-digital is output from the front end to the digital conditioning block.



Top: Sine Waveform

Bottom: Clock for Time-to-Digital Converter

Figure 2: Phase Detection Method

The front-end output delivers a digital number that is proportional to the angle of the magnetic field (at the rate of 800kHz) in a straightforward and open-loop manner.

Sensor (Magnet Mounting)

The sensitive volume of the MA600 is confined to a region less than 400µm wide. This area contains multiple TMR bridges. The volume is located horizontally within 50µm of the center of the package. Vertically, the sensitive volume is centered at approximately 300µm under the surface. The sensor detects the angle of the magnetic field projected in a plane parallel to the package's upper surface. This means that the only relevant magnetic field is the in-plane component (X and Y components) within the sensitive volume (see Figure 3).

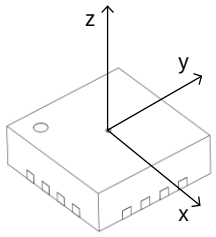


Figure 3: Space Coordinates
(Field is Sensed on the XY Plane)

By default, when looking at the top of the package, the angle increases when the magnetic field rotates clockwise. Figure 4 shows the zero angle of a sensor that has not been configured, where the cross indicates the sensitive point. Both the rotation direction and the zero angle can be configured.

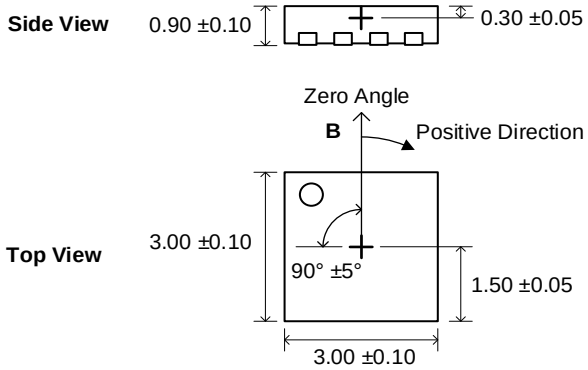


Figure 4: Detection Point and Default Positive Direction

This type of detection provides flexibility for the angular encoder design. The sensor requires the magnetic vector to remain within the sensor plane with an amplitude within the recommended operating range.

The most straightforward mounting method is to place the MA600 sensor on the rotation axis of a permanent magnet, such as a diametrically magnetized cylinder (see Figure 5 on page 13).

Consider a Neodymium alloy (N35) cylinder magnet with Ø5x2.5mm dimensions inserted into an aluminum shaft, with a 2mm air gap between the magnet and the sensor (surface of the package). For optimal linearity, the sensor is positioned on the magnet's rotation axis with a 5% precision of the magnet outer diameter.

For more information about the sensor and magnet placement, refer to the related application note on the MPS website (Selecting the Right Magnet for the MagAlpha in End-of-Shaft Mounting).

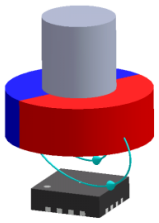


Figure 5: End-of-Shaft Mounting

If the end-of-shaft position is not available, the sensor can be positioned away from the rotation axis of a cylinder or ring magnet (see Figure 6).

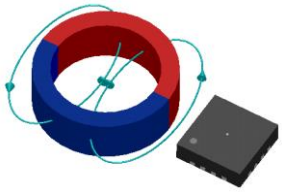


Figure 6: Side-Shaft Mounting

In this case, the magnetic field angle is no longer directly proportional to the mechanical angle. The MA600 can be adjusted to compensate for this effect, and to recover the linear relation between the mechanical angle and the sensor output. With multiple pole pair magnets, the MA600 indicates multiple rotations for each mechanical turn.

Electrical Mounting and Power Supply Decoupling

The two decoupling capacitors are connected to the supply lines (AVDD and DVDD) via a low-impedance path (see Figure 7).

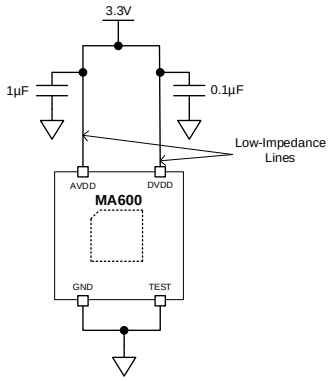


Figure 7: Power Supply Decoupling

If the decoupling capacitors are placed close to the sensor, the target magnetic field may be influenced and negatively impact the sensor's accuracy (INL) due to the MA600's high accuracy. For example, an SMD capacitor (0603) placed 1.5mm from the MA600's edge can create a second harmonic non-linearity up to 0.2°. To avoid magnetic interference that affects sensor accuracy, place the capacitor as far from the MA600 as practically feasible for the design. Place the capacitors a 5mm radius from the MA600 to avoid magnetic interference.

Keep the high current path and ground as far away from the MA600 as possible to prevent potential interference.

It is recommended to float the MA600's exposed pad to minimize mechanical stress.

Serial Interface

The sensor supports the serial peripheral interface (SPI) for angle reading and register configuration. Alternatively, the synchronous serial interface (SSI) protocol can be used for angle reading. Configuration through the SSI is not supported.

Serial Peripheral Interface (SPI)

The SPI is a four-wire, synchronous, serial communication interface. The MA600 supports SPI mode 3 and mode 0. Table 1 shows the SPI specifications.

Table 1: SPI Specifications

	Mode 0	Mode 3
SCLK Idle State	Low	High
Data Capture	On SCLK rising edge	
Data Transmission	On SCLK falling edge	
/CS Idle State	High	
Data Order	MSB first	

The SPI mode (0 or 3) is detected automatically by the sensor, and does not require additional action from the user. The maximum SPI clock frequency supported by MA600 is 25MHz. There is no minimum clock rate. Real maximum data rates depend on the PCB layout quality and signal trace length.

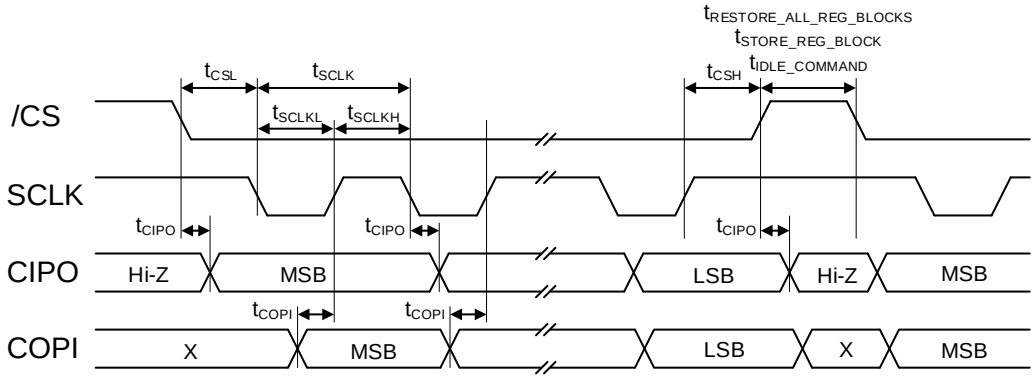
Table 2 shows the standard SPI values.

Table 2: SPI Standard

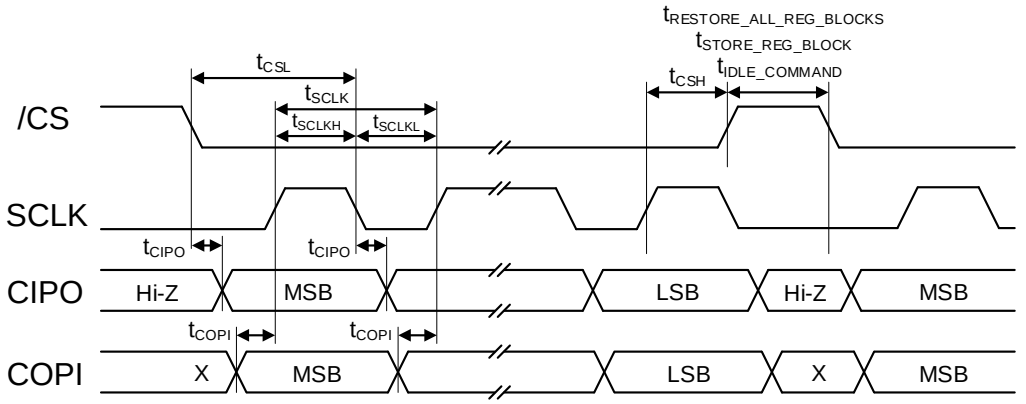
	Mode 0	Mode 3
CPOL	0	1
CPHA	0	1
Data Order (DORD)	0 (MSB first)	

All commands to the MA600 (whether for writing or reading register content) must be transferred through the SPI COPI pin. See the SPI Communication section on page 16 for details.

Figure 8 shows the SPI timing diagram for mode 3 and mode 0, where COPI is the controller output peripheral input, and CIPO is the controller input peripheral output. Figure 9 on page 15 shows the minimum idle time, and Table 3 shows the SPI timing.



SPI Mode 3



SPI Mode 0

Figure 8: SPI Timing Diagram

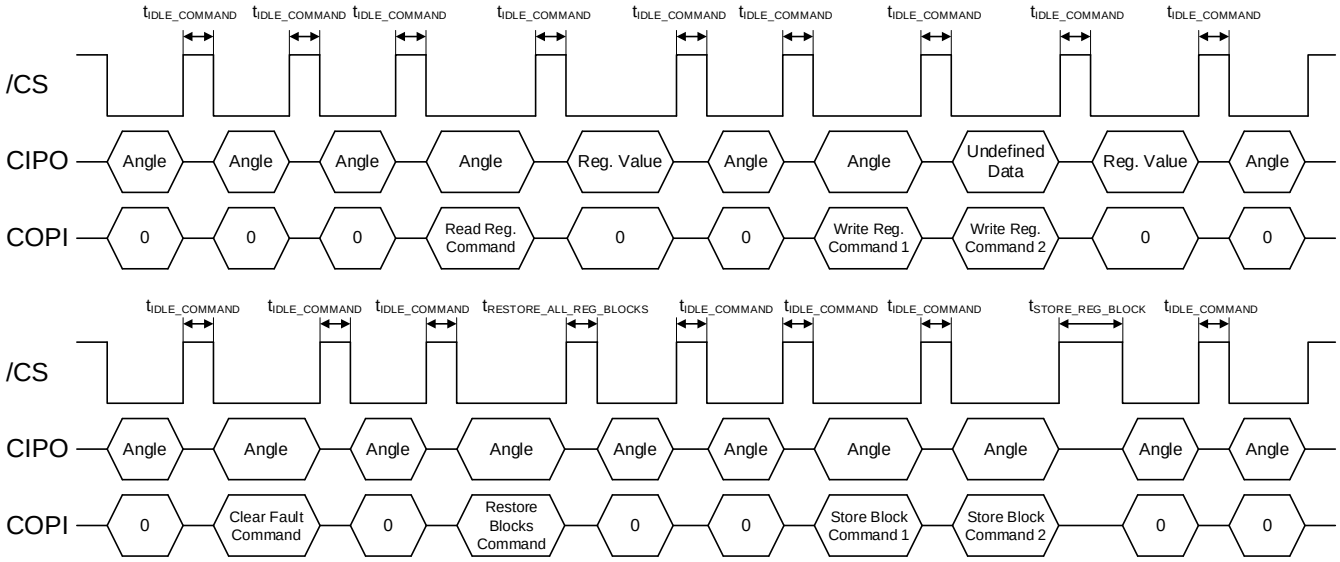


Figure 9: Minimum Idle Time

Table 3: SPI Timing

Parameter (7)	Description	Min	Max	Unit
$t_{IDLE\_COMMAND}$	Idle time between transmissions	120		ns
$t_{STORE\_REG\_BLOCK}$	Time required to store a register block to the NVM	600		ms
$t_{RESTORE\_ALL\_REG\_BLOCKS}$	Time required to restore all register blocks from the NVM	240		us
t_{CSL}	Time between /CS falling edge and SCLK falling edge	20		ns
t_{SCLK}	SCLK period	40		ns
t_{SCLKL}	Low level of the SCLK signal	20		ns
t_{SCLKH}	High level of the SCLK signal	20		ns
t_{CSH}	Time between the SCLK rising edge and /CS rising edge	20		ns
t_{CIPO}	SCLK setting edge to data output valid		15	ns
t_{COPI}	Data input valid to SCLK rising edge	15		ns

Note:

7) All values are guaranteed by design.

The MA600 resolution may be affected by the sampling frequency (/CS frequency) (see Figure 10).

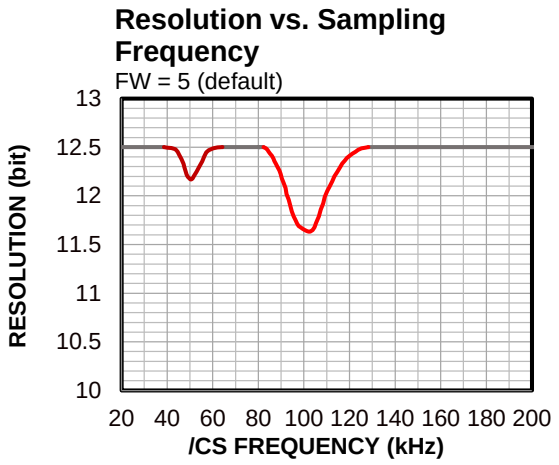


Figure 10: Resolution and Sampling Frequency

In some frequency ranges (e.g. between 90kHz and 110kHz), the resolution drop can be visible at certain angles. A smaller drop can also be visible between 40kHz and 60kHz.

SPI Communication

The sensor supports eight types of SPI operation:

- Read angle
- Read multi-turn
- Read speed
- Read register
- Write register
- Store a single register block to the NVM
- Restore all register blocks from the NVM
- Clear error flags

Each operation has a specific frame structure described below.

SPI Read Angle

The refresh period is $1/f_{REFRESH}$. New data is transferred into the output buffer each refresh period. The controller device triggers the reading by pulling /CS low.

When a trigger event is detected, the data remains in the output buffer until the /CS signal is de-asserted (see Table 4).

Table 4: Sensor Data Timing

Event	Action
/CS falling edge	Start reading and freeze the output buffer
/CS rising edge	Release the output buffer

A full angle reading requires 16 clock pulses. The angle output value is read with the most significant bit (MSB) first. Figure 11 shows a diagram of a full SPI angle reading.

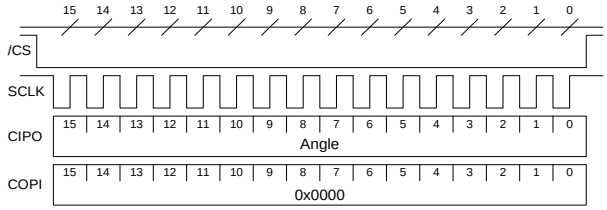


Figure 11: Diagram of a Full 16-Bit SPI Angle Reading

The angle in degrees can be calculated with Equation (1):

$$\text{angle (deg)} = \frac{\text{angle (dec)}}{2^{16}} \times 360 \qquad (1)$$

If less resolution is sufficient, the angle can be read by sending fewer clock counts since the MSB is first. Figure 12 shows a diagram of a partial 8-bit SPI angle reading.

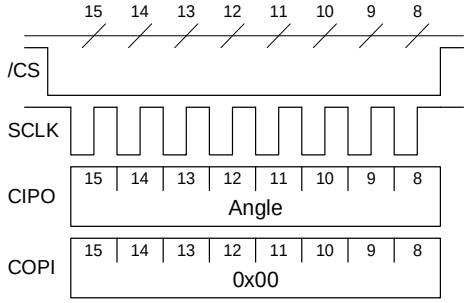


Figure 12: Diagram of a Partial 8-Bit SPI Angle Reading

If there are very fast reading cycles, the MA600 continues sending the same data until the data refreshes. See the General Characteristics section on page 6 for the refresh rate.

SPI Read Multi-Turn/Speed

By sending 32 clock pulses, the user can obtain the multi-turn or speed information.

The first 16 bits returned on the CIPO line contain the angle value. When MTSP in register 28 is set to 0 (default setting), the second 16 bits contain the multi-turn count; when MTSP is set

to 1, the second 16 bits contain the speed (see Figure 13).

See Multi-Turn Output section on page 35 for more details on multi-turn.

See the Speed Output and Calculation section on page 34 for more details of speed.

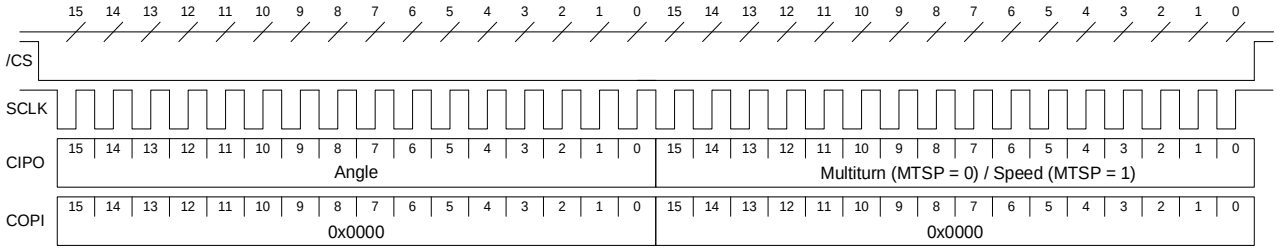
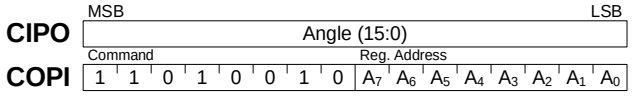


Figure 13: 32-Bit Frame Read Multi-Turn/Speed Operation

SPI Read Register

A read register operation consists of two 16-bit frames. The first frame sends a read request, which contains the 8-bit read command followed by the 8-bit register address. The second frame returns the 8-bit angle value (MSB byte) with the requested 8-bit register value (LSB byte).

The first 16-bit SPI frame (read request) is:



The second 16-bit SPI frame (response) is:

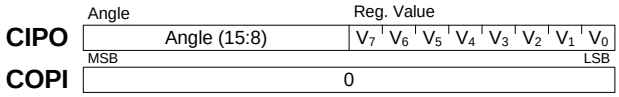


Figure 14 shows a complete transmission.

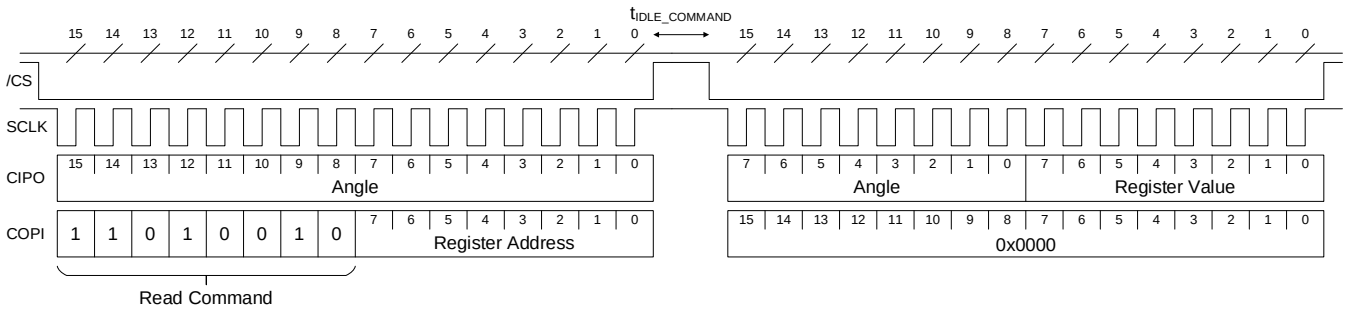
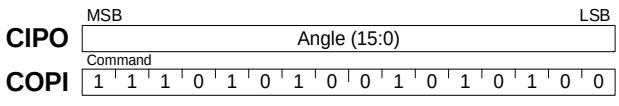


Figure 14: Overview of a Read Register Operation with Two 16-Bit Frames

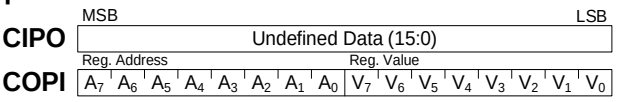
SPI Write Register

A write register operation consists of three 16-bit frames. The first frame sends a write request, that contains the 16-bit write command. The second frame sends the 8-bit register address and the 8-bit value (MSB first). The third frame returns the newly written register value with an 8-bit angle value.

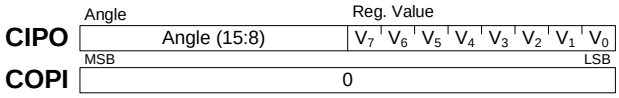
The first 16-bit SPI frame (write request) is:



The second 16-bit SPI frame (address and value) is:

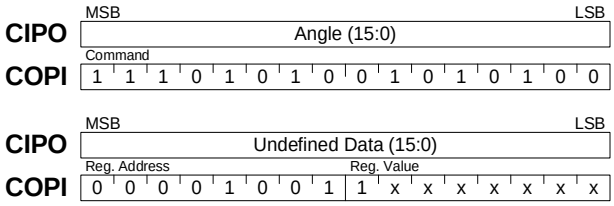


The third 16-bit SPI frame (response) is:



The readback register content can be used to verify the register configurations.

For example, to set the value of the output rotation direction (RD) to counterclockwise (RD bit = 1), write register 9 by sending the following first and second frames on page 18:



Then send the third frame. If the register is written correctly, the reply is:

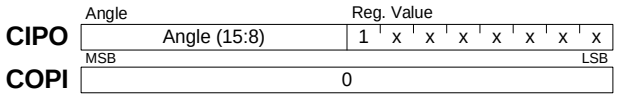


Figure 15 shows a complete transmission.

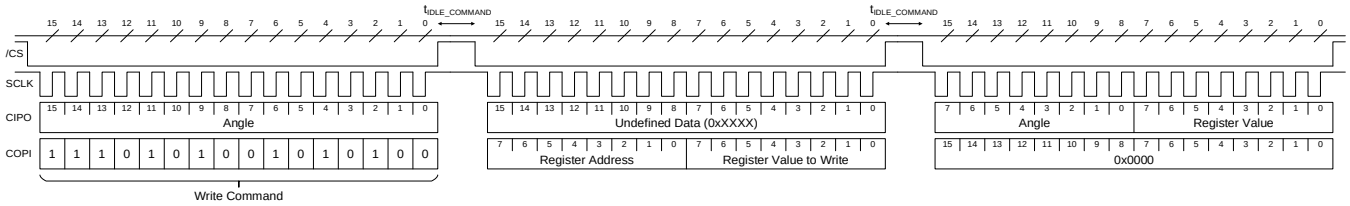


Figure 15: Overview of a Write Register Operation with Two 16-Bit Frames

Non-Volatile Memory (NVM) Operation

The sensor contains a non-volatile memory (NVM) that is divided into two separate memory blocks. Each block contains 32 registers. Block 0 contains register 0 to register 31, and block 1 contains register 32 to register 63. The values stored in the NVM are automatically loaded into the sensor's registers during start-up.

It is possible to manually force the restoration of the NVM values to the registers by using the Restore All Register Blocks SPI command.

Copy the register block values to the NVM by using the Store a Single Register Block to the NVM SPI command.

If two NVM commands are sent successively within a time period shorter than $t_{STORE\_REG\_BLOCK}$ in Table 3 on page 15, the second command is ignored and the ERRMEM flag is raised.

SPI Store a Single Register Block to the NVM

This command stores all register values in the corresponding NVM (see Figure 16). The register value is set to 0 to store register 0 to register 31. The register value is set to 1 to store register 32 to register 63 (see Table 9 on page 24).

This command is ignored if the NVM is busy executing a previously received command, and the ERRMEM flag is active.

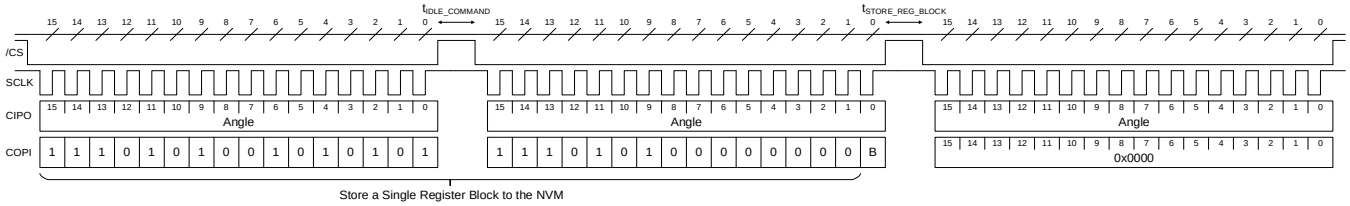


Figure 16: Overview of Store a Single Register Block to the NVM Operation with Three 16-Bit Frames

SPI Restore All Register Blocks from the NVM

This command restores all register blocks from the NVM (see Figure 17). This operation is done automatically (without user intervention) at each start-up.

This command is ignored if the NVM is busy executing a previously received command, and the ERRMEM flag is active.

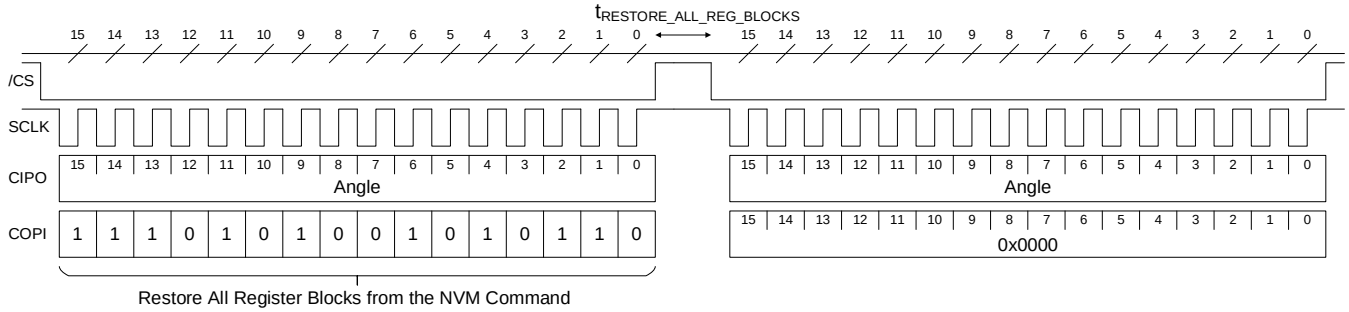


Figure 17: Overview of Restore All Register Blocks from the NVM Operation with Two 16-Bit Frames

SPI Clear Error Flags

This command clears all error flags in register 26, including NVMB, ERRCRC, ERRMEM, and ERRPAR (see Figure 18).

Table 5 on page 20 shows a summary of all SPI commands.

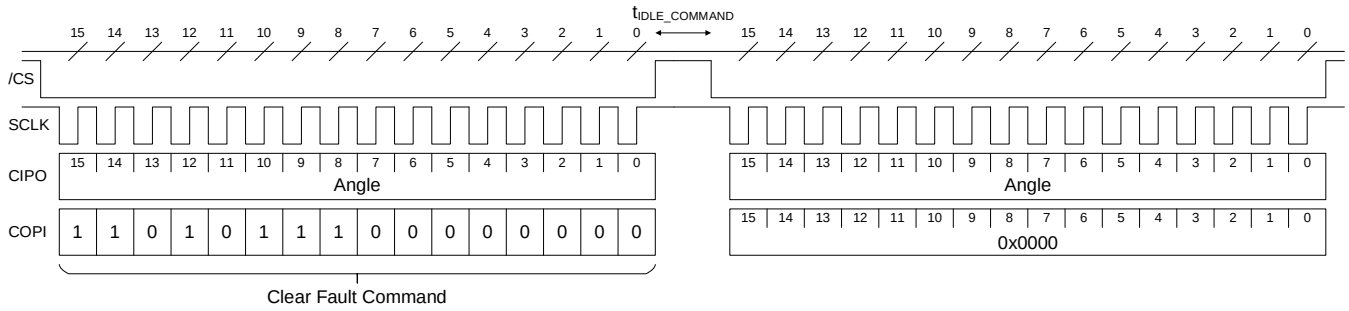


Figure 18: Overview of Clear Error Flags Operation with Two 16-Bit Frames

Table 5: SPI Commands List Overview

Command Function	Transaction Length	Command		Returned Value on Last Command
Read Angle	1 x 16-bit	0x0000		16-bit angle
Read Multi-Turn	1 x 32-bit	0x00000000		16-bit angle + 16-bit multi-turn
Read Speed	1 x 32-bit	0x00000000		16-bit angle + 16-bit speed
Read Register	2 x 16-bit	1st command	0xd2 (8) + 8-bit reg. address	8-bit angle MSB + 8-bit reg. value
		2nd command	0x0000	
Write Register	3 x 16-bit	1st command	0xea54 (8)	8-bit angle MSB + 8-bit reg. value
		2nd command	8-bit reg. address + 8-bit reg. value	
		3rd command	0x0000	
Store a Single Register Block to the NVM	3 x 16-bit	1st command	0xea55 (8)	16-bit angle
		2nd command	0xea00 (8) for block 0, 0xea01 (8) for block 1	
		3rd command	0x0000	
Restore All Register Blocks from the NVM	2 x 16-bit	1st command	0xea56 (8)	16-bit angle
		2nd command	0x0000	
Clear Error Flags	2 x16-bit	1st command	0xd700 (8)	16-bit angle
		2nd command	0x0000	

Note:

8) These values are in hexadecimal format. For example, 0xd2 indicates 1101 0010 in binary format.

SPI Parity Check

SPI parity check is enabled by setting PRT in register 28 to 1. The parity sign is determined by PRTS, where the sign is even by default (PRTS = 0), and can be changed to odd by setting PRTS to 1. When parity check is enabled, changing the PRTS value leads to the ERRPAR flag becoming active.

When SPI parity check is enabled, the controller must send one parity bit after the 16-bit command. The MA600 also returns one parity bit after the 16-bit data. Figure 19 shows the SPI read angle with parity check.

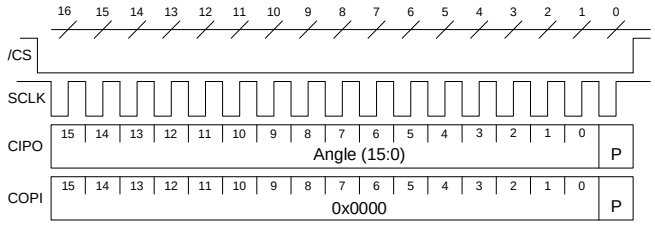


Figure 19: SPI Read Angle When SPI Parity Check is Enabled

If the parity bit sent by controller is wrong, the error bit (ERRPAR) in register 26 is set to 1. See the ERRPAR section on page 35 for more details.

Table 6 on page 21 shows a summary of SPI commands with parity check.

Table 6: SPI Commands with Parity Check Overview

Command Function	Command Sent by Controller	Returned Value	Action when Parity Sent by Controller is Wrong
Read Angle	0x0000 + parity bit	16-bit angle + parity bit	ERRPAR = 1
Read Multi-Turn/Speed	0x0000 + parity bit + 0x0000 + parity bit	16-bit angle + parity bit + 16-bit multi-turn/speed + parity bit	ERRPAR = 1
Read/Write Register	Several 17-bit commands, where each command is a 16-bit command + parity bit	Several 17-bit replies, where each reply is a 16-bit reply + parity bit	ERRPAR = 1, the command is discarded
Store/Restore NVM			
Clear Error Flags			

SPI Angle Parity Check on CIPO

SPI angle parity check can be enabled by setting APRT in register 28h to 1.

If APRT = 1, the least significant bit (LSB) of the 16-bit angle output on CIPO is replaced by the angle parity bit. Figure 20 shows an example of angle reading with the angle parity bit, where AP stands for the angle parity bit.

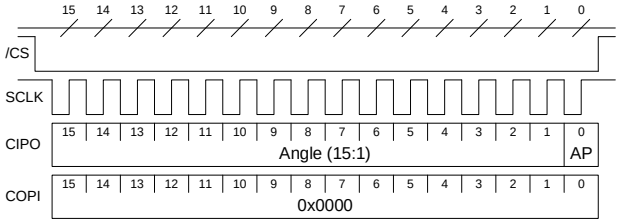


Figure 20: Angle Output with Parity Bit when APRT = 1

When APRT = 1, SPI angle parity check is applied to all SPI CIPO replies containing a 16-bit angle.

The angle parity bit sign is controlled by PRTS in register 28h.

SPI parity check and angle parity check can be enabled at the same time. Figure 21 shows an example of angle reading with both the angle parity bit and SPI parity bit, where P stands for the parity bit of the previous 16-bit data.

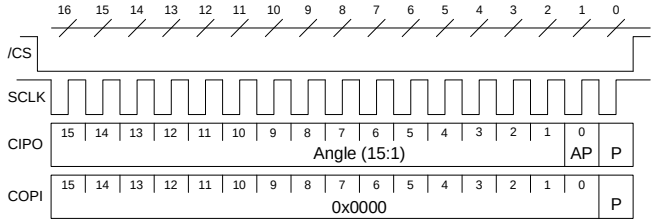


Figure 21: Angle Output with Parity Bit when PRT = 1 and APRT = 1

Synchronous Serial Interface (SSI)

The SSI is a 2-wire, synchronous, serial interface, and the sensor operates as a peripheral to the external SSI controller.

Only angle reading can be done by the SSI. It is not possible to read or write registers using the SSI.

The maximum SSI clock frequency supported by the MA600 is 5MHz. Real maximum data rates depend on the PCB layout quality and signal trace length.

Figure 22 on page 22 shows the SSI timing for mode A and mode B, and Table 7 shows the timing of SSI communication.

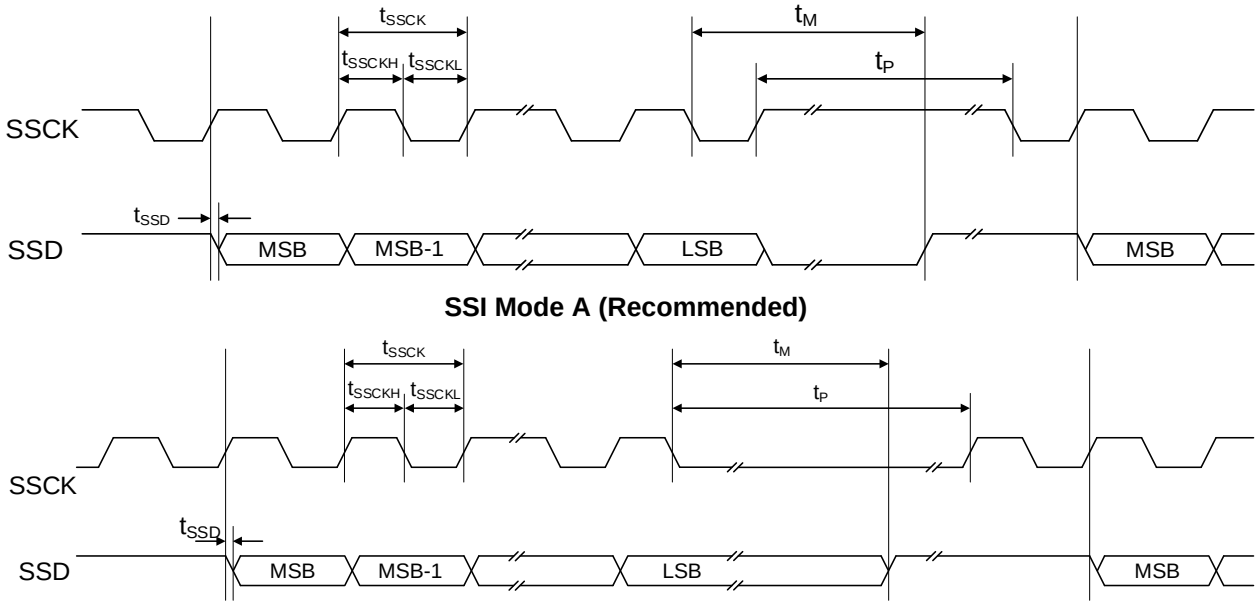


Figure 22: SSI Timing for Mode A and Mode B (Both Modes are Supported)

Table 7: SSI Timing

Parameter	Description	Min	Max	Unit
t_{SSD}			81	ns
t_{SSCK}	SSCK period	0.2	16	µs
t_{SSCKL}	Low level of the SSCK signal	0.1	8	µs
t_{SSCKH}	High level of the SSCK signal	0.1	8	µs
t_M	Transfer timeout (monoflop time)	25		µs
t_P	Dead time: SSCK high time for the next data reading	40		µs

SSI Read Angle

The MSBs are transmitted first. Every refresh period, new data is transferred into the output buffer.

The first clock count is a dummy clock to start the transmission. The first MSB data is then transmitted on the second clock count. The controller device triggers the reading by driving SSCK high.

The MA600's data length is 16 bits long, meaning a full reading requires one dummy clock and 16 clock counts (see Figure 23 on page 23). The reading can also be performed with fewer than 17 clock counts. For example, if an application requires only 12-bit angle information, it is sufficient to send the first dummy clock to start the transmission and 12 further clock cycles to read the angle data.

When a trigger event is detected, the data remains in the output buffer until the transfer timeout passes (see Table 8).

Figure 24 shows the timing for consecutive angle readings.

Table 8: Sensor Data Timing

Trigger Event	Release of the Output Buffer
First SSCK rising edge after dummy clock	Last SSCK falling edge + time out (t_M) (see Figure 22 on page 21)

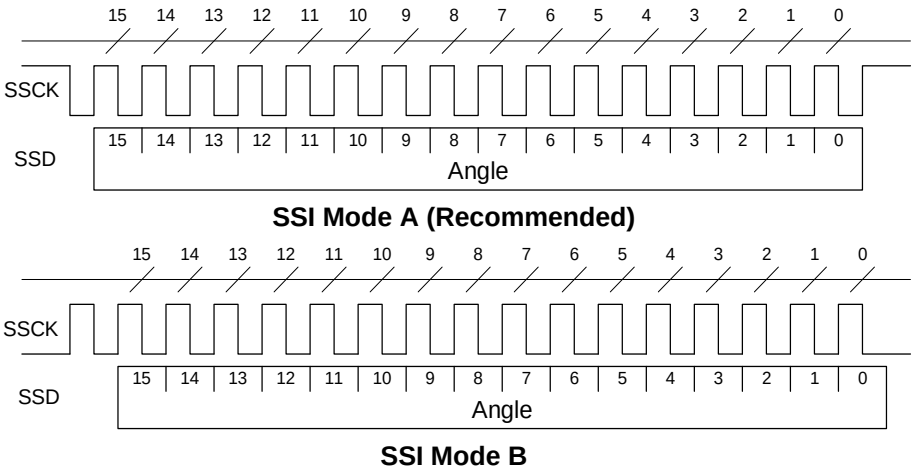


Figure 23: Diagram of a Full 16-Bit SSI Angle Reading (with First Dummy Clock)

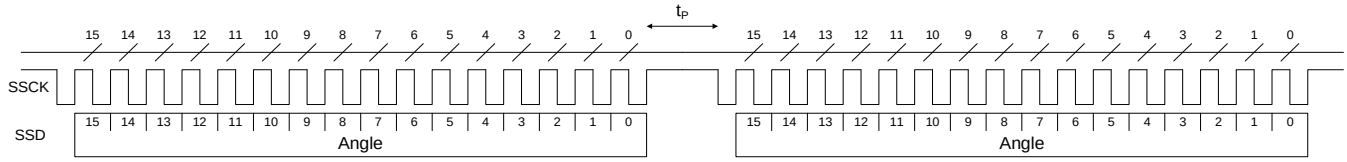


Figure 24: Two Consecutive 16-Bit SSI Angle Readings (with Required Dead Time Between the Frames)

SSI Parity Check

The SSI parity check is enabled by default. To obtain the parity bit, the user must send one dummy clock and 17 clock counts. The parity bit follows the LSB of the angle data (see Figure 25).

The parity sign is even parity by default and can be configured to odd parity by setting PRTS in register 28 to 1 with an SPI command.

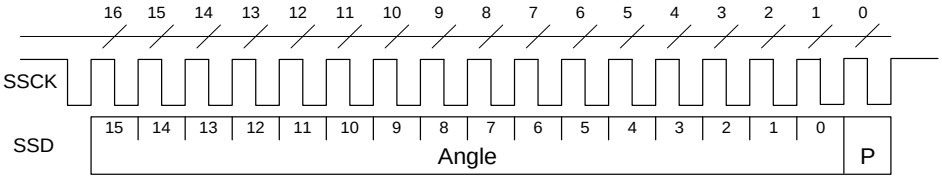


Figure 25: 17-Bit SSI Angle Reading with Parity Check (with First Dummy Clock)

REGISTER MAP

Table 9: Register Map (9)

#	Block	Hex	R/W	Bit[7] (MSB)	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0] (LSB)
0	0	0x00	R/W	Z[7:0]							
1		0x01	R/W	Z[15:8]							
2		0x02	R/W	BCT[7:0]							
3		0x03	R/W	-	-	-	-	-	-	ETY	ETX
4		0x04	R/W	PPT[2:0]			ILIP[3:0]				PPT[11]
5		0x05	R/W	PPT[10:3]							
7		0x07	R/W	NPP[2:0]			-	-	-	-	-
8		0x08	R/W	PWMM	PWMF	-	-	-	-	-	-
9		0x09	R/W	RD	-	-	-	-	-	-	-
10		0x0A	R/W	DAISY	-	-	-	-	-	-	RWM
11		0x0B	R/W	OD615	OD243	SPULLIN	TRISTATE	-	-	-	-
12		0x0C	R/W	HYS[7:0]							
13		0x0D	R/W	-	-	-	-	FW[3:0]			
14		0x0E	R/W	INTF_SEL[2:0]			-	-	DAZ	-	CK100
18		0x12	R/W* (10)	MTOFFSET[7:0]							
19		0x13	R/W* (10)	MTOFFSET[15:8]							
26		0x1A	R	NVMB	-	-	-	-	ERRCRC	ERRMEM	ERRPAR
28		0x1C	R/W* (10)	MTSP	-	PRT	PRTS	APRT	FTA[1:0]		FTM
30		0x1E	R	SUFFIXID[7:0]							
31		0x1F	R	PRODUCTID[7:0]							
32	1	0x20	R/W	CORR0							
33		0x21	R/W	CORR1							
…		…	…	…							
62		0x3E	R/W	CORR30							
63		0x3F	R/W	CORR31							
132	4	0x84	R/W	-	-	-	-	-	-	-	UR10

Notes:

9) "-" indicates bits that are not accessible by the user.
10) R/W* indicates write access to the register only. Values are not stored in the NVM.

Table 10: Factory Default Value

#	Block	Hex	R/W	Value in Decimal	Bit[7] (MSB)	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0] (LSB)
0	0	0x00	R/W	0	0	0	0	0	0	0	0	0
1		0x01	R/W	0	0	0	0	0	0	0	0	0
2		0x02	R/W	0	0	0	0	0	0	0	0	0
3		0x03	R/W	0	0	0	0	0	0	0	0	0
4		0x04	R/W	224	1	1	1	0	0	0	0	0
5		0x05	R/W	63	0	0	1	1	1	1	1	1
7		0x07	R/W	0	0	0	0	0	0	0	0	0
8		0x08	R/W	192	1	1	0	0	0	0	0	0
9		0x09	R/W	0	0	0	0	0	0	0	0	0
10		0x0A	R/W	0	0	0	0	0	0	0	0	0
11		0x0B	R/W	32	0	0	1	0	0	0	0	0
12		0x0C	R/W	16	0	0	0	1	0	0	0	0
13		0x0D	R/W	5	0	0	0	0	0	1	0	1
14		0x0E	R/W	0	0	0	0	0	0	0	0	0
18		0x12	R/W* (11)	0	0	0	0	0	0	0	0	0
19		0x13	R/W* (11)	0	0	0	0	0	0	0	0	0
26		0x1A	R	0	0	0	0	0	0	0	0	0
28		0x1C	R/W* (11)	0	0	0	0	0	0	0	0	0
30		0x1E	R	0	0	0	0	0	0	0	0	0
31		0x1F	R	60	0	0	1	1	1	1	0	0
32	1	0x20	R/W	0	0	0	0	0	0	0	0	0
33		0x21	R/W	0	0	0	0	0	0	0	0	0
…		…	…									
62		0x3E	R/W	0	0	0	0	0	0	0	0	0
63		0x3F	R/W	0	0	0	0	0	0	0	0	0
132	4	0x84	R/W	0	0	0	0	0	0	0	0	0

Note:

11) R/W* indicates write access to the register only. Values are not stored in the NVM.

Table 11: Configuration Parameters

Parameters	Symbol	# of Bits	Description	Reference
Zero setting	Z	16	Set the zero position	Table 13
Bias current trimming	BCT	8	For side-shaft configuration: reduces the bias current of the X or Y Hall device	Table 15
Enable trimming X	ETX	1	Biased current trimmed in the X direction Hall device	Table 16
Enable trimming Y	ETY	1	Biased current trimmed in the Y direction Hall device	Table 16
Pulses per turn	PPT	12	Number of pulses per turn of the ABZ output	Table 19
Index length / index position	ILIP	4	Parametrization of the ABZ index pulse	Figure 36
Number of pair poles	NPP	3	Number of pair poles of the UVW output	Table 23
PWM mode	PWMM	1	Adds error detection to the PWM frame	Table 25
PWM frequency	PWMF	1	Sets pulse-width modulated output frequency	Table 24
Rotation direction	RD	1	Determines the sensor positive direction	Table 14
Daisy chain	DAISY	1	Enables daisy chain mode	-
Reduced wiring mode	RWM	1	Enables reduced wiring mode	Table 34
Open drain on IO6, IO1, and IO5	OD615	1	Determines the output circuits of pins IO6, IO1, and IO5: open-drain or push-pull	Table 30
Open drain on IO2, IO4, and IO3	OD243	1	Determines the output circuits of pins IO2, IO4, IO3: open drain or push-pull	Table 31
SPI input pins configuration	SPULLIN	1	Determines the output circuits of /CS, SCLK and COPI pin	Table 32
SPI output pin configuration	TRISTATE	1	Determines the internal circuit of CIPO pin	Table 33
Hysteresis	HYS	8	Hysteresis of the ABZ output	Table 21
Filter window	FW	4	Digital filter size	Table 12
Interface selection	INTF_SEL	3	Choice of the interface at IO1-IO6 pins	Table 29
DAZ interface	DAZ	1	Direction, increment, and index interface	-
Clock monitor	CK100	1	100kHz system clock available at CK100 pin	-
Multi-turn offset	MTOFFSET	16	Multi-turn offset value	-
NVM busy	NVMB	1	Indicates that the NVM is busy	-
NVM CRC error flag	ERRCRC	1	CRC error detected during NVM restoration	-
Write when NVM busy	ERRMEM	1	SPI write when the NVM is busy, ignores SPI command	-
SPI parity error	ERRPAR	1	Parity error detected on the COPI line, ignores SPI command	-
Multi-turn or speed	MTSP	1	Determines the SPI[31:16] data content	-
Parity option	PRT	1	Parity at the 17th and 33rd bit	-
Angle parity	APRT	1	16th bit of the SPI angle data is replaced by the parity bit	-
Parity sign	PRTS	1	Odd or even polarity	-

Table 11: Configuration Parameters *(continued)*

Parameters	Symbol	# of Bits	Description	See Table
Diagnostic	FTA	2	Functional test angle	18
Diagnostic	FTM	1	Functional test mode	18
Suffix ID	SUFFIXID	8	Suffix “xxxx” version	-
Product ID	PRODUCTID	8	Product version	-
User correction table	CORR0-31	32x8	User correction table (32 x 8 bits) for linear interpolation	17
Unlock register 10	UR10	1	Unlocks register 10 and enters RWM or DAISY chain mode	

REGISTER SETTINGS

Digital Filter Configuration

The filter window (FW) setting controls the sensor's resolution of the angle output (defined as the ±3σ noise interval), the latency, and the cutoff frequency (f_{CUTOFF}).

Table 12 provides the filter setting options and resulting performance. It is not recommended to use FW 1 to 4 and 13 to 15.

Table 12: Filter Settings

FW [3:0]	τ (μs)	Resolution (bits)	Latency Cancellation at Constant Speed	f_{CUTOFF} (kHz) (17)
0	0	12.3	No	17
5 (default)	40	12.5	Yes	12
6	80	13	Yes	5.8
7	160	13.5	Yes	2.7
8	320	14	Yes	1.3
9	640	14.3	Yes	0.63
10	1280	14.6	Yes	0.31
11	2560	14.8	Yes	0.15
12	5120	15	Yes	0.075

Note:

12) f_{CUTOFF} is defined as -3dB frequency on the spectrum.

The cutoff frequency is 17kHz when FW = 0. With this setting, the digital filter and latency cancellation are disabled.

See the Typical Characteristics section on page 9 for more details on the spectrum and phase for different FW settings.

To accurately model the system and analyze the control loop stability, the front-end signal's transfer function (H_{FE}) can be calculated with Equation (2):

$$H_{FE} = \frac{1}{(1+\tau_{FE}s)^2} \quad (2)$$

The digital filter's transfer function (H_{FILTER}) can be calculated with Equation (3):

$$H_{FILTER} = \frac{1+(2+\delta)\tau s}{(1+\tau s)^2} \quad (3)$$

The sensor's transfer function (H) can then be calculated with Equation (4):

$$H = H_{FE} \times H_{FILTER} \quad (4)$$

If τ_{FE} = 5.3μs, $\delta = \frac{L}{\tau}$, the time constant (τ) can be determined based on Table 12, L is given in General Characteristics section on page 6.

Figure 26 shows a simplified block diagram of the transfer function of the system.

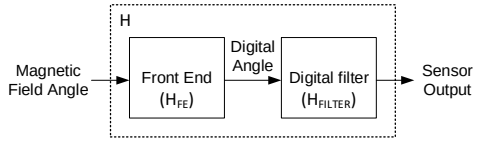


Figure 26: Simplified Block Diagram

Zero Setting

The zero position (a_0) of the MA600 can be configured with 16 bits of resolution. The angle outputted by the MA600 (a_{OUT}) can be calculated by Equation (5):

$$a_{OUT} = a_{RAW} - a_0 \quad (5)$$

Where a_{RAW} is the raw angle provided by the MagAlpha front end.

The Z[15:0] parameter is zero by default and is the zero-angle position. a_0 can be calculated in decimals with Equation (6):

$$a_0 = \frac{Z[15:0]}{2^{16}} \times 360 \quad (6)$$

Table 13 shows the zero setting parameter.

Table 13: Zero Setting Parameter

Z[15:0]	Zero Position a_0 (deg)
0	0
1	0.005
2	0.011
…	…
65534	359.989
65535	359.995

Zero Position Example

To set the zero position to 20 degrees, the Z[15:0] parameter can be calculated with Equation (7):

$$Z[15:0] = \frac{20°}{360°} \times 2^{16} = 3641 \quad (7)$$

In binary, it is written as 0000 1110 0011 1001.

Rotation Direction

By default, when looking at the top of the package, the angle increases when the magnetic

field rotates clockwise (CW) (see Figure 27 on page 29).

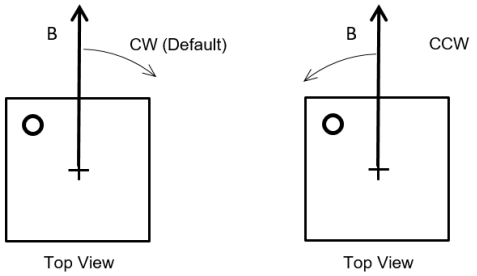


Figure 27: Positive Rotation Direction of the Magnetic Field

Table 14 shows the rotation direction parameter.

Table 14: Rotation Direction Parameter

RD	Positive Direction
0	Clockwise (CW)
1	Counterclockwise (CCW)

BIAS CURRENT TRIMMING (BCT) Settings

Side-Shaft

When the MA600 is mounted on the side of the magnet, the relation between the field angle and the mechanical angle is no longer directly linear. This effect is related to the fact that the tangential magnetic field is usually smaller than the radial field. Calculate the field ratio (k) with Equation (8):

$$k = \frac{B_{RAD}}{B_{TAN}} \quad (8)$$

Where B_{RAD} is the maximum radial magnetic field, and B_{TAN} is the maximum tangential magnetic field (see Figure 28).

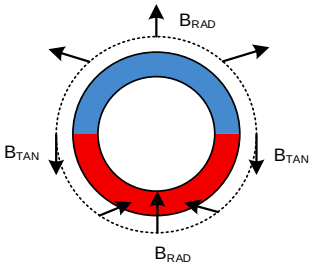


Figure 28: Side-Shaft Field

The *k* ratio depends on the magnet geometry and distance to the sensor. If the *k* ratio does not equal 1, the sensor output response is nonlinear with respect to the mechanical angle. The error curve has the shape of a double sinewave (see Figure 30). E is the amplitude of this error.

The bias current of the X or Y TMR bridge can be reduced to recover linearity. The direction in which the bias current is reduced corresponds to the direction where the field amplitude is the largest. The ETX and ETY parameters control this direction. The current reduction is set by the bias current trimming parameter (BCT[7:0]), which is an integer from 0 to 255. If BCT > 200, the compensation result can be affected by the temperature.

In side-shaft configuration (when the sensor's center is located beyond the magnet's outer diameter), the *k* ratio exceeds 1. For optimal compensation, the radial axis current should be reduced by setting BCT[7:0], which can be calculated with Equation (9):

$$BCT[7:0] = 258 \times \left(1-\frac{1}{k}\right) \quad (9)$$

Equation (9) is plotted in Figure 29 and Table 15.

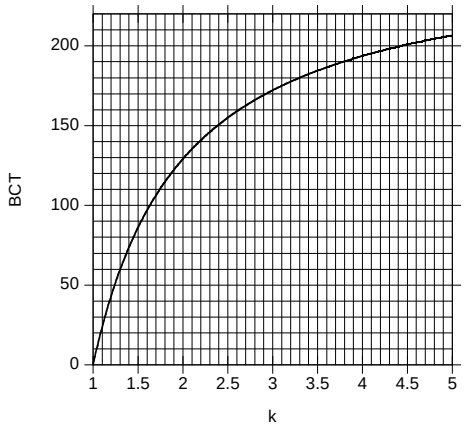


Figure 29: Relation Between the *k* Ratio and the Optimal BCT to Recover Linearity

Table 15: Example of BCT Settings

E (deg)	Magnet Ratio (*k*)	BCT[7:0]
0	1	0
11.5	1.5	86
19.5	2	129
25.4	2.5	155
30.0	3	172
33.7	3.5	184
36.9	4	194
39.5	4.5	201
41.8	5	207

Determining *k*

It is possible to deduce the k ratio from the error curve obtained with the default BCT setting (BCT = 0). Rotate the magnet one revolution and record the MA600's output.

Next, plot the error curve (the MA600's output minus the real mechanical position vs. the real mechanical position) and extract two parameters: the maximum error (E), and the position of the maximum with respect to a zero crossing (a_M) (see Figure 30). The *k* ratio can be calculated with Equation (10):

$$k = \frac{\tan(E + a_m)}{\tan(a_m)} \quad (10)$$

Figure 30 shows the error curve.

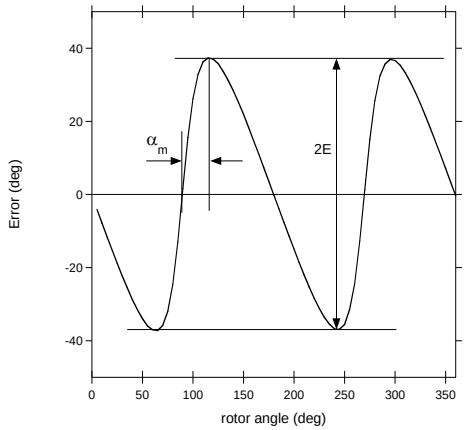


Figure 30: Error Curve in Side-Shaft Configuration with BCT = 0

Table 15 on page 29 shows examples of BCT settings. Alternatively, the *k* parameter can be obtained using Figure 31.

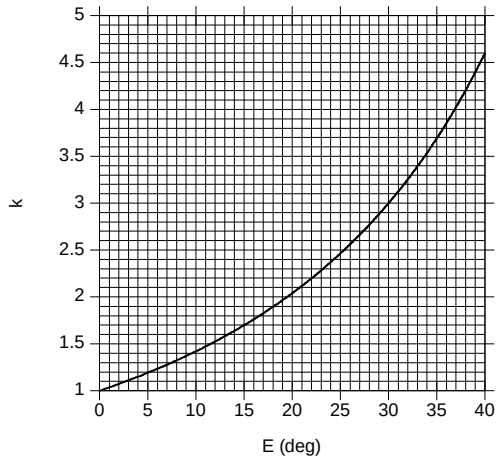


Figure 31: Relationship between the Error Measured with BCT = 0 and the Magnet Ratio *k*

Sensor Orientation

The dot marked on the package indicates whether the radial field is aligned with the sensor coordinate X or Y (see Figure 32).

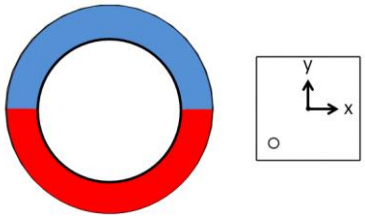


Figure 32: Package Top View with X- and Y-Axes

Determine which axis should be reduced based on the qualitative field distribution around a ring (see Figure 28 on page 29).

For example, Figure 28 shows that the field along the sensor's Y direction is tangential and weaker. This means that the X-axis should be reduced (ETX = 1 and ETY = 0).

If both ETX and ETY are set to 1, the current bias is reduced in both directions the same way (e.g. the linearity is the same as BCT = 0).

Table 16: Trimming Direction Parameters

ETX	Enable Trimming of the X-Axis
0	Disabled
1	Enabled
ETY	**Enable Trimming of the Y-Axis**
0	Disabled
1	Enabled

Factory Output Linearization

The sensor is factory-calibrated with the precision (see the General Characteristics section on page 6) at the nominal magnetic field and room temperature.

User Output Calibration

The MA600 features a lookup table for in-system calibration. This enables the sensor to compensate for any residual errors such as the error induced by the magnetic configuration (misalignments and magnet defaults). The user calibration consists of storing error values in the NVM for 32 equidistant positions of the MagAlpha output, which is referred to as out_i (the error when the uncorrected MagAlpha output is 0°, 11.25°, 22.5°, etc., where i = 0,…,31).

During operation, the sensor makes a linear interpolation using the two out_I surrounding the present output to determine the correct compensation to apply (see Figure 33).

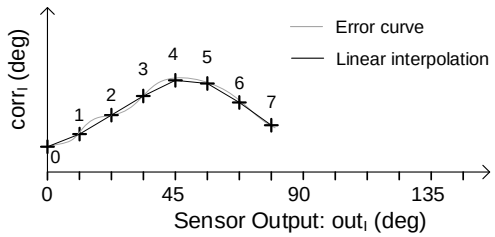


Figure 33: Linear Interpolation for On-Chip Calibration

Figure 34 shows an example comparing error before and after calibration.

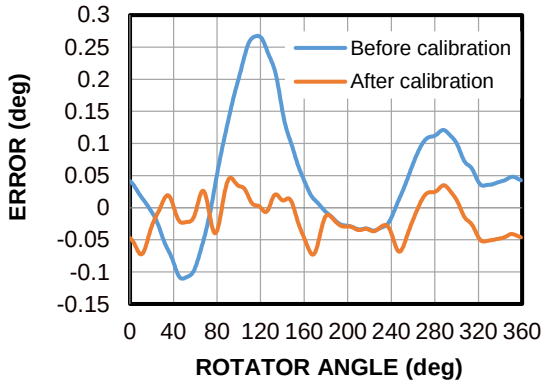


Figure 34: Error Before and After Calibration

The out_I values refer to the sensor output with the default zero setting, not the user-configured zero setting. Therefore, calibration should be performed prior to zero setting.

The 32 correction values ($corr_I$ (deg)) can be experimentally determined with Equation (11):

$$corr_I(deg) = ref_I(deg) - out_I(deg) \quad (11)$$

Where ref_I (deg) is the real mechanical angle in degrees. For example, ref_I (deg) can be delivered by a precise encoder. out_I (deg) is the MA600's output in degrees.

The user then stores the 32 collected values into block 1 (register 32 to register 63), which is reserved for calibration. The correction values are coded on 8 bits and range from -11.25º to +11.25º. The format is in signed integers.

If $corr_I$ (deg) ≥ 0, $corr_I$ (dec) can be calculated with Equation (12):

$$corr_I(dec) = \frac{corr_I(deg)}{360} \times 128 \times 32 \quad (12)$$

If $corr_I$ (deg) < 0, $corr_I$ (dec) can be calculated with Equation (13):

$$corr_I(dec) = \frac{corr_I(deg)}{360} \times 128 \times 32 + 256 \quad (13)$$

Calibration Example

Before starting the calibration, register 32 to register 63 must be set to 0x00. As the first step, the 32 correction values are measured and calculated. Table 17 shows the correction values.

Table 17: Calibration Table Example

#	out_I (deg)	$corr_I$ (deg)	$corr_I$ (dec)
0	0	0.45	5
1	11.25	0.33	4
2	22.5	0.12	1
3	33.75	-0.07	255
…	…	…	…
31	348.75	0.53	6

Then store $corr_I$ (dec) into the NVM on block 1.

In-system calibration can also be done without a reference encoder, with a magnet rotating at constant speed. The maximum recommended magnet speed is 5krpm. The calibration flow is described below:

- To fit the error curve accurately, calculate the 1st, 2nd, 4th, and 8th harmonics of the error curve as a function of the MA600 output
- At every 11.25°, calculate $corr_I$ (deg) using the fitting curve and convert the 32 obtained values from degrees to decimal
- Store the 32 $corr_I$ (dec) values into the NVM

In principle, user digital calibration can be used instead of BCT adjustment for side-shaft configuration. When the *k* ratio is large though, the 11.25° range of the digital calibration is not sufficient, and BCT adjustment should be done first.

If multiple settings are used, the settings should be configured in the following order:

1. BCT setting
2. User calibration
3. Zero setting

Functional Test

The functional test verifies the integrity of the sensor signal treatment. When setting FTM to 1, the signal from the TMR front end is replaced by a predetermined reference signal. The system reverts to normal operation as soon as FTM is set back to 0.

With the FTA bits, the reference signal can be virtually rotated by 90-degree steps (see Table 18).

Table 18: Functional Test Mode

FTM	FTA[1:0]	Angle Output (deg)
1	00	0
1	01	90
1	10	180
1	11	270

ABZ Incremental Encoder Output

The MA600's ABZ output emulates an incremental encoder (e.g. an optical encoder) to provide logic pulses in quadrature (see Figure 35). Compared to signal A, signal B is shifted by a quarter of the pulse period.

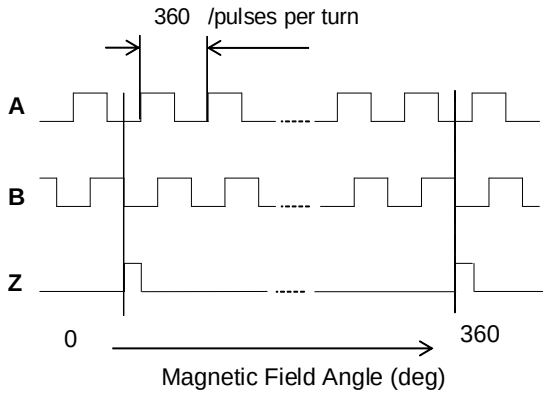


Figure 35: ABZ Output Timing

Across one revolution, signal A pulses n times, where n is configurable between 1 pulse and 4096 pulses per revolution. The number of pulses per channel per revolution is configured by setting the parameter PPT, which consists of 12 bits split between register 4 and register 5 (see Table 9 on page 24). The factory default is 512 pulses per turn. Table 19 shows how to configure PPT[11:0] to set the required resolution.

Table 19: PPT

PPT[11:0]	Pulses per Turn	Edges per Turn	
0000 0000 0000	1	4	Min
0000 0000 0001	2	8	
0000 0000 0010	3	12	
0000 0000 0011	4	16	
…	…	…	…
0111 1111 1110	2047	8188	
0111 1111 1111	2048	8192	
…	…	…	…
1111 1111 1101	4094	16376	
1111 1111 1110	4095	16380	
1111 1111 1111	4096	16384	Max

For example, to set 120 pulses per revolution (480 edges), set PPT to 120 - 1 = 119 (binary: 0000 0111 0111). Table 20 shows the required settings for register 4 and register 5.

Table 20: Register 4 and Register 5

Reg	B7	B6	B5	B4	B3	B2	B1	B0
4	1	1	1	0	0	0	0	0
5	0	0	0	0	1	1	1	0

Signal Z (zero or index) is raised only once per turn at the zero-angle position. The Z pulse's position and length is configurable via ILIP[3:0] in register 5 (see Figure 36).

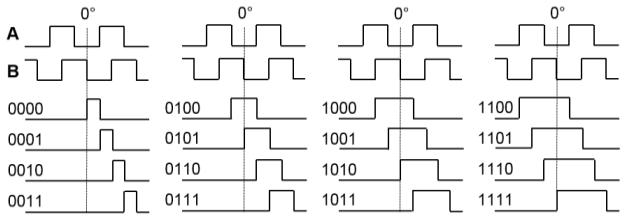


Figure 36: ILIP Parameter Effect on Index Shape

By default, the ILIP parameter is 0000. The index rising edge is aligned with the channel B falling edge, and the index length is half of the A or B pulse length.

ABZ Hysteresis

The hysteresis is set by the parameter HYS. The hysteresis (H) in degrees can be calculated with Equation (14):

$$H\,(\text{deg}) = 2.8 \times \frac{HYS}{256} \qquad (14)$$

Table 21 shows the HYS configuration.

Table 21: HYS

HYS[7:0]	H (deg)
00000000	0
00000001	0.011
00000010	0.022
…	…
11111110	2.778
11111111	2.789

Figure 37 shows the incremental output hysteresis.

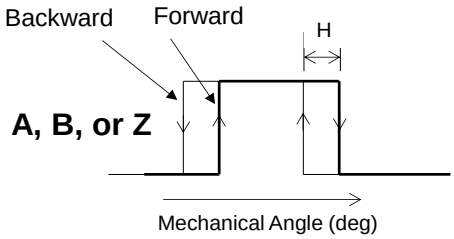


Figure 37: Incremental Output Hysteresis

Table 22 shows the recommended settings of HYS and hysteresis to avoid spurious transitions.

Table 22: Recommended Settings of HYS

FW	Resolution (Bit)	HYS[7:0] (decimal)	Hysteresis (deg)
0	12.3	22	0.24
5 (default)	12.5	16	0.18
6	13	11	0.12
7	13.5	7	0.08
8	14	5	0.05
9	14.3	4	0.04
10	14.6	3	0.03
11	14.8	3	0.03
12	15.0	3	0.03

DAZ Interface

For angular speed-related applications, the ABZ interface can be converted to DAZ (where D is the direction, A is the pulsing signal, and Z is the index) by configuring the DAZ bit to 1.

In this configuration, the D signal indicates CW (logic 0) or CCW (logic 1) magnetic field rotation. The A and Z signals remain unchanged compared to the ABZ interface.

UVW Incremental Encoder Output

The UVW output emulates the three Hall switches that are typically used for the block commutation of a 3-phase brushless motor. The three logic signals have a duty cycle of 50% and are shifted by 60° relative to each other (see Figure 38).

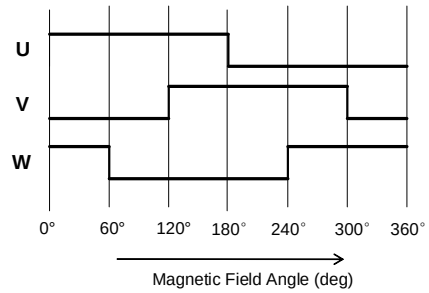


Figure 38: UVW Output for 1 Pole Pair Rotor during Rotation

If the number of the rotor's pole pairs exceeds the number of pole pairs of the target magnet, then the MA600 generates more than one UVW cycle per revolution by dividing the digital angle into the required number of commutation steps per 360-degree revolution. The NPP[2:0] parameter sets the number of emulated pole pairs and the corresponding commutation step angle for the UVW signals.

Table 23 shows the rotor pole pair options.

Table 23: Number of UVW Pair Poles

NPP[2:0]	Pole Pairs	States per Revolution	State Width (deg)
000	1	6	60
001	2	12	30
010	3	18	20
011	4	24	15
100	5	30	12
101	6	36	10
110	7	42	8.6
111	8	48	7.5

Figure 39 shows an example of the 30º UVW commutation signal spacing for a 4-pole (2-pole pair) motor.

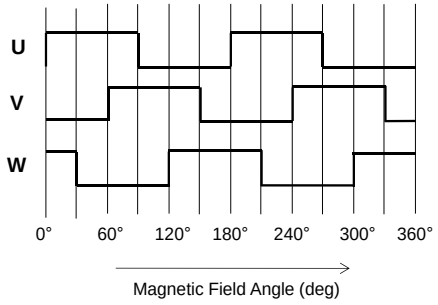


Figure 39: UVW Commutation Signals for a 4-Pole (2-Pole Pair) Motor

UVW Hysteresis

A hysteresis larger than the output noise is introduced on the UVW output to avoid any spurious transitions (see Figure 40).

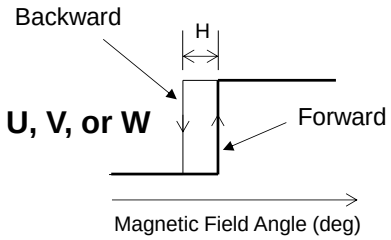


Figure 40: Hysteresis of the UVW Signal PWM

The UVW hysteresis is also set by HYS and is subject to the same recommendations (see Table 21 on page 33).

Absolute Output

This output provides a logic signal with a duty cycle corresponding to the magnetic field angle.

The signal frame consists of four different segments:

- Start band (always high)
- Error
- Data
- End band (always low)

Figure 41 shows one period of the PWM signal.

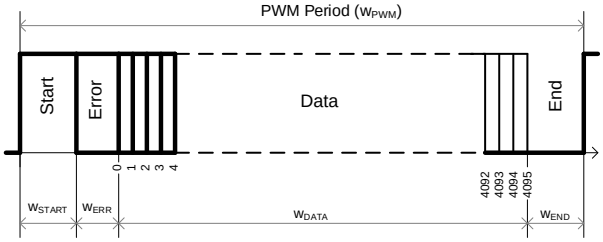


Figure 41: PWM Frame Composed of Four Bands (Start, Error, Data, End)

To display errors in the PWM frame, enable the PWMM parameter. In normal conditions the error band (w_{ERR}) is 1.

w_{ERR} is 0 if one of the following flags is raised to 1:

- ERRCRC
- ERRMEM
- ERRPAR

If PWMM is enabled and an error is detected, then the data remains zero.

The frequency can be selected with the PWMF. parameter. Table 24 shows the PWM frequency selection.

Table 24: PWM Frequency Selection

PWMF	PWM Frequency
0	250Hz
1	1kHz

The PWM total period (t_{PWM}) is the inverse of the PWM frequency. The PWM frequency can deviate from the values given in Table 24 by a tolerance (see the General Characteristics section on page 6).

Table 5 shows the PWM time durations in counts.

Table 25: PWM Time Durations in Counts

PWMM	PWMF	WPWM	WSTART	WERR	WDATA	WEND
0	0	4119	16	0	4095	8
0	1	4119	16	0	4095	8
1	0	4119	12	4	4095	8
1	1	4119	12	4	4095	8

Speed Output and Calculation

When MTSP in register 28 is set to 1, the user can obtain the 16-bit speed output from SPI communication (see the SPI Read Multi-Turn/Speed section on page 16).

The speed is transmitted as a signed 16-bit number using two's complement representation. When calculating the signed decimal value, the user must multiply the MSB of the 16-bit speed value by -1 instead of 1.

The speed scale is 5.722rpm/LSB, which is based on a 100kHz inner clock. Therefore, the measured speed range is from -187498rpm to +187492rpm (see Table 26).

Table 26: Speed Conversion

16-bit Signed Value	Signed Decimal Value	Speed (rpm)
0000 0000 0000 0000	0	0
0000 0000 0000 0001	1	+5.722
1111 1111 1111 1111	-1	-5.722
1000 0000 0000 0000	-32768	-187498.496
0111 1111 1111 1111	32767	+187492.774

Speed Output Example

If the readback 16-bit signed speed value is 1110 0100 1110 1010, then the decimal value can be calculated with Equation (15):

$$\begin{aligned} \text{Decimal} &= (-1) \times 2^{15} + 1 \times 2^{14} + 1 \times 2^{13} + 1 \times 2^{10} + 1 \times 2^{7} \\ &\quad + 1 \times 2^{6} + 1 \times 2^{5} + 1 \times 2^{3} + 1 \times 2^{1} \\ &= -6934 \end{aligned} \quad (15)$$

The corresponding speed can be calculated with Equation (16):

$$\begin{aligned} \text{Speed} &= 5.722 \times (-6934) \\ &= -39676.348(\text{rpm}) \end{aligned} \quad (16)$$

Table 27 shows the speed output's resolution, time constant, and cutoff frequency.

Table 27: Speed Output Typical Parameters

Resolution at 5krpm (Bits)	Time Constant (τ) (µs)	Cutoff Frequency (Hz)
9.5	320	500

If the user wants to monitor the clock frequency and achieve a more precise speed calculation, the clock related to S_{SPEED} is available on CK100 by setting register 14, bit[0] to 1.

The relationship between S_{SPEED} and the CK100 frequency can be calculated with Equation (17):

$$S_{SPEED}(\text{rpm/LSB}) = 5.722 \times \frac{f_{CK100}(\text{kHz})}{100(\text{kHz})} \quad (17)$$

Multi-Turn Output

If MTSP in register 28 is set to 0 (default setting), the user can obtain the 16-bit multi-turn output from SPI communication (see the SPI Read Multi-Turn/Speed section on page 16).

When the angle detected by the MA600 passes the zero position in a positive direction (CW), the multi-turn count increases by 1; when the detected angle passes the zero position in a negative direction (CCW), the multi-turn count decreases by 1.

It is possible to set a multi-turn offset by configuring MTOFFSET[15:0] in register 18 and register 19. The multi-turn count (MT) returned by the sensor is computed by adding this offset value to the measured multi-turn (MT_{MEAS}).

MT can be calculated with Equation (18):

$$MT = MT_{MEAS} + MTOFFSET \quad (18)$$

MT_{MEAS} and MTOFFSET is set to 0 at system start-up. Consider that the MTOFFSET setting cannot be stored to the NVM. The user must set MTOFFSET after each start-up event if the offset is required.

Multi-turn is a signed 16-bit value. The user must multiply the MSB of the 16-bit multi-turn value by -1 instead of 1 (see Equation (15)).

The measured multi-turn range is from -32768 to 32767 (see Table 28).

Table 28: Multi-Turn Conversion

16-Bit Signed Value	Signed Multi-Turn Decimal Value
0000 0000 0000 0000	0
0000 0000 0000 0001	1
1111 1111 1111 1111	-1
1000 0000 0000 0000	-32768
0111 1111 1111 1111	32767

Status Byte

Register 26 contains one status bit (NVMB) and three error bits (ERRPAR, ERRMEM, and ERRCRC) that trigger a flag when some errors are detected. These bits can be cleared by sending the Clear Error Flags command.

NVMB

When the Store a Single Register Block to the NVM command or the Restore All Register Blocks from the NVM command is sent to the MA600, the NVM is busy until the operation is executed. During this busy period, the NVMB status bit is temporarily set to 1 and then reset back to 0 after the operation is executed.

ERRMEM

If a command triggers NVM access (store or restore) while the NWM is busy, it is ignored and the ERRMEM bit is set to 1.

ERRPAR

When parity check is enabled by PRT, the controller must send a parity bit on the COPI line after the 16-bit command.

The MA600 checks the parity of this 17-bit long frame. If a parity error occurs, the command is discarded and the ERRPAR bit is set to 1. The angle data return in the next frame.

When parity check is enabled, if the user only sends a 16-bit command, ERRPAR does not assert and the command is discarded.

ERRCRC

The restoration of register values from the NVM is secured by a CRC algorithm. A mismatch between the generated CRC result with the previously stored value is flagged by the ERRNVM bit being asserted (set to 1).

I/O Matrix

The I/O output of the digital I/O pins (IO1 to IO6) can be set by INTF_SEL[2:0] (see Table 29).

Table 29: IO Matrix

INTF_SEL[2:0]	IO6	IO1	IO5	IO2	IO4	IO3
000 (default)	U	V	W	A	B	Z
001	U	V	W	SSD	SSCK	PWM
010	SSCK	SSD	PWM	A	B	Z
011	U	V	W	/V	/U	/W
100	/B	/A	/Z	A	B	Z
101	U	V	W	-	-	-
110	-	-	-	A	B	Z
111	SSCK	SSD	PWM	-	-	-

Digital I/O Pin Circuit

The digital I/O pins (IO1 to IO6) are set to push-pull by default and can be changed to open drain to allow I/O voltages different than V_{DD} (up to 5.5V). If the I/O pin is set as SSCK by INTF_SEL, it is affected by neither OD615 nor OD243.

Table 30 shows the internal circuit of the IO6, IO1, IO5 pins.

Table 30: IO6, IO1, IO5 Pin Internal Circuit

OD615	Internal Circuit
0 (default)	Push-pull
1	Open drain

Table 31 shows the internal circuit of the IO2, IO4, and IO3 pins.

Table 31: IO2, IO4, IO3 Pin Internal Circuit

OD243	Internal Circuit
0 (default)	Push-pull
1	Open drain

Figure 42 shows the internal circuits of IO1 to IO6.

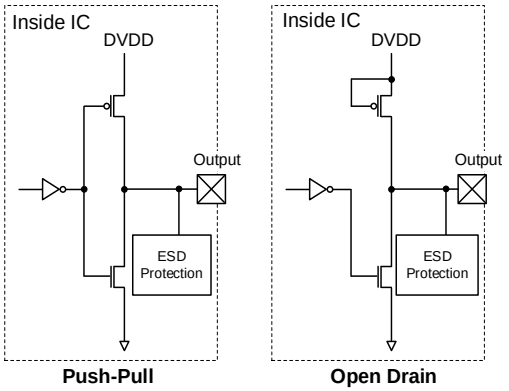


Figure 42: Output Circuits Inside IC for IO1 to IO6

The SPI input pins (/CS, SCLK, and COPI) are configured as pull-up or pull-down by default.

If required, the SPI inputs can be set to high impedance by the SPULLIN parameter (see Table 32 on page 37). When the internal pin impedance is high, it is recommended to pull SCLK and COPI to GND externally, and pull /CS to DVDD to prevent any voltage buildup and inadvertent configuration when the SPI interface is idle (e.g. high /CS).

Table 32: SPI Input Pin Circuit

SPULLIN	SPI Input Pins	
	/CS	SCLK, COPI
0	Hi-Z	Hi-Z
1 (default)	Pull-up	Pull-down

Figure 43 shows the inside circuit of the SPI inputs.

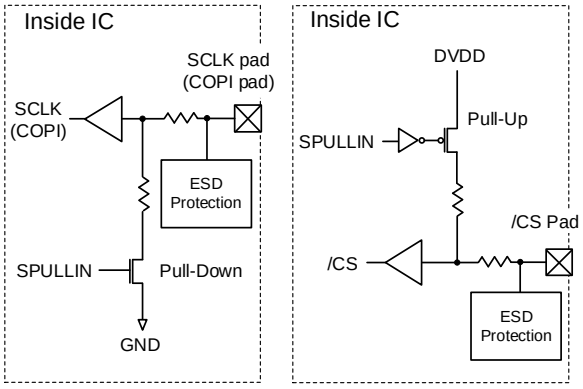


Figure 43: Circuit of SPI Input Pins in the IC

The SPI output pin (CIPO) is configured as push-pull when the SPI is active. CIPO is configured as pull-down by default when the SPI interface is idle. CIPO can be configured to a high-impedance (Hi-Z) state when the SPI is idle via TRISTATE (see Table 33).

Table 33: SPI Output Pin Circuit

TRISTATE	SPI Output Pin
	CIPO
0 (default)	Pull-down when idle
1	Hi-Z when idle

This configuration allows connecting multiple devices on the same bus. Figure 44 shows the CIPO pin's internal circuit.

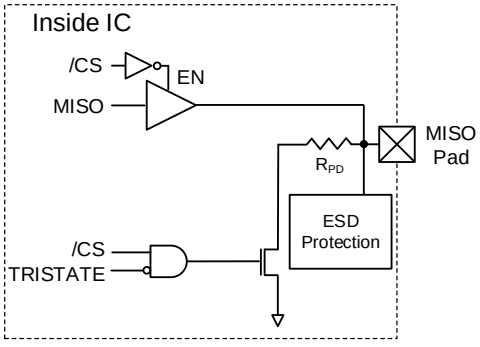


Figure 44: CIPO Pin Circuit in the IC

Special Interfaces

The MA600 supports special interfaces such as reduced wiring mode and daisy chain, which provide more flexibility to communicate with the controller.

DAISY and RWM in register 10 can disable the SPI communication permanently. A security mechanism is built in to avoid accidental configuration of register 10.

The security mechanism process is described below:

- By default, register 10 is locked, meaning the RWM and DAISY parameters cannot be written
- To unlock register 10, the UR10 parameter in register 132 must be enabled
- RWM or DAISY mode are effective only when UR10 is reset to zero

To enable the RWM or DAISY for temporary testing purposes, follow the steps below:

1. Set UR10 to 1.
2. Set RWM or DAISY to 1.
3. Set UR10 to 0.

At this stage, RWM or DAISY mode is enabled. After shutting down and starting up, the MA600 returns to normal SPI mode.

To switch to RWM or DAISY permanently, follow the steps below:

1. Set UR10 to 1.
2. Set RWM or DAISY to 1.
3. Store register block 0 to the NVM.
4. Set UR10 to 0, or shut down and start up the MA600.

Reduced Wiring Mode

The MA600 supports reduced wiring mode by setting RWM to 1.

Reduced wiring mode enables the user to configure the chip during a set-up stage, and then transforms the SPI pin into outputs with other functionalities for normal operation to save three connections.

Table 34 shows the RWM and redirection of pin functionality.

Table 34: RWM and Redirection of Pin Functionality

RWM	Pin 4	Pin 5	Pin 7	Pin 12
0 (default)	COPI	/CS	CIPO	SCLK
1	IO3	IO4	CIPO	IO2

For example, if only the ABZ output is required, the user can configure the ABZ-related parameters first via SPI communication, then redirect the ABZ signal to the SPI pins. In this case, no additional wiring is needed at IO2, IO3, and IO4. A similar process applies if only UVW, SSI, or PWM is required. The functionality of IO2 to IO4 is determined by INTF_SEL.

Daisy Chain

When connecting multiple sensors on the same bus, the daisy chain configuration enables saving the I/O pins. Daisy chain mode is enabled by setting DAISY to 1.

In this mode, the CIPO data output of each peripheral sensor is chained to the COPI data input of the next peripheral sensor. The CIPO data output of the last peripheral sensors is connected back to the controller's CIPO input (see Figure 45).

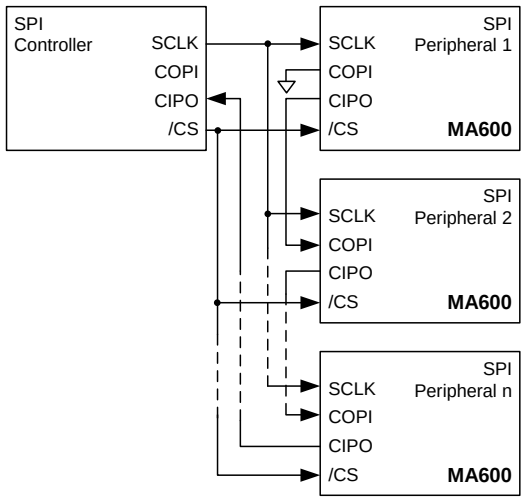


Figure 45: Daisy Chain Mode Configuration

In daisy chain mode, data can be only read. n x 16 clock counts are required, where n is the number of connected devices. The SPI bus chip select signal (/CS) should remain low during the n x 16 clock counts.

The first 16 bits are the angle data from the last peripheral (n) device in the chain, followed by the 16-bit angle data from the preceding (n - 1) device, and so on. Figure 46 shows an example of the SPI read angle for two daisy-chained MA600 devices.

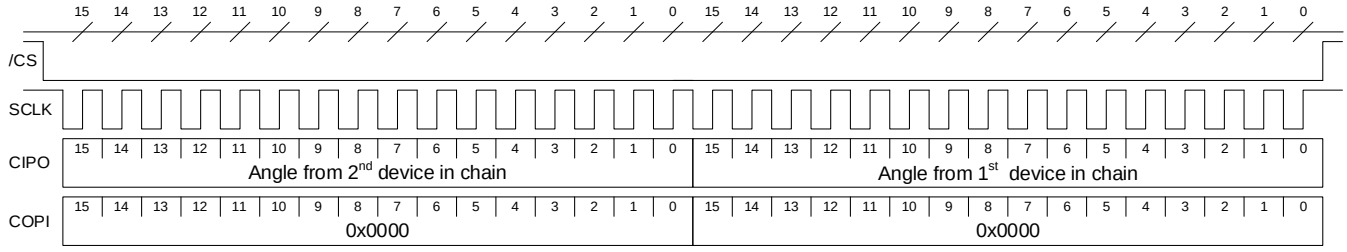


Figure 46: SPI Read Angle for Two Daisy0Chained MA600 Devices

TYPICAL APPLICATION CIRCUIT

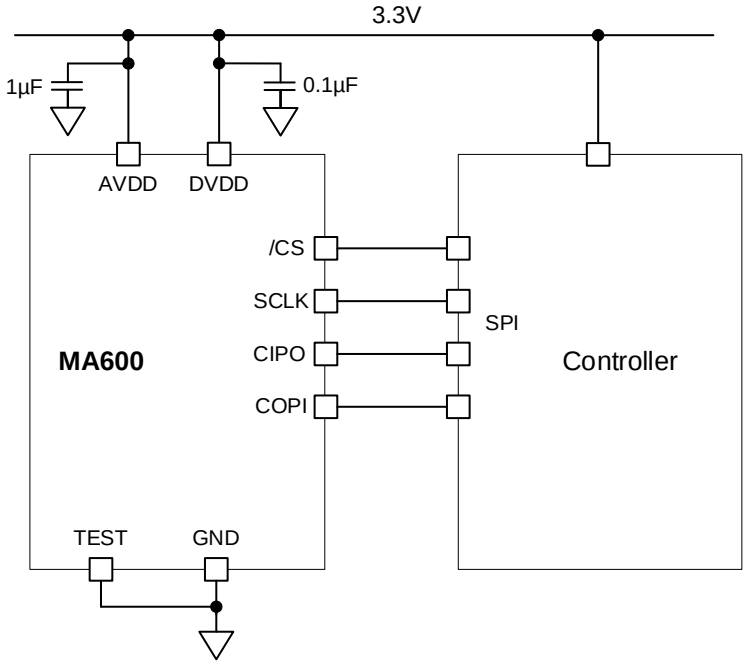
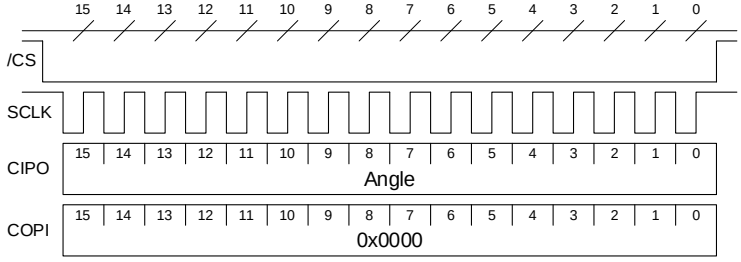


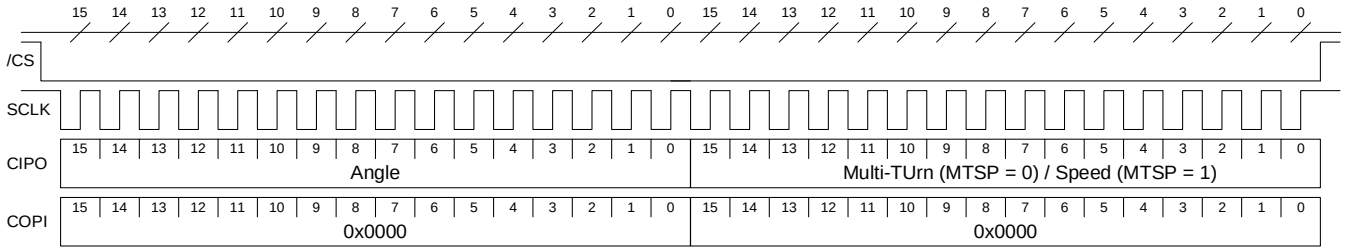
Figure 47: Typical Application Circuit (Configuration Using SPI Interface)

APPENDIX A: SPI COMMUNICATION CHEATSHEET

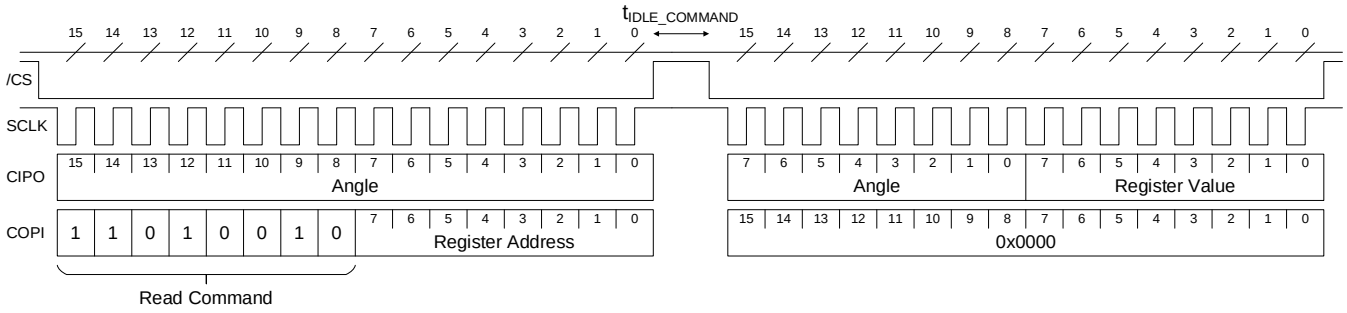
Read Angle (see the SPI Read Angle section on page 16)



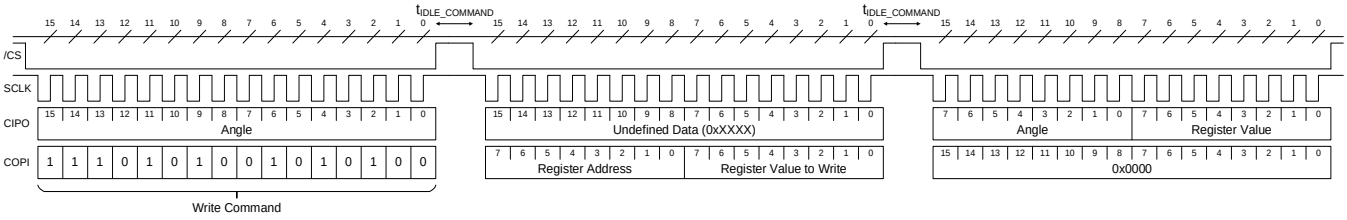
32-Bit Frame Read Multi-Turn/Speed Operation (see the SPI Read Multi-Turn/Speed section on page 16)



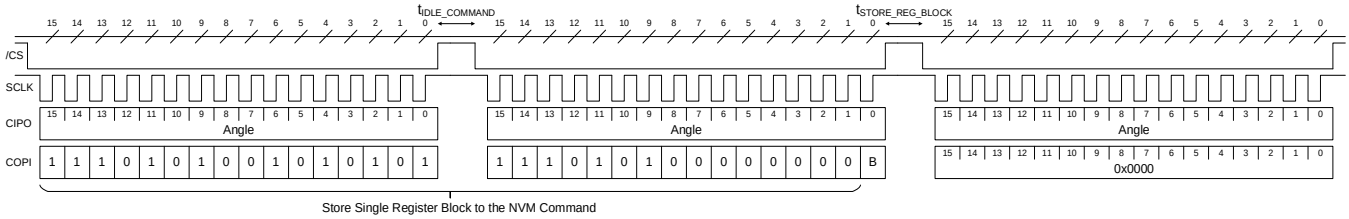
Read Register (see the SPI Read Register section on page 17)



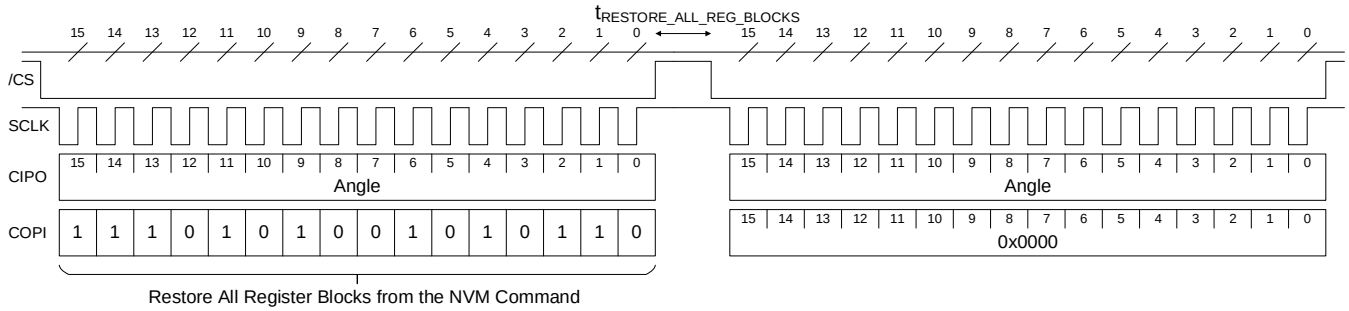
Write Register (see the SPI Write Register on page 17)



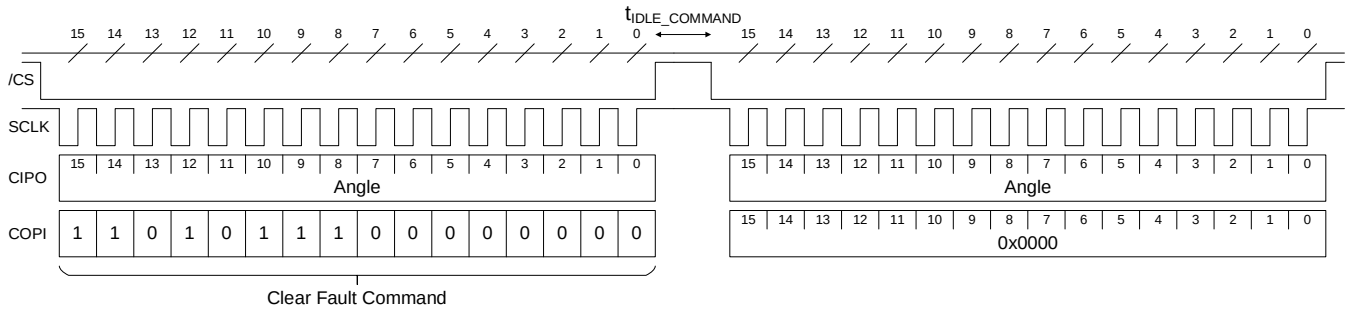
Store a Single Register Block to the NVM (see the SPI Store a Single Register Block to the NVM section on page 18)



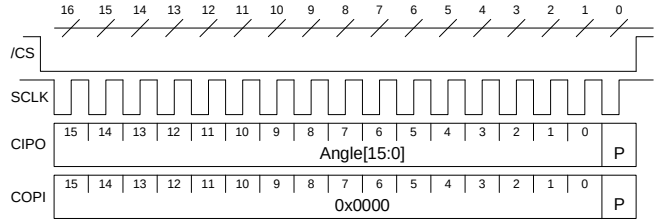
Restore All Register Blocks from the NVM (see the SPI Restore All Register Blocks from the NVM section on page 19)



Clear Error Flags (see the SPI Clear Error Flags section on page 19)

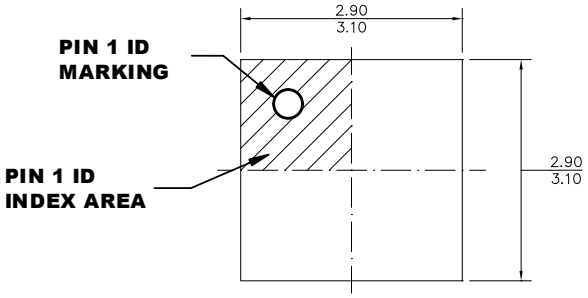


Read Angle When SPI Parity Check is Enabled (see the SPI Parity Check section on page 20)

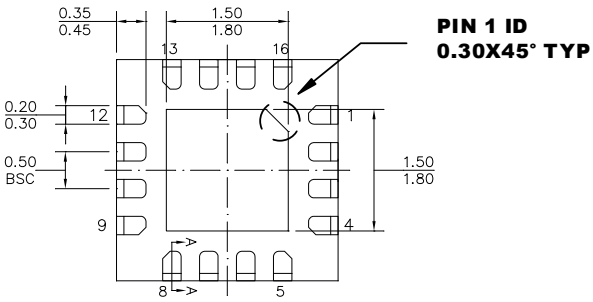


PACKAGE INFORMATION

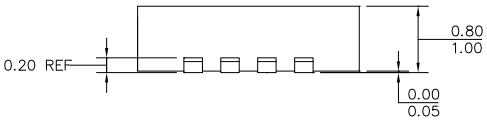
QFN-16 (3mmx3mm)
Wettable Flank



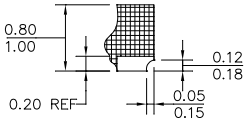
TOP VIEW



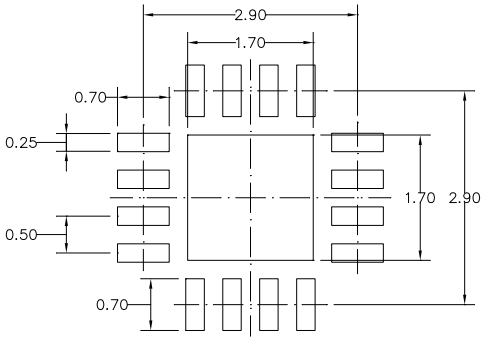
BOTTOM VIEW



SIDE VIEW



SECTION A-A

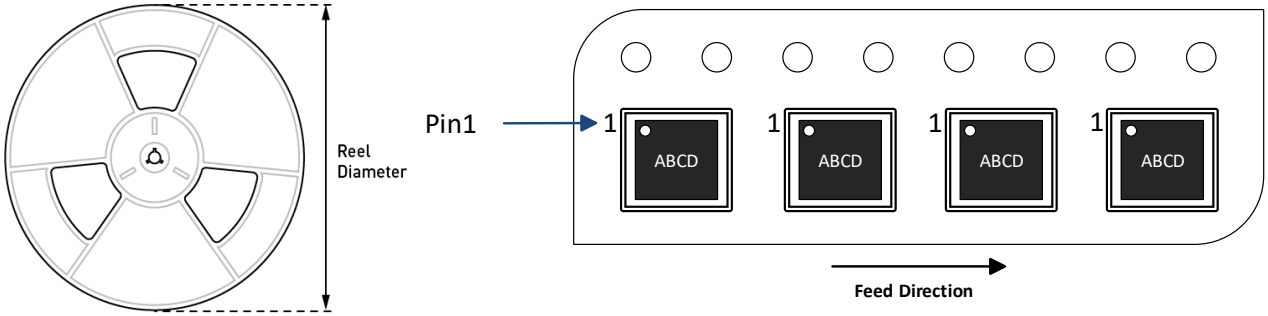


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MA600GQE-xxxx-Z	QFN-16 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	06/28/2023	Initial Release	-