eDSP™
Sensor Fusion Engine
MA60000

Datasheet

Rev. 1.0

Table of Contents

1 Overview

MegaChips' eDSP is a state-of-the-art sensor fusion engine developed to perform high-end arithmetic processing in real-time at a fraction of the power compared to most microcontrollers in the market today. The eDSP integrates a 32-bit programmable DSP core, 256K RAM for instruction, 256K RAM for data, and various peripherals and interfaces to enable a vast array of IoT sensor applications, capable of the most fundamental to computationally intensive programs. The DSP core "ParaForce" includes a 3-way VLIW (Very Long Instruction Word) and a 4-way floating point SIMD (processing multiple data with a single instruction). It can perform multi-way branching and conditional execution allowing programs to explicitly specify instructions to execute concurrently, and in parallel. This unique feature provides higher-performance, and lower power without the complexity inherent to other microprocessor based designs.

With the available software tools, the eDSP is ideal for developers who want to develop their own customized fusion algorithm from concept to production using the same platform reducing their time-to-market, and cost.

2 Applications

- PDR (Pedestrian Dead Reckoning)
- VDR (Vehicle Dead Reckoning)
- Gesture recognition
- Voice recognition
- Motion tracking
- Sports/fitness
- Context aware
- Self-learning

3 Block Diagram

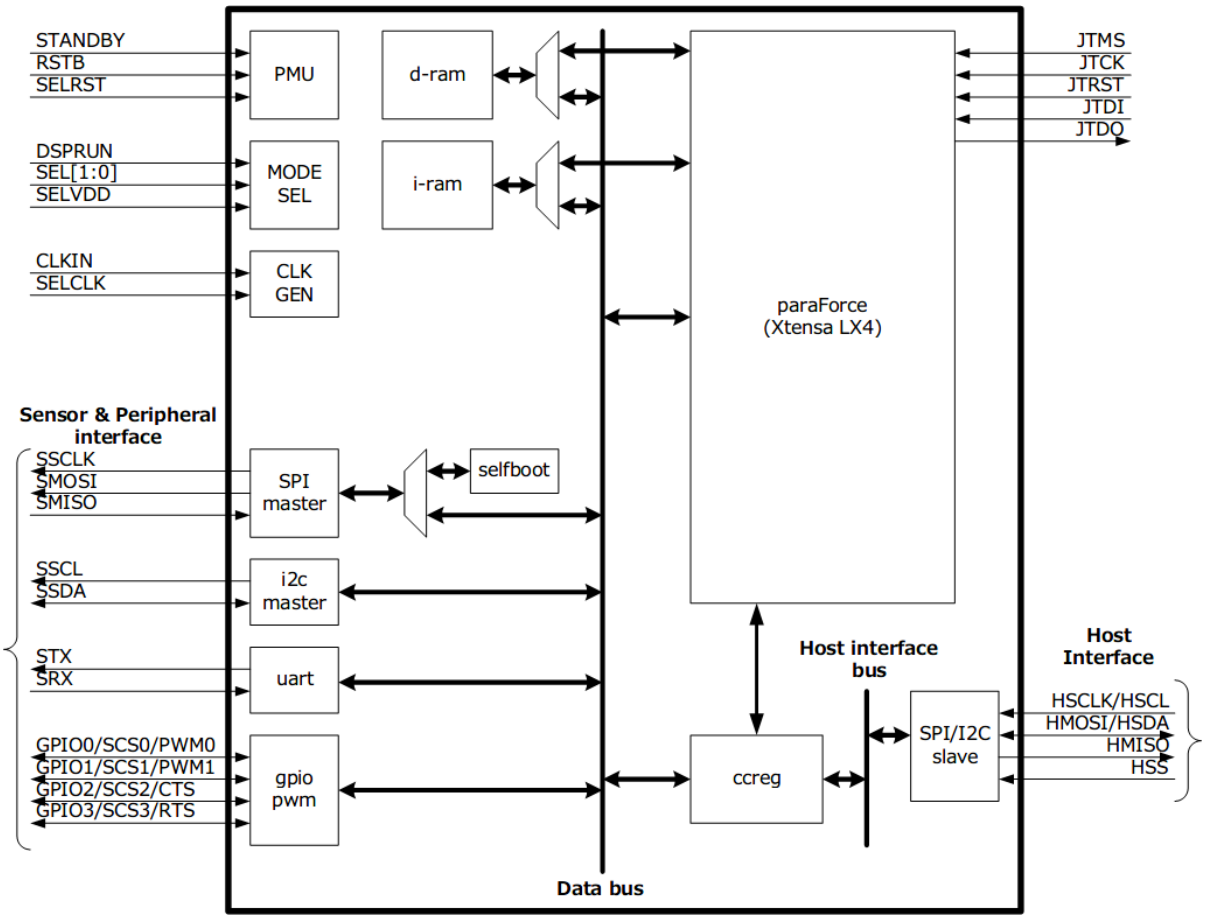


Figure 3-1 eDSP block Diagram

4 Specifications

Table 4-1 eDSP Specification[1]

Item		Spec	Notes
Power	Core	+1.2V +/-10%	
	IO	+1.8V +/-10% +3.3V +/-10%	IO: 1.8-3.3V is available
Package	Package shape	FBGA	
	Package size	3.5 x 3.5mm	
	Ball number	49	
	Ball pitch	0.4mm	
	Thickness	0.65mm	Max
System	Data RAM	256kbyte	
	Instruction RAM	256kbyte	
	Clock input method	External x1Internal x2	
	External clock frequency	40MHz	Typ
	Internal clock frequency	・Slow:100kHz ・Fast :40MHz	
	Clock setting	- selected external or internal by SELCLK pin - selected internal frequency(slow or fast) by register	
	DSP	paraForce (Xtensa LX4)	・3way VLIW ・Floating Point 4way SIMD
	External interrupt	2ch	Alternative GPIO
Host interface	SPI (Slave)	Alternative	
	I2C (Slave)		
Sensor interface	SPI (Master)	1ch(4 chip select)	Chip selects are alternaive GPIO
	I2C (Master)	1ch	
General interface	UART	1ch	
	GPIO	4ch	
	PWM	2ch(resolution:2^16)	Alternative GPIO
Others	Ambient Operating Temp.	-20-85 degrees C	

[1] eDSP supports 1.8V to 3.3V I/O voltage, it is design assurance.

5 Pinout/Description

Table 5-1 Pinout Description

No	Area	Ball Name	Alt0(Default)			Alt1		Alt2		Pin state@Reset		Power
			Signal Name	Dir	Function	Dir	Function	Dir	Function			
1	System	STANDBY	STANDBY	I	Stanby mode set (0:Stanby mode 1:Normal)	-	-	-	-	I	(Hi-Z)	
2		DSPRUN	DSPRUN	I	DSP Run mode set(0:Run 1:Stall)					I	(Hi-Z)	
3		CLKIN	CLKIN	I	External Clock Input	-	-	-	-	I	(Hi-Z)	
4		SEL0	SEL0	I	Mode setting 0	-	-	-	-	I	(Hi-Z)	
5		SEL1	SEL1	I	Mode setting 1	-	-	-	-	I	(Hi-Z)	
6		SELCLK	SELCLK	I	Ext/Int Clock switch (0: internal, 1: external)	-	-	-	-	I	(Hi-Z)	
7		SELVDD	SELVDD	I	IO voltage select (0V : IO voltage=3.3V 1.8V : IO voltage=1.8V)	-	-	-	-	I	(Hi-Z)	
8		RSTB	RSTB	I	External Reset (0:Reset 1:Normal)	-	-	-	-	I	Pull-up	
9		SELRST	SELRST	I	Reset Signal Select (0:POR 1:External Reset)	-	-	-	-	I	Pull-down	
10	Host IF	HSCLK	HSCLK/HSCL	I	Host IF SPI Clock Input	I	Host IF I2C SCL Input	-	-	I	(Hi-Z)	
11		HMOSI	HMOSI/HSDA	I	Host IF SPI Data Input	I/O	Host IF I2C SDA signal	-	-	I	(Hi-Z)	
12		HMISO	HMISO	O	Host IF SPI Data Output	-	-	-	-	I	(Hi-Z)	
13		HSS	HSS	I	Host IF SPI Chip Select Input	-	-	-	-	I	(Hi-Z)	1.8～
14	Sensor	SSCLK	SSCLK	O	Sensor IF SPI Clock Output	-	-	-	-	O	(Hi-Z)	3.3V
15	IF	SMOSI	SMOSI	O	Sensor IF SPI Data Output	-	-	-	-	O	(Hi-Z)	
16		SMISO	SMISO	I	Sensor IF SPI Data Input	-	-	-	-	I	(Hi-Z)	
17		SSCL	SSCL	O	Sensor IF I2C SCL Output	-	-	-	-	I	(Hi-Z)	
18		SSDA	SSDA	I/O	Sensor IF I2C SDA Signal	-	-	-	-	I	(Hi-Z)	
19	UART	STX	STX	O	UART Data Output	-	-	-	-	O	(Hi-Z)	
20		SRX	SRX	I	UART Data Input	-	-	-	-	I	(Hi-Z)	
21	GPIO/PWM	GPIO0	GPIO0/SCS0/PWM0	I/O	GPIO0(SelfBoot CS)	O	Sensor IF SPI Chip Select Output 0	O	PWM0	I	(Hi-Z)	
22		GPIO1	GPIO1/SCS1/PWM1	I/O	GPIO1	O	Sensor IF SPI Chip Select Output 1	O	PWM1	I	(Hi-Z)	
23		GPIO2	GPIO2/SCS2/CTS	I/O	GPIO2(Ext INT Input. Level Only)	O	Sensor IF SPI Chip Select Output 2	I	UART Master Transmission ACK	I	(Hi-Z)	
24		GPIO3	GPIO3/SCS3/RTS	I/O	GPIO3(Ext INT Input. Level Only)	O	Sensor IF SPI Chip Select Output 3	O	UART Master Transmission Request	I	(Hi-Z)	
25	JTAG	JTMS	JTMS	I	JTAG TMS	-	-	-	-	I	Pull-up	
26		JTCK	JTCK	I	JTAG TCK	-	-	-	-	I	Pull-down	
27		JTRST	JTRST	I	JTAG RST	-	-	-	-	I	Pull-up	
28		JTDI	JTDI	I	JTAG Data Input	-	-	-	-	I	Pull-up	
29		JTDO	JTDO	O	JTAG Data Output	-	-	-	-	O	Pull-up	

6 System Specifications and settings

6.1 Mode Settings

The device carries out operation mode settings by SEL[1:0] pins. Self-boot performs a boot process from external serial flash ROM. Host download boot is conducted from host device connected to host interface. Please refer to Table 6-1 for details.

Table 6-1 Settings of boot mode and host interface mode

Ball/Pad		Boot Modes
SEL0	SEL1	
L	L	Host download boot SPI Mode0
L	H	Host download boot SPI Mode3
H	L	Host download boot I2C
H	H	Self-Boot

6.2 Low Power Modes

The device support low power modes in order to reduce power consumption when ParaForce stops operating. Please refer to 6.7 Low Power Modes for details.

6.3 ParaForce Initial Settings

DSPRUN pin can set ParaForce initial settings after reset release. Generally, DSPRUN pin is set to "H" (Stall). When debugging by JTAG, DSPRUN pin is set to "L" (Run).

6.4 I/O Power Settings

The device I/O power can be selected from 1.8V I/O or 3.3V I/O by SELVDD pin. I/O power settings can apply to only one voltage, either 1.8V or 3.3V. When the device's I/O power is used at 1.8V, SELVDD pin is applied to 1.8V, and when 3.3V is used, SELVDD pin is applied to 0V.

6.5 Reset Specifications

eDSP has function (POR : Power On Reset) to internally generate reset signal. Therefore, the external reset forming circuit is unnecessary when you use POR.

6.5.1 POR (Power On Reset)

POR output waveform and characteristics is below Figure 6-1 and Table 6-2.

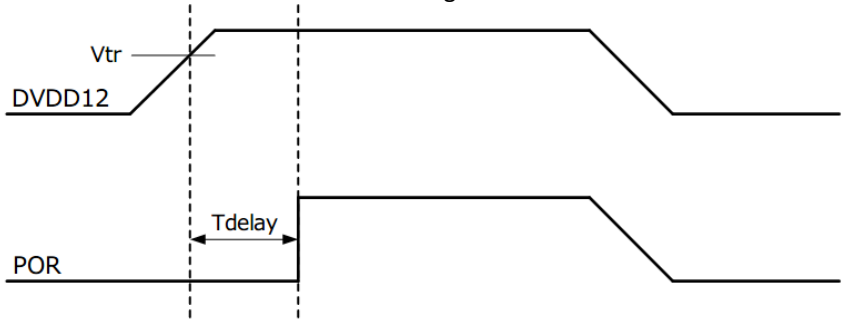


Figure 6-1 POR output waveform

Table 6-2 POR Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Condition
Reset Trigger Level	Vtr	0.4	0.6	1.0	V	1V/1s power up ratio
Reset Delay Time	Tdelay	20	40	1000	us	1V/1us power up ratio

- POR output: "L" is reset on, "H" is reset off.
- POR is available when DVDD12 rump-up time is between 1V/us and 1V/s.
- If DVDD12 is set 1.2V -> 0V -> 1.2V, DVDD12, 0V period has to be kept over 200ms as shown on Figure 6-2.

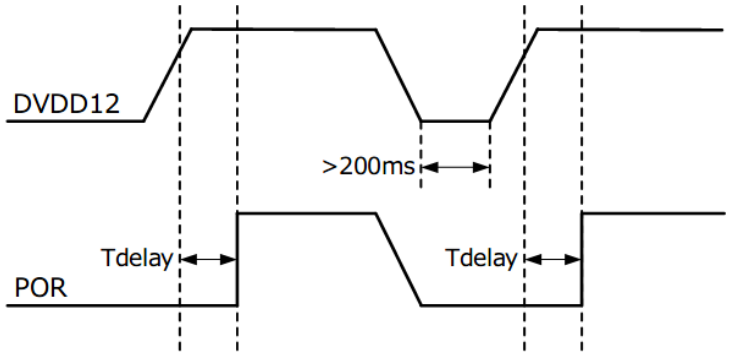


Figure 6-2 POR output waveform when DVDD12 sets OFF to ON

6.5.2 External Reset Input

It is possible to input the external reset input signal and use for eDSP reset control. To activate the external reset input, set SELRST pin to "H", and input control signal to RSTB pin. In this case, make RSTB pin logic so that "L" is reset on and "H" is reset off, same as specification of POR.

6.6 System Clock

The device has 3 clock sources that can select system clock. Specifications for 3 clock sources are as below.

- External input clock (Clock input at CLKIN pin)
- Internal slow clock (ROSC1 100kHz)
- Internal fast clock (ROSC2 40MHz)

Clock tree is shown on Figure 6-3.

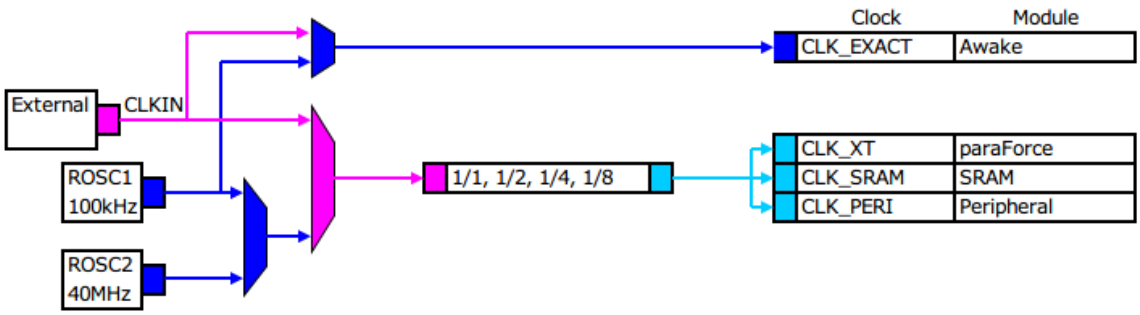


Figure 6-3 Clock tree

CLK_EXACT is for Awake timer. CLK_EXACT source can be selected by CLKIN or ROSC1. It requires CLKIN input to change CLK_EXACT source.

6.6.1 External Input Clock

This clock frequency is 40MHz (typ).

6.6.2 Internal Slow Clock (ROSC1)

ROSC1 Electrical Characteristics is shown on Table 6-3.

Table 6-3 ROSC1 Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Condition
Output frequency	F_{osc}	65	100	135	kHz	
Duty cycle	D	40	50	60	%	
Startup time when power on	T_{on1}		200		us	

ROSC1, 2 Startup waveform is shown on Figure 6-4. ROSC1 output is unstable during Ton1 period.

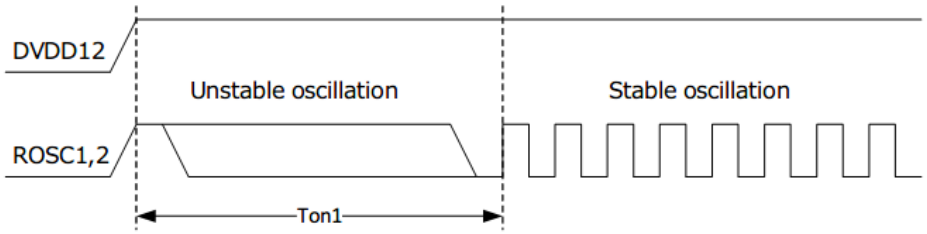


Figure 6-4 ROSC1, 2 Startup waveform

6.6.3 Internal Fast Clock (ROSC2)

ROSC2 Electrical Characteristics is shown on Table 6-4. PD (Power Down) can be controlled by xmode0[11] register.

Table 6-4 ROSC2 Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Condition
Output frequency	F_{osc}	26	40	54	MHz	
Duty cycle	D	40	50	60	%	
Startup time when power on	T_{on1}		20		us	
Startup time when "PD" enabled	T_{on2}		20		us	

For T_{on1} and T_{on2}, please refer to Table 6-3 and Table 6-4. The unstable output at T_{on2} isn't be blocked, and when PD is changed from 1 to 0, please wait for T_{on2} to start operation.

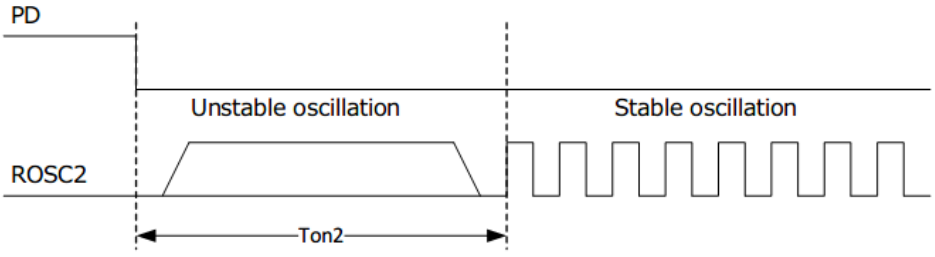


Figure 6-5 ROSC2 Startup Waveform (T_{on2})

6.7 Low Power Modes

The device supports three low power modes as below.

- Sleep mode

In sleep mode, only the ParaForce is stopped. All clocks are running. When system clock is set to internal low-speed (100kHz) during sleep mode, the mode is slow-CLK sleep mode. And when system clock is set internal high-speed (40MHz) or to external clock input during sleep mode, the mode is fast-CLK sleep mode. In fast-CLK sleep mode, host device can access to eDSP internal RAM and register. All peripherals continue to operate and can wake up the ParaForce when an interrupt occurs.

- Stop mode

In stop mode, the ParaForce is stopped and all clocks except the ParaForce clock are stopped. Register needs to be set before the ParaForce is stopped and can wake up the ParaForce when an Awake interrupt occurs.

- Standby mode

The Standby mode is used to achieve the lowest power consumption. The internal power switch is off so that the 1.2V domain is powered off. All clocks are stopped except the internal low speed clock (100kHz). The device enters to Standby mode when external STANDBY pin is set to L, and to be back to normal mode, external STANDBY pin needs to be set to H. All SRAM and register are initialized when the device exits the Standby mode. Please refer to Table 6-5.

Table 6-5 Low power modes specifications[2]

Low Power Mode		Sleep		Stop	Standby
		Fast-CLK	Slow-CLK		
Entry	Start	WAITI instruction	<-	STOPREG 1'b1 set and WAITI instruction	STANDBY pin H->L
Wake up	Start	All interrupt events	<-	The Awake timer interrupt	STANDBY pin L->H
	recovery time	<10us	<2ms	50us-2ms	(depend on boot program size)

[2] The recovery time and power consumption value is estimated by simulation, and there is no guarantee.

7 Host Interface Specifications

This is the interface to connect with Host Device and has two kinds of interfaces, SPI slave and I2C slave. The details of Host Interface are as follows.

7.1 Address Map

Figure 7-1 shows Address Map of Host Interface. SPI is accessible to address width of [13:0] area, and I2C is accessible to address width of [7:0] area.

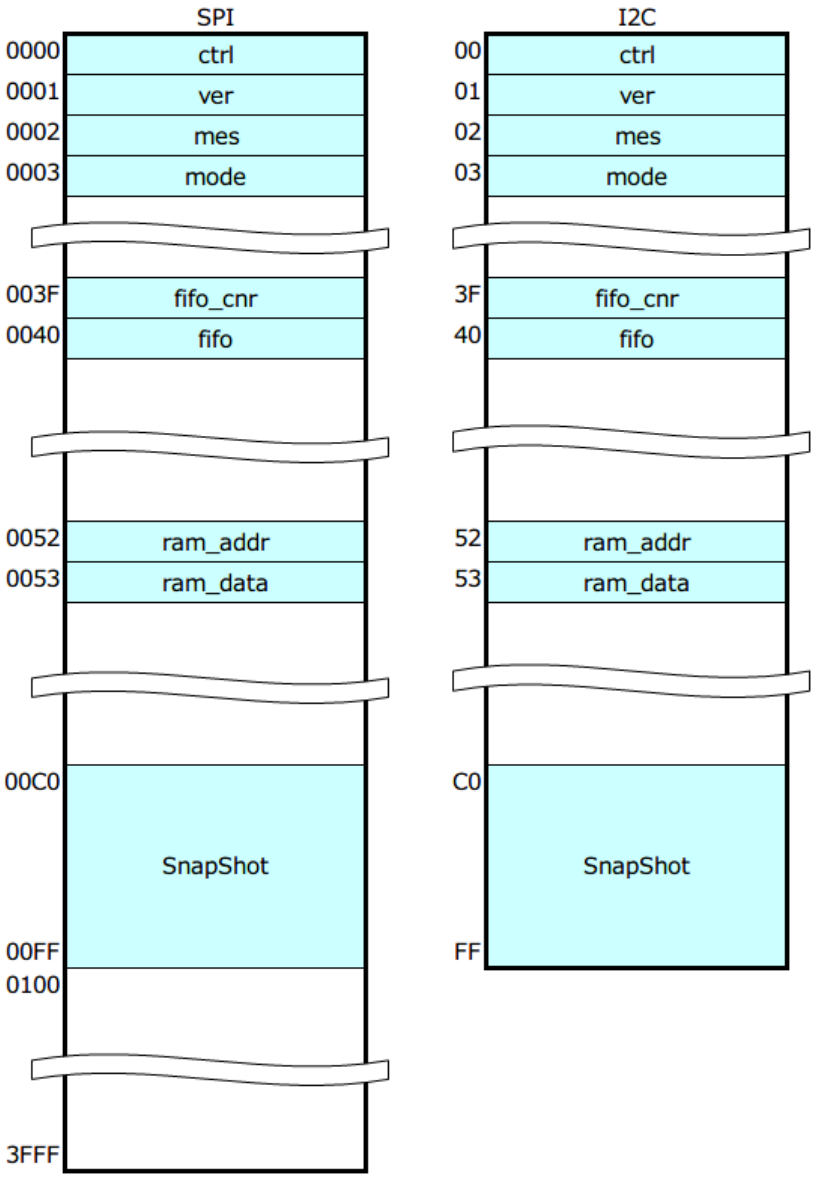


Figure 7-1 Address Map of Host Interface

7.2 SPI/I2C

SPI (Serial Peripheral Interface) interface that multiplex I2C is available. They are alternative functions and can be operated in slave mode. The external pin SEL0 and SEL1 select SPI or I2C interface.

Figure 7-2 shows Host interface SPI timing diagram.

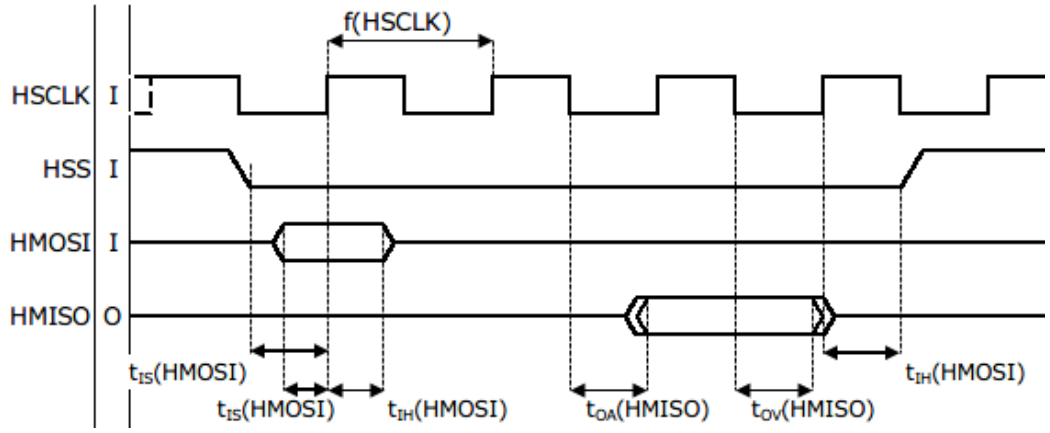


Figure 7-2 Host interface SPI timing diagram

Table 7-1 shows Host interface SPI dynamic characteristics.

Table 7-1 Host interface SPI dynamic characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
IO voltage 3.3V						
SPI Clock Frequency	f (HSCLK)		-	-	40	MHz
Data input setup Time	t_{IS}(HMOSI)		4	-	-	ns
	t_{IS}(HSS)		6	-	-	ns
Data input hold Time	t_{IH}(HMOSI)		1	-	-	ns
	t_{IH}(HSS)		1	-	-	ns
Data output Access time	t_{OA}(HMISO)	35pF load	-	-	9.5	ns
		20pF load	-	-	8.8	ns
		10pF load			8.2	ns
Data output Valid time	t_{OV}(HMISO)		1	-	-	ns
IO voltage 1.8V						
SPI Clock Frequency	f (HSCLK)		-	-	20	MHz
Data input setup Time	t_{IS}(HMOSI)		4	-	-	ns
	t_{IS}(HSS)		6	-	-	ns
Data input hold Time	t_{IH}(HMOSI)		1	-	-	ns
	t_{IH}(HSS)		1	-	-	ns
Data output Access time	t_{OA}(HMISO)	20pF load	-	-	14.0	ns
		10pF load			13.0	ns
Data output Valid time	t_{OV}(HMISO)		1	-	-	ns

Figure 7-3 shows I2C waveform.

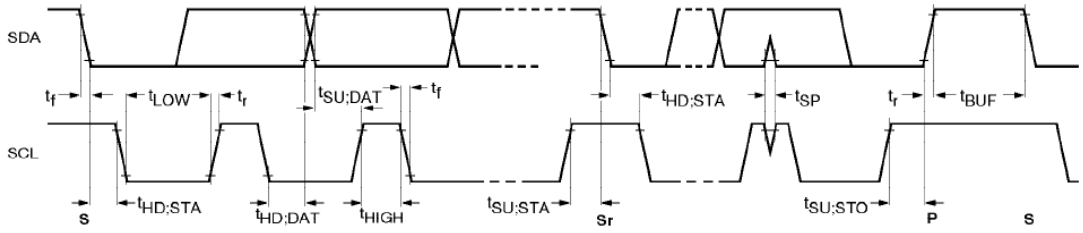


Figure 7-3 I2C waveform

Table 7-2 shows I2C Characteristics.

Table 7-2 I2C Characteristics

Symbol	Parameter	Condition	Standard-mode		Fast-mode		Fast-mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
$t_{HD;STA}$	hold time (repeated) START condition	After this period, the first clock pulse is generated.	4.0	-	0.6	-	0.26	-	us
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	us
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	us
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	us
$t_{HD;DAT}$	data hold time		0	-	0	-	0	-	us
tSU;dAT	data set-up time		250	-	100	-	50	-	ns
t_r	rise time of both SDA and SCL signals		-	1000	20	300	-	120	ns
t_f	fall time of both SDA and SCL signals		-	300	20* (VDD/ 5.5V)	300	20* (VDD/ 5.5V)	120	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	us
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	us
$t_{VD;DAT}$	data valid time		-	3.45	-	0.9	-	0.45	us
$t_{VD;ACK}$	data valid acknowledge time		-	3.45	-	0.9	-	0.45	us

7.3 Access to DPBUF(Dual Purpose Buffer)

The data exchange between ParaForce and Host Interface takes place via DPBUF (Dual Purpose Buffer).There are 2 operation modes, FIFO and Snapshot. The mode switching between FIFO and Snapshot is performed in register fifo_ctr[1]. Before switching mode, FIFO reset (register ctrl[3]) must be performed.

7.3.1 FIFO Mode

This is the mode to access to register fifo.

7.3.2 Snapshot Mode

This is the mode to access to 0x00C0-00FF area. Only read is available to access to this area from Host Interface.

7.4 Access to I-RAM/D-RAM

While ParaForce is being stalled, internal I-RAM/D-RAM area can be accessible from Host Interface. The register ram_adr and ram_data are used to access from Host Interface to I-RAM/D-RAM. The address to set in register ram_adr must be 1 word unit. Table 7-3 shows the address number to set ram_adr. The address number is different from Sensor Interface Address Map Figure 8-1.

Table 7-3 the address number to set ram_adr

Access to RAM area	ram_adr to set address
D-RAM0	00000000h – 00007FFFh
D-RAM1	00008000h – 0000FFFFh
I-RAM0	00010000h – 00017FFFh
I-RAM1	00018000h – 0001FFFFh

8 Sensor Interface and Peripheral Specifications

The device provides following interfaces to collect sensor data and connect to other devices.

- I2C master
- SPI master
- GPIO
- PWM
- UART
- Timer

These interfaces are controlled by ParaForce and connected to Data Bus. The details of Sensor Interface and Peripherals are given below.

8.1 Address Map

Figure 8-1 shows Address Map of Sensor Interface.

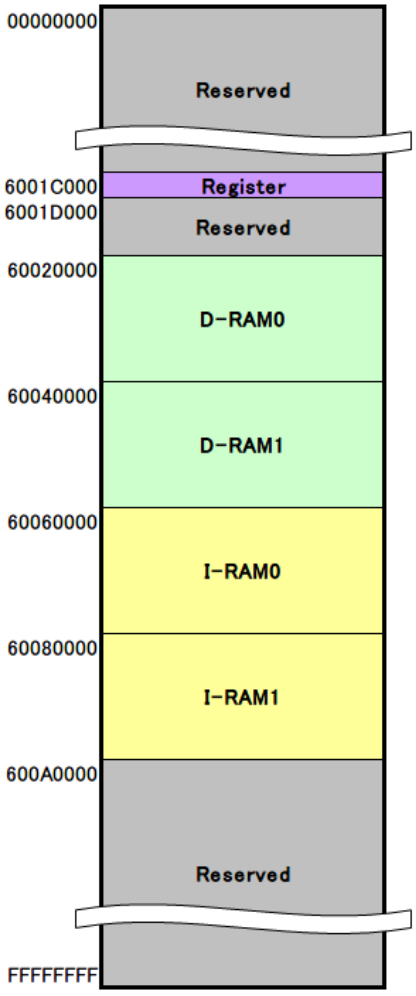


Figure 8-1 Address Map of Sensor Interface

8.2 I2C

Table 8-1 shows Sensor Interface I2C implementation.

Table 8-1 Sensor Interface I2C implementation

Function	Content
Master/Slave	Master
Clock	CLK_PERI
Specification	• Data width : 8bit (ACK signal of 1 bit data is added after 8 bit data) • I2C bus format is based on Philips 1995 Update. The device can distinguish between start-condition and stop-condition form the state of I2C bus line. • Standard-mode (transfer at rates of up to 100kbit/s) is available. • Fast-mode (transfer at rates of up to 400kbps) is available.
Interrupt signal	int_i2c

For I2C characteristics, please refer to Figure 7-3 and Table 7-2.

8.3 SPI

Table 8-2 shows Sensor Interface SPI implementation.

Table 8-2 Sensor Interface SPI implementation

Function	Content
Master/Slave	Master
Clock	CLK_PERI
Specification	• 3-wired serial interface • Slave select signal are available up to 4 • Data width : 8bit • Fast bit of serial data : Alternative of MSB or LSB
Interrupt signal	int_spim

Figure 8-2 shows Sensor Interface SPI Timing Diagram.

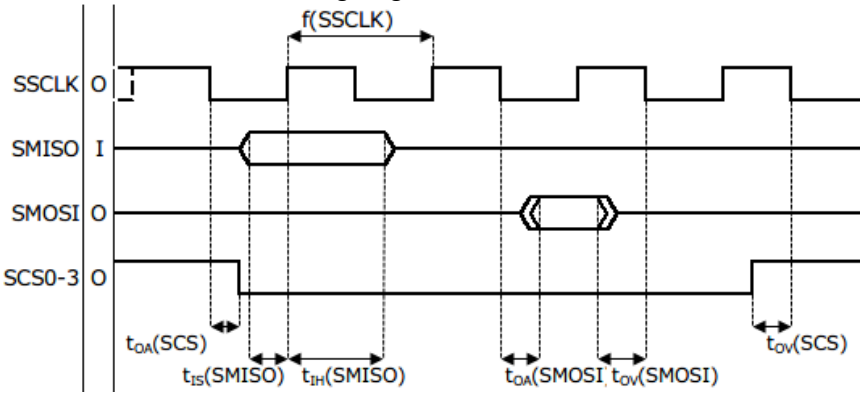


Figure 8-2 Sensor Interface SPI Timing Diagram

Table 8-3 shows Sensor Interface SPI dynamic characteristics.

Table 8-3 Sensor Interface SPI dynamic characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SPI Clock Frequency	f(SSCLK)		-	8	10.8[3]	MHz
Data input setup Time	t_{IS}(SMISO)		14.5	-	-	ns
Data input hold Time	t_{IH}(SMISO)		0	-	-	ns
Data output Access time	t_{OA}(SMOSI)	output load 35pF@3.3V or 20pF@1.8V	-	-	2.5	ns
	t_{OA}(SCS)	↑	-	-	2.5	ns
Data output Valid time	t_{OV}(SMOSI)	↑	-	-	8	ns
	t_{OV}(SCS)	↑	-	-	8	ns

[3] SPI clock maximum frequency is one five of CLK_PERI.

8.4 GPIO

Table 8-4 shows Peripheral GPIO implementation.

Table 8-4 Peripheral GPIO implementation

Function	Content
Port number	Up to 4 (alternative of SS signal for SPI, PWM output, and CTS/RTS signal for UART)
Specification	• General purpose input and output • Hi-Z output after reset-release • GPIO2 and GPIO3 can be used external interrupt input.
Interrupt signal	int_gpio2, int_gpio3

8.5 PWM

Table 8-5 shows Peripheral PWM implementation.

Table 8-5 Peripheral PWM implementation

Function	Content
Channel number	Up to 2
Specification	• Duty setting : 0.0015-99.9985% • Period setting : Divide CLK_PERI into 1/2-1/65535 • Minimum resolution : (2 / CLK_PERI) sec
Interrupt signal	(none)

8.6 UART

Table 8-6 shows Peripheral UART .

Table 8-6 Peripheral UART implementation

Function	Content
Clock	CLK_PERI
Specification	• Baud rate : CLK_PERI / 4080 – CLK_PERI / 16 bps • Format : ・ Data bit : 5 - 8bits ・ Stop bit : 1 or 2 bits ・ Parity bit : odd, even, not use • FIFO size : Transfer 128byte, Receiver 128byte • Hardware flow control is available
Interrupt signal	int_uart

8.7 Timer

8.7.1 General-purpose timers

Table 8-7 shows General-purpose timers implementation.

Table 8-7 General-purpose timers implementation

Function	Content
Channel number	3 independent channels
Specification	• 32-bit resolution interval timer • Counter clock : CLK_XT • Interval period settings : 0 ~ 2^{32} - 1
Interrupt signal	TIM0, TIM1, TIM2

8.7.2 Awake timer

Table 8-8 shows Awake timer implementation.

Table 8-8 Awake timer implementation

Function	Content
Channel number	1
Specification	• 32-bit resolution interval timer • Counter clock : ROSC1 (100kHz) or external clock • Interval period settings : 0 ~ 2^{32} - 1
Interrupt signal	int_awake

9 Interrupt

There are 16 interrupt at the ParaForce, including 4 external interrupt. Please refer User's Manual about interrupt details.

Table 9-1 Interrupt controller

#	Name	Interrupt Event	Priority level	type
0	TIM0	General-purpose timer0	1	Timer
1	TIM1	General-purpose timer1	2	Timer
2	message		4	Level
3	TIM2	General-purpose timer	3	Timer
4	AWake	Awake timer	4	Level
5	I2C master		1	Level
6	UART Master		1	Level
7	GPIO3	External interrupt 1	1	Level
8	(not use)	-	-	-
9	SPI Master		1	Level
10	GPIO2	External interrupt 0	1	Level
11	(not use)	-	-	-
12	(not use)	-	-	-
13	FIFO RD	DPBUS FIFO	1	Edge
14	GPIO3	External interrupt 1	1	Edge
15	GPIO2	External interrupt 0	1	Edge

10 Absolute Maximum Ratings

Table 10-1 Absolute Maximum Ratings

Ratings	Symbol	Min.	Max.	Unit
I/O Power Supply Voltage	DVDD18	-0.5	3.63	V
Core Power Supply Voltage	DVDD12	-0.5	1.32	V
Analog Power Supply Voltage	ROSC_AVDD	-0.5	1.32	V
IO Voltage	VPAD	-0.5	DVDD18 + 0.5	V
Junction Operating Temperature	Tj	-40	125	C
Storage Temperature range for packed material	-	5	35	C
Storage Humidity range for packed material	-	-	85	%RH

11 Recommended Operating Conditions

Table 11-1 Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
I/O Power Supply	DVDD18	1.8V	1.62	1.8	1.98	V
		2.5V	2.25	2.5	2.75	V
		2.8V	2.52	2.8	3.08	V
		3.0V	2.7	3	3.3	
		3.3V	2.97	3.3	3.63	V
Core Power Supply	DVDD12	1.2V	1.08	1.2	1.32	V
Analog Power Supply	ROSC_AVDD	1.2V	1.08	1.2	1.32	V
Ambient Temperature	Ta	-	-20	-	85	C

12 DC Characteristics

Table 12-1 DC Characteristics

Parameter	Symbol	Condition		Min	Typ	Max	Unit
High-Level Input Voltage	VIH	DVDD18=1.8V	-	0.7*DVDD18	-	DVDD18+0.3	V
		DVDD18=3.3V	-	0.7*DVDD18	-	DVDD18+0.3	V
Low-Level Input Voltage	VIL	DVDD18=1.8V	-	DVSS-0.3	-	0.3*DVDD18	V
		DVDD18=3.3V	-	DVSS-0.3	-	0.3*DVDD18	V
Hysteresis Schmitt Trigger	VHYS	-	-	0.4	-	-	V
DC Current	IOH	DVDD18=1.8V VOH=DVDD18-0.4	2mA	3.6	-	-	mA
			4mA	7.3	-	-	mA
			8mA	9.8	-	-	mA
			12mA	13.5	-	-	mA
		DVDD18=2.5V VOH=DVDD18-0.4	2mA	3.8	-	-	mA
			4mA	5.7	-	-	mA
			8mA	9.5	-	-	mA
			12mA	11.5	-	-	mA
		DVDD18=3.3V VOH=DVDD18-0.4	2mA	4.9	-	-	mA
			4mA	7.3	-	-	mA
			8mA	12.3	-	-	mA
			12mA	14.8	-	-	mA
	IOL	DVDD18=1.8V VOH=0.4V	2mA	4.3	-	-	mA
			4mA	8.7	-	-	mA
			8mA	11.7	-	-	mA
			12mA	16	-	-	mA
		DVDD18=2.5V VOH=0.4V	2mA	4.4	-	-	mA
			4mA	6.6	-	-	mA
			8mA	11.1	-	-	mA
			12mA	13.1	-	-	mA
		DVDD18=3.3V VOH=0.4V	2mA	5.5	-	-	mA
			4mA	8.2	-	-	mA
			8mA	13.8	-	-	mA
			12mA	16.6	-	-	mA
Static Output Voltage High	VOH	DVDD18=1.62V	2mA	DVDD18-0.4	-	-	V
			12mA	DVDD18-0.4	-	-	V
		DVDD18=2.97V	2mA	DVDD18-0.4	-	-	V
			12mA	DVDD18-0.4	-	-	V
Static Output Voltage Low	VOL	DVDD18=1.62V	2mA	-	-	0.4	V
			12mA	-	-	0.4	V
		DVDD18=2.97V	2mA	-	-	0.4	V
			12mA	-	-	0.4	V
Pull-down current	IPD	DVDD18=1.8V	-	23	42	85	uA
		DVDD18=3.3V	-	44	81	154	uA
Pull-up current	IPU	DVDD18=1.8V	-	29	51	91	uA
		DVDD18=3.3V	-	54	89	144	uA
Leakage current	$IDDQ_{on}$	DVDD12=1.32V, Core: Active (STANDBY pin = "H")				4	mA
	$IDDQ_{off}$	DVDD12=1.32V, Core: Standby (STANDBY pin = "L")				0.06	mA
Dynamic current	IDD_{on}	DVDD12=1.32V, Core: Active (STANDBY pin = "H")				20	mA
	IDD_{off}	DVDD12=1.32V, Core: Standby (STANDBY pin = "L")				0.2	mA

13 AC Characteristics

Table 13-1 AC Characteristics (DVDD=1.8V)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Propagation Delay	tPD	Output 12mA	CLOAD=20pF	-	3.5	-	ns
		Input	CLOAD=0.2pF	-	1.1	-	ns
		Input with schmitt		-	1.2	-	ns
Rise Time 10% to 90%	tr	Output 12mA	CLOAD=20pF	-	2	-	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns
Fall Time 90% to 10%	tf	Output 12mA	CLOAD=20pF	-	1.7	-	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns

Table 13-2 AC Characteristics (DVDD=3.3V)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Propagation Delay	tPD	Output 12mA	CLOAD=20pF	-	2.6	-	ns
		Input	CLOAD=0.2pF	-	0.7	-	ns
		Input with schmitt		-	0.9	-	ns
Rise Time 10% to 90%	tr	Output 12mA	CLOAD=20pF	-	1.6	-	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns
Fall Time 90% to 10%	tf	Output 12mA	CLOAD=20pF	-	1.7	-	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns

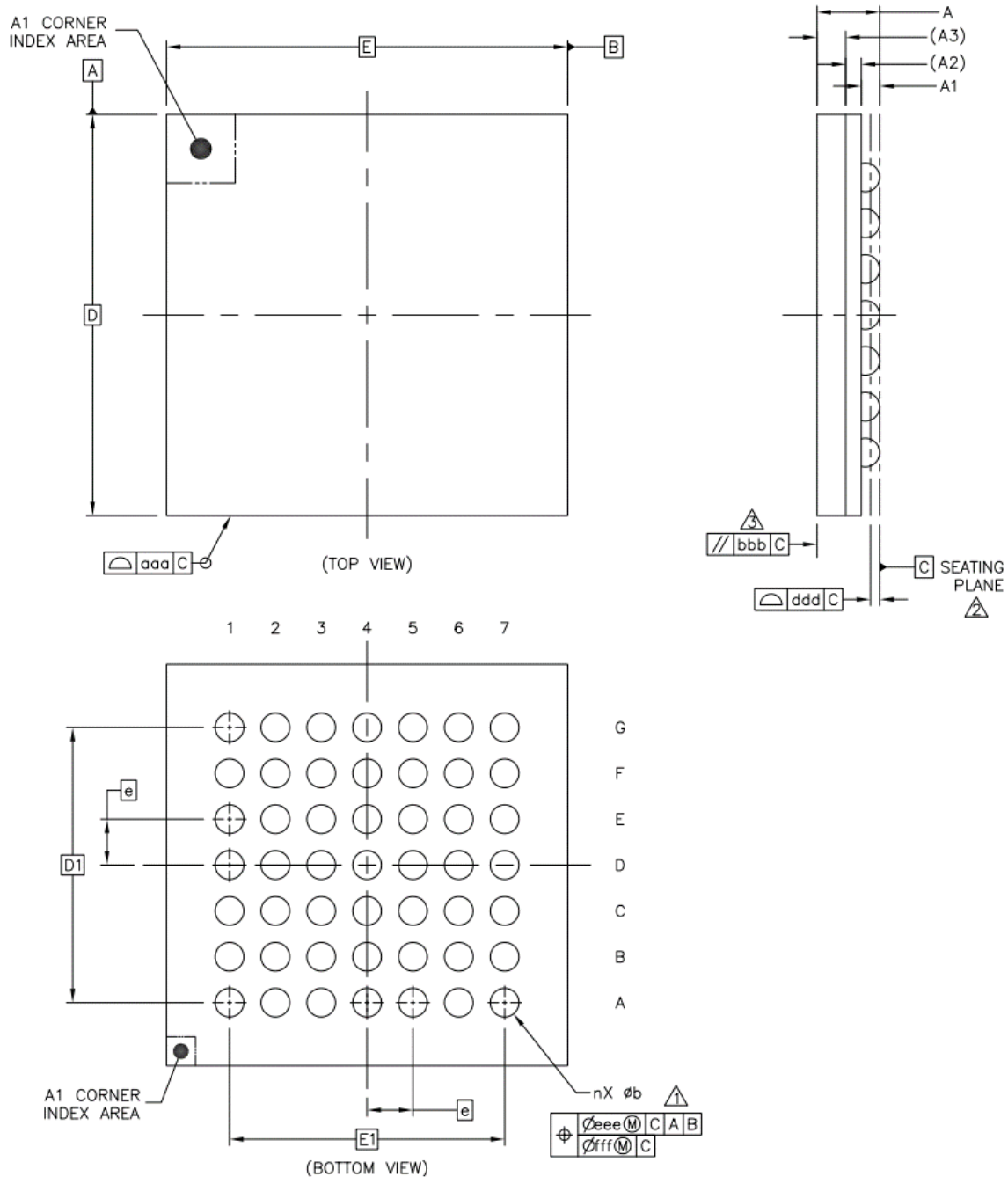
14 Ball Map

	1	2	3	4	5	6	7	
A	NC	DVSS	CLKIN	DVDD12	DVSS	DVDD18	NC	A
B	DVDD12	DVDD18	SELCLK	DSPRUN	STANDBY	HSS	HMISO	B
C	GPIO0	GPIO3	SEL0	SEL1	SELVDD	HMOSI	HSCLK	C
D	JTCK	GPIO1	GPIO2	DVSS	SELRST	DVDD12	ROSC_ AVDD	D
E	JTRST	JTDO	SRX	DVSS	RSTB	DVSS	ROSC_ AVSS	E
F	JTMS	JTDI	STX	SMISO	SSCLK	SMOSI	DVDD18	F
G	NC	DVDD18	DVSS	DVDD12	SSCL	SSDA	NC	G
	1	2	3	4	5	6	7	

Figure 14-1 Ball Map (Top View)

In Figure 14-1, NC pin MUST be non-connection, be careful not to connect to Power Pin (DVDD12, DVDD18, ROSC_AVDD), GND pin (DVSS, ROSC_DVSS), and other signal pins.

15 Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	0.65
STAND OFF	A1	0.11	---	0.21
SUBSTRATE THICKNESS	A2		0.136	REF
MOLD THICKNESS	A3		0.25	REF
BODY SIZE	D		3.5	BSC
	E		3.5	BSC
BALL DIAMETER			0.25	
BALL OPENING			0.22	
BALL WIDTH	b	0.2	---	0.3
BALL PITCH	e		0.4	BSC
BALL COUNT	n		49	
EDGE BALL CENTER TO CENTER	D1		2.4	BSC
	E1		2.4	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

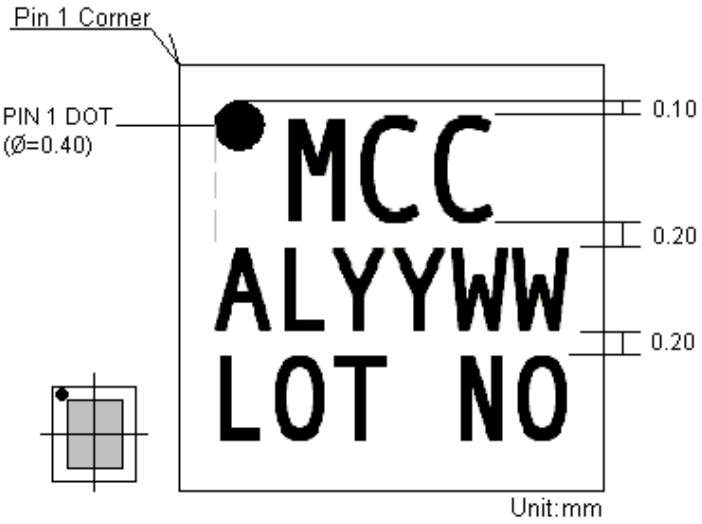
NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 15-1 Package Outline Drawing[4][5][6]

[4] The unit of package outline drawing is a millimeter.
[5] REF stands for Reference. BSC stands for Basic Spacing between Centers.
[6] BALL DIAMETER means ball size before ball mount, BALL WIDTH means ball size after ball mount.

16 Marking Specification



	Description	Position	Font Type	Height ↕	Width ↔	Space ↔	Max Width ⟷	Max chars
Line 1	MCC	Center	ARIAL-0.FNT	0.88 mm	0.50 mm	0.10 mm	1.70 mm	3
Line 2	ALYYWW	Center	ARIAL-0.FNT	0.70 mm	0.40 mm	0.10 mm	2.90 mm	6
Line 3	LOT NO	Center	ARIAL-0.FNT	0.70 mm	0.40 mm	0.10 mm	2.90 mm	6

Figure 16-1 Marking Specification

17 Recommended Land Pattern

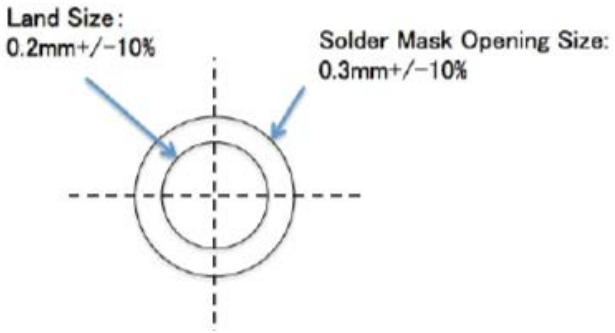


Figure 17-1 Recommended Land Pattern

18 Power Sequence

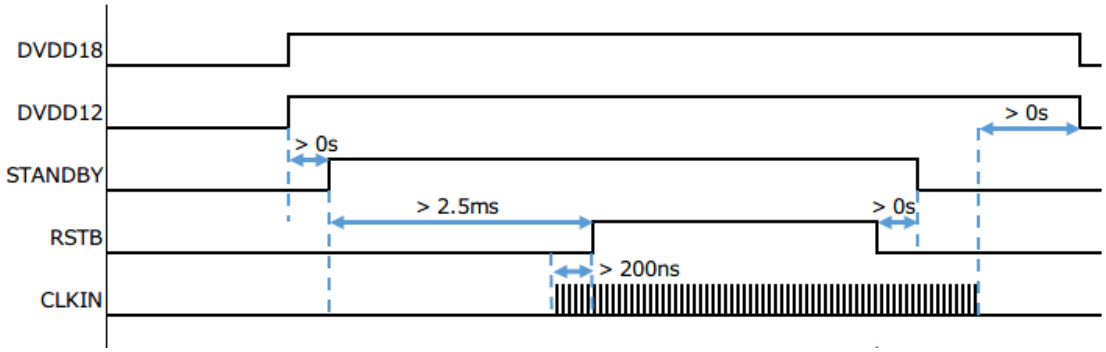


Figure 18-1 Power Sequence

All input signals, including STANDBY pin, should be worked after DVDD18 and DVDD12 are stable.

19 Pin Configuration / Peripherals

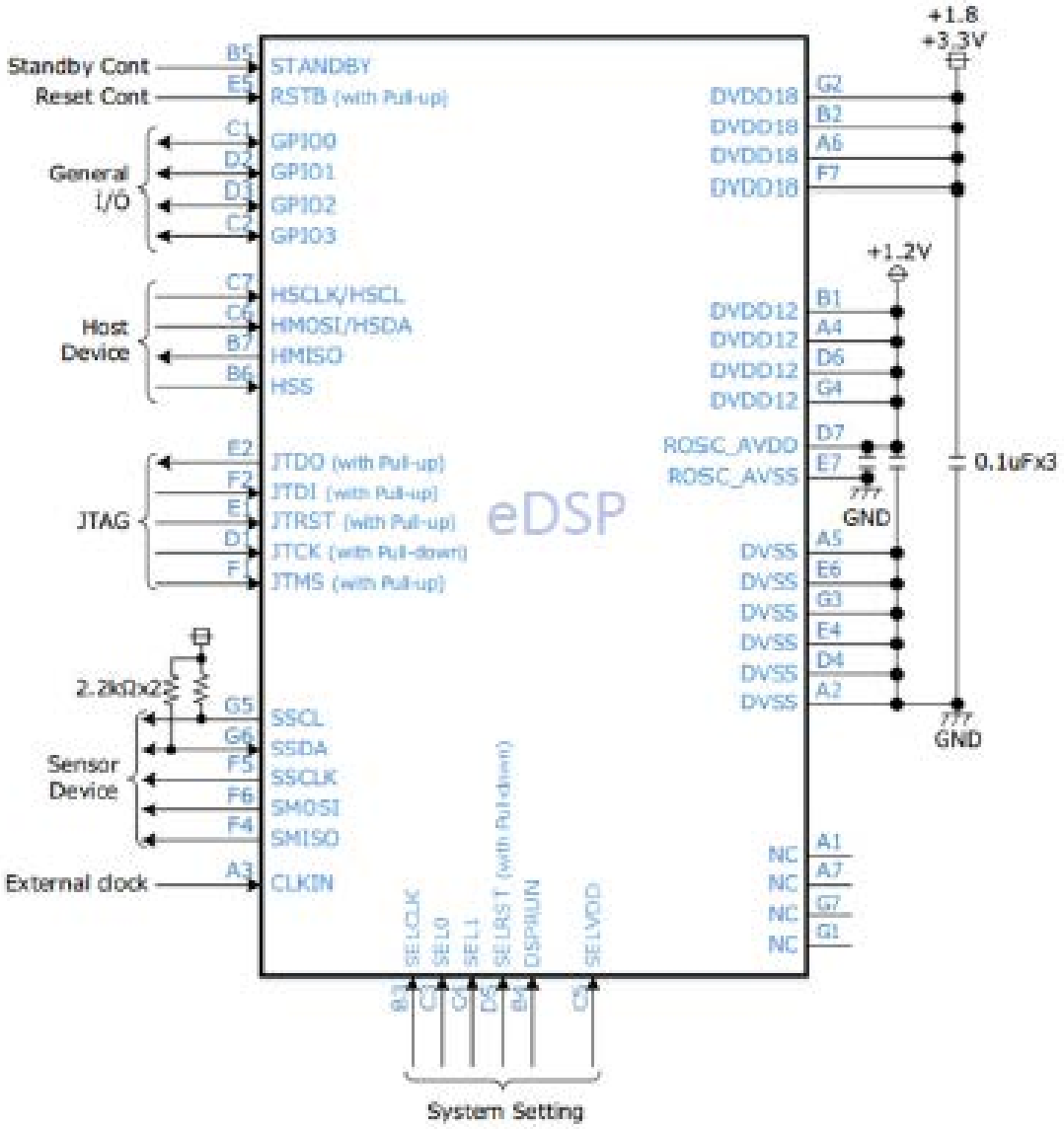


Figure 19-1 Pin Configuration/Peripherals

20 Notices

1. Prohibition on copying and disclosure.
These specifications include intellectual property and know-how belonging to MegaChips Corporation ("MCC") and its partner companies. Therefore, do not use these specifications for any purpose other than the purpose expressly agreed to by MCC's customer and MCC. Also, do not duplicate, copy, or reproduce these specifications, nor reveal these specifications to any third party without MCC's prior written consent.

2. No guarantee of rights
MCC does not warrant that it owns or controls any of the information, patents, copyrights or other intellectual property rights contained in these specifications. MCC grants no license of patents, copyrights or other intellectual property rights contained in these specifications. MCC disclaims all liability arising from the use of the specifications with regard to infringement of any patents, copyrights or other intellectual property rights.

3. Safety designs such as redundancy
While MCC has been making continuous effort to enhance the quality and reliability of its devices, the possibility of malfunction cannot be eliminated entirely. To minimize risk of damage or injury to persons or property arising from a malfunction in a device, customer must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features. (If the customer intends to use the devices for applications other than those specified between the customer and MCC, please contact MCC sales representative before such use.)

4. Restriction on use
MCC provides no warranty relating to the use of the devices, where there is risk of serious damage, environmental pollution, loss of life, injury or damage to property, or where reliability or special quality is essential, such as life support, military use, or space exploration.

5. Radiation-proof design
This device has not been designed to be radiation-resistant.

6. Export restriction
The export of this device may be regulated by the government under customs, anti-proliferation rules, or other regulations, and export may be prohibited without governmental license.

7. No prior notice of revision
These specifications are based on materials dated 9/26/2016, and MCC reserves the right to revise these specifications without any prior notice. For mass production planning, please reference the latest version of the specifications.

Definition/Revision History			
Standard	eDSP Product Specification	No.	SPS-MA60000-EN-B

Date of D/R/A	Rev.	Contents of Definition/Revision	D/R/A by			
			Final Aprv.	Aprv.	Rvw.	Crt.
09/16/2016	1.0	Released	Silverman	Navid		