Marconi
Electronic Devices

Three Phase Pulse Width Modulation Waveform Generator

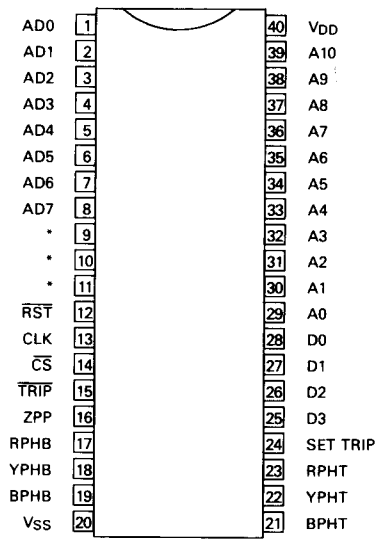
994058

MA818

PRELIMINARY DATA SHEET

FEATURES

* Fully digital operation
* Interfaces with many popular processors
* Selectable pulse delay time and minimum pulse deletion time
* Wide power frequency range
* Carrier frequency selectable
* 'Silent' inverter operation possible
* Waveform stored in external EPROM/ROM
* Trip feature
* Double edged regular sampling
* 0°–70° commercial grade package
* 40 pin DIL package



DESCRIPTON

The PWM generator has been designed to provide waveforms for the control of variable speed AC machines, uninterruptible power supplies, and other forms of power electronic devices which require pulse width modulation (PWM) as a means of efficient power control.

The six TTL level PWM signal outputs (Fig. 1) control the six switches in a three phase inverter bridge. This is usually via an external isolation and amplification stage.

Information contained within the pulse width modulated sequences control the shape, power frequency, amplitude, and rotational direction (as defined by the red-yellow-blue phase sequence) of the output waveform. Furthermore parameters such as the carrier frequency, minimum pulse width, and pulse delay time may be defined during the initialisation of the device.

The pulse delay time controls the delay between turning on and off the two power switches in each output phase of the inverter bridge. Variations in the turn-on and turn-off times of families of power devices can therefore be accommodated.

An 8 bit bidirectional, multiplexed data bus is used for interface with a microprocessor/microcontroller. MA818 address and data information is transmitted via the bus. This is a standard bus compatible with many industry standard microprocessor/microcontrollers.

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MA818 Three Phase Pulse Width Modulation Waveform Generator

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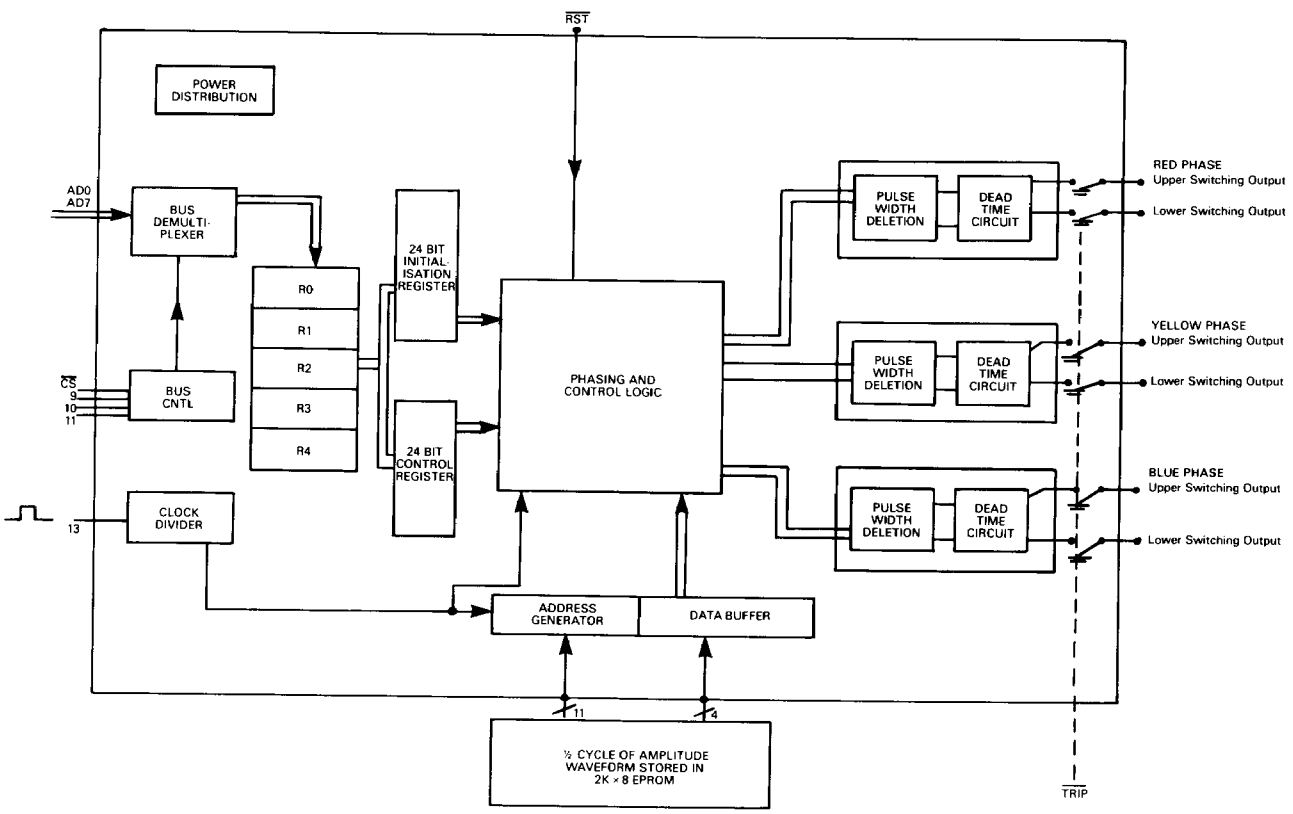

Fig. 1 Internal Block Diagram

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Three Phase Pulse Width Modulation Waveform Generator MA818

PRELIMINARY DATA SHEET

PIN FUNCTIONS

Pin	Name	Type	Function
1	AD0	I	Multiplexed Address/Data (LSB)
2	AD1	I	Multiplexed Address/Data
3	AD2	I	Multiplexed Address/Data
4	AD3	I	Multiplexed Address/Data
5	AD4	I	Multiplexed Address/Data
6	AD5	I	Multiplexed Address/Data
7	AD6	I	Multiplexed Address/Data
8	AD7	I	Multiplexed Address/Data (MSB)
9	***	I	Bus control (See table below)
10	***	I	Bus control (See table below)
11	***	I	Bus control (See table below)
12	$\overline{RST}$	I	Resets internal counters
13	CLK	I	Clock input
14	$\overline{CS}$	I	Chip Select, input
15	$\overline{TRIP}$	O	Output Trip Status
16	ZPP	O	Zero Phase Pulse
17	RPHB	O	Red Phase (Bottom power switch)
18	YPHB	O	Yellow Phase (Bottom power switch)
19	BPHB	O	Blue Phase (Bottom power switch)
20	V_{SS}	I	Negative power supply (0V)
21	BPHT	O	Blue Phase (Top power switch)
22	YPHT	O	Yellow Phase (Top power switch)
23	RPHT	O	Red Phase (Top power switch)
24	SET TRIP	I	Set output Trip
25	D3	I	EPROM Data (MSB)
26	D2	I	EPROM Data
27	D1	I	EPROM Data
28	D0	I	EPROM Data (LSB)
29	A0	O	EPROM Address (LSB)
30	A1	O	EPROM Address
31	A2	O	EPROM Address
32	A3	O	EPROM Address
33	A4	O	EPROM Address
34	A5	O	EPROM Address
35	A6	O	EPROM Address
36	A7	O	EPROM Address
37	A8	O	EPROM Address
38	A9	O	EPROM Address
39	A10	O	EPROM Address (MSB)
40	V_{DD}	I	Positive power supply (+5V)

BUS CONTROL

9	R/$\overline{W}$	I	Read Write Select	MOTOROLA TYPE MPU
10	DS	I	Data Strobe	BUS SIGNALS
11	AS	I	Address Strobe	
9	$\overline{WR}$	I	Write Strobe	INTEL TYPE MPU
10	$\overline{RD}$	I	Read Strobe	BUS SIGNALS
11	ALE	I	Address Latch Enable	

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ABSOLUTE MAXIMUM RATINGS

Parameter	Range	Units
Supply voltage V_{DD} max	10	Volts
Maximum positive voltage on any pin	$V_{DD}+0.3$	Volts
Maximum negative voltage on any pin	$V_{SS}-0.3$	Volts
Maximum current through any I/O pin	10	mA
Maximum frequency clock input	10	MHz
Maximum storage temperature range	−65 to +125	°C
Maximum operating temperature range	0 to +70	°C

NOTE: Stresses exceeding those listed as absolute maximum ratings may cause permanent damage to the device. Functional performance for extended periods at the absolute maximum ratings may adversely affect device reliability.

ELECTRICAL CHARACTERISTICS at 5V and 25°C

Type	Parameter	Descripton	Conditions	Min	Max	Units
INPUTS	V_{IH}	Input high volts		2	–	V
	V_{IL}	Input low volts		–	0.8	V
	I_{IN}	Input leakage	V_{IN} = V_{SS} or V_{DD}	–	10	μA
OUTPUTS	V_{OH}	Output high volts	at −2mA	4.0	–	V
	V_{OL}	Output low volts	at 4mA	–	0.5	V

NOTE: The SET input (pin 24) has an internal pull-up resistor with an approximate value of 90K ohms.

MICROPROCESSOR INTERFACE

The MA818 interfaces to the controlling processor by means of a multiplexed bus of the MOTEL* format. The term MOTEL* is derived from the ability of the bus to adapt automatically to the timing of certain MOTorola and IntEL interface busses (hence MOTEL*). Internally the detection circuitry latches the status of the DS (or RD) line when AS (or ALE) goes high. If the result is high then the INTEL mode is used, conversely if a low is latched then the MOTOROLA mode is invoked.

Industry standard microprocessors such as the 8085, 8088, etc., and microcontrollers such as the 8051, 8052 and 6805 are compatible with the interface implemented on the MA818. This interface consists of 8 data lines (write only in this instance), which are multiplexed to carry both the address and data information, three bus control lines, and a chip enable function. The type of microprocessor chosen will determine the connections to pins 9, 10 and 11.

MOTOROLA MODE

The address is latched on the falling edge of the AS line. Data is written from the bus into the MA818 (only when R/$\overline{W}$ is low), on the falling edge of DS (providing $\overline{CE}$ is low).

INTEL MODE

The address is latched by the falling edge of ALE. Data is written from the bus into the MA818 on the rising edge of $\overline{WR}$. $\overline{RD}$ is not used in this mode because the registers in the MA818 are write only. However this pin must be connected to $\overline{RD}$ (or tied high) to enable the PWM waveform generator to select the correct interface format during the power up sequence.

*MOTEL is a registered trademark of Motorola Corp. and Intel Corp.

A.C. PERFORMANCE

Conditions: V_{DD} = 5V, Temperature = 25°C

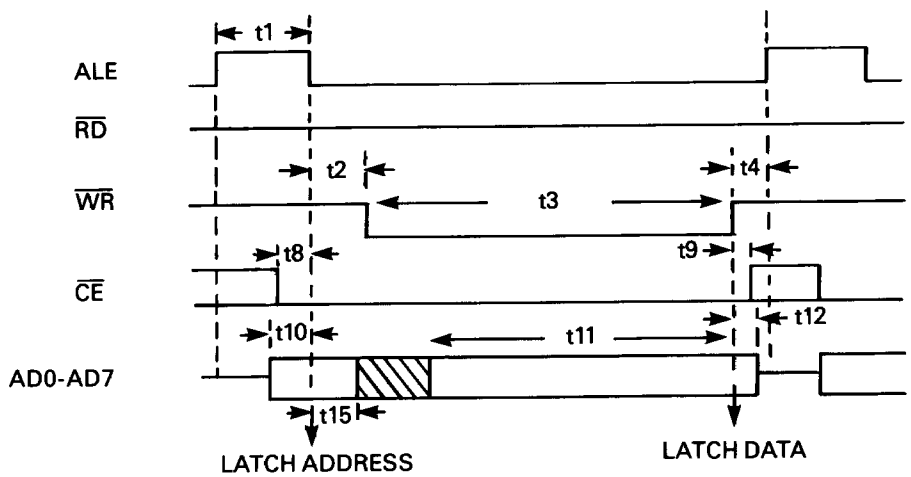


Fig. 2 INTEL mode Bus Interface Waveforms

Parameter	Symbol	Min	Typ	Max	Units
ALE high period	t1	70			ns
Delay time, ALE to $\overline{WR}$	t2	40			ns
$\overline{WR}$ low period	t3	200			ns
Delay time $\overline{WR}$ = 1 to ALE	t4	10			ns
$\overline{CE}$ setup time	t8	20			ns
$\overline{CE}$ hold time	t9	0			ns
Address setup time	t10	30			ns
Address hold time	t15	30			ns
Data setup time	t11	100			ns
Data hold time	t12	25			ns

A.C. PERFORMANCE

Conditions: V_{DD} = 5V, Temperature = 25°C

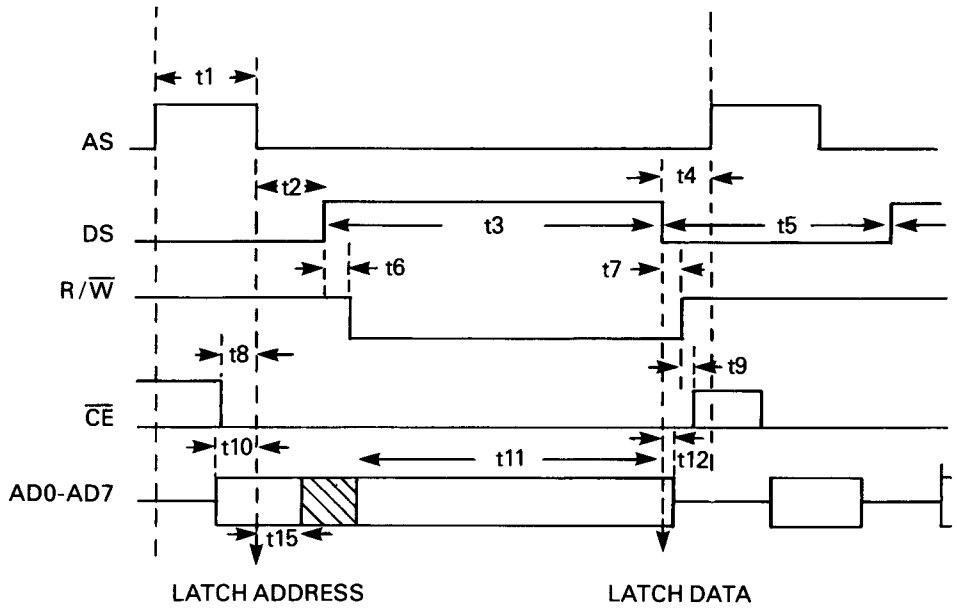


Fig. 3 Motorola mode Bus Interface Waveforms

Parameter	Symbol	Min	Typ	Max	Units
AS high period	t1	90			ns
Delay time, AS low to DS high	t2	40			ns
DS high period	t3	210			ns
Delay time DS low to AS high	t4	40			ns
DS low period	t5	200			ns
DS high to R/$\overline{W}$ low setup time	t6	10			ns
R/$\overline{W}$ hold time	t7	10			ns
$\overline{CE}$ setup time	t8	20			ns
$\overline{CE}$ hold time	t9	0			ns
Address setup time	t10	30			ns
Address hold time	t15	30			ns
Data setup time (WR)	t11	110			ns
Data hold time (WR)	t12	30			ns

ROM/EPROM INTERFACE

The MA818 requires 8 bit waveform amplitude data to generate output signals. This data is stored in an external 2K × 8 ROM/EPROM, and connected to the MA818 via pins 25 to 39.

A.C. REQUIREMENTS

Parameter	Conditions	Min	Unit
Address to data valid	10MHz clock; 25°C	1.6	μs

REGISTER FUNCTIONS

The MA818 has five Write Only registers, R0–R4. R0, R1 and R2 each hold 8 bit data, while R3 and R4 are 'dummy' registers. Writing to R3 and R4 transfers the data held in registers R0–R2 to the 24 bit Control and Initialisation registers respectively. Hence data is entered byte by byte into the temporary registers via the MOTEL interface and then loaded in parallel into the appropriate 24 bit 'active' register. This method has been employed to allow input data to span 8 bit boundaries as in the case of the 12 bit Power Frequency Select word.

The registers are selected by the address lines AD0, AD1 and AD2.

Register	Function
R0	Temporary Storage (bits 7– 0 of 24 bit word)
R1	Temporary Storage (bits 15– 8 of 24 bit word)
R2	Temporary Storage (bits 23–16 of 24 bit word)
R3	Transfer R0–R2 to the 24 bit Control register
R4	Transfer R0–R2 to the 24 bit Initialisation register

Fig. 4 shows the way in which each register is addressed.

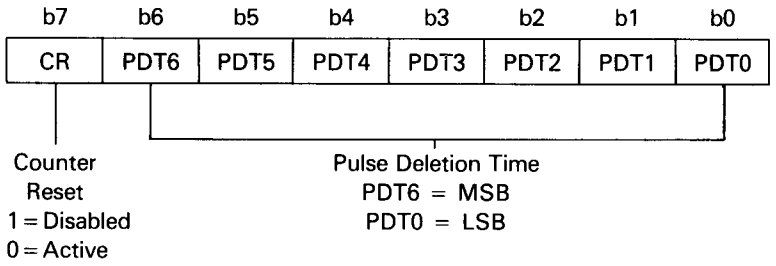
A0	A1	A2	Register	Comment
0	0	0	R0	Temporary register R0
0	0	1	R1	Temporary register R1
0	1	0	R2	Temporary register R2
0	1	1	R3	Transfers Control data
1	0	0	R4	Transfers Initialisation data

INITIALISATION REGISTER

The 24 bit Initialisation register contains parameters which, under normal operation, will be defined during the power up sequence. Variables such as the Pulse Deletion Time and Pulse Delay Time are defined for the particular drive circuitry employed. Changing these parameters during a PWM cycle is therefore not recommended. Information in these registers should only be modified whilst $\overline{RST}$ is active (low), so that the PWM outputs are inhibited (low) during the updating process.

Data is transferred to the Initialisation register from the temporary registers R0, R1 and R2 by performing a write to the 'dummy' register R4. It is recommended that all three temporary registers are updated before writing to R4 in order to ensure that a conformal set of data is transferred to the Initialisation register for execution.

Register 0 INITIALISATION



COUNTER RESET (CR)

Register 0 bit b7

The Counter Reset when active (low) sets the internal power frequency phase counter to 0 (i.e. zero degrees) for the red phase. The power frequency is now set to 0 and cannot be changed via the normal frequency control. The rest of the chip performs as required — producing PWM as defined by the data fed in from the waveform store.

PULSE DELETION TIME (PDT) **Register 1 bits b0–b6**

A pure PWM sequence produces pulses which vary in width from 50% duty cycle to duty cycles of 0% and 100%. Therefore, in theory, pulse widths can become infinitesimally small. In practice this causes problems in the power switches due to storage effects, and therefore a finite pulse width time is required. To eliminate short PWM pulses the true PWM pulse train is passed through a pulse deletion circuit. The pulse deletion circuitry, with its preset minimum pulse width, measures incoming pulse widths and if a pulse exceeds the minimum width it is passed through unaltered, otherwise the pulse is deleted.

The minimum allowable pulse width is defined by the clock frequency, the CFS 3 bit word and the 7 bit Pulse Deletion Time word (PDT). The numerical value of the Pulse Deletion Time is defined by:

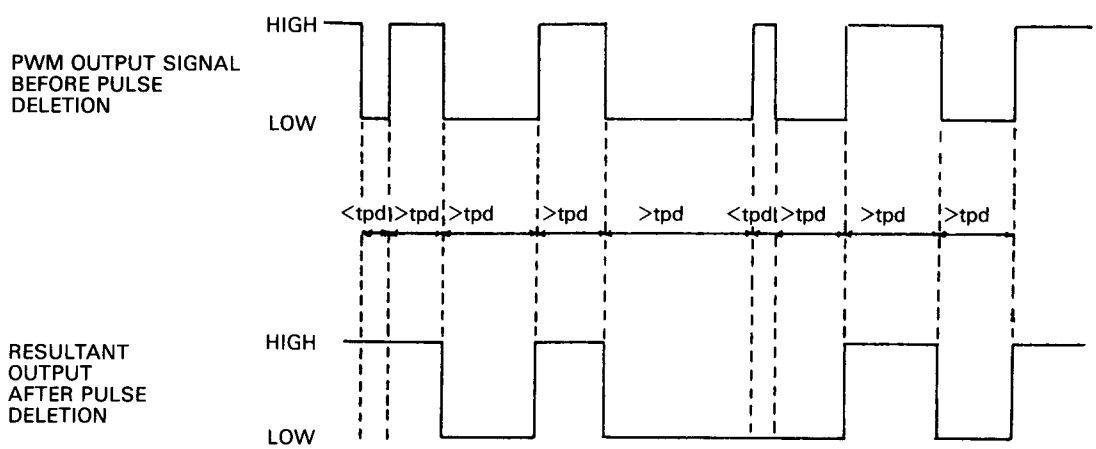
Pulse Deletion Time = $(1/k) \times n \times pdt$ Seconds

where pdt = 1, 2, 3, 4, 5, etc. to 128 as set by PDT

k = clock frequency

n = 1, 2, 4, 8, 16 or 32 (as set by CFS)

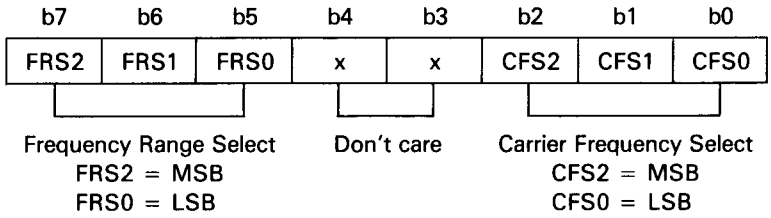
PDT word	1111111	1111110	...etc...	0000000
Value of pdt	1	2	...etc...	128



tpd = minimum pulse width allowable

Fig. 5 Pulse Deletion

Register 1 INITIALISATION



FREQUENCY RANGE SELECT (FRS) **Register 1 bits b7–b5**

The frequency range select word sets the range of the 12 bit Power Frequency Select (PFS) control word. The numerical value of the power frequency is defined by:

Power Frequency = $k/1024/192 \times (f/4096) \times (m/n)$ Hz

where f = decimal value of 12 bit power frequency select word (PFS)

m = 1, 2, 4, 8, 16,32 or 64 (as set by FRS)

k = clock frequency

n = 1, 2, 4, 8, 16 or 32 (as set by CFS)

FRS word	110	101	100	011	010	001	000
Value of m	64	32	16	8	4	2	1

A typical frequency range for ultrasonic operation is achieved with a 10MHz clock, CFS = 000, and FRS = 001. This produces a power frequency range of 0 to 101.7Hz with a resolution of approximately 0.025Hz using all 12 bits of the PFS word.

CARRIER FREQUENCY SELECT (CFS) — Register 1 bits b0–b2

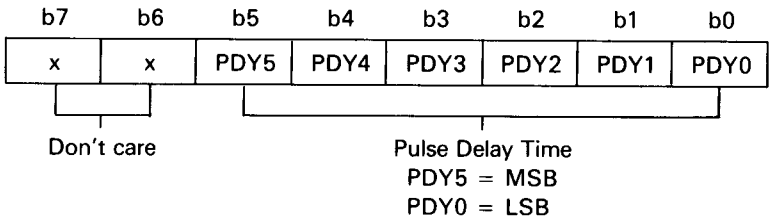
The carrier frequency is determined by the external clock frequency and the 3 bit control word set during initialisation. Numerically:

Carrier Frequency = k/512/n Hz
where k = clock frequency
n = 1, 2, 4, 8, 16 or 32 (as set by CFS)

CFS word	101	100	011	010	001	000
Value of n	32	16	8	4	2	1

Example: For ultrasonic operation, selecting a clock frequency of 10MHz and CFS = 000 (binary), results in a carrier frequency of approximately 19.5kHz

Register 2 INITIALISATION



PULSE DELAY TIME (PDY) — Register 2 bits b0–b5

The pulse delay time word affects all six PWM outputs identically, and is normally set during the initialisation process. Each output phase requires two control signals, one for the top switch connected to the positive inverter D.C. supply and one for the bottom switch connected to the negative inverter D.C. supply. The states of these two switches are complementary. However, when changing the state of the output pair it is desirable to provide a delay period, during which both outputs are off, in order to avoid a short circuit through the switching elements. This delay is sometimes referred to as 'Underlap' and is determined, on the MA818, by the clock frequency, the 3 bit CFS word and the 6 bit PDY word.

The numerical value of this delay is defined by:

Pulse Delay Time = $1/k \times n \times pdy$ Seconds
where pdy = 1, 2, 3, 4, 5, etc. to 64 (as set by PDY)
k = clock frequency
n = 1, 2, 4, 8, 16 or 32 (as set by CFS)

PDY word	111111	111110	...etc...	000000
Value of pdy	1	2	...etc...	64

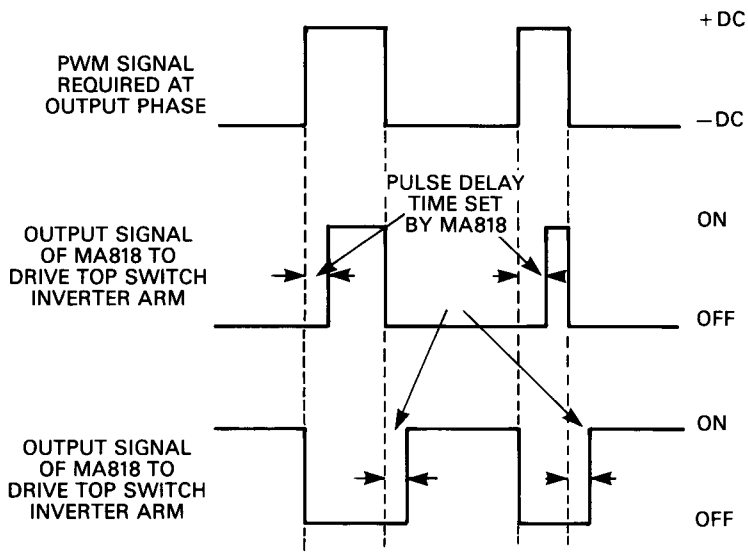
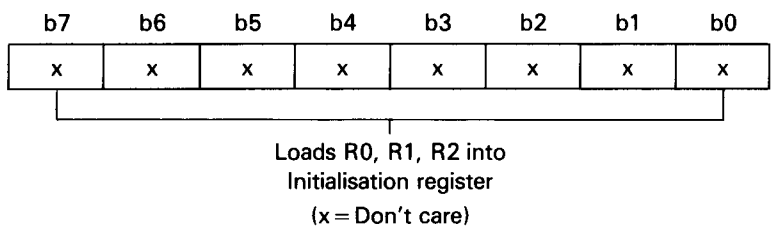


Fig. 6 Effect of Pulse Delay Logic

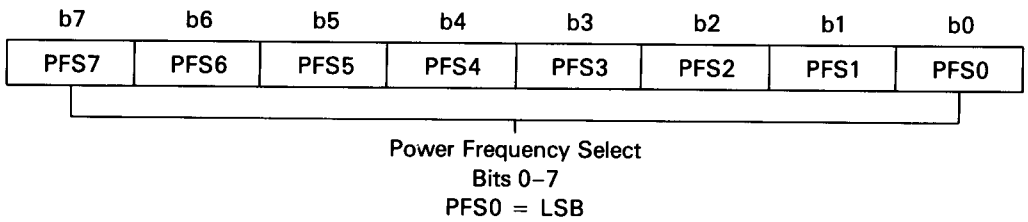
REGISTER 4



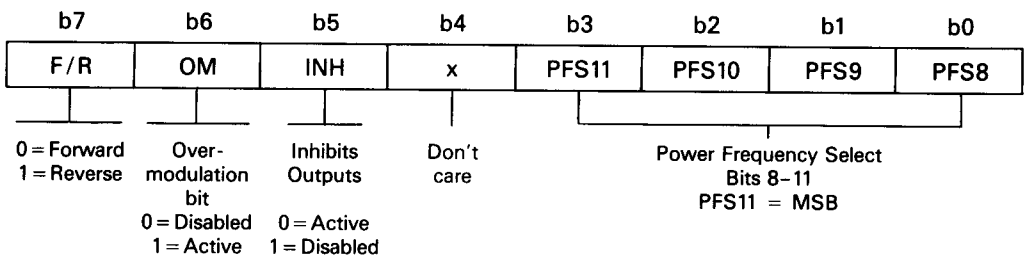
CONTROL REGISTER

This 24 bit register contains the parameters that will normally be modified during PWM cycles. Typical variables in this category include amplitude, forward/reverse selection, power frequency (speed), etc. As with the initialisation register, data is written into the temporary registers R0, R1 and R2, but the transfer of the data to the 24 bit 'active' register is instigated by performing a write to the 'dummy' register R3 (not R4). It is recommended that all three temporary registers are updated before writing to R3 in order to ensure that a conformal set of data is transferred to the control register for execution.

REGISTER 0 CONTROL



REGISTER 1 CONTROL



POWER FREQUENCY SELECT (PFS) **Register 0 Register 1 bits b0–b3**

The power frequency is controlled by three separate control words, namely, CFS (3 bit), FRS (3 bit) and the 12 bit PFS word. Both the CFS and FRS words form part of the initialisation word and their function is described in detail under the initialisation register heading. The 12 bit PFS register spans temporary registers R0 and R1 and it is therefore essential that both these registers, (together with R2), are updated with the new 12 bit frequency word before writing to R3. The numerical value of the power frequency is given below:

$$\text{Power Frequency} = k/1024/192 \times (f/4096) \times (m/n)\ \text{Hz}$$

where f = decimal value of 12 bit power frequency select word (PFS)
m = 1, 2, 4, 8, 16, 32 or 64 (as set by FRS)
k = clock frequency
n = 1, 2, 4, 8, 16 or 32 (as set by CFS)

OVERMODULATION SELECT (OM) **Register 1 bit b6**

The overmodulation bit is, in effect, the ninth bit (MSB) of the amplitude word. When set (high) the output waveform will be controlled in the 100% to 200% range by the amplitude word. The percentage amplitude control now becomes:

$$\text{Amplitude} = (256 + A)/255 \times 100\%$$

where A = decimal value of the 8 bit AMP word

INHIBIT **Register 1 bit b5**

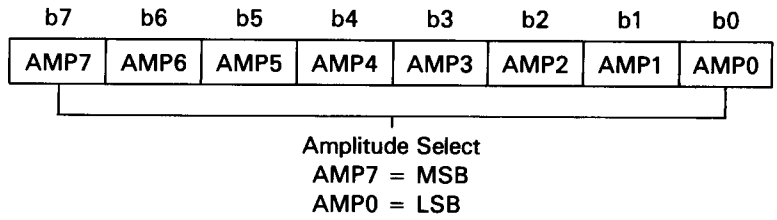
The output inhibit when active (low) sets all the PWM outputs to the off (low) state. No other internal operation of the device is affected. When inhibit is released PWM outputs continue immediately. Note pulses shorter than the minimum pulse width may be produced initially. This is because inhibit is asserted after the pulse delay and pulse deletion circuitry.

FORWARD/REVERSE (F/R)

Register 1 bit b7

The phase sequence of the required three-phase output waveforms is controlled by this bit. The actual effect of changing the state of this bit is to reverse the power frequency phase counter from incrementing the phase angle to decrementing it (or vice versa). The required output waveforms are all continuous with time during a forward/reverse change. In the forward mode the output phase sequence is red-yellow-blue whereas in the reverse mode the sequence is blue-yellow-red.

REGISTER 2 CONTROL



AMPLITUDE SELECT (AMP)

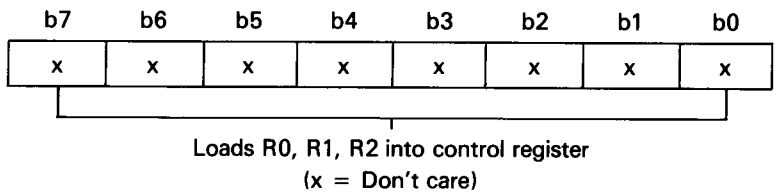
Register 2 bits b0–b7

The amplitude of the waveform can be controlled by the amplitude word, the over modulation bit and the waveform stored in the external ROM/EPROM. The MA818 reads the data from the waveform store, which has been defined over the amplitude range 0 to 255, and scales it according to the value stored in the amplitude select word. Thus the percentage of amplitude control is equal to:

$$\text{Amplitude} = A/255 \times 100\ \%$$

where A = decimal value of the 8 bit AMP word

REGISTER 3



HARDWARE I/O FUNCTIONS

Set Output Trip (SET TRIP) **Pin 24 (Input)**

When SET TRIP is taken to a logic high, the output trip latch is activated. This results in the output $\overline{\text{TRIP}}$ and the six PWM outputs being forced to a low state. This condition can only be cleared by the rising edge of the RESET signal.

Note: SET TRIP overrides the action of RESET such that the state of the output trip latch cannot be changed whilst SET TRIP is active (high).

This input is provided to allow an external source to override the microprocessor and provide a rapid shutdown facility. For example, logic signals from overcurrent sensing circuitry and the microprocessor 'watchdog' might be used to activate the SET TRIP input.

Reset ($\overline{\text{RST}}$) **Pin 12 (Input)**

Reset is active low and performs the following functions:

(1) Forces all the PWM outputs to a low state (thereby turning off the drive switches in the bridge).

(2) Resets all internal counters to zero. (This corresponds to 0° for the red phase output.)

(3) When released, the rising edge resets the output of the output trip latch such that the output SET TRIP is set to a high state and PWM waveforms are available from the six output pins. (This assumes SET TRIP is inactive, i.e. low.)

Note: RESET does not affect the contents of the registers R0, R1 and R2, or the contents of the 24 bit Initialisation and Control registers.

Output Trip Status ($\overline{\text{TRIP}}$) **Pin 15 (Output)**

The $\overline{\text{TRIP}}$ output indicates the status of the output trip latch and is active low.

Zero Phase Pulse (ZPP) **Pin 16 (Output)**

The ZPP is an output whose frequency is equal to that of the power frequency and has a mark-space ratio of 1:2. When the device is in the forward mode of operation, the falling edge (rising edge for reverse mode) of ZPP corresponds to 0° for the red phase output.

Clock (CLK) **Pin 13 (Input)**

The clock input waveform should conform to TTL specifications with a frequency in the 0–10MHz range and a mark-space ratio of 1:1 (±20%).

WAVEFORM DEFINITION AND STORAGE

The waveform amplitude data used to construct the PWM output sequences is held in an external ROM/EPROM. This enables the user to define the exact waveform amplitude required. Good resolution and hence accuracy of the stored waveform is achieved whilst using a standard 2K × 8 ROM/EPROM and taking up a minimum of 15 I/O pins. The way in which data is stored is also optimised. It has been assumed that the data is symmetrical around the 90° axis and positive in amplitude throught the 0° to 180° span. The MA818 uses these samples to calculate the three instantaneous amplitudes for the three phases. The waveform amplitude data consists of 768 8 bit amplitude samples. Each one is linearly spaced over the 0° to 180° range. The angular resolution is therefore approximately 0.2°.

Pin count is minimised by using only 4 of the 8 ROM/EPROM data lines. The most significant nibble D7–D4 are not used and therefore may be left unprogrammed. The 8 bit data is obtained by accessing two 4 bit nibbles.

Waveform Segment (degrees)	Sample Address (ROM/EPROM)
0 - 58.8	0 - 255
60	256
60.2 - 119.8	257 - 511
120	512
120.2 - 179.8	513 - 767

Fig. 7 180° of the 360° cycle is divided into 768 8 bit samples

These are then concatenated internally by the MA818. This results in the 768 8 bit samples being stored as 1546 4 bit samples. Figure 8 illustrates the method in which the waveform data is mapped in the waveform store. The least significant nibble is stored sequentially from location 0H to 300H, whilst the most significant nibble is stored from 400H to 700H. In effect, address line A10 is used to select the high and low nibbles of the waveform amplitude byte.

Note: Sample 768 is not stored in the waveform store as this value is the same as the value stored in sample 0 (i.e. the value at 0° and 180° have identical amplitudes). (F.H.).

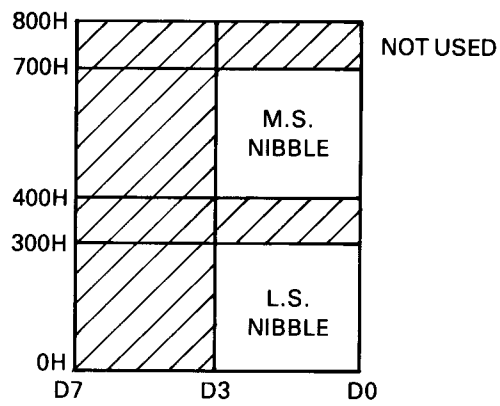


Fig. 8 ROM/EPROM Memory Map

APPLICATION DIAGRAM

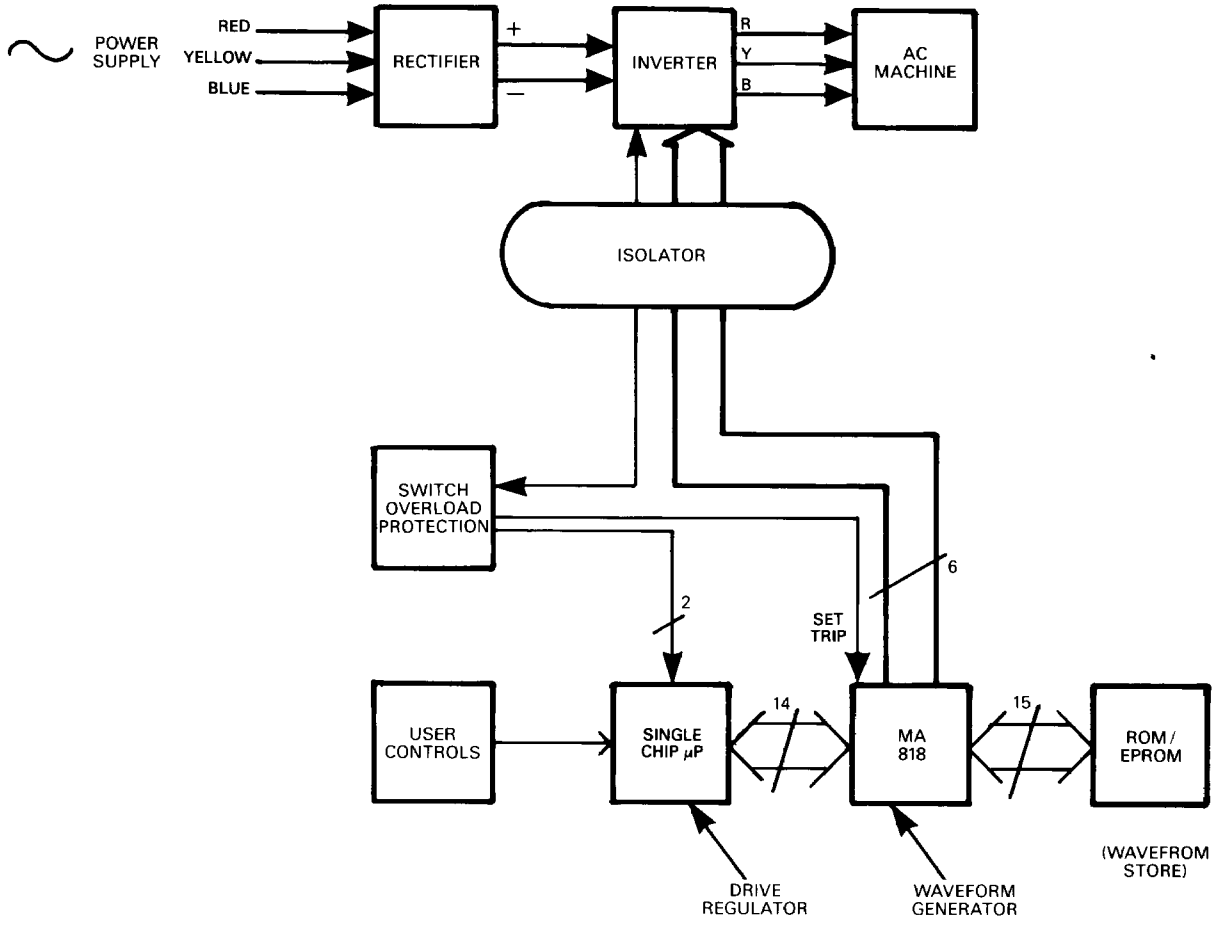
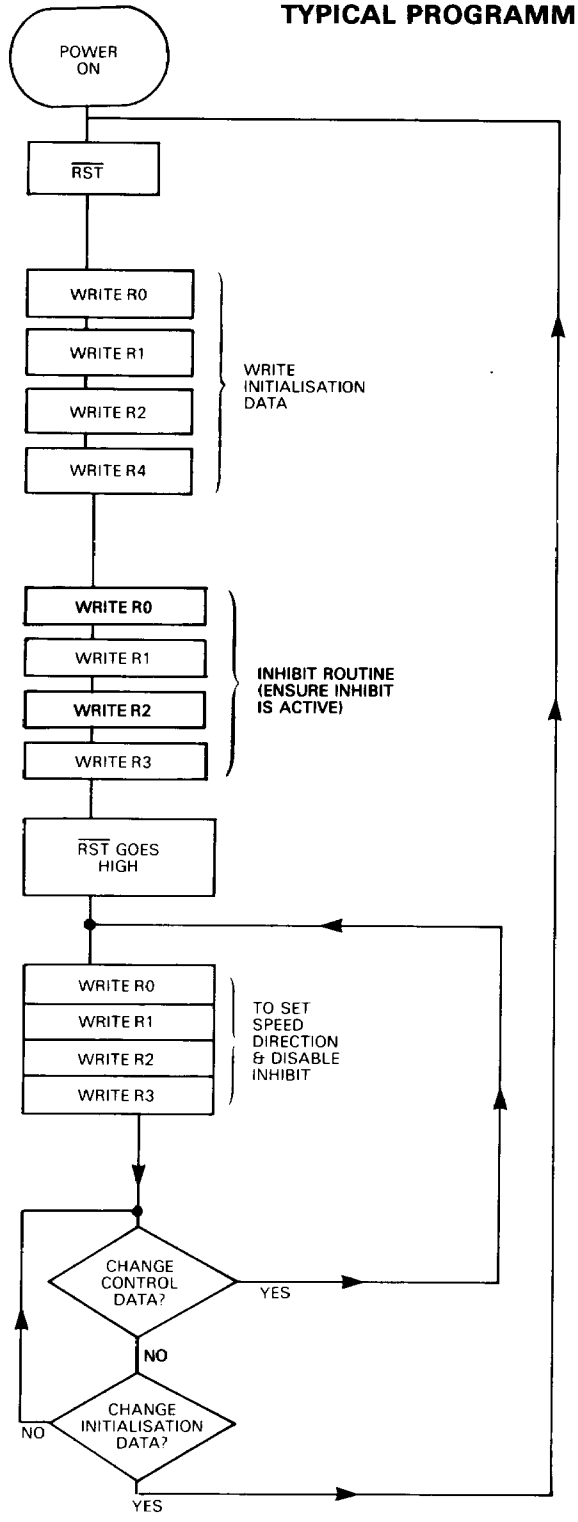


Figure 9

TYPICAL PROGRAMMING ROUTINE FOR MA818



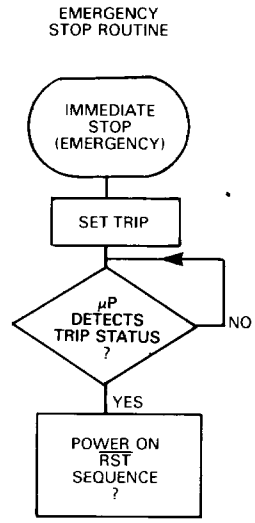


Figure 10