Power Management Bias Controller/Sequencer Supply :-6V, +5V

MABC-11040B
Rev V2

Features

- Quad Output I²C programmable analogue outputs using 12bit DACs with rail to rail output voltage range
  - High output current capability +100mA / -60mA
  - Programmable gate-current limit
  - I²C clock rates up to 400kHz
- Internal and external temperature sensor supporting temperature compensation in application
- Built in sequencing with drain bias control support
- Sequenced auxiliary current source
- Internal EEPROM for autonomous operation
- Two 12bit Telemetry ADC inputs
- General purpose GPIO interface
- Optional internal negative voltage generator, generating –5V from the positive 5V supply
- Supply voltage range –6V, 5V

Applications

- GaN FET bias Controller
- HEMT bias Controller
- Circuit Temperature Compensation

The MABC-11040 is a flexible bias generation and temperature supervision IC.

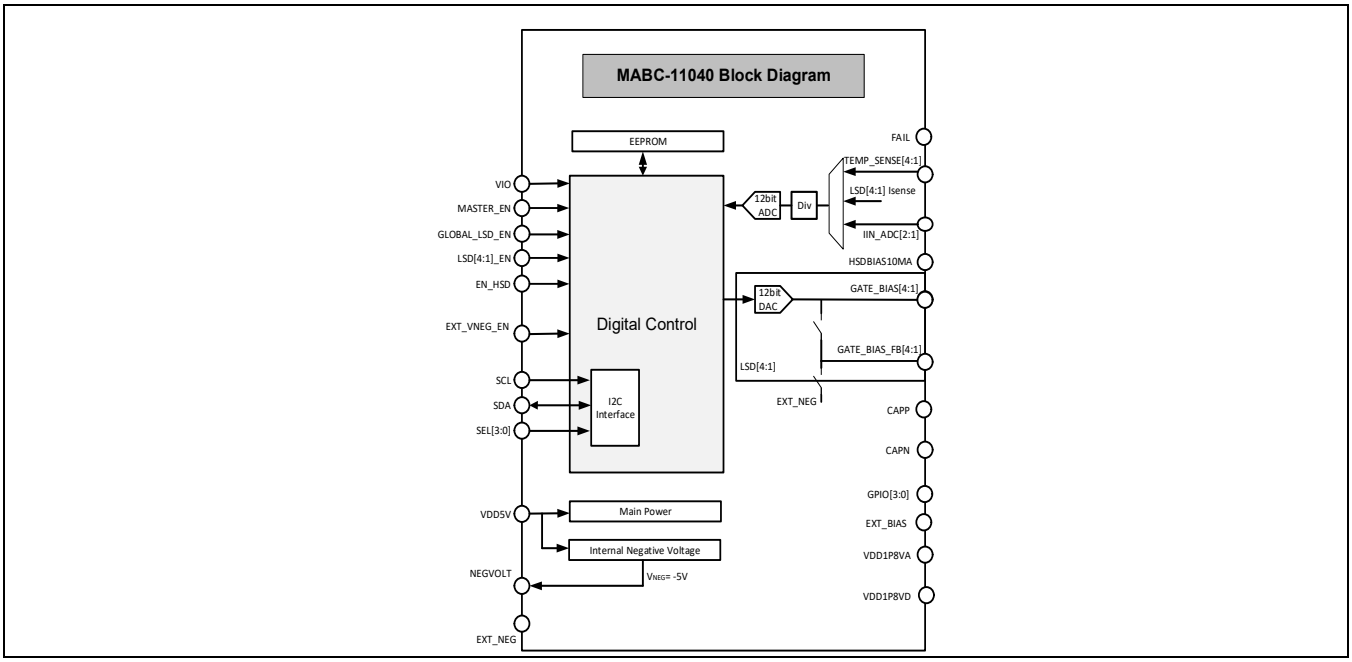
The MABC-11040 contains four highly integrated, temperature-controlled DACs that support a negative output range from -6V to 0V and are capable of handling large output currents. The four DACs can be programmed independently by four separate user-defined temperature-to-voltage functions stored in the internal EEPROM, allowing any temperature effects to be corrected without additional external circuitry. Each output can be switched to the load individually through the use of dedicated control pins.

The MABC-11040 provides bias sequencing for safe power up and power down. The drain voltage may be applied with a control signal via the internal drain bias control once the IC has powered up and correct biasing has been asserted.

Once powered up, the device operates autonomously, without intervention from the system controller, providing a complete solution for setting and compensating bias voltages and currents in control applications. Additionally, the device supports up to four thermistors placed closely to the PAs for more accurate temperature reading.

The digital interface allows control and monitoring of all four Low side drivers, gate current, and temperature of the PA. In addition, the drain current of the PA can be monitored via an external high-side current sense amplifier and an internal ADC.

Functional Schematic



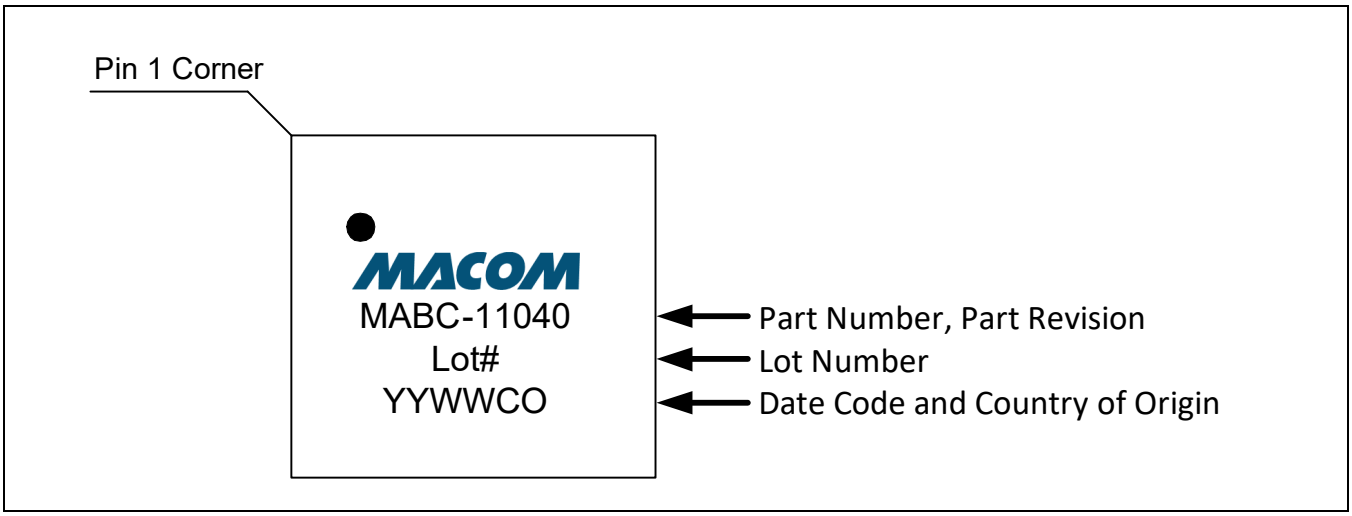
Ordering Information

Part Number	Package	Operating Temperature
MABC-11040B	6 x 6 mm PQFN48	-40°C to +125°C
MABC-11040B-SB1PPR	EVM Kit	-40°C to +125°C

Revision History

Revision	Level	Date	Description
V2	Release	Oct, 2022	Updated pinout and function description; Removed application chapter
V1	Release	May, 2022	Updated Pin-out diagram, Updated electrical specifications
V5P	Preliminary	May, 2021	Updated LSD Current Limit. and Application diagram
V1P	Preliminary	May, 2021	Preliminary Initial release

Figure 1-1. MABC-11040 Marking Diagram



1.0 Electrical Characteristics

Unless noted otherwise, specifications in this section are valid with VDD5V = 5 V, VDD1P8V = 1.8 V, EXT_NEG = -5 V, and an ambient temperature of 25°C.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
VDD5V	Positive Supply Voltage (5V)	1,2			5.5	V
VIO	Digital Power Supply	1,2			3.6	V
EXT_NEG	Negative Analog Voltage Input	1,2	-6.05			V
T_{sold}	Lead Soldering Temperature	1,2			260	°C
$T_{J,ABS}$	Junction Temperature	1,2,3,4			140	°C
C_ldo	Output Capacitor on Pin 23, Pin 43	5			1	uF
T_{Store}	Storage Temperature	1,2,3,4			140	°C
V_{HBM}	Human-body model		-2000	—	+2000	V
V_{CDM}	Charged-device model		-500	—	+500	V
ϑ_{JC}	Thermal resistance junction to paddle	6		2		°C/W
ϑ_{JA}	Thermal resistance ambient to junction	6		15.7		°C/W

NOTE:

1. Exceeding any one or a combination of these parameter limits may cause permanent damage to the device and cause the device to not function properly.
2. MACOM does not recommend sustained operation near these survivability limits
3. Operating with normal conditions with TJ ≤ 150°C will ensure MTTF > TBD hours.
4. Tj, Junction temperature is based on Theta JC (bottom) = 2°C/W.
5. If use internal LDO for 1.8V supply.
6. No airflow

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
VDD5V	Positive Supply Voltage (5V)		4.75	5	5.25	V
VIO	Digital Power Supply		1.65		3.6	V
EXT_NEG	Negative Analog Voltage Input		-6	-5	-4.5	V
I_{VDD5V}	Current consumption in low power mode (MASTER_EN = Low)				9	mA
	Charge pump enable (default setting)	1	--	26	--	mA
	Charge pump disabled	3	-	10	--	mA
I_{VIO}	Current consumption for VIO		0	0.5	1	mA
I_{NEG}	Supply Current from Negative Supply	4	-	16	--	mA
T_j	Operating Junction Temperature	2	-40		125	°C

NOTE:

1. Quiescent current for charge pump is ~2mA/Mhz based on the working frequency. Pin 16 and 17 shorted. Mid code for all LSD,no load, the current on all 5V and VIO. With internal 1.8V Supply.Current sense of LSD off
2. Tj, Junction temperature is based on Theta JC (bottom) = 2°C/W.
3. Charge pump is disabled. Pin 16 and Pin 17 is opened. Mid code and no load on LSD. Measure the current to all positive supply.With internal 1.8V Supply
4. Typical current on EXT_NEG when for MABC11040 With internal 1.8V Supply

Table 1-3. Electrical Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
		Low Side Driver				
R_{STAB}	Stability Resistance			0.5		Ω
TLSD_RDY	Response time from power on to all LSD_rdy with load capacitor=10uF			10		msec
VCPRI	Output Voltage Ripple on charge pump	2		50		mV
VLDRI	Output Voltage Ripple on charge pump	1		0.2	150	mV
BW_LSD	-3 dB Bandwidth of LSD	3	72			KHz
Cstab	Stability capacitance	1	1	10		uF
GERR_SOURCE_M1V	Gate Control Voltage Error Over iload sourcing current, process & mismatch variation @ -1V		-49			mV
GERR_SOURCE_VNEG_PLUS_1V	Gate Control Voltage Error Over iload sourcing current, process & mismatch variation @ VNEG+1V		-62			mV
GERR_SINK_M1V	Gate Control Voltage Error Over iload sinking current, process & mismatch variation @ -1V				27	mV
GERR_SINK_VNEG_PLUS_1V	Gate Control Voltage Error Over iload sinking current, process & mismatch variation @ VNEG+1V				44	mV
VLD_RES	Adjustable Gate Control Voltage Resolution	3,4		1.2		mV
NOTE: 1. -10mA to 6mA load. 2. Cfly=1uF, Cout=22uF, load of charge pump<150mA. 3. Clsd=10uF. 4. Minimum capacitance required for on-chip OPAMP stability/ 5. 10µF at FAST_CHARGEx /10nF at GATE_BIASx, measured from GLOBAL_LSD_EN or LSD_EN pin transitions to gate bias pin rising from -5V to -1V. 6. 12-bit DAC,depends on feedback resistor accuracy in note 4. 7. 0.1% resistor tolerance between the feedback resistor of LSD versus the resistor on ext_bias pin.						
		LSD Driver Characteristics				
V_{GATE_INT}	Adjustable Gate Voltage using integrated charge-pump	0mA Sourced	1	-VDD5V	0	V
		100mA Sourced		-1		
		60mA Sunk		-4.2		
V_{GATE_EXT}	Adjustable Gate Voltage using external charge-pump	0mA Sourced	2	EXT_NEG	0	V
		100mA Sourced		-1		
		60mA Sunk		EXT_NEG+ 0.8		

Table 1-3. Electrical Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
V_{HRMN}	Headroom voltage from LSD_DRV/LSD_DAC to negative voltage	0mA Sourced		10		mV
		100mA Sourced	3	400		
		60mA Sunk		400		
V_{HRMP}	Headroom voltage from GND to LSD_DRV/LSD_DAC, source	0mA Sourced		10		mV
		100mA Sourced	3	400		
		60mA Sunk		400		
NOTE: 1. VDD5V = 5V; Rgate = 6Ω 2. External negative supply = EXT_NEG 3. Including bond wire loss, the chip need such minimum headroom for output to meet the spec						
LSD_DRV Current Characteristics						
ILIMIT	Adjustable Gate Current sourcing Typical Limit		20		110	mA
ILIMITRES_ER	Current Limit Resolution Error			10		mA
LSD_SSD	Slow Shutdown Response Time	1		10		msec
LSD_LRT	Limiter response time (Time constant)			20		usec
NOTE: 1. 10uF output capacitor.						
LSD_DRV Current Sense						
LSD_CUR	Gate Current from LSD1_DRV- LSD4_DRV, Source / Sinking	1	-60		100	mA
LSD_IRES	Gate Current Digitised Readout Resolution (12-bit)			24		uA
LSD_IRES_SINK_ER1	Gate Current Measurement Error	2	-10	0	10	%
LSD_IRES_SINK_ER2	Gate Current Measurement Error	3	-1000	0	1000	uA
LSD_IRES_SINK_ER3	Gate Current Measurement Error	4	-6	0	6	mA
LSD_IRES_SOURCE_ER1	Gate Current Measurement Error	2	-10	0	10	%
LSD_IRES_SOURCE_ER2	Gate Current Measurement Error	3	-1000	0	1000	uA
LSD_IRES_SOURCE_ER3	Gate Current Measurement Error	5	-10	0	10	mA

Table 1-3. Electrical Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
LSD_CUR_RT	Gate Current Measurement Error			750		usec
NOTE: 1. Max total gate current from each LSD drivers 2. System errors all added together, Absolute value of (LSD_CUR)>10mA, output range between (-1V, EXT_NEG+1V) 3. System errors all added together, Absolute value of (LSD_CUR)<10mA,output range between (-1V, EXT_NEG+1V) 4. System errors all added together, LSD_CUR=-60mA,output range between (-1V, EXT_NEG+1V) 5. System errors all added together, LSD_CUR=+100mA,output range between (-1V, EXT_NEG+1V).						
LSD Temperature Sense						
THERM_VRANGE	Input Voltage range for TEMP_SENSEx pins		0		2	V
Fail Alert						
FAIL_RT	Fail alert response time				2	msec
HSD Driver Current Characteristocs						
HSD_CUR_ON	Typical Current bias range for high side driver	1	3	--	10	mA
HSD_CUR_STEP	Eight Steps	1		1		mA
HSD_CUR_OFF	Current sunk at “OFF” state	2	--	--	0.1	mA
HSD_SW	HSD turn on time	3	--	--	10	msec
HSD_CAP	PFET capacitance allowed	4			20	uF
HSD_accuracy	Current accuracy		-5		5	%
NOTE: 1. Current sunk in on state 2. Current sunk in off state 3. Configurable; From EN_HSD pin to voltage on gate bias pin settle 4. no data sheet of PMIC, application note only						
ADC Electrical Specification						
ADC_RANGE	Input Range	--	0	--	1	V
ADC_RES	ADC resolution	--	--	0.244	--	mV
ADC_DNL	DNL		--	1	1	LSB
ADC_INL	INL			10		LSB
ADC_IMP	Input impedance	--	600	--	--	KΩ
ADC_RT	Response time	--	--	1	--	msec
ADC_SR_single	Conversion time, single channel	1	--	0.05	--	msec
ADC_SR_Row	Conversion time, whole channel	2	--	0.75	--	msec

Table 1-3. Electrical Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
ADC_OFF	Input offset	--	--	1	--	mV
ADC_ERROR_FS	ADC error at full scale excitation	--	-1.5	--	1.5	%

NOTE:
1. Sample rate for each channel
2. Sample rate for whole channel

Table 1-4. Control/Interface Logic Static Specifications (EN_HSD, GLOBAL_LSD_EN, MASTER_EN, EXT_VNEG_EN, LSDx_EN, GPIO-3,FAIL)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
VIH	Input Logic High Threshold		0.65*VIO			V
VIL	Input Logic Low Threshold				0.35*VIO	V
Vhyst1	hysteresis of Schmit trigger input(VIH-VIL)		0.05*VIO	0.1*VIO		V
VOH	VOH Output Logic High	1	VIO-0.4			V
VOL	VOL Output Logic Low	2,3			0.4	V
Tdhl	delay from pad to core, high to low	4		8	12	nS
Tdlh	delay from pad to core, low to high	4		8	12	nS
C_{IN}	I/O pins internal capacitance			1.5		pF
I2C_CAP	Board capacitance on I2C nodes	5		65		pF

NOTE:
1. With 3mA sinking load
2. with 3mA source load
3. Fail pin is open drain so only VOL applied to it
4. run with Trise=Tfall=6ns input signal, measure between middle points
5. Total capacitor on the bus should not be higher than 65pF

2.0 Package Outline Drawing, Pinout Diagram, and Pin Descriptions

2.1 MABC-11040 Pinout

Figure 2-1. MABC-11040 Pinout

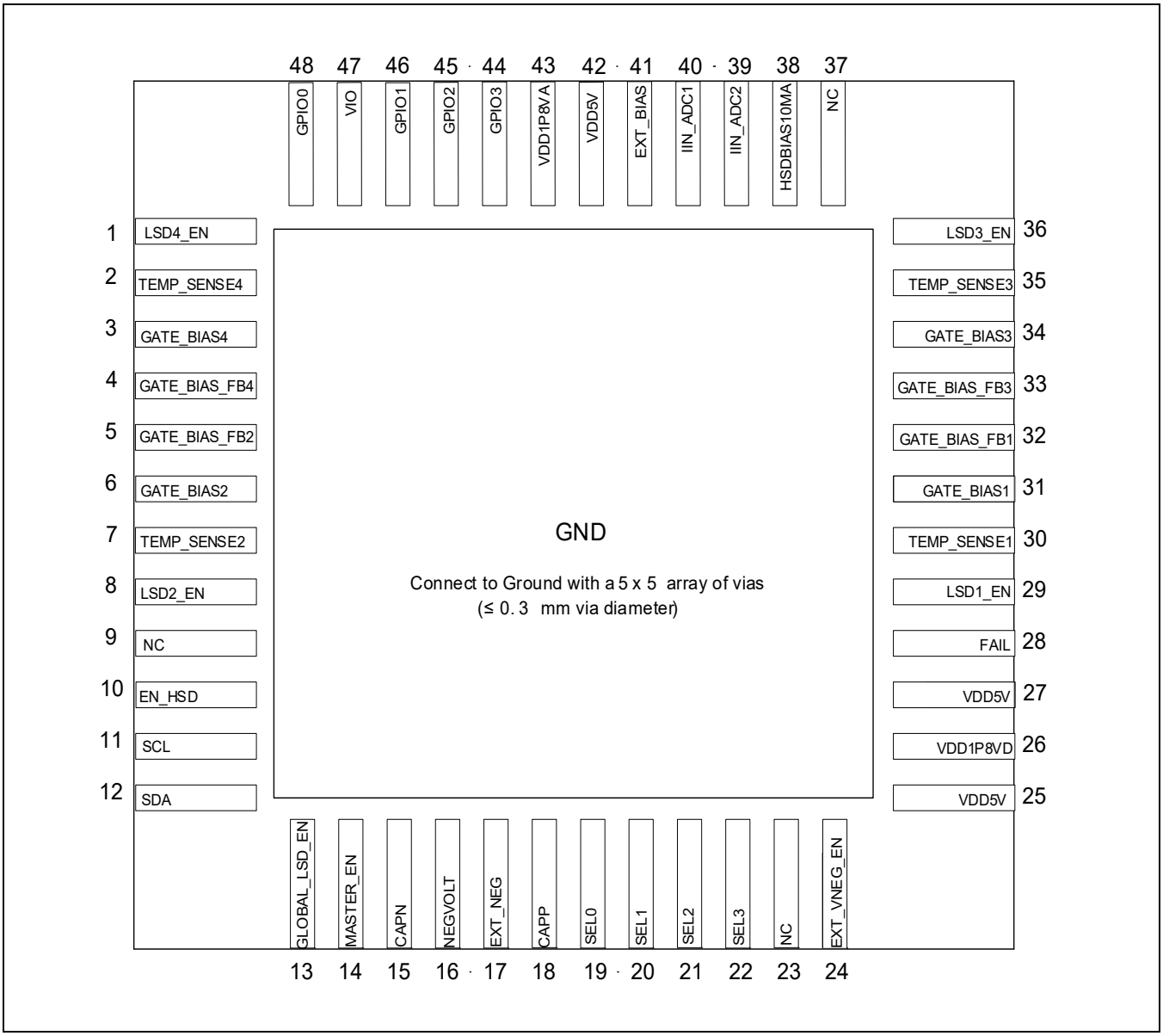


Table 2-1. Pin Configuration

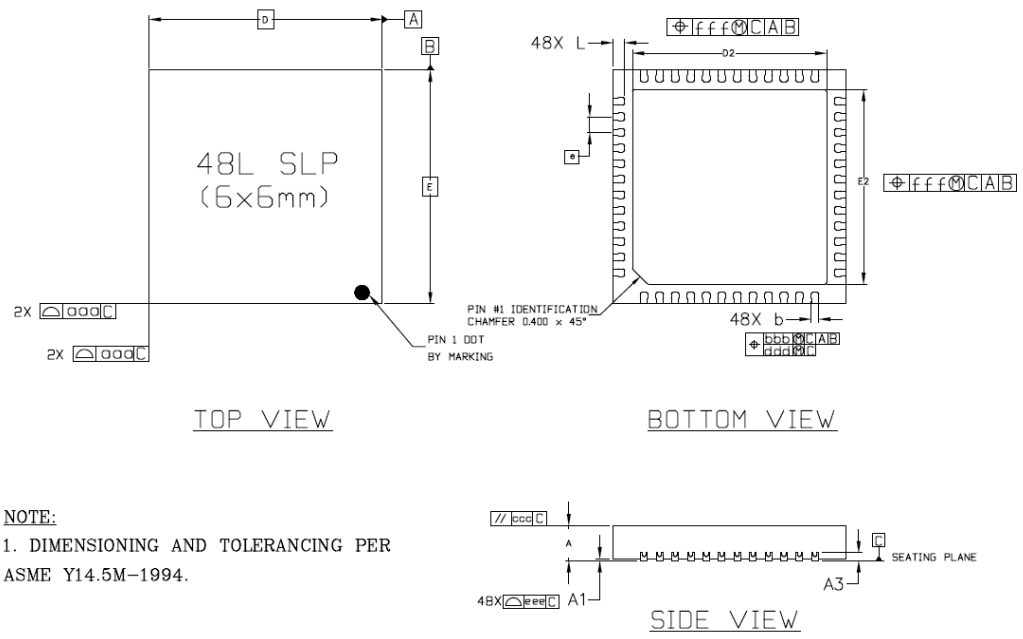
Pin Name	Pin Number	Type	Description
VDD5V	25, 27, 42	Power	5V Power Supply.
VIO	47	Power	GPIO power supply, 1.8V or 3.3V.
EXT_NEG	17	Power	External negative input power supply -6V to -4.5V.
IIN_ADC[2:1]	39, 40	Analog Input	Inputs to internal ADC
EXT_BIAS	41	Analog Input	Connected to external 12.1Kohm 0.1% resistor to Ground.
CAPN	15	Analog Input	Negative terminal for Charge pump capacitor. A 10uF capacitor needed between CAPP and CAPN, 400mA
CAPP	18	Analog Input	Positive terminal for Charge pump capacitor. A 10uF capacitor needed between CAPP and CAPN, 400mA
TEMP_SENSE[4:1]	2, 35, 7, 30	Analog Input	LSD driver[4:1] positive pin for thermistor
NEGVOLT	16	Analog Output	Negative voltage output, -5V typ. Connect to EXT_NEG if internal Charge Pump is used.
VDD1P8VA	43	Analog Output	1.8V internal supply, connect 4.7uF to Ground
VDD1P8VD	26	Analog Output	1.8V internal supply, connect 4.7uF to Ground
GATE_BIAS[4:1]	3, 34, 6, 31	Analog Output	LSD DAC [4:1] 60mA
GATE_BIAS_FB[4:1]	4, 33, 5, 32	Analog Output	LSD feedback
HSDBIAS10mA	38	Analog Output	Predriver current bias pin, 10mA. NMOS Open Drain, cannot exceed +5VDC.
MASTER_EN	14	Digital Input	Master enable signal, internal 85K ohm pull-down. Referred to VIO. H: Normal operation. L: Device in Standby Mode.
EN_HSD	10	Digital Input	External enable pin to enable high side driver, Internal 85K ohm pull-down. Referred to VIO. H: HSD Enabled L: HSD Disabled
GLOBAL_LSD_EN	13	Digital Input	Global LSD Output Enabled, internal 60K ohm pull-up. H: LSD Drivers Enabled L: LSD Drivers Disabled
LSD[4:1]_EN	1, 36, 8, 29	Digital Input	Enable signal of LSD drivers, internal 60K ohm pull-up. This pins overrides pin GLOBAL_LSD_EN H: LSD Driver Enabled L: LSD Driver Disabled
EXT_NEG_EN	24	Digital Input	Enables internal negative supply voltage, internal 60K ohm pull-down. Referred to VIO. H: Internal negative voltage disabled, use external negative power supply to pin EXT_NEG L: Internal negative voltage enabled, internal Charge Pump is enabled.
GPIO[3:0]	44, 45, 46, 48	Digital I/O	General purpose I/O, internal 100k ohm pull up to VIO.

Table 2-1. Pin Configuration

Pin Name	Pin Number	Type	Description
Fail	28	Digital Output	Fail alarm status, Open drain, needs a 10k ohm external pull. Referred to VIO.
SCL	11	Digital Input	I2C Interface SLCK
SDA	12	Digital I/O	I2C Interface SDA
SEL[3:0]	22, 21, 20, 19	Digital Input	I2C slave address selection pin, internal 100k ohm pull-up to VDD5V.
NC	9, 23, 37	No connect	Do not connect, leave floating.

2.2 Package Outline Drawing

Figure 2-2. 6 x 6 mm PQFN48 Package Outline Drawing



NOTE:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

Dimensional Ref.			
REF.	Min.	Nom	Max.
A	0.800	0.850	0.900
A1	0.000	—	0.050
A3	0.203 REF		
D	6.000 BSC		
E	6.000 BSC		
D2	4.050	5.000	5.050
E2	4.050	5.000	5.050
b	0.150	0.200	0.250
e	0.400 BSC		
L	0.250	0.300	0.350

Dimensional Tol.	
aaa	0.050
bbb	0.100
ccc	0.050
ddd	0.050
eee	0.080
fff	0.050

3.0 Functional Description

3.1 Overview

The MABC-11040 is a highly integrated Power Management Integrated Circuit (PMIC) which provides all the features necessary to safely and intelligently sequence and bias a multi-stage GaN Power Amplifier. It consists of a single High Side Driver (HSD), four Low Side Drivers (LSDs), an internal negative charge pump, four general purpose GPIO pins, an integrated temperature sensor, four external temperature sensors, and ADC.

At its core the MABC-11040 is a quad temperature-dependent low side bias generator and drivers (LSD) whose temperature-to-voltage transfer functions are user-defined. This device contains a digitized temperature sensor that addresses four independently programmable look-up tables (LUTs). The outputs of LUTs are sent on to their respective 12-bit DACs to produce four independent output voltages.

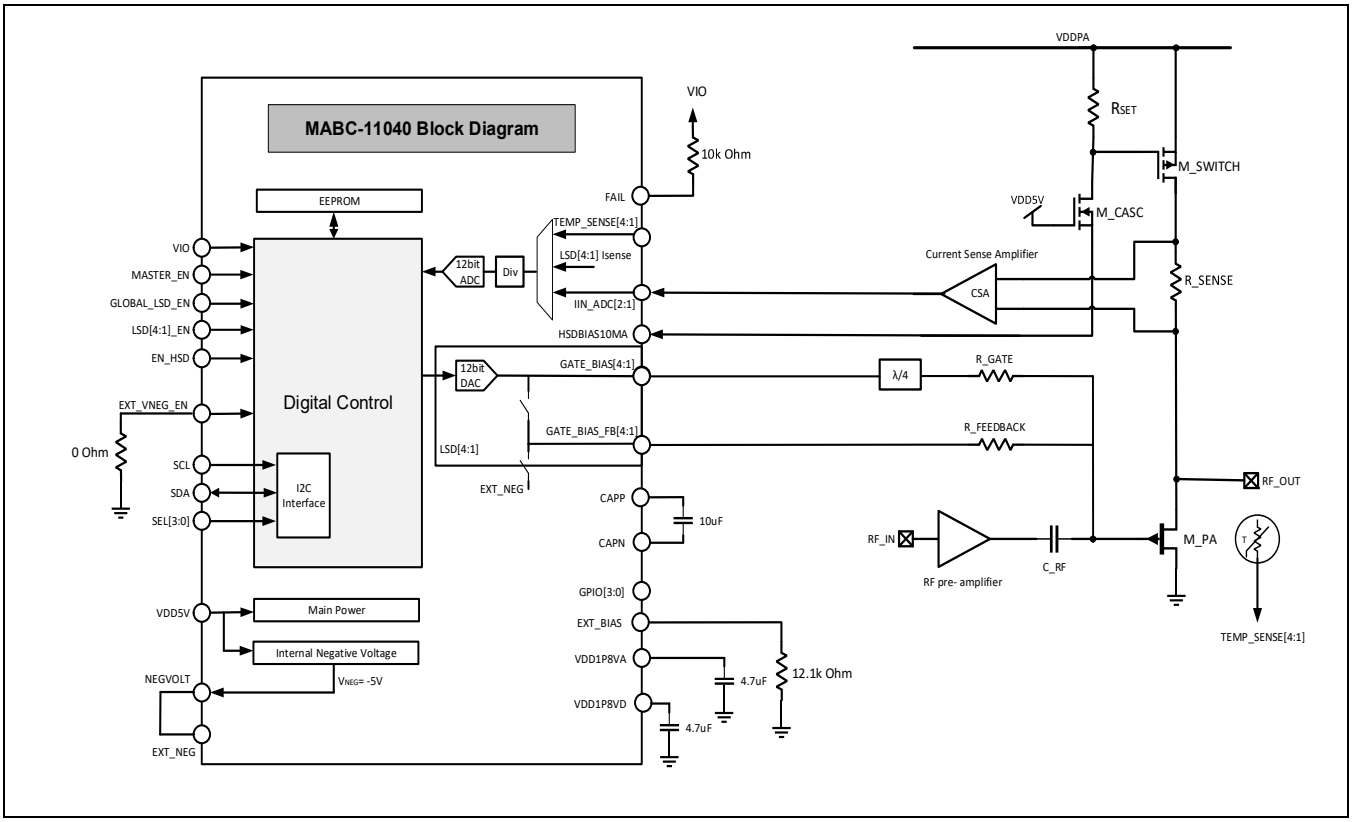
As well as providing four independent LSDs, the MABC-11040 also includes an HSD. The HSD enables an off-chip pass gate, which can be used to correctly sequence all PA biasing.

In applications requiring rapid ON/OFF switching of the bias voltage, the MABC-11040 provides asynchronous control over its outputs. Dedicated digital input pins control analogue output switching. Each LSD can be independently controlled with its dedicated control pin or alternatively all four LSDs can be switched together by a single enable pin. When this pin is set to low then all four LSDs are turned off, and when this pin is set to high, then each LSD is controlled by its own enable control.

All aspects of the device functionality are controlled through internal registers. These registers, and the LUTs, are accessible through the I^2C-compatible interface.

The MABC-11040 can operate autonomously of the system controller, once LUT coefficients have been committed to its EEPROM's non-volatile memory. Upon power up the EEPROM content is automatically transferred to the operating memory, and the device begins to produce the required bias voltages.

Figure 3-1. Functional Block Description



3.2 Device Power up/down

3.2.1 Power up Sequence

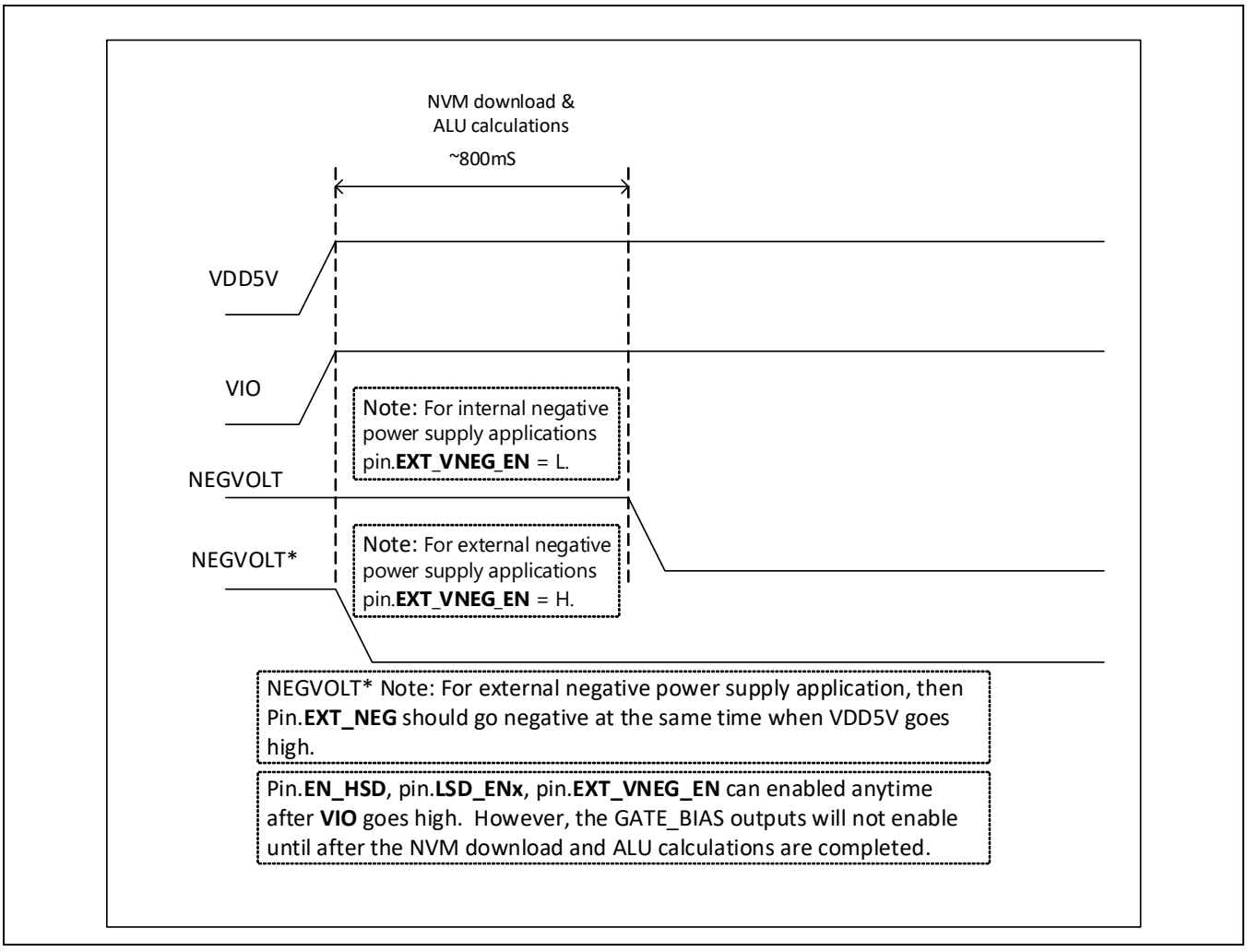
Figure 3-2 shows the recommended power up sequence

VIO should be become enabled at the same time that **VDD5V** is turned on.

If the external negative enable pin is low, the negative supply will turn on after about 800ms the **VDD5V** supplies are turned on.

If an external negative power supply applications, pin.**EXT_VNEG_EN** should be set to High and -5V should be applied to pin.**NEGVOLT** after VDD5V and VIO are enabled. The pin.**EXT_VNEG_EN** should be high and the negative supply will go negative after **VDD5V** is turned on.

Figure 3-2. Power-up Sequencing



3.2.2 Power Down Sequence

It's recommended that the device is disabled with pin.MASTER_EN = LOW before VDD5V and VIO are turned off.

3.2.3 Initial Register Settings

The 50V supply for the GaN (VDD_GaN) should be turned on first, followed by the power up sequence for the MABC-11040(refer to 3.2.1) while pin.**EN_HSD** must be kept low. After power up, load the following passwords to the MABC-11040:

Password for Page0x00h: write Page 0x00h Register 0xFAh with value 0x20h;

Password for Page0x01h/02h: write Page 0x00h Register 0xFBh with value 0x19h;

Password for Page0x80h/ 0x81h: write Page 0x00h Register 0xFCh with value 0x07h;

Password for Page0x90h/91h/92h/93h: write Page 0x00h Register 0xFDh with value 0x04h;

Pin.**EN_HSD** and pin.**EN_LSD[1:4]** should be set to High to enable the LSDs.

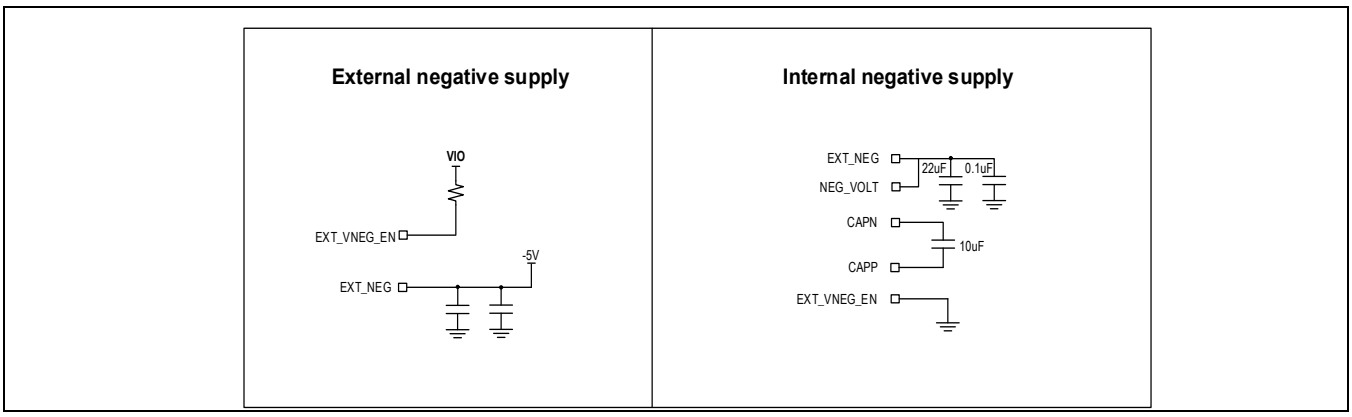
3.2.4 Negative Charge Pump

For applications where there is no negative voltage on the board, MABC-11040B includes a negative charge pump which can invert the positive supply voltage provided to **VDD5V** (the input to the charge pump). The negative pin.internal charge pump requires external bypassing of 22 uF on pin.**NEGVOLT**, and a 10uF fly-back capacitor between **CAPN** and pin.**CAPP**. There is a dedicated external pin.**EXT_VNEG_EN**, which enables or disables the internal charge pump. In the case of using the negative charge pump, **NEGVOLT** and **EXT_NEG** need to be shorted on the PCB.

If an external negative voltage supply is to be used, VDD5V should be applied to the pin.**EXT_VNEG_EN** to disable the internal charge pump and pin.**NEGVOLT** should be connected to GND. If the external negative voltage is used as a supply for LSDs, the negative voltage should turn on at the same time when the **VDD5V** is applied. The pin.**MASTER_EN** will be pulled low at start-up, disabling the internal negative supply.

See Figure 3-3 for the application schematic.

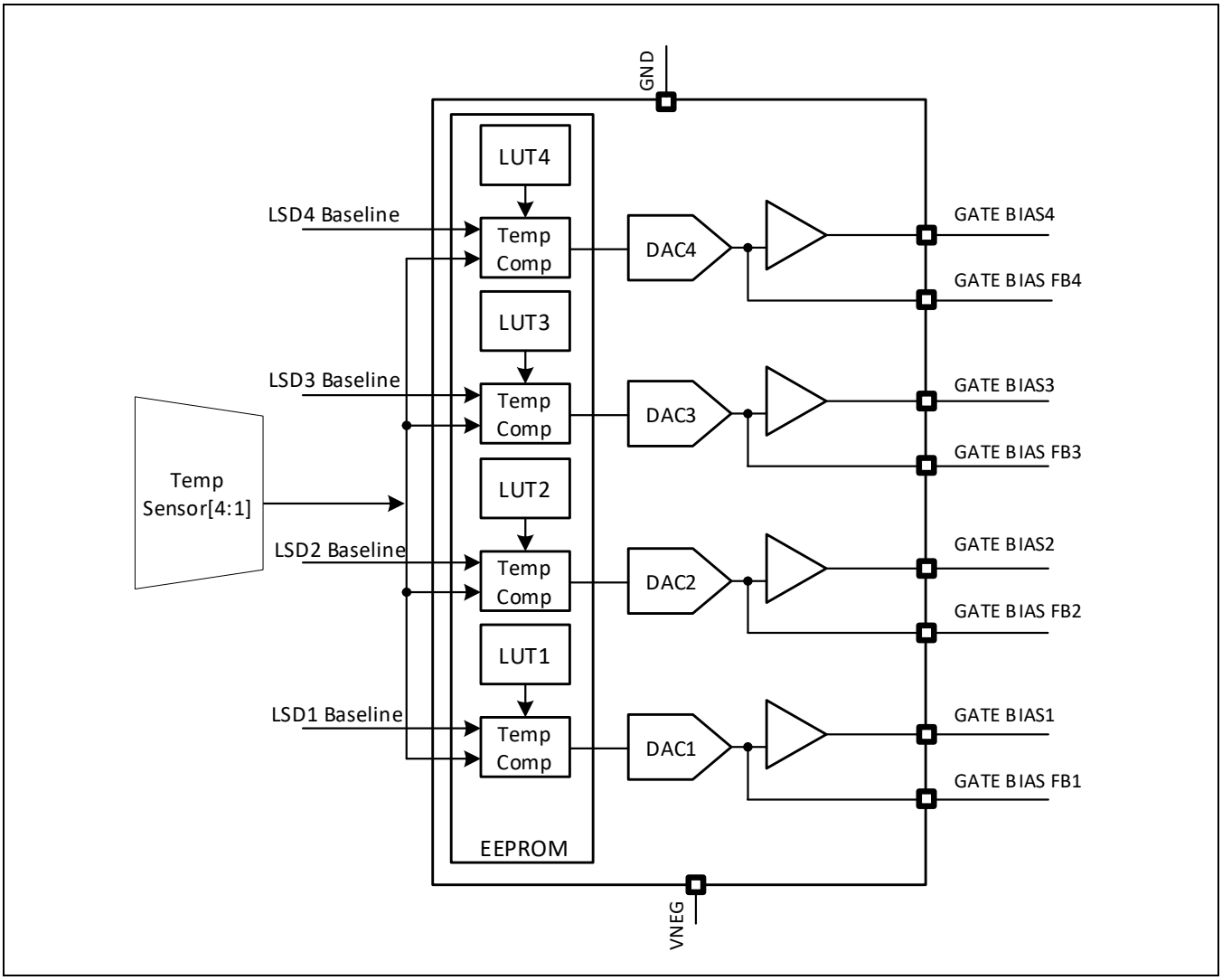
Figure 3-3. Internal and External Negative voltage supply application schematic



3.3 Low Side Driver (LSD)

The Low Side Driver is a DAC that provides a negative voltage for the gate of a GaN device. The Low Sides Drivers are compensated over temperature by means of Look-Up Tables (LUTs), which are stored in an on-chip EEPROM. The negative voltage can be an external power supply or an internal negative charge pump (refer to Section 3.2.4). The LSD can source up to 100mA and sink up to 60mA load with a configurable current limiting threshold.

Figure 3-4. LSD Block Diagram



3.3.1 12-bit DAC

Each LSD has a 12-bit resolution. The output range is equal to the 4*1.22*Rfb/Rext_bias where Rfb is an internal 12.4kohms, Rext_bias is an external 12.1k resistor to ground on pin.EXT_BIAS and 1.22mV is the DAC resolution. The typical output range is 0V to –5V with no resistive load.

For any input DAC word D_{in} in decimal, the ideal output voltage with no resistive load is given by the following equation:

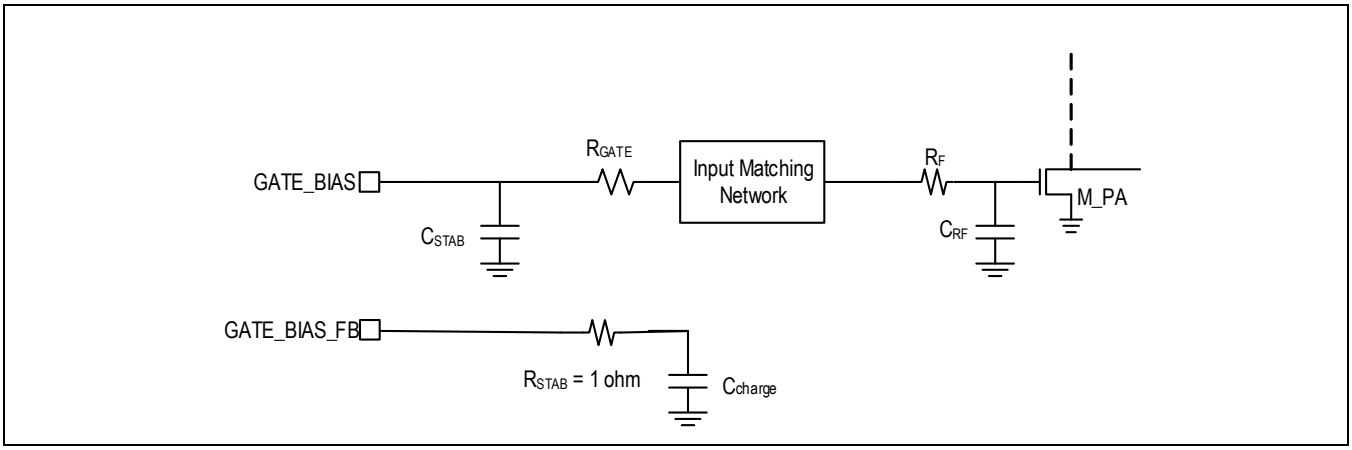
$$V_{OUT} = -5 \cdot \frac{D_{in}}{2^{12} - 1}(V)$$

The upper and lower voltage limits can be programmed by using two registers. For example, LSD1 the upper limit is controlled by registers 0xAA Bits[7:0](MSB) and 0xAC Bits[7:4](LSB); The bottom limit is controlled by registers 0xAE Bits[7:0](MSB) and 0xAF Bits[7:4](LSB)

The LSD is configured as below. The capacitor C_{STAB}, is a stability capacitor, typically around 1-10 µF. The current limiter is also set by the user.Current limit Resistor R_{GATE} should be between 5-10 Ω in value.

The specification for minimum capacitance on the **GATE_BIAS** nodes (C_{STAB}) is associated with the stability of the Low Side Driver. This capacitor also serves in decoupling the Low Side Driver from the RF gate. The default option is to open the integrated feedback resistor loop and use an external feedback resistor. This is done in order to allow the loop to correct the IR drop on resistor R_{GATE}.

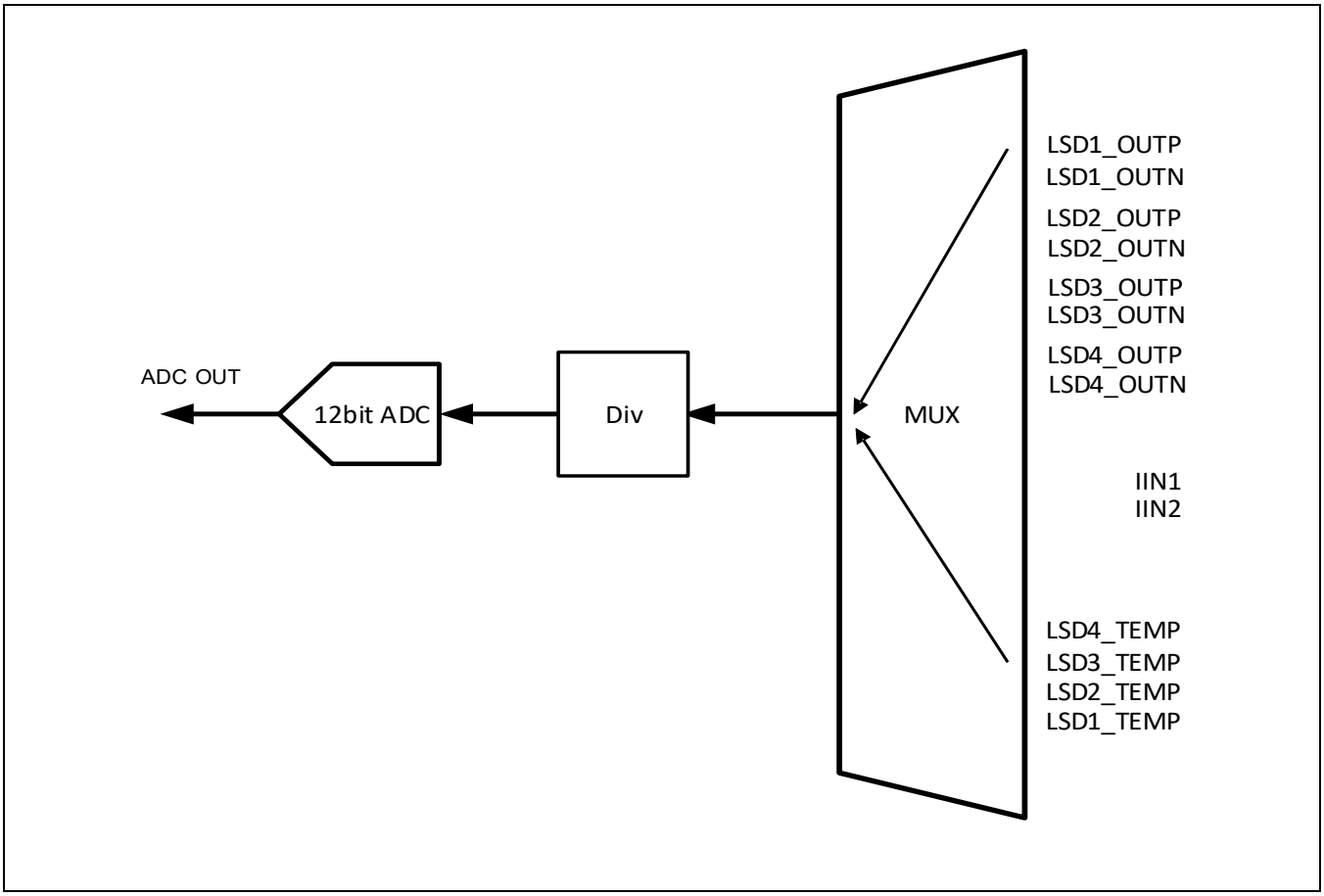
Figure 3-5. LSD_DAC_OUT Application Schematic



3.3.2 12-bit ADC

The device integrates a 12-bit SAR ADC which inputs are configurable by the I^2C. The ADC allows monitoring of the internal temperature sensor, 2 external input pins.**IIN_ADC[2:1]**, all four low side driver gate-currents and all four thermistor input pins.**TEMP_SENSE[4:1]**. The cycling mux has a frequency at 0.75ms.

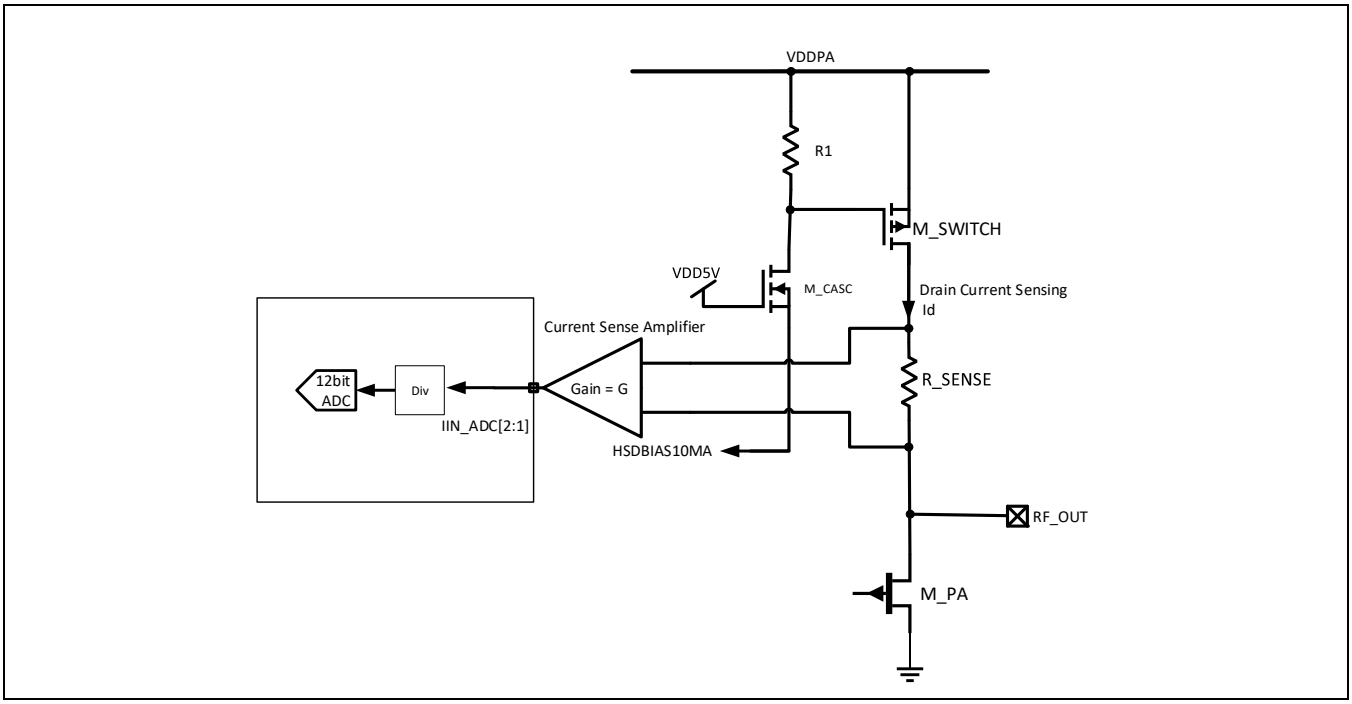
Figure 3-6. ADC Block Diagram



3.3.2.1 LSD Drain Current Sensing Using ADC

The drain current I_d comes out from M_Switch and fed to the 12-bit ADC. A drain current going through R_sense and current sense amplifier to generate the 12bits ADC code. The user needs to ensure that the voltage range at the output of the current-sense amplifier is within the specifications for the ADC input range **IIN_ADC1** and **IIN_ADC2**. This range corresponds to the range of currents, which are expected to be sensed. The voltage range for ADC is 0 to 1V, so I_d*R_Sense*G should not be larger than 1V. The resolution for 12-bit ADC is 2.44mV/LSB. The gain for CSA should be 0.5.

Figure 3-7. Drain Current Sensing Block Diagram

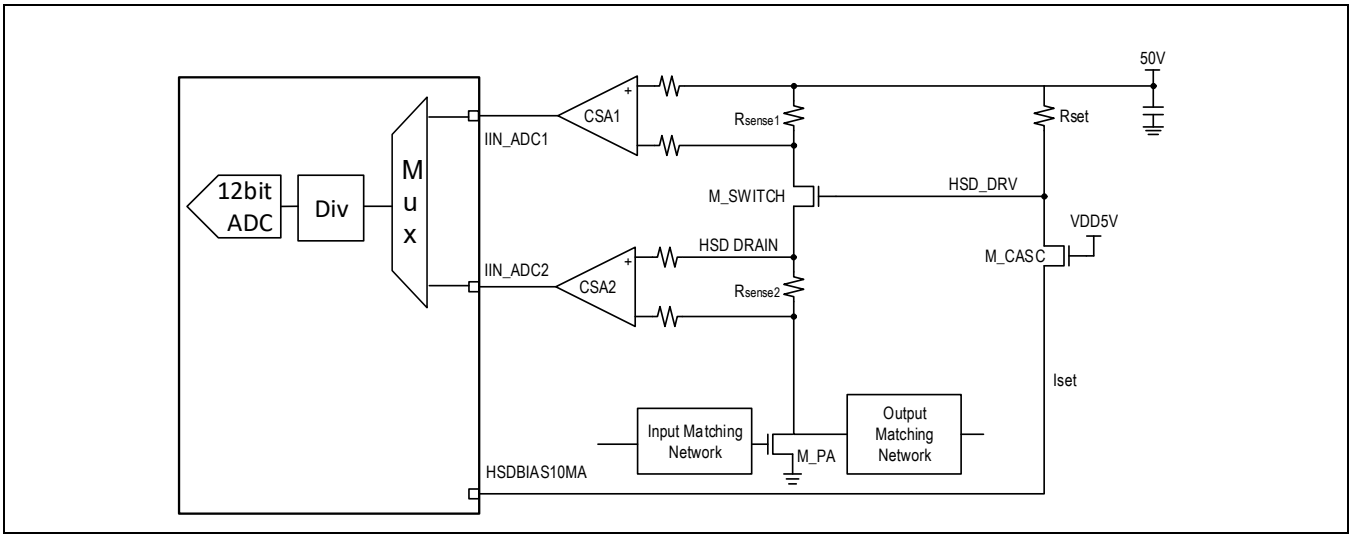


3.3.2.2 LSD Drain Current Sensing Example

A source-sense resistor, R_{sense2}, is placed on the board on the drain of M_SWITCH. This allows the monitoring of the PA current of the output stage, M_PA. An external current-sense amplifier is used to provide a voltage into the IC, which is fed to the ADC and converted to digital signal. A secondary resistor, R_{sense1}, is be placed at the drain of the first two amplifier stages to provide a more accurate current reading.(See Figure 3-8)

There is flexibility in the selection of the current-sense amplifiers and the current-sense resistors. The user needs to ensure that the voltage range at the output of the current-sense amplifier is within the specifications for the ADC input range **IIN_ADC1** and **IIN_ADC2**. This range corresponds to the range of currents, which are expected to be sensed.

Figure 3-8. LSD Drain Current Sensing Schematic



Example of LSD Current-Sense Resistors & Current-Sense Amplifiers

In the table Table 3-1, an example is given that includes a 0.1Ω sense resistor with a maximum drain current of 16 A, and a minimum drain current of 1A. Then the input range of current sense amplifier is Id * R_{sense} from 0.1V to 1.6V. And the gain required from current sense amplifier should be 0.5. The ADC voltage range is from 0V to 1V. As ADC is 12-bit, the voltage resolution is 2.44mV/LSB.

Table 3-1. Example Calculations for HSD Current-Sense Resistors and Current-Sense Amplifiers

Parameter	Variable	Equation	Value	Unit
Id_{MAX}	Id_{MAX}	--	16.00	A
Id_{MIN}	Id_{MIN}	--	1.00	A
Resistor	R_{sense}	--	0.10	Ω
CSA Input voltage for minimum current	$V_{MIN,CSA}$	Id_{MIN}*R_{sense}	0.10	V
CSA Input voltage for maximum current	$V_{MAX,CSA}$	Id_{MAX}*R_{sense}	1.60	v
CSA input voltage range	$V_{range,CSA}$	$V_{MAX,CSA}$-$V_{MIN,CSA}$	1.50	V
Gain required from CSA	$Gain_{CSA}$	$V_{range,ADC}$ / $V_{range,CSA}$	0.500	V/V
ADC minimum voltage	$V_{MIN,ADC}$	--	0	V
ADC maximum voltage	$V_{MAX,ADC}$	--	1.0	V
ADC input voltage range	$V_{range,ADC}$	$V_{MAX,ADC}$ - $V_{MIN,ADC}$	1.0	V
12-bit ADC - voltage resolution	V_{res}	($V_{range,ADC}$ / 2^12)*1000	2.44	mV
Recommend ADC minimum voltage	V_{MIN,ADC_r}	--	0.125	V
Recommend ADC maximum voltage	V_{MAX,ADC_r}	--	0.875	V

3.3.2.3 LSD Gate current sensing Using ADC

The gate current is sensed by integrated current sensors and fed to the 12-bit ADC via the multiplexer. A current reading is provided to the system in the range of –60 to 100 mA.

There are two currents stored for each measurement: the currents in the PMOS and the currents in the NMOS. The output current is the current in the PMOS minus the current in the NMOS. There are four channels of the LSD gate drive currents that are measured. The currents, which are 12 bits, are stored in two registers where the 8 most significant bits are measured in one register, and the four least significant bits are stored in another register.

For example, the 12 bits for the LSD1 PMOS are stored in the 2 registers named CHNL1_MSB and CHNL1_LSB. The 12 bits for the LSD1 NMOS are stored in the 2 registers named CHNL5_MSB and CHNL5_LSB. The total current sent to the LSD1 gate is the difference between the current stored in the 12-bit PMOS registers (I_{PMOS}) and the current stored in the 12-bit NMOS registers (I_{NMOS}).

The accurate current calculation takes into account an adjustment for the internal DAC current, the formula to calculate I_{load} is shown in Figure 3-9.

Figure 3-9. Formula for Calculating Gate Currents

$$I_{PMOS} = \begin{cases} \dfrac{ADC\ Code\ -403}{3.2\ x\ 10} & , ADC\ Code\ \geq 706 \\ \dfrac{ADC\ Code\ -447}{3.2\ x\ 8.55} & , ADC\ Code < 706 \end{cases}$$

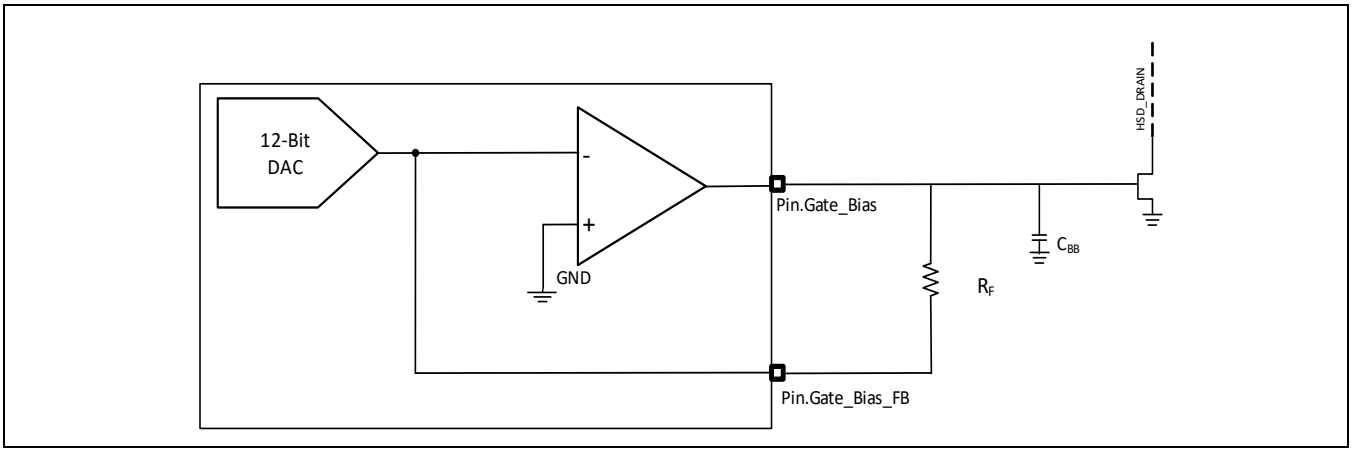
$$I_{NMOS} = \begin{cases} \dfrac{ADC\ Code\ -420}{3.2\ x\ 10} & , ADC\ Code\ \geq 825 \\ \dfrac{ADC\ Code\ -450}{3.2\ x\ 9.26} & , ADC\ Code < 825 \end{cases}$$

$$I_{DAC} = \frac{ADC\ Code}{4095\ x\ 0.4\ mA}$$

3.3.3 Gate Bias Close Loop

In order to have the gate voltage constant, the DAC current I_{DAC}(0-400mA) provided to the LSD is generated on an external feedback resistor R_F. Pin.**Gate_Bias** is connected to an internal amplifier output and provides the negative voltage directly to the gate of the GaN device, while pin **Gate_Bias_FB** is used to connect an external feedback resistor R_F to the negative input of the amplifier.The capacitor C_{BB} connected to node **GATE_BIAS** according to the DAC input control. The equation for voltage at pin.**GATE_BIAS** is $V_{GB} = -I_{DAC}* R_F$. The typical R_F resistor value is 12.5k ± 1% ohms to get the full range of V_{GB}(0-5V).

Figure 3-10. Gate Bias Close Loop Circuit diagran

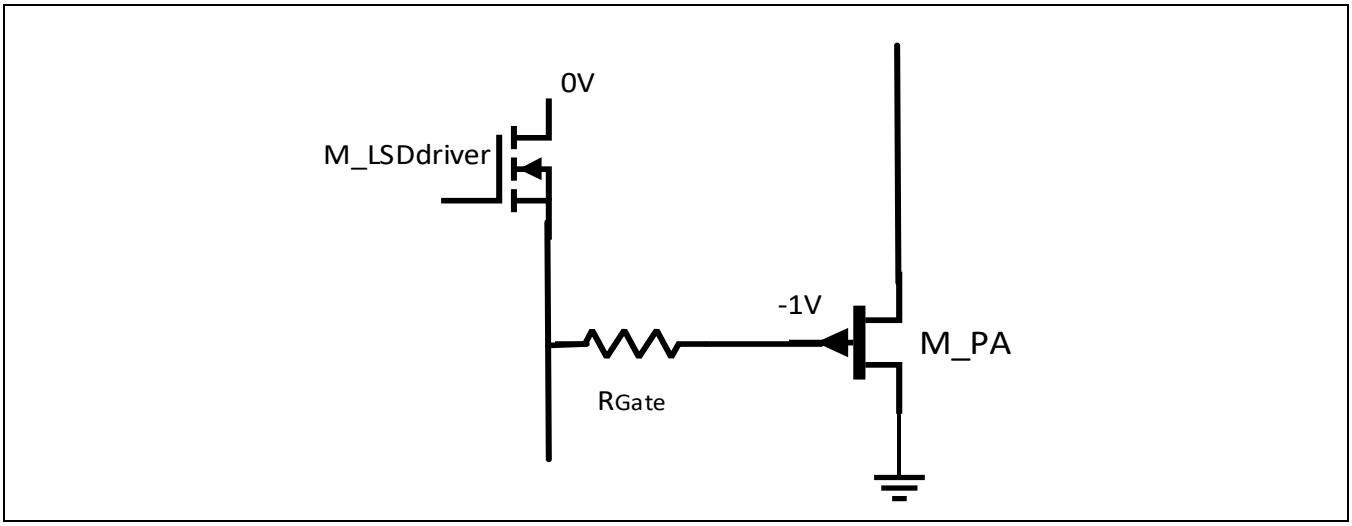


3.3.4 LSD Headroom

Resistor R_{GATE} should be between 5-10 Ω in value. R_{GATE} should be designed to allow for some gate voltage headroom (Figure 3-11).

- Example 1: With 100mA current and 4.99Ω R_{gate}, the voltage on gate resistor is 0.499V. As V_{gate} is 1V. There will be 0.501V on non-gate side of R_{gate}. With 0.4V max LSD headroom. The margin for headroom is 0.101V.
- Example 2: With 100mA current and 5.6Ω R_{gate}, the voltage on gate resistor is 0.56V. As V_{gate} is 1V. There will be 0.44V on non-gate side of R_{gate}. With 0.4V max LSD headroom. The margin for headroom is 0.04V.

Figure 3-11. LSD Headroom with 100 mA Sourced



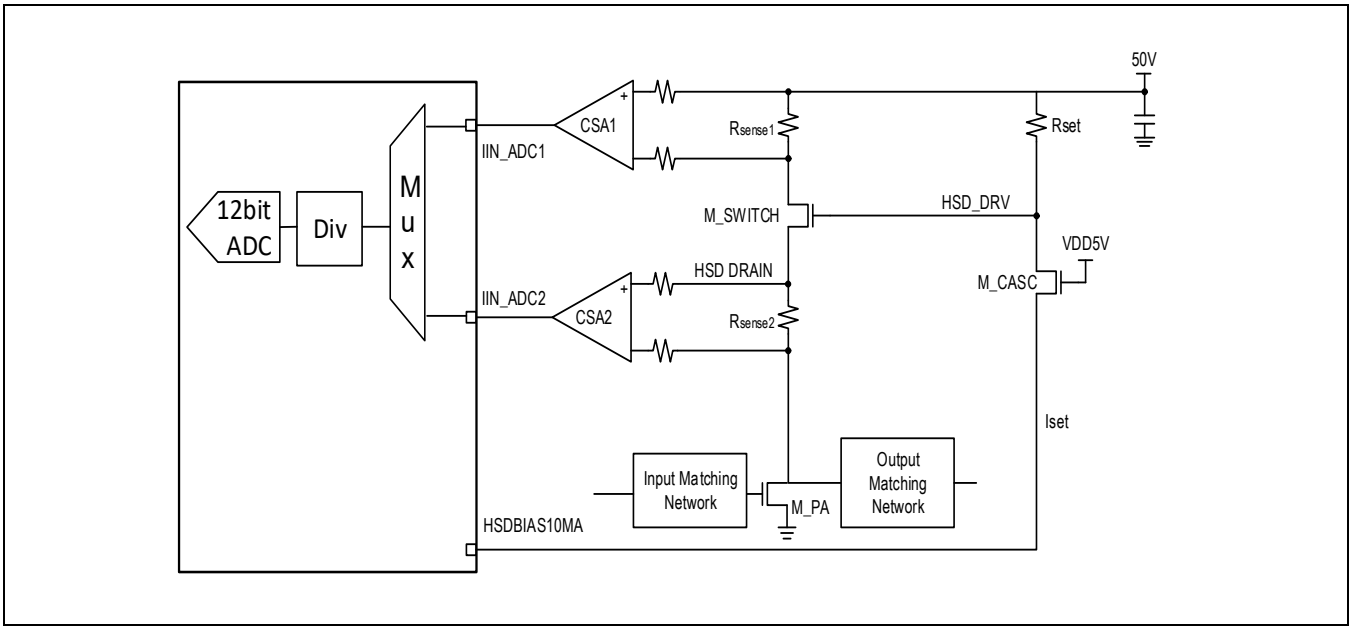
3.4 High Side Driver

EN_HSD is used to enable to high side driver. There is an internal pull-down for pin.**EN_HSD**, so that the high side driver is disabled during start-up.

The HSD provides the control for an external high voltage Pass Gate Power FET (M_SWITCH), typically used to connect the high voltage supply to the Power Amplifier stages. In addition to the pass gate, the MABC-11040 also requires an off chip resistor and FET M_CASC to protect it from the high drain voltage. To turn on the external pass gate FET, the HSD turns on a programmable current source I_{SET} at **HSDBIAS10MA**, which pulls a current through R_{SET} (see Figure 3-12), such that the **HSD_DRV** voltage is dropped by I_{SET}*R_{SET}. For example, if I_{SET} is 10mA and R_{SET} is 1k ohms leading to a voltage drop across R_{SET} of 10 V to turn on the pass gate FET(M_SWITCH). With the 10V drop across R_{SET} the voltage at the **HSD_DRV** location becomes 40V (a 10 V drop from 50V). Note that the resistor selection /required voltage drop is application specific.

When pin.**EN_HSD** is pulled high, a 10 mA current will be drawn from pin.**HSDBIAS10MA** and will turn on the M_CASC after t_{SWON} (Page 00h, Address 80h[7:4]). After the M_CASC is on, LSD will then provide the voltages from the internal LUT, based on the multiple temperature inputs. Setting the pin.**EN_HSD** down will turn the GaN device off. After a delay of t_{SWOFF} (Page 00h, Address 80h[3:0]), the M2 will turn off.

Figure 3-12. High Side Driver Schematic



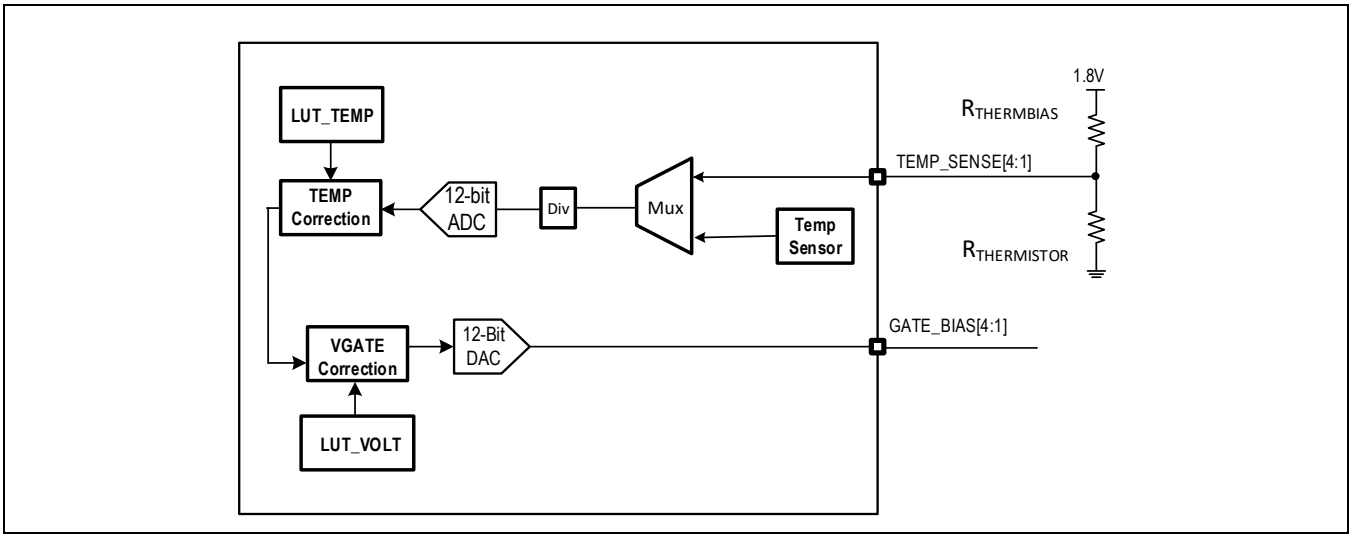
3.5 Look up Table

The current going to the power amplifier has to be carefully sustain over temperature. For this compensation, the MABC-11040 features two Look Up Tables that compensates for nonlinearities in the external thermistor used and the gate current going to the Power Amplifier. The LSD_DAC_OUT temperature compensation using an external thermistor will be done in two steps as follows:

1. Temperature LUT, reg.LUT_TEMP: Compensates for the external thermistor or internal temperature sensor nonlinearities .
2. Gate Bias LUT, reg.LUT_VOLT: Provides a current vs. temperature profile to the power amplifier, user defined.

Figure 3-13 shows the temperature compensation circuitry using an external thermistor.

Figure 3-13. LSD_DAC_OUT Temperature Compensation using an external thermistor



3.5.1 Look Up Table for Temperature

The temperature linearizion uses the 256 words stored in the TEMP LUT (Register page 0x80h and 0x81h). For example, given the temperature range from –40°C to 120°C with 256 steps, the step size is 0.625°C. When using an external thermistor, the ADC codes must be re-defined over temperature by LSDx_TEMP output voltage and mapped to the LUT_TEMP having a resolution up to 0.625°C/ADC code. The temperature readings are taken either from an integrated temperature sensor or an external thermistor placed close to the power amplifier device(s).

Two different methods are specified for temperature sensing and readout. In both cases, a 12-bit temperature reading is obtained based on a total range of 160^{o}C, -40^{o}C to +120^{o}C, 0.04^{o}C steps. Note that, in the case of the external thermistor, the temperature calibration is done using 8 bits, i.e. every 256 steps, while a linear interpolation is performed between the 1/256 steps. The MABC-11040 will monitor the four pins.**LSD_TEMP[4:1]** and continue to update each temperature reading from the temperature calibration registers for each LSD temperature sensor based on the voltage reading.

Note: If no thermistor is used, pins.**TEMP_SENSE[4:1]** should be tied to **VIO**. This would prevent over temperature faults from occurring.

The temperature BASELINE at which extracted LUT_TEMP is defined in LUT_TEMP_BS_MSB and LUT_TEMP_BS_LSB as 12bit data from -40C to 120C. LSDx_TS_BS_MSB/LSB give the ADC reading of LSDx_TEMP pin as the BASE value. LUT_TEMP_BS_ADDRESS give the address in the LUT_TEMP that BASE is stored. The overall transfer function is stored in the LUT as a set of unsigned 12-bit increments from the base value, that is, each LUT location stores the value of the decrement Δ1 per 0.625C.

3.5.2 Look Up Table for Voltage

The gate voltage temperature calibration uses only the 6 most significant bits of the 12-bit temperature reading. which is typically defined for a temperature range from -40^{o}C to 120^{o}C, therefore the step is typically 2.5C and a total of 64 steps within the voltage look-up table. This range can be adjusted, according to the users' needs, and the MABC-11040 is functional and operational within the required range of the use case. Between each 2.5C step within the VOLT LUT, a linear interpolation is applied using the remaining 6 bits of the temperature reading. The linear interpolation step is 0.04^{o}C.

3.5.2.1 Offset voltage correction

The calibration procedure described above is using look-up values from VOLT LUT, which have been measured over temperature and are assumed to be the same for all devices of the same type. When a new device is used in the system, these look-up values need updating. Also each GaN device needs to be calibrated for V_{th} offset. This is one more look-up value, unique for each GaN device, which is added to the gate voltage correction values of its family.

3.5.2.2 Register Settings to use LUT Voltage

- Enable look up tables by writing Page0x02h, Register0x08h Bit[2] with Value 1.
- Load the desired settings to each page and register.
- Terminate NVM control and reflect the changes by writing Page0x02h, Register0x08h Bit[2] with Value 0.

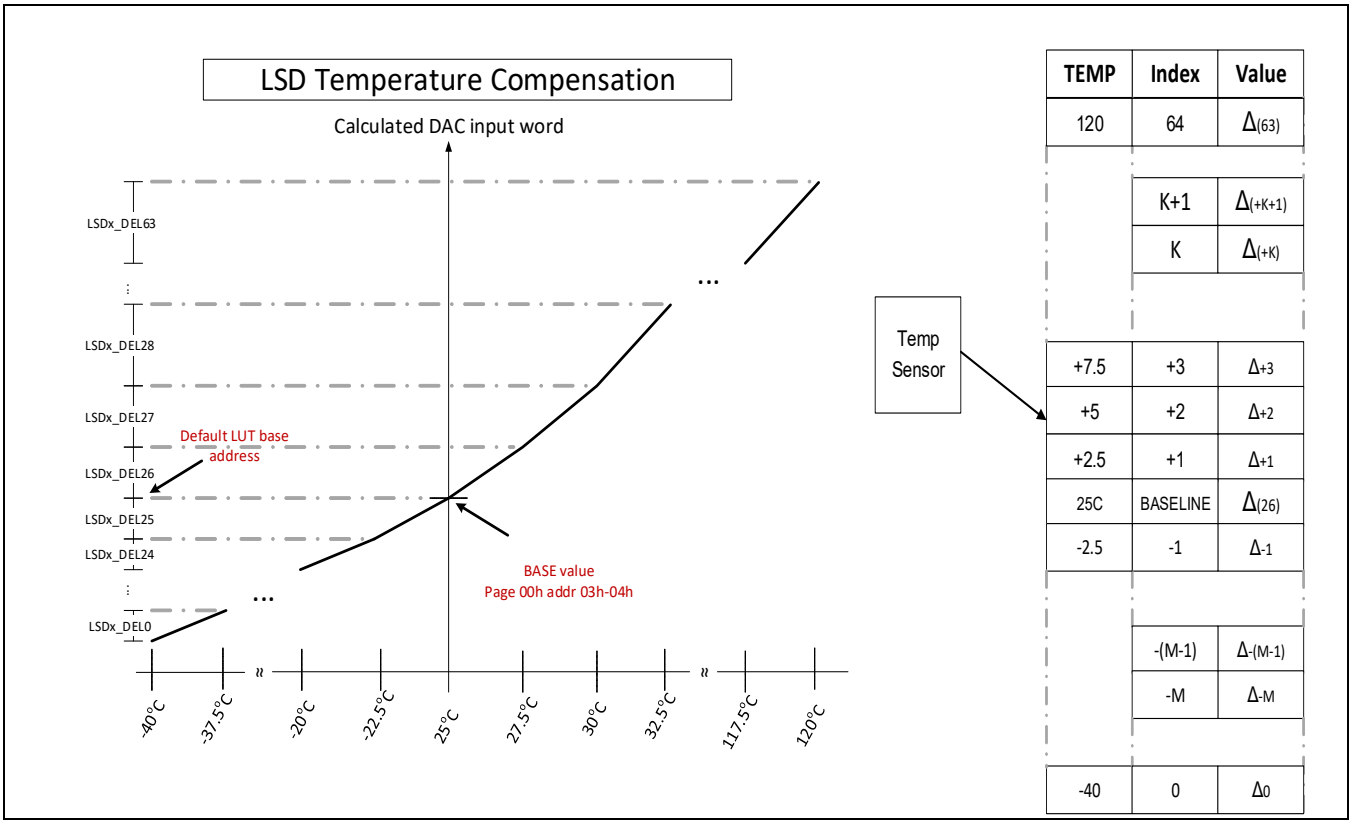
3.5.2.3 LUT Voltage Calculation

In order to minimize the storage requirements, MABC-11040 LUTs are indexed in 2.5°C increments. Also, the stored values are only the increments, or first derivatives (Δs) of the modeled transfer function. The internal ALU reconstructs the original transfer function by integrating the coefficients stored in the LUTs. The errors due to the coarseness of the temperature quantization are significantly reduced through the use of linear interpolation, which is also implemented in the ALU. ALU output will be limited to{000, FFF}. Consider the example shown in Figure 3-14. The target output vs temperature is shown in the top graph. VDACx is a smooth, monotonic function with, ideally, infinite precision. The LUT stores only the increments, or the rise, within each 2.5°C interval.

In order to recreate the original transfer function, the series of increments must be summed together and added to the constant BASE value. This process must also be referenced to the common temperature point. This reference temperature is called BASELINE and is defined in TS_PTAT_BS_TEMP<11:0> and LUT_TEMP_BS_TEMP<11:0> depends on internal (TS_PTAT, TS_VBG) or external temperature sensor (TS1/2/3/4)used.

MABC-11040 has VOLT LUTs for each LSD driver defined in page 90h/91h/92h/93h. The VOLT LUTs start from the BASE address and extend to 64 steps. Each step of data shows the differential DAC code between previous temperature and current temperature. The base voltage value in hexadecimal is calculated by: Dec to Hex[Gate Voltage/1.22mV];The base temp value in hexadecimal is calculated by: Dec to Hex[(Temp(°C)+40°C) /0.625°C]. For more details, please contact MACOM team.

Figure 3-14. LUT Voltage Table



3.6 Addition features

3.6.1 EEPROM Programming Procedure

The following are the instructions to program the EEPROM.

1. Enable Look up table: write Page 0x02h Register 0x08h with value 0x04h.
2. Clear the trim and the test bits: write Page 0x00h Register 0x7Fh with value 0x00h; write Page 0x01h Register 0x00h with value 0x00h; write Page 0x01h Register 0x01h with value 0x00h; write Page 0x01h Register 0x02h with value 0x00h;
3. Write password to enable each page: write Page 0x00h Register 0xFAh with value 0x20h; write Page 0x00h Register 0xFBh with value 0x19h; write Page 0x00h Register 0xFCh with value 0x07h; write Page 0x00h Register 0xFDh with value 0x04h;
4. Enable look up table: write Page 0x02h Register 08h with value 0x04h.
5. Write the desired setting to each page and registers.
6. To permanently program in the settings: write Page 0x02h Register 0x03h with value 0xFFh; write Page 0x02h Register 0x06h with value 0x01h; write Page 0x02h Register 0x08h with value 0x00h

3.6.2 GPIO pins

There are four general purpose CMOS output pins, **GPIO[3:0]**, available to the user. They can be used to adjust the attenuation setting of a Digital Step Attenuator (DSA), which can be used to control the gain in a power amplifier lineup or they can be used in order to set the phase of a digital phase shifter. Since the step attenuator is set during initial calibration, the GPIO signal can be treated as low frequency, such as 1 KHz.

The status of the GPIO pins will be controlled by the internal GPIO_CTRL0 register.

The logic level of these pins is determined by pin **VIO**. Depending on the voltage provided at pin **VIO**, the logic level can be between 1.8 and 3.3V.

3.6.3 Internal Temperature Sensor

There is an internal temperature sensor available. There is a set alarm threshold value (“TS_PTAT_OT_S_THD”) and reset alarm threshold value (“TS_PTAT_OT_R_THD”) based on the internal temperature sensor. If an alarm does assert, the faults can be can also be masked (disabled) using “ALARM_MASK2” (Page 02h, Address A5h).

Set bit [4] to 1 to mask “TS_PTAT_Alarm”.

3.6.4 External Temperature Sensors

External temperature sensor pins (**TEMP_SENSE[4:1]**) are available for users to place thermistors to monitor external temperature. The threshold set value (“TEMP[4:1]_OT_THD”) and reset value (“TEMP[4:1]_OT_R_THD”) must be programmed into the chip based on the thermistor characteristics. If the temperature exceeds the threshold temperature, the over-temperature alarm asserts (sets). If the temperature falls below the reset tIf an alarm does assert, the faults can be can also be masked (disabled) using “ALARM_MASK2” (Page 02h, Address A5h).:

- Set bit [3] to 1 to mask “LSD4_TS_Alarm”.
- Set bit [2] to 1 to mask “LSD3_TS_Alarm”.
- Set bit [1] to 1 to mask “LSD2_TS_Alarm”.

Set bit [0] to 1 to mask “LSD1_TS_Alarm”.emperature threshold, the alarm de-asserts (resets).

3.6.5 Fail Alert

A fail alert mechanism provides an output to alert the system that there are certain operating conditions found to be outside the defined acceptable range. There are two types of alarms, the real-time and latched alarm. The difference between the alarms is a reset is required to clear the latch alarm. The real time alarm outputs are used so that faults are captured as they occur. Latched alarms assert when an alarm event occurs and must be reset to check if the alarm event is still occurring. Below is a summary of the alarm types on the MABC-11040

The **FAIL** pin output is active low to indicate an alarm condition. This alert can be used by the system in order to turn off the power amplifier and protect it from being damaged. The polarity of the alarm bit can be changed by using the “Fail_flip_polar” register bit (Page 00h, Address A2h[4]). If this bit is change to “1”, the Fail alarm output will become active high to indicate an alarm condition.

The **FAIL** pin is open drain, and is internally pulled down so that the FAIL pin is low at turn-on. The “Fail_out_cmos” register bit (**Page 00h, Address A2h[5**]) can be used to convert this pin from open-drain, “0”, to a CMOS output < “1”. When the **FAIL** pin is open-drain, a 4.7k external pull-up resistor to VIO is required but a CMOS output does not require an external pull up resistor.

The “FAIL_PIN_MODE” register bit (Page 00h, Address A2h[0]) controls the behavior of the **FAIL** pin between. Trigger lock and interrupt mode. The duration that the **FAIL** pin is indicates an alarm condition is defined by “Fail_interrupt_duration” **(Page 00h, Register A2h[3:1]**) and can be set between 12 and 84 clock cycles.

“alarm_clear” is used to clear all the latched alarms in the following registers, “TEMP_ALARM”, “ALARM0”, and “ALARM1”, by setting this bit “1” and then back to “0

- “ALARM_MASK0” is used to mask (disable) all the alarm statuses in the “ALARM0” register (Page 00h, reg.A3h).
- “ALARM_MASK1” is used to mask (disable) all the alarm statuses in the “ALARM1” register(Page 00h, reg.A4h).
- “ALARM_MASK2” is used to mask (disable) all the alarm statuses in the “TEMP_ALARM” register(Page 00h, reg.A5h).
- “ALARM_MASK3” is used to mask (disable) all the alarm statuses in the “TEMP_ALARM” register(Page 00h, reg.A6h).

The logic block diagram of the fail circuitry can be found in Figure 3-16.

3.6.5.1 Drain Current Alarms

The drain current limit is predefined. If the drain current seen at **IIN_ADC1** or **IIN_ADC2** exceeds the current limit, the alarm bit will assert.

- “iin1_cl_lt”, Page 02h, Address 3Fh[7], is associated to the **IIN_ADC1** pin.
- “iin2_cl_lt”, Page 02h, Address 3Fh[6], is associated to the **IIN_ADC2** pin.

3.6.5.2 Gate Current Alarms

The gate current limit is predefined. If the gate current seen at the GATE_BIAS pin exceeds the predefined limit, the alarm bit will assert.

- “lsd1_cl_rt”, Page 02h, Address 40h[6], is associated to the **GATE_BIAS1** pin.
- “lsd2_cl_rt”, Page 02h, Address 40h[5], is associated to the **GATE_BIAS2** pin.

- “lsd3_cl_rt”, Page 02h, Address 40h[4], is associated to the **GATE_BIAS3** pin.
- “lsd4_cl_rt”, Page 02h, Address 40h[3], is associated to the **GATE_BIAS4** pin.

3.6.5.2.1 Voltage Alarms

There are four under-voltage alarms addressing all four voltage supply pins, **V_NEG**, **VDD5A**, **VDD1P8VA**, and **VDD1P8VD**. If the predefined threshold is less negative for **V_NEG** or less positive for the other three supplies, the resulting fault condition will disable the **GATE_BIAS** and HSD. There is a predefined amount of hysteresis and low pass filtering to prevent false triggering of the fault condition.

V_NEG is monitored by the alarm bit “neg_uv_rt”. This alarm bit will go high,“1”, when V_NEG is less negative than the voltage threshold defined by “vneg_rdy_vth”.

VDD5A is monitored by “undervoltage_alarm_rt”. This alarm bit will go high,“1”, when VDD5A is less positive than the voltage threshold defined by “UV_alarm_vth”.

VDD1P8VA is monitored by the alarm bit “v1p8a_uv_rt”. This alarm bit will go high,“1”, when VDD1P8VA is less positive than 1.44V.

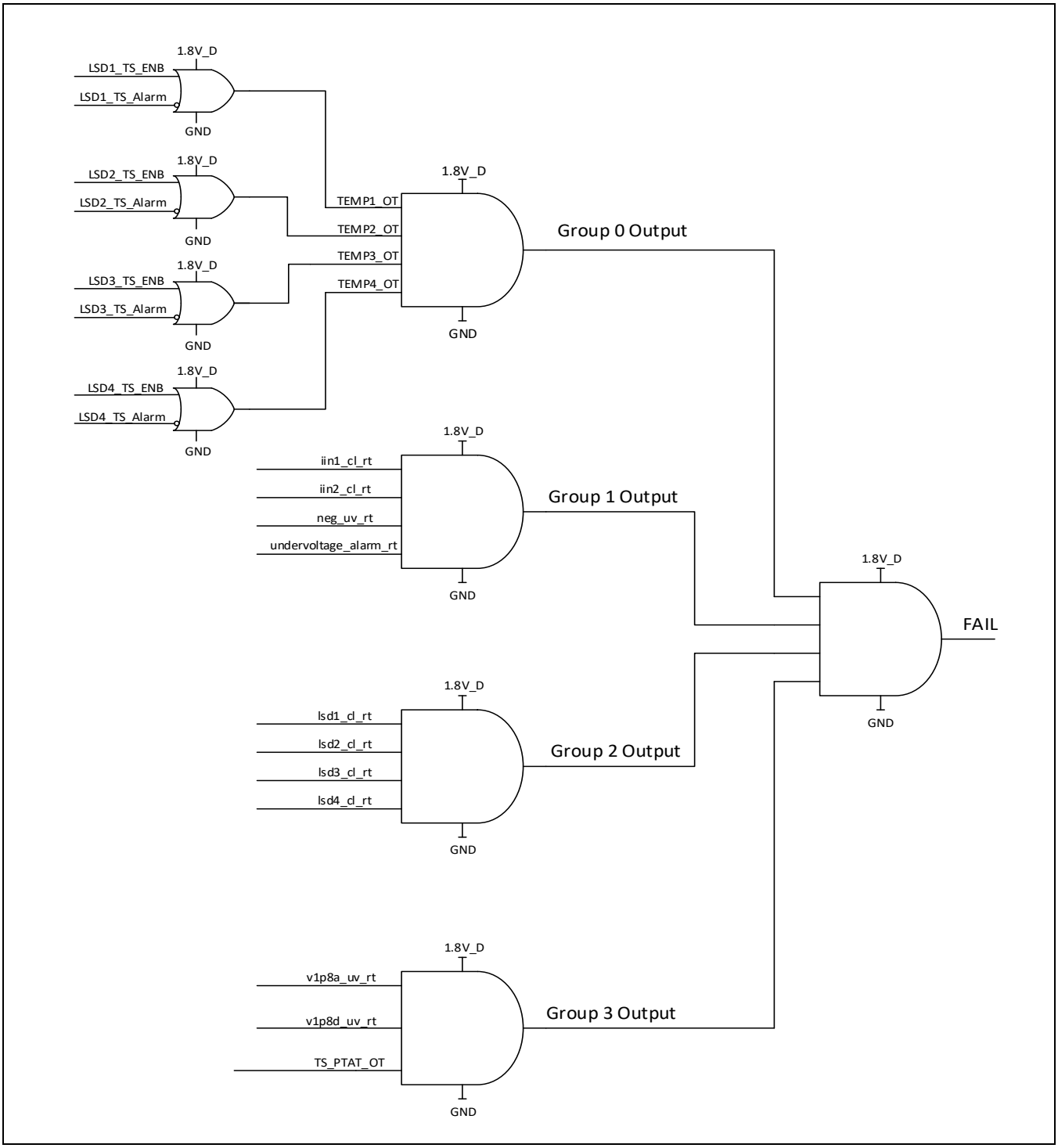
VDD1P8VD is monitored by the alarm bit “v1p8d_uv_rt”. The alarm bit will go high,“1”, when VDD1P8VD is less positive than 1.44V.

3.6.5.3 Thermal Shutdown

The thermal shutdown circuitry uses a BJT on the die. VBE on the BJT is compared with predefined voltages to sense if the temperature has reached the shutdown thresholds of 130°C, 140°C, or 150°C. If the temperature has reached the selected thermal shutdown temperature, the low side drivers (LSDs) and high side driver (HSD) will be disabled.

There is an option to disable thermal shutdown for HTOL testing. “OT_Shutdown_Threshold” by setting both bits in page 00h, address 93h[5:4]) = 1.

Figure 3-15. Fail Circuitry Logic



3.7 Digital Interface

Using the **SEL[3:0]** pin, a static I^2C address can be used to identify individual MABC-11040 devices in a system so that a controller can write to or read from each device. There are three available addresses for each device (Table 3-2). There is also a broadcast address common to all devices so a controller can communicate with all devices at the same time.

Table 3-2. I^2C Timing Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
fscl	Clock Frequency, SCL				400	KHz
tlow	Clock Pulse Width Low		160			ns
thigh	Clock Pulse Width High		60			ns
tAA	Clock Low to Data Out Valid		0		70	ns
tHD,STA	Start Hold Time		160			ns
tSU,STA	Start Set-up Time		160			ns
tHD,DAT	Data In Hold Time		0			ns
RPULL-UP	Outputs (SDA,SCL) internal pull-up resistor value to VIO			250		KΩ
tSU,STO	Stop Set-up Time		160			ns
tDH	Data Out Hold Time		5			ns

Figure 3-16. I^2C Timing Characteristics

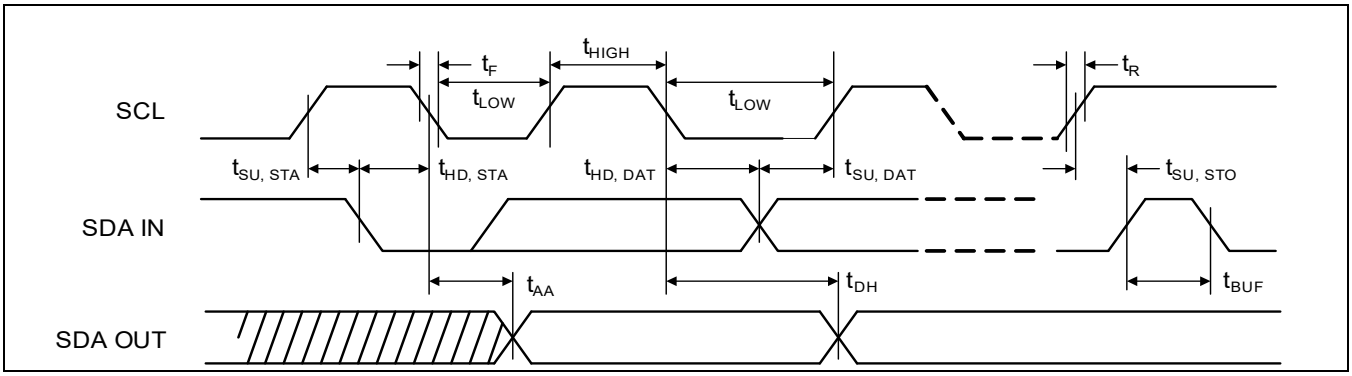


Table 3-3. I^2C Address Table

I2C Address (Hex)		Input Setting				I2C Address (Hex)		Input Setting			
MSB	LSB	SEL3	SEL2	SEL1	SEL0	MSB	LSB	SEL3	SEL2	SEL1	SEL0
0	0	RESERVED				1	D	GND	VIO	VDD5V	VIO
0	1	GND	GND	GND	VIO	1	E				N/C
0	2				N/C	1	F				VDD5V
0	3				VDD5V	2	0		N/C	GND	GND
0	4			VIO	GND	2	1				VIO
0	5				VIO	2	2				N/C
0	6				N/C	2	3				VDD5V
0	7				VDD5V	2	4			VIO	GND
0	8			N/C	GND	2	5				VIO
0	9				VIO	2	6				N/C
0	A				N/C	2	7				VDD5V
0	B				VDD5V	2	8			N/C	GND
0	C			VDD5V	GND	2	9				VIO
0	D				VIO	2	A				N/C
0	E				N/C	2	B				VDD5V
0	F				VDD5V	2	C			VDD5V	GND
1	0		VIO	GND	GND	2	D				VIO
1	1				VIO	2	E				N/C
1	2				N/C	2	F				VDD5V
1	3				VDD5V	3	0		VDD5V	GND	GND
1	4			VIO	GND	3	1				VIO
1	5				VIO	3	2				N/C
1	6				N/C	3	3				VDD5V
1	7				VDD5V	3	4			VIO	GND
1	8			N/C	GND	3	5				VIO
1	9				VIO	3	6				N/C
1	A				N/C	3	7				VDD5V
1	B				VDD5V	3	8			N/C	GND
1	C			VDD5V	GND	3	9				VIO

Table 3-3. I^2C Address Table

I2C Address (Hex)		Input Setting				I2C Address (Hex)		Input Setting			
MSB	LSB	SEL3	SEL2	SEL1	SEL0	MSB	LSB	SEL3	SEL2	SEL1	SEL0
3	A	GND	VDD5V	N/C	N/C	5	7	VIO	VIO	VIO	VDD5V
3	B				VDD5V	5	8			N/C	GND
3	C			VDD5V	GND	5	9				VIO
3	D				VIO	5	A				N/C
3	E				N/C	5	B				VDD5V
3	F				VDD5V	5	C			VDD5V	GND
4	0	VIO	GND	GND	GND	5	D				VIO
4	1				VIO	5	E				N/C
4	2				N/C	5	F				VDD5V
4	3				VDD5V	6	0		N/C	GND	GND
4	4			VIO	GND	6	1				VIO
4	5				VIO	6	2				N/C
4	6				N/C	6	3				VDD5V
4	7				VDD5V	6	4			VIO	GND
4	8			N/C	GND	6	5				VIO
4	9				VIO	6	6				N/C
4	A				N/C	6	7				VDD5V
4	B				VDD5V	6	8			N/C	GND
4	C			VDD5V	GND	6	9				VIO
4	D				VIO	6	A				N/C
4	E				N/C	6	B				VDD5V
4	F				VDD5V	6	C			VDD5V	GND
5	0		VIO	GND	GND	6	D				VIO
5	1				VIO	6	E				N/C
5	2				N/C	6	F				VDD5V
5	3				VDD5V	7	0		VDD5V	GND	GND
5	4			VIO	GND	7	1				VIO
5	5				VIO	7	2				N/C
5	6				N/C	7	3				VDD5V

Table 3-3. I^2C Address Table

I2C Address (Hex)		Input Setting				I2C Address (Hex)		Input Setting			
MSB	LSB	SEL3	SEL2	SEL1	SEL0	MSB	LSB	SEL3	SEL2	SEL1	SEL0
7	4	VIO	VDD5V	VIO	GND	7	C	VIO	VDD5V	VDD5V	GND
7	5				VIO	7	D				VIO
7	6				N/C	7	E				N/C
7	7				VDD5V	7	F				VDD5V

4.0 Control Registers Map and Descriptions

4.1 Register Map General Overview

The MABC-11040 has a lot of functions that can be controlled via registers, the register map is divided with several register pages to help distribute these functions as described in the following

Register Map Description Summary

Function		Comment
Low Side Driver	00h	LSD Control, DAC, ADC mux, Alarm Masks
EEPROM	01h	EEPROM, user defined information
Global	02h	Global control, ADC, Alarm calibration
Look Up Table for Temperature	80h	LUT Temp[0:127]
	81h	LUT Temp[128:255]
Look Up Table for Voltage	90h	LSD1 LUT Voltage[0:63]
	91h	LSD2 LUT Voltage[0:63]
	92h	LSD3 LUT Voltage[0:63]
	93h	LSD4 LUT Voltage[0:63]

NOTES:

- After power up or software reset, the default page in 00h.
- Write the password to switch pages (refer to section3-2-1 for password)
- Write page number to register0xFE to select page. Register 0xFEis accessible from any page.

Table 4-1 shows the register map for the MABC-11040. Should any reserved registers or bits need to be written, use with their default value listed. Registers not listed in Table 4-1 are reserved with default value of 00h.

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
00h	00h	CHECKSUMSEED	checksumseed<7:0>								55'h	R/W
00h	03h	LSD1_LUTV_BS_LSB	*RSVD*		LSD1_BY-PASS	LSD1_POL	LSD1_BASE<3:0>				10'h	R/W
00h	04h	LSD1_LUTV_BS_MSB	LSD1_BASE<11:4>								00'h	R/W
00h	05h	LSD1_LUTV_BS_ADD	LSD1_LUTV_BS_ADD<7:0>								17'h	R/W
00h	06h	LSD2_LUTV_BS_LSB	*RSVD*		LSD2_BY-PASS	LSD2_POL	LSD2_BASE<3:0>				10'h	R/W
00h	07h	LSD2_LUTV_BS_MSB	LSD2_BASE<11:4>								00'h	R/W
00h	08h	LSD2_LUTV_BS_ADD	LSD2_LUTV_BS_ADD<7:0>								17'h	R/W
00h	09h	LSD3_LUTV_BS_LSB	*RSVD*		LSD3_BY-PASS	LSD3_POL	LSD3_BASE<3:0>				10'h	R/W
00h	0Ah	LSD3_LUTV_BS_MSB	LSD3_BASE<11:4>								00'h	R/W
00h	0Bh	LSD3_LUTV_BS_ADD	LSD3_LUTV_BS_ADD<7:0>								17'h	R/W
00h	0Ch	LSD4_LUTV_BS_LSB	*RSVD*		LSD4_BY-PASS	LSD4_POL	LSD4_BASE<3:0>				10'h	R/W
00h	0Dh	LSD4_LUTV_BS_MSB	LSD4_BASE<11:4>								00'h	R/W
00h	0Eh	LSD4_LUTV_BS_ADD	LSD4_LUTV_BS_ADD<7:0>								17'h	R/W
00h	0Fh	LUT_TEMP_BS_MSB	LUT_TEMP_BS_TEMP<11:4>								00'h	R/W
00h	10h	LUT_TEMP_BS_LSB	LUT_TEMP_BS_TEMP<3:0>				*RSVD*				00'h	R/W
00h	11h	LUT_TEMP_BS_ADD	LUT_TEMP_BS_ADD<7:0>								68'h	R/W
00h	12h	LSD1_TS_BS_MSB	LSD1_TS_BS<11:4>								00'h	R/W
00h	13h	LSD2_TS_BS_MSB	LSD2_TS_BS<11:4>								00'h	R/W
00h	14h	LSD12_TS_BS_LSB	LSD2_TS_BS<3:0>				LSD1_TS_BS<3:0>				00'h	R/W
00h	15h	LSD3_TS_BS_MSB	LSD3_TS_BS<11:4>								00'h	R/W
00h	16h	LSD4_TS_BS_MSB	LSD4_TS_BS<11:4>								00'h	R/W
00h	17h	LSD34_TS_BS_LSB	LSD4_TS_BS<3:0>				LSD3_TS_BS<3:0>				00'h	R/W
00h	1Fh	VER_CTRL	*RSVD*				VERSION<3:0>				60'h	R/W
00h	33h	ADC_CHNL_ENABLE0	EN_LSD3_OUTN	EN_LSD2_OUTN	EN_LSD1_OUTN	EN_LSD4_OUTP	EN_LSD3_OUTP	EN_LSD2_OUTP	EN_LSD1_OUTP	*RSVD*	FF'h	R/W
00h	53h	ADC_INPUT_MULTIPLI-ER0	mult_ADC_INPUT14<1:0>		mult_ADC_INPUT13<1:0>		mult_ADC_INPUT12<1:0>		mult_ADC_INPUT11<1:0>		3F'h	R/W
00h	54h	ADC_INPUT_MULTIPLI-ER1	mult_ADC_INPUT18<1:0>		mult_ADC_INPUT17<1:0>		mult_ADC_INPUT16<1:0>		mult_ADC_INPUT15<1:0>		00'h	R/W
00h	55h	ADC_INPUT_MULTIPLI-ER2	mult_ADC_INPUT22<1:0>		mult_ADC_INPUT21<1:0>		mult_ADC_INPUT20<1:0>		mult_ADC_INPUT19<1:0>		30'h	R/W
00h	56h	ADC_INPUT_MULTIPLI-ER3	mult_ADC_INPUT2<1:0>		mult_ADC_INPUT1<1:0>		mult_ADC_INPUT10<1:0>		mult_ADC_INPUT23<1:0>		54'h	R/W
00h	57h	ADC_INPUT_MULTIPLI-ER4	mult_ADC_INPUT6<1:0>		mult_ADC_INPUT5<1:0>		mult_ADC_INPUT4<1:0>		mult_ADC_INPUT3<1:0>		55'h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
00h	58h	ADC_INPUT_MULTIPLI-ER5	mult_ADC_INPUT10<1:0>		mult_ADC_INPUT9<1:0>		mult_ADC_INPUT8<1:0>		mult_ADC_INPUT7<1:0>		55'h	R/W
00h	66h	LSD1_CTRL1	*RSVD*	LSD1_C-SP_EN	LSD1_CSN_EN	*RSVD*	LSD1_Rset<1:0>		*RSVD*		00'h	R/W
00h	67h	LSD2_CTRL0	LSD2_CL<2>	LSD2_CL<1>	LSD2_CL<0>	*RSVD*		RSVD	RSVD	LSD2_REG_EN	8B'h	R/W
00h	68h	LSD2_CTRL1	*RSVD*	LSD2_C-SP_EN	LSD2_CSN_EN	*RSVD*	LSD2_Rset<1:0>		*RSVD*		00'h	R/W
00h	69h	LSD3_CTRL0	LSD3_CL<2>	LSD3_CL<1>	LSD3_CL<0>	*RSVD*		RSVD	RSVD	LSD3_REG_EN	8B'h	R/W
00h	6Ah	LSD3_CTRL1	*RSVD*	LSD3_C-SP_EN	LSD3_CSN_EN	*RSVD*	LSD3_Rset<1:0>		*RSVD*		00'h	R/W
00h	6Bh	LSD4_CTRL0	LSD4_CL<2>	LSD4_CL<1>	LSD4_CL<0>	*RSVD*		RSVD	RSVD	LSD4_REG_EN	8B'h	R/W
00h	6Ch	LSD4_CTRL1	*RSVD*	LSD4_C-SP_EN	LSD4_CSN_EN	*RSVD*	LSD4_RSET<1:0>		*RSVD*		00'h	R/W
00h	6Dh	OVERRIDE_CTRL	DAC_ORD <3:0>				TEMP_ORD <3:0>				00'h	R/W
00h	6Eh	DAC_LSD1_MSB	DAC_LSD1<11:4>								00'h	R
00h	6Fh	DAC_LSD1_LSB	DAC_LSD1<3:0>				*RSVD*				00'h	R
00h	70h	DAC_LSD1_ORD_MSB	DAC_LSD1_ORD<11:4>								00'h	R/W
00h	71h	DAC_LSD1_ORD_LSB	DAC_LSD1_ORD<3:0>				*RSVD*				00'h	R/W
00h	72h	DAC_LSD2_MSB	DAC_LSD2<11:4>								00'h	R
00h	73h	DAC_LSD2_LSB	DAC_LSD2 <3:0>				*RSVD*				00'h	R
00h	74h	DAC_LSD2_ORD_MSB	DAC_LSD2_ORD<11:4>								00'h	R/W
00h	75h	DAC_LSD2_ORD_LSB	DAC_LSD2_ORD<3:0>				*RSVD*				00'h	R/W
00h	76h	DAC_LSD3_MSB	DAC_LSD3<11:4>								00'h	R
00h	77h	DAC_LSD3_LSB	DAC_LSD3<3:0>				*RSVD*				00'h	R
00h	78h	DAC_LSD3_ORD_MSB	DAC_LSD3_ORD<11:4>								00'h	R/W
00h	79h	DAC_LSD3_ORD_LSB	DAC_LSD3_ORD<3:0>				*RSVD*				00'h	R/W
00h	7Ah	DAC_LSD4_MSB	DAC_LSD4<11:4>								00'h	R
00h	7Bh	DAC_LSD4_LSB	DAC_LSD4<3:0>				*RSVD*				00'h	R
00h	7Ch	DAC_LSD4_ORD_MSB	DAC_LSD4_ORD<11:4>								00'h	R/W
00h	7Dh	DAC_LSD4_ORD_LSB	DAC_LSD4_ORD<3:0>				*RSVD*				00'h	R/W
00h	7Eh	PREDRIVER_CTRL0	Pre_driver_current<3:0>				Tswoff_infinity	HSD_driver_current<2:0>			57'h	R/W
00h	7Fh	GPIO_CTRL0	*RSVD*				gpio_status<3:0>				00'h	R/W
00h	80h	HSD_Timing	ton<1:0>		tswon<1:0>		tswoff<1:0>		toff<1:0>		D3'h	R/W
00h	94h	IIN1_THRESHOLD	IIN1_THRESHOLD<7:0>								F8'h	R/W
00h	95h	IIN2_THRESHOLD	IIN2_THRESHOLD<7:0>								F8'h	R/W
00h	96h	TEMP1_OT_S_THD	TEMP1_OT_THD<7:0>								F8'h	R/W
00h	97h	TEMP1_OT_R_THD	TEMP1_OT_R_THD<7:0>								F0'h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
00h	98h	TEMP2_OT_S_THD	TEMP2_OT_THD<7:0>								F8'h	R/W
00h	99h	TEMP2_OT_R_THD	TEMP2_OT_R_THD<7:0>								F0'h	R/W
00h	9Ah	TEMP3_OT_S_THD	TEMP3_OT_THD<7:0>								F8'h	R/W
00h	9Bh	TEMP3_OT_R_THD	TEMP3_OT_R_THD<7:0>								F0'h	R/W
00h	9Ch	TEMP4_OT_S_THD	TEMP4_OT_THD<7:0>								F8'h	R/W
00h	9Dh	TEMP4_OT_R_THD	TEMP4_OT_R_THD<7:0>								F0'h	R/W
00h	9Eh	TS_VBG_OT_THD	TS_VBG_OT_S_THD<7:0>								F8'h	R/W
00h	9Fh	TS_VBG_OT_R_THD	TS_VBG_OT_R_THD<7:0>								F0'h	R/W
00h	A0h	TS_PTAT_OT_THD	TS_PTAT_OT_S_THD<7:0>								F8'h	R/W
00h	A1h	TS_PTAT_OT_R_THD	TS_PTAT_OT_R_THD<7:0>								F0'h	R/W
00h	A2h	FAIL_CTRL	alarm_clear	*RSVD*	Fail_out_cmos	Fail_flip_polar	Fail_interrupt_duration			FAIL_PIN_-MODE	20'h	R/W
00h	A3h	ALARM_MASK0	Alarmmask0<7:0>								00'h	R/W
00h	A4h	ALARM_MASK1	Alarmmask1<7:0>								00'h	R/W
00h	A5h	ALARM_MASK2	Alarmmask2<7:0>								03'h	R/W
00h	A6h	ALARM_MASK3	Alarmmask3<7:0>								03'h	R/W
00h	AAh	UPLIMIT_LSD1_MSB	UPLIMIT_LSD1<11:4>								FF'h	R/W
00h	ABh	UPLIMIT_LSD2_MSB	UPLIMIT_LSD2<11:4>								FF'h	R/W
00h	ACh	UPLIMIT_LSD12_LSB	UPLIMIT_LSD1<3:0>				UPLIMIT_LSD2<3:0>				FF'h	R/W
00h	ADh	UPLIMIT_LSD3_MSB	UPLIMIT_LSD3<11:4>								FF'h	R/W
00h	AEh	UPLIMIT_LSD4_MSB	UPLIMIT_LSD4<11:4>								FF'h	R/W
00h	AFh	UPLIMIT_LSD34_LSB	UPLIMIT_LSD3<3:0>				UPLIMIT_LSD4<3:0>				FF'h	R/W
00h	B0h	BTLIMIT_LSD1_MSB	BTLIMIT_LSD1<11:4>								00'h	R/W
00h	B1h	BTLIMIT_LSD2_MSB	BTLIMIT_LSD2<11:4>								00'h	R/W
00h	B2h	BTLIMIT_LSD12_LSB	BTLIMIT_LSD1<3:0>				BTLIMIT_LSD2<3:0>				00'h	R/W
00h	B3h	BTLIMIT_LSD3_MSB	BTLIMIT_LSD3<11:4>								00'h	R/W
00h	B4h	BTLIMIT_LSD4_MSB	BTLIMIT_LSD4<11:4>								00'h	R/W
00h	B5h	BTLIMIT_LSD34_LSB	BTLIMIT_LSD3<3:0>				BTLIMIT_LSD4<3:0>				00'h	R/W
00h	B6h	LUT_VOLT_CTRL	*RSVD*				LUTVOLT_TEMP_SEL<3:0>				08'h	R/W
00h	B7h	I2C_CONTROL	*RSVD*	i2c_add_reg							80'h	R/W
00h	B8h	I2C_ALLCALL	*RSVD*	i2c_allcall_adr<6:0>							55'h	R/W
00h	E0h	NVM_BURN_COUNT1	NVM_BURN_COUNT<7:0>								00'h	R
00h	E1h	NVM_BURN_COUNT2	NVM_BURN_COUNT<15:8>								00'h	R
00h	FAh	PASSWORD0	PASSWORD0<7:0>								00'h	R/W
00h	FBh	PASSWORD1	PASSWORD1<7:0>								00'h	R/W
00h	FCh	PASSWORD2	PASSWORD2<7:0>								00'h	R/W
00h	FDh	PASSWORD3	PASSWORD3<7:0>								00'h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
00h	FEh	PAGE	PAGE<7:0>								00'h	R/W
02h	00h	CHIPID	CHIPID								47'h	R
02h	01h	REVID	REVID								1F'h	R
02h	02h	SOFT_RESET	SOFT_RESET								00'h	R/W
02h	09h	I2C_ANA	I2C_allcall_dis	I2C_ana<6:0>							41'h	R
02h	10h	CHNL0_LSB	*RSVD*				Access_ctrl<3:0>				00'h	R
02h	11h	CHNL1_MSB	ADC_LSD1_OUTP<11:4>								00'h	R
02h	12h	CHNL1_LSB	ADC_LSD1_OUTP<3:0>				*RSVD*				00'h	R
02h	13h	CHNL2_MSB	ADC_LSD2_OUTP<11:4>								00'h	R
02h	14h	CHNL2_LSB	ADC_LSD2_OUTP<3:0>				*RSVD*				00'h	R
02h	15h	CHNL3_MSB	ADC_LSD3_OUTP<11:4>								00'h	R
02h	16h	CHNL3_LSB	ADC_LSD3_OUTP<3:0>				*RSVD*				00'h	R
02h	17h	CHNL4_MSB	ADC_LSD4_OUTP<11:4>								00'h	R
02h	18h	CHNL4_LSB	ADC_LSD4_OUTP<3:0>				*RSVD*				00'h	R
02h	19h	CHNL5_MSB	ADC_LSD1_OUTN<11:4>								00'h	R
02h	1Ah	CHNL5_LSB	ADC_LSD1_OUTN<3:0>				*RSVD*				00'h	R
02h	1Bh	CHNL6_MSB	ADC_LSD2_OUTN<11:4>								00'h	R
02h	1Ch	CHNL6_LSB	ADC_LSD2_OUTN<3:0>				*RSVD*				00'h	R
02h	1Dh	CHNL7_MSB	ADC_LSD3_OUTN<11:4>								00'h	R
02h	1Eh	CHNL7_LSB	ADC_LSD3_OUTN<3:0>				*RSVD*				00'h	R
02h	1Fh	CHNL8_MSB	ADC_LSD4_OUTN<11:4>								00'h	R
02h	20h	CHNL8_LSB	ADC_LSD4_OUTN<3:0>				*RSVD*				00'h	R
02h	27h	CHNL12_MSB	ADC_IIN1<11:4>								00'h	R
02h	28h	CHNL12_LSB	ADC_IIN1<3:0>				*RSVD*				00'h	R
02h	29h	CHNL13_MSB	ADC_IIN2<11:4>								00'h	R
02h	2Ah	CHNL13_LSB	ADC_IIN2<3:0>				*RSVD*				00'h	R
02h	2Fh	CHNL16_MSB	ADC_LSD4_TEMP<11:4>								00'h	R
02h	30h	CHNL16_LSB	ADC_LSD4_TEMP<3:0>				*RSVD*				00'h	R
02h	31h	CHNL17_MSB	ADC_LSD3_TEMP<11:4>								00'h	R
02h	32h	CHNL17_LSB	ADC_LSD3_TEMP<3:0>				*RSVD*				00'h	R
02h	33h	CHNL18_MSB	ADC_LSD2_TEMP<11:4>								00'h	R
02h	34h	CHNL18_LSB	ADC_LSD2_TEMP<3:0>				*RSVD*				00'h	R
02h	35h	CHNL19_MSB	ADC_LSD1_TEMP<11:4>								00'h	R
02h	36h	CHNL19_LSB	ADC_LSD1_TEMP<3:0>				*RSVD*				00'h	R
02h	39h	CHNL21_MSB	ADC_EXT_VNEG<11:4>								00'h	R
02h	3Ah	CHNL21_LSB	ADC_EXT_VNEG<3:0>				*RSVD*				00'h	R

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
02h	3Fh	TEMP_ALARM	iin1_cl_lt	iin2_cl_lt	TS_VB-G_Alarm	TS_PTAT_Alarm	LSD4_TS_Alarm	LSD3_TS_Alarm	LSD2_TS_Alarm	LSD1_TS_Alarm	00'h	R
02h	40h	ALARM0	neg_uv_rt	lsd1_cl_rt	lsd2_cl_rt	lsd3_cl_rt	lsd4_cl_rt	v1p8d_uv_rt	v1p8a_uv_rt	undervolt-age_alarm_rt	00'h	R
02h	41h	ALARM1	neg_uv_lt	lsd1_cl_lt	lsd2_cl_lt	lsd3_cl_lt	lsd4_cl_lt	v1p8d_uv_lt	v1p8a_uv_lt	undervolt-age_alarm_lt	00'h	R
02h	42h	ALARM_LUT_TEMP	lsd4_lut_-temp_p	lsd4_lut_-temp_n	lsd3_lut_-temp_p	lsd3_lut_-temp_n	lsd2_lut_-temp_p	lsd2_lut_-temp_n	lsd1_lut_-temp_p	lsd1_lut_-temp_n	00'h	R
02h	43h	ALARM_LUT_VOLT	lsd4_lut_-volt_p	lsd4_lut_-volt_n	lsd3_lut_-volt_p	lsd3_lut_-volt_n	lsd2_lut_-volt_p	lsd2_lut_-volt_n	lsd1_lut_-volt_p	lsd1_lut_-volt_n	00'h	R
02h	46h	OFFCHIP_TEMP_MSB	offchip_temp<11:4>								00'h	R/W
02h	47h	OFFCHIP_TEMP_LSB	offchip_temp<3:0>				*RSVD*				00'h	R/W
02h	48h	CAL_TS1_MSB	cal_ts1<11:4>								00'h	R
02h	49h	CAL_TS1_LSB	cal_ts1<3:0>				*RSVD*				00'h	R
02h	4Ah	CAL_TS2_MSB	cal_ts2<11:4>								00'h	R
02h	4Bh	CAL_TS2_LSB	cal_ts2<3:0>				*RSVD*				00'h	R
02h	4Ch	CAL_TS3_MSB	cal_ts3<11:4>								00'h	R
02h	4Dh	CAL_TS3_LSB	cal_ts3<3:0>				*RSVD*				00'h	R
02h	4Eh	CAL_TS4_MSB	cal_ts4<11:4>								00'h	R
02h	4Fh	CAL_TS4_LSB	cal_ts4<3:0>				*RSVD*				00'h	R
02h	50h	CAL_INT_BG_MSB	cal_int_TS_VBG<11:4>								00'h	R
02h	51h	CAL_INT_BG_LSB	cal_int_TS_VBG<3:0>				*RSVD*				00'h	R
02h	52h	CAL_INT_PTAT_MSB	cal_int_ts_ptat<11:4>								00'h	R
02h	53h	CAL_INT_PTAT_LSB	cal_int_ts_ptat<3:0>				*RSVD*				00'h	R
01h	6Ch	VENDOR_CODE	VENDOR_CODE								00'h	R/W
01h	6Dh	UNI_MOD_TYP_NO1	UNI_MOD_TYP_NO1								00'h	R/W
01h	6Eh	UNI_MOD_TYP_NO2	UNI_MOD_TYP_NO2								00'h	R/W
01h	6Fh	POWER_LSB	POWER_LSB								00'h	R/W
01h	70h	DL_FREQ_LOW1	DL_FREQ_LOW1								00'h	R/W
01h	71h	DL_FREQ_LOW2	DL_FREQ_LOW2								00'h	R/W
01h	72h	DL_FREQ_HIGH1	DL_FREQ_HIGH1								00'h	R/W
01h	73h	DL_FREQ_HIGH2	DL_FREQ_HIGH2								00'h	R/W
01h	74h	CODE_YEAR	CODE_YEAR								00'h	R/W
01h	75h	CODE_WEEK	CODE_WEEK								00'h	R/W
01h	76h	MODULE_NAME1	MODULE_NAME1								00'h	R/W
01h	77h	MODULE_NAME2	MODULE_NAME2								00'h	R/W
01h	78h	MODULE_NAME3	MODULE_NAME3								00'h	R/W
01h	79h	MODULE_NAME4	MODULE_NAME4								00'h	R/W
01h	7Ah	MODULE_NAME5	MODULE_NAME5								00'h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
01h	7Bh	MODULE_NAME6	MODULE_NAME6								00'h	R/W
01h	7Ch	MODULE_NAME7	MODULE_NAME7								00'h	R/W
01h	7Dh	MODULE_NAME8	MODULE_NAME8								00'h	R/W
01h	7Eh	MODULE_NAME9	MODULE_NAME9								00'h	R/W
01h	7Fh	MODULE_NAME10	MODULE_NAME10								00'h	R/W
80h	00h-7Fh	LUT_TEMP[0:127]	LUT_TEMP[0:127] Bit[7:0]								00'h	R/W
80h	FAh	PASSWORD0	PASSWORD0<7:0>								00'h	W
80h	FBh	PASSWORD1	PASSWORD1<7:0>								00'h	W
80h	FCh	PASSWORD2	PASSWORD2<7:0>								00'h	W
80h	FDh	PASSWORD3	PASSWORD3<7:0>								00'h	W
80h	FEh	PAGE	page[7:0]								00'h	R/W
81h	00h-7Fh	LUT_TEMP[128:255]	LUT_TEMP[128:255] Bit[7:0]								00'h	R/W
90h	00h-3Fh	LSD1_VOLT[0:63]	LSD1_VOLT[0:63] Bit[7:0]								00'h	R/W
91h	00h-3Fh	LSD2_VOLT[0:63]	LSD2_VOLT[0:63] Bit[7:0]								00'h	R/W
92h	00h-3Fh	LSD3_VOLT[0:63]	LSD3_VOLT[0:63] Bit[7:0]								00'h	R/W
93h	00h-3Fh	LSD4_VOLT[0:63]	LSD4_VOLT[0:63] Bit[7:0]								00'h	R/W

Page: 00h
Address: FAh
Register Name: PASSWORD0
Default Value: 00'h
Description: password for level 0 control; write only to the end of this page

Bit(s)	Name	Description	Default	Type
[7:0]	PASSWORD0<7:0>	0000 0000b: Password does not match 0000 0001b: Password matches	0000 0000b	R

Page: 00h
Address: FBh
Register Name: PASSWORD1
Default Value: 00'h
Description: password for level 1 control

Bit(s)	Name	Description	Default	Type
[7:0]	PASSWORD1<7:0>	0000 0000b: Password does not match 0000 0001b: Password matches	0000 0000b	R

Page: 00h
Address: FCh
Register Name: PASSWORD2
Default Value: 00'h
Description: password for level 2 control

Bit(s)	Name	Description	Default	Type
[7:0]	PASSWORD2<7:0>	0000 0000b: Password does not match 0000 0001b: Password matches	0000 0000b	R

Page: 00h
Address: FDh
Register Name: PASSWORD3
Default Value: 00'h
Description: password for level 3 control

Bit(s)	Name	Description	Default	Type
[7:0]	PASSWORD3<7:0>	0000 0000b: Password does not match 0000 0001b: Password matches	0000 0000b	R

Page: GLOBAL
Address: FEh
Register Name: PAGE
Default Value: 00'h
Description: Register page

Bit(s)	Name	Description	Default	Type
[7:0]	Page<7:0>	Register page.	0000 0000b	R/W

Page: 00h
Address: 00h
Register Name: CHECKSUMSEED
Default Value: 55'h
Description: checksumseed

Bit(s)	Name	Description	Default	Type
[7:0]	checksumseed<7:0>	Seed value to ensure a non-zero checksum initialization value	0101 0101b	R/W

Page: 00h
Address: 03h
Register Name: LSD1_LUTV_BS_LSB
Default Value: 10'h
Description: LSB for the temperature look-up-table baseline register of the LSD1 and control.

Bit(s)	Name	Description	Default	Type
[7:6]	*RSVD*	*Reserved (set to default)*	00b	R
[5]	LSD1_BYPASS	1b: Always use baseline register for DAC output, 0b: Normal operation	0b	R/W
[4]	LSD1_POL	LSD output 0b: neg/decrease by LUT/TEMP 1b: pos/increase by LUT/TEMP,	1b	R/W
[3:0]	LSD1_BASE<3:0>	LSD1 baseline register LSB for LUT_TEMP	0000b	R/W

Page: 00h
Address: 04h
Register Name: LSD1_LUTV_BS_MSB
Default Value: 00'h
Description: MSB for the temperature look-up-table baseline register of the LSD1.

Bit(s)	Name	Description	Default	Type
[7:0]	LSD1_BASE<11:4>	LSD1 baseline register MSB for LUT_TEMP	0000 0000b	R/W

Page: 00h
Address: 05h
Register Name: LSD1_LUTV_BS_ADD
Default Value: 17'h
Description: Store the address of the LSD1_DEL which baseline of temperature is stored.

Bit(s)	Name	Description	Default	Type
[7:0]	LSD1_LUTV_BS_ADD<7:0>	Address of the baseline for LSD1 gate voltage output (LSD1_DEL)	0001 0111b	R/W

Page: 00h
Address: 06h
Register Name: LSD2_LUTV_BS_LSB
Default Value: 10'h
Description: LSB for the temperature look-up-table baseline register of the LSD2 and control.

Bit(s)	Name	Description	Default	Type
[7:6]	*RSVD*	*Reserved (set to default)*	00b	R
[5]	LSD2_BYPASS	1b: Always use baseline register for DAC output, 0b: Normal operation	0b	R/W
[4]	LSD2_POL	LSD output 0b: neg/decrease by LUT/TEMP 1b: pos/increase by LUT/TEMP,	1b	R/W
[3:0]	LSD2_BASE<3:0>	LSD2 baseline register LSB for LUT_TEMP	0000b	R/W

Page: 00h
Address: 07h
Register Name: LSD2_LUTV_BS_MSB
Default Value: 00'h
Description: MSB for the temperature look-up-table baseline register of the LSD2.

Bit(s)	Name	Description	Default	Type
[7:0]	LSD2_BASE<11:4>	LSD2 baseline register MSB for LUT_TEMP	0000 0000b	R/W

Page: 00h
Address: 08h
Register Name: LSD2_LUTV_BS_ADD
Default Value: 17'h
Description: Store the address of the LSD2_DEL which baseline of temperature is stored.

Bit(s)	Name	Description	Default	Type
[7:0]	LSD2_LUTV_BS_ADD<7:0>	Address of the baseline for LSD2 gate voltage output (LSD2_DEL)	0001 0111b	R/W

Page: 00h
Address: 09h
Register Name: LSD3_LUTV_BS_LSB
Default Value: 10'h
Description: LSB for the temperature look-up-table baseline register of the LSD3 and control.

Bit(s)	Name	Description	Default	Type
[7:6]	*RSVD*	*Reserved (set to default)*	00b	R
[5]	LSD3_BYPASS	1b: Always use baseline register for DAC output, 0b:Normal operation	0b	R/W
[4]	LSD3_POL	LSD output 0b: neg/decrease by LUT/TEMP 1b: pos/increase by LUT/TEMP,	1b	R/W
[3:0]	LSD3_BASE<3:0>	LSD3 baseline register LSB for LUT_TEMP	0000b	R/W

Page: 00h
Address: 0Ah
Register Name: LSD3_LUTV_BS_MSB
Default Value: 00'h
Description: MSB for the look-up-table baseline register of the LSD3 gate voltage output.r

Bit(s)	Name	Description	Default	Type
[7:0]	LSD3_BASE<11:4>	LSD3 baseline register MSB for LUT_TEMP	0000 0000b	R/W

Page: 00h
Address: 0Bh
Register Name: LSD3_LUTV_BS_ADD
Default Value: 17'h
Description: MSB for the temperature look-up-table baseline register of the LSD3.

Bit(s)	Name	Description	Default	Type
[7:0]	LSD3_LUTV_BS_ADD<7:0>	Address of the baseline for LSD3 gate voltage output (LSD3_DEL)	0001 0111b	R/W

Page: 00h
Address: 0Ch
Register Name: LSD4_LUTV_BS_LSB
Default Value: 10'h
Description: LSB for the temperature look-up-table baseline register of the LSD4 and control..

Bit(s)	Name	Description	Default	Type
[7:6]	*RSVD*	*Reserved (set to default)*	00b	R
[5]	LSD4_BYPASS	1b: Always use baseline register for DAC output, 0b: Normal operation	0b	R/W
[4]	LSD4_POL	LSD output 0b: neg/decrease by LUT/TEMP 1b: pos/increase by LUT/TEMP,	1b	R/W
[3:0]	LSD4_BASE<3:0>	LSD4 baseline register LSB for LUT_TEMP	0000b	R/W

Page: 00h
Address: 0Dh
Register Name: LSD4_LUTV_BS_MSB
Default Value: 00'h
Description: MSB for the look-up-table baseline register of the LSD4 gate voltage output.

Bit(s)	Name	Description	Default	Type
[7:0]	LSD4_BASE<11:4>	LSD4 baseline register MSB for LUT_TEMP	0000 0000b	R/W

Page: 00h
Address: 0Eh
Register Name: LSD4_LUTV_BS_ADD
Default Value: 17'h
Description: Store the address of the LUT_VOLT which baseline of temperature is store, a value between 0-63

Bit(s)	Name	Description	Default	Type
[7:0]	LSD4_LUTV_BS_ADD<7:0>	Address of the baseline for LSD4 gate voltage output (LSD4_DEL)	0001 0111b	R/W

Page: 00h
Address: 0Fh
Register Name: LUT_TEMP_BS_MSB
Default Value: 00'h
Description: MSB for the temperature look-up-table baseline register of the LSD3t

Bit(s)	Name	Description	Default	Type
[7:0]	LUT_TEMP_BS_MSB<11:4>	MSB for the temperature look-up-table baseline register of the LSD4	0000 0000b	R/W

Page: 00h
Address: 10h
Register Name: LUT_TEMP_BS_LSB
Default Value: 00'h
Description: Store the temperature when the baseline for LUT_TEMP and LUT_VOLT are extracted;12 bit

Bit(s)	Name	Description	Default	Type
[7:4]	LUT_TEMP_BS_LSB<3:0>	User defined	0000b	R/W
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 00h
Address: 11h
Register Name: LUT_TEMP_BS_ADDRESS
Default Value: 68'h
Description: Store the address of the LUT_TEMP which BASE value is stored, a value between 0-255.Default is 104 which gives -40+104*0.625=25C

Bit(s)	Name	Description	Default	Type
[7:0]	LUT_TEMP_BS_ADD<7:0>	User defined	0110 1000b	R/W

Page: 00h
Address: 12h
Register Name: LSD1_TS_BS_MSB
Default Value: 00'h
Description: Store the LUT_TEMP MSB of the baseline ADC reading for LSD1 TEMP pin

Bit(s)	Name	Description	Default	Type
[7:0]	LSD1_TS_BS<11:4>	User defined	0000 0000b	R/W

Page: 00h
Address: 13h
Register Name: LSD2_TS_BS_MSB
Default Value: 00'h
Description: Store the LUT_TEMP MSB of the baseline ADC reading for LSD2 TEMP pin

Bit(s)	Name	Description	Default	Type
[7:0]	LSD2_TS_BS<11:4>	User defined	0000 0000b	R/W

Page: 00h
Address: 14h
Register Name: LSD12_TS_BS_LSB
Default Value: 00'h
Description: Store the LUT_TEMP LSB of the baseline ADC reading for LSD1 and LSD2 TEMP pin

Bit(s)	Name	Description	Default	Type
[7:4]	LSD2_TS_BS<3:0>	User defined	0000b	R/W
[3:0]	LSD1_TS_BS<3:0>	User defined	0000b	R/W

Page: 00h
Address: 15h
Register Name: LSD3_TS_BS_MSB
Default Value: 00'h
Description: Store the LUT_TEMP MSB of the baseline ADC reading for LSD3 TEMP pin

Bit(s)	Name	Description	Default	Type
[7:0]	LSD3_TS_BS<11:4>	User defined	0000 0000b	R/W

Page: 00h
Address: 16h
Register Name: LSD4_TS_BS_MSB
Default Value: 00'h
Description: Store LUT_TEMP MSB of the baseline ADC readingfor LSD4 TEMP pin

Bit(s)	Name	Description	Default	Type
[7:0]	LSD4_TS_BS<11:4>	User defined	0000 0000b	R/W

Page: 00h
Address: 17h
Register Name: LSD4_TS_BS_LSB
Default Value: 00'h
Description: Store the LUT_TEMP LSB of baseline ADC reading for T=25C for LSD3and LSD4 TEMP pin

Bit(s)	Name	Description	Default	Type
[7:4]	LSD4_TS_BS<3:0>	User defined	0000b	R/W
[3:0]	LSD3_TS_BS<3:0>	User defined	0000b	R/W

Page: 00h
Address: 1Fh
Register Name: VER_CTRL
Default Value: 60'h
Description: write 6xH to show it is a macom part

Bit(s)	Name	Description	Default	Type
[7:4]	*RSVD*	*Reserved (set to default)*	0110b	R
[3:0]	VERSION<3:0>	Version number	0000b	R/W

Page: 00h
Address: 33h
Register Name: ADC_CHNL_ENABLE0
Default Value: FF'h
Description: input select of ADC,power down LSDx_TEMP also mean the disable the coresponds TS. Disable one channel means the next channel will take place of it. For example, if only one channel is left, then ADC will keep sample it.Digital need to send a enable signal at the previous channel of a current sense channel to garantee the settling time

Bit(s)	Name	Description	Default	Type
[7]	EN_LSD3_OUTN	0b: Disable 1b: Enable	1b	R/W
[6]	EN_LSD2_OUTN	0b: Disable 1b: Enable	1b	R/W
[5]	EN_LSD1_OUTN	0b: Disable 1b: Enable	1b	R/W
[4]	EN_LSD4_OUTP	0b: Disable 1b: Enable	1b	R/W
[3]	EN_LSD3_OUTP	0b: Disable 1b: Enable	1b	R/W
[2]	EN_LSD2_OUTP	0b: Disable 1b: Enable	1b	R/W
[1]	EN_LSD1_OUTP	0b: Disable 1b: Enable	1b	R/W
[0]	*RSVD*	*Reserved (set to default)*	1b	R/W

Page: 00h
Address: 53h
Register Name: ADC_INPUT_MULTIPLIER0
Default Value: 3F'h
Description: ADC front end amplifier

Bit(s)	Name	Description	Default	Type
[7:6]	mult_ADC_INPUT14[1:0]	00b: x1/2 10b: x1/4 11b: x1 01b: x1/3	00b	R/W
[5:4]	mult_ADC_INPUT13[1:0]	00b: x1/2 10b: x1/4 11b: x1 01b: x1/3	11b	R/W
[3:2]	mult_ADC_INPUT12[1:0]	00b: x1/2 10b: x1/4 11b: x1 01b: x1/3	11b	R/W
[1:0]	mult_ADC_INPUT11[1:0]	00b: x1/2 10b: x1/4 11b: x1 01b: x1/3	11b	R/W

Page: 00h
Address: 54h
Register Name: ADC_INPUT_MULTIPLIER1
Default Value: 00'h
Description: ADC front end amplifier

Bit(s)	Name	Description	Default	Type
[7:6]	mult_ADC_INPUT18[1:0]	00b: x1/2 10b: x1/4 11b: x1 01b: x1/3	00b	R/W
[5:4]	mult_ADC_INPUT17[1:0]	00b: x1/2 10b: x1/4 11b: x1 01b: x1/3	00b	R/W
[3:2]	mult_ADC_INPUT16[1:0]	00b: x1/2 10b: x1/4 11b: x1 01b: x1/3	00b	R/W
[1:0]	mult_ADC_INPUT15[1:0]	00b: x1/2 10b: x1/4 11b: x1 01b: x1/3	00b	R/W

Page: 00h
Address: 55h
Register Name: ADC_INPUT_MULTIPLIER2
Default Value: 30'h
Description: ADC front end amplifier

Bit(s)	Name	Description	Default	Type
[7:6]	mult_ADC_INPUT22[1:0]	00b: x1/2 10b: x1/4 11b: x1 01b: x1/3	00b	R/W
[5:4]	mult_ADC_INPUT21[1:0]	00b: x1/2 10b: x1/4 11b: x1 01b: x1/3	11b	R/W
[3:2]	mult_ADC_INPUT20[1:0]	00b: x1/2 10b: x1/4 11b: x1 01b: x1/3	00b	R/W
[1:0]	mult_ADC_INPUT19[1:0]	00b: x1/2 10b: x1/4 11b: x1 01b: x1/3	00b	R/W

Page: 00h
Address: 56h
Register Name: ADC_INPUT_MULTIPLIER3
Default Value: 54'h
Description: ADC front end amplifier

Bit(s)	Name	Description	Default	Type
[7:6]	mult_ADC_INPUT2[1:0]	ADC_Code=M . I [uA]+409 00-->M = 3.6, 01--> M = 3.2, 10--> M= 2.88, 11--> M= 2.66	01b	R/W
[5:4]	mult_ADC_INPUT1[1:0]	ADC_Code=M . I [uA]+409 00-->M = 3.6, 01--> M = 3.2, 10--> M= 2.88, 11--> M= 2.66	01b	R/W
[3:2]	mult_ADC_INPUT0[1:0]	ADC_Code=M . I [uA]+409 00-->M = 3.6, 01--> M = 3.2, 10--> M= 2.88, 11--> M= 2.66	01b	R/W
[1:0]	mult_ADC_INPUT23[1:0]	ADC_Code=M . I [uA]+409 00-->M = 3.6, 01--> M = 3.2, 10--> M= 2.88, 11--> M= 2.66	00b	R/W

Page: 00h
Address: 57h
Register Name: ADC_INPUT_MULTIPLIER4
Default Value: 55'h
Description: ADC front end amplifier

Bit(s)	Name	Description	Default	Type
[7:6]	mult_ADC_INPUT6[1:0]	ADC_Code=M . I [uA]+409 00-->M = 3.6, 01--> M = 3.2, 10--> M= 2.88, 11--> M= 2.66	01b	R/W
[5:4]	mult_ADC_INPUT5[1:0]	ADC_Code=M . I [uA]+409 00-->M = 3.6, 01--> M = 3.2, 10--> M= 2.88, 11--> M= 2.66	01b	R/W
[3:2]	mult_ADC_INPUT4[1:0]	ADC_Code=M . I [uA]+409 00-->M = 3.6, 01--> M = 3.2, 10--> M= 2.88, 11--> M= 2.66	01b	R/W
[1:0]	mult_ADC_INPUT3[1:0]	ADC_Code=M . I [uA]+409 00-->M = 3.6, 01--> M = 3.2, 10--> M= 2.88, 11--> M= 2.66	01b	R/W

Page: 00h
Address: 58h
Register Name: ADC_INPUT_MULTIPLIER5
Default Value: 55'h
Description: ADC front end amplifier

Bit(s)	Name	Description	Default	Type
[7:6]	mult_ADC_INPUT10[1:0]	ADC_Code=M . I [uA]+409 00-->M = 3.6, 01--> M = 3.2, 10--> M= 2.88, 11--> M= 2.66	01b	R/W
[5:4]	mult_ADC_INPUT9[1:0]	ADC_Code=M . I [uA]+409 00-->M = 3.6, 01--> M = 3.2, 10--> M= 2.88, 11--> M= 2.66	01b	R/W
[3:2]	mult_ADC_INPUT8[1:0]	ADC_Code=M . I [uA]+409 00-->M = 3.6, 01--> M = 3.2, 10--> M= 2.88, 11--> M= 2.66	01b	R/W
[1:0]	mult_ADC_INPUT7[1:0]	ADC_Code=M . I [uA]+409 00-->M = 3.6, 01--> M = 3.2, 10--> M= 2.88, 11--> M= 2.66	01b	R/W

Page: 00h
Address: 65h
Register Name: LSD1_CTRL0
Default Value: 8B'h
Description: LSD Channel 1, Control Byte 0

Bit(s)	Name	Description	Default	Type
[7:5]	LSD1_CL	Set the current limit threshold from 20mA to 100mA with 20mA per step, LSD1_CL<2:0>=<111> to disable current limiter 111b: Disable current limiter 110b: 101b: 100b: 011b: 010b: 001b: 000b:	100b	R/W
[4:1]	*RSVD*	*Reserved (set to default)*	0101b	R
[0]	LSD1_REG_EN	1b: Enable digital LSD 0b: Disable digital LSD	1b	R/W

Page: 00h
Address: 66h
Register Name: LSD1_CTRL1
Default Value: 00'h
Description: LSD Channel 1, Control Byte 1

Bit(s)	Name	Description	Default	Type
[7]	*RSVD*	*Reserved (set to default)*	0b	R
[6]	LSD1_CSP_EN	1b: Enable LSD1 PMOS current sense 0b: Disable LSD1 PMOS current sense	0b	R/W
[5]	LSD1_CSN_EN	1b: Enable LSD1 NMOS current sense 0b: Disable LSD1 NMOS current sense	0b	R/W
[4:0]	*RSVD*	*Reserved (set to default)*	0 0000b	R

Page: 00h
Address: 67h
Register Name: LSD2_CTRL0
Default Value: 8B'h
Description: LSD2 driver control bytes;- DISABLED mode, where the LSDs are disabled and the gates are not connected to the buffers
- SAFE mode, where the LSDs are enabled but the gates are connected to the negative supply (or whatever the lower limit is specified)
- LIVE mode, where the LSDs are enabled and their output is connected to the gates

Bit(s)	Name	Description	Default	Type
[7:5]	LSD2_CL	Set the current limit threshold from 20mA to 100mA with 20mA per step, LSD2_CL<2:0>=<111> to disable current limiter 111b: Disable current limiter 110b: 101b: 100b: 011b: 010b: 001b: 000b:	100b	R/W
[4:1]	*RSVD*	*Reserved (set to default)*	0101b	R
[0]	LSD2_REG_EN	1b: Enable digital LSD 0b: Disable digital LSD	1b	R/W

Page: 00h
Address: 68h
Register Name: LSD2_CTRL1
Default Value: 00'h
Description:

Bit(s)	Name	Description	Default	Type
[7]	*RSVD*	*Reserved (set to default)*	0b	R
[6]	LSD2_CSP_EN	1b: Enable LSD2 PMOS current sense 0b: Disable LSD2 PMOS current sense	0b	R/W
[5]	LSD2_CSN_EN	1b: Enable LSD2 NMOS current sense 0b: Disable LSD2 NMOS current sense	0b	R/W
[4:0]	*RSVD*	*Reserved (set to default)*	0 0000b	R

Page: 00h
Address: 69h
Register Name: LSD3_CTRL0
Default Value: 8B'h
Description: LSD3 driver control bytes;- DISABLED mode, where the LSDs are disabled and the gates are not connected to the buffers
- SAFE mode, where the LSDs are enabled but the gates are connected to the negative supply (or whatever the lower limit is specified)
- LIVE mode, where the LSDs are enabled and their output is connected to the gates

Bit(s)	Name	Description	Default	Type
[7:6]	LSD3_CL	Set the current limit threshold from 20mA to 100mA with 20mA per step, LSD3_CL=<111> to disable current limiter 111b: Disable current limiter 110b: 101b: 100b: 011b: 010b: 001b: 000b:	100b	R/W
[4:1]	*RSVD*	*Reserved (set to default)*	0101	R
[0]	LSD3_REG_EN	1b: Enable digital LSD 0b: Disable digital LSD	1b	R/W

Page: 00h
Address: 6Ah
Register Name: LSD3_CTRL1
Default Value: 00'h
Description:

Bit(s)	Name	Description	Default	Type
[7]	*RSVD*	*Reserved (set to default)*	0b	R
[6]	LSD3_CSP_EN	1b: Enable LSD3 PMOS current sense 0b: Disable LSD3 PMOS current sense	0b	R/W
[5]	LSD3_CSN_EN	1b: Enable LSD3 NMOS current sense 0b: Disable LSD3 NMOS current sense	0b	R/W
[4:0]	*RSVD*	*Reserved (set to default)*	0 0000b	R

Page: 00h
Address: 6Bh
Register Name: LSD4_CTRL0
Default Value: 8B'h
Description: LSD4 driver control bytes;- DISABLED mode, where the LSDs are disabled and the gates are not connected to the buffers
- SAFE mode, where the LSDs are enabled but the gates are connected to the negative supply (or whatever the lower limit is specified)
- LIVE mode, where the LSDs are enabled and their output is connected to the gates

Bit(s)	Name	Description	Default	Type
[7:5]	LSD4_CL	Set the current limit threshold from 20mA to 100mA with 20mA per step, LSD4_CL=<111> to disable current limiter 111b: Disable current limiter 110b: 101b: 100b: 011b: 010b: 001b: 000b:	100b	R/W
[4:1]	*RSVD*	*Reserved (set to default)*	0101b	R
[0]	LSD4_REG_EN	1b: Enable digital LSD 0b: Disable digital LSD	1b	R/W

Page: 00h
Address: 6Ch
Register Name: LSD4_CTRL1
Default Value: 00'h
Description:

Bit(s)	Name	Description	Default	Type
[7]	*RSVD*	*Reserved (set to default)*	0b	R
[6]	LSD4_CSP_EN	1b: Enable LSD4 PMOS current sense 0b: Disable LSD4 PMOS current sense	0b	R/W
[5]	LSD4_CSN_EN	1b: Enable LSD4 NMOS current sense 0b: Disable LSD4 NMOS current sense	0b	R/W
[4:0]	*RSVD*	*Reserved (set to default)*	0 0000b	R

Page: 00h
Address: 6Dh
Register Name: OVERRIDE_CTRL
Default Value: 00'h
Description: Normal working , the codes to DAC are digital generated. Write to following bytes will override the generated control bytes. Override control register form 4x DAC

Bit(s)	Name	Description	Default	Type
[7:4]	DAC_ORD <3:0>	LSD4,LSD3,LSD2,LSD1; 0001b: Enable override, 0000b: Normal operation	0000b	R/W
[3:0]	TEMP_ORD <3:0>	Use the data in OFFCHIP_TEMP<11:0> to override the cal_tsx<11:0> , LSD4,LSD3,LSD2,LSD1; 0001b: Enable override of cal_ts[1:4] 0000b: Normal operation	0000b	R/W

Page: 00h
Address: 6Eh
Register Name: DAC_LSD1_MSB
Default Value: 00'h
Description: MSB of the DAC for LSD1 from digital

Bit(s)	Name	Description	Default	Type
[7:0]	DAC_LSD1<11:4>	MSB of the DAC for the out LSD1	0000 0000b	R

Page: 00h
Address: 6Fh
Register Name: DAC_LSD1_LSB
Default Value: 00'h
Description: LSB of the DAC for LSD1 from digital

Bit(s)	Name	Description	Default	Type
[7:4]	DAC_LSD1<3:0>	LSB of the DAC for the out LSD1	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 00h
Address: 70h
Register Name: DAC_LSD1_ORD_MSB
Default Value: 00'h
Description: Override MSB of LSD1 from GUI

Bit(s)	Name	Description	Default	Type
[7:0]	DAC_LSD1_ORD<11:4>	User defined	0000 0000b	R/W

Page: 00h
Address: 71h
Register Name: DAC_LSD1_ORD_LSB
Default Value: 00'h
Description: Override LSB of LSD1 from GUI

Bit(s)	Name	Description	Default	Type
[7:4]	DAC_LSD1_ORD<3:0>	User defined	0000b	R/W
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 00h
Address: 72h
Register Name: DAC_LSD2_MSB
Default Value: 00'h
Description: MSB of the DAC for output LSD2 from digital

Bit(s)	Name	Description	Default	Type
[7:0]	DAC_LSD2<11:4>	User defined	0000 0000b	R

Page: 00h
Address: 73h
Register Name: DAC_LSD2_LSB
Default Value: 00'h
Description: LSB of the DAC for output LSD2 from digital

Bit(s)	Name	Description	Default	Type
[7:4]	DAC_LSD2 <3:0>	LSB of the DAC for output LSD2 from digital	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 00h
Address: 74h
Register Name: DAC_LSD2_ORD_MSB
Default Value: 00'h
Description: Override MSB of LSD2 from GUI

Bit(s)	Name	Description	Default	Type
[7:0]	DAC_LSD2_ORD<11:4>	User defined	0000 0000b	R/W

Page: 00h
Address: 75h
Register Name: DAC_LSD2_ORD_LSB
Default Value: 00'h
Description: Override LSB of LSD2 from GUI

Bit(s)	Name	Description	Default	Type
[7:4]	DAC_LSD2_ORD<3:0>	User defined	0000b	R/W
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 00h
Address: 76h
Register Name: DAC_LSD3_MSB
Default Value: 00'h
Description: MSB of the DAC for output LSD3 from digital

Bit(s)	Name	Description	Default	Type
[7:0]	DAC_LSD3<11:4>	User defined	0000 0000b	R

Page: 00h
Address: 77h
Register Name: DAC_LSD3_LSB
Default Value: 00'h
Description: LSB of the DAC for output LSD2 from digital

Bit(s)	Name	Description	Default	Type
[7:4]	DAC_LSD3<3:0>	User defined	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 00h
Address: 78h
Register Name: DAC_LSD3_ORD_MSB
Default Value: 00'h
Description: override MSB of LSD3 from GUI

Bit(s)	Name	Description	Default	Type
[7:0]	DAC_LSD3_ORD<11:4>	User defined	0000 0000b	R/W

Page: 00h
Address: 79h
Register Name: DAC_LSD3_ORD_LSB
Default Value: 00'h
Description: override LSB of LSD3 from GUI

Bit(s)	Name	Description	Default	Type
[7:4]	DAC_LSD3_ORD<3:0>	User defined	0000b	R/W
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 00h
Address: 7Ah
Register Name: DAC_LSD4_MSB
Default Value: 00'h
Description: MSB of the DAC for output LSD4 from digital

Bit(s)	Name	Description	Default	Type
[7:0]	DAC_LSD4<11:4>	User defined	0000 0000b	R

Page: 00h
Address: 7Bh
Register Name: DAC_LSD4_LSB
Default Value: 00'h
Description: LSB of the DAC for output LSD4 from digital

Bit(s)	Name	Description	Default	Type
[7:4]	DAC_LSD4<3:0>	User defined	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 00h
Address: 7Ch
Register Name: DAC_LSD4_ORD_MSB
Default Value: 00'h
Description: override MSB of LSD4 from GUI

Bit(s)	Name	Description	Default	Type
[7:0]	DAC_LSD4_ORD<11:4>	User defined	0000 0000b	R/W

Page: 00h
Address: 7Dh
Register Name: DAC_LSD4_ORD_LSB
Default Value: 00'h
Description: override LSB of LSD4 from GUI

Bit(s)	Name	Description	Default	Type
[7:4]	DAC_LSD4_ORD<3:0>	User defined	0000b	R/W
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 00h
Address: 7Eh
Register Name: PREDRIVER_CTRL0
Default Value: 57'h
Description: reserved

Bit(s)	Name	Description	Default	Type
[7:4]	Pre_driver_current<3:0>	From 4.0mA to 11.5mA, 0.5mA/ step:6.5mA is the default setting,the current is source type from supply	0101b	R/W
[3]	Tswoff_infinity	Extend the Tswoff timer to infinity, shutdown opam in 4x LSD won't shutdown HSD sequencly	0b	R/W
[2:0]	HSD_driver_current<2:0>	HSD output current setting, from 3mA to 10mA 1mA per step	111b	R/W

Page: 00h
Address: 7Fh
Register Name: GPIO_CTRL0
Default Value: 00'h
Description: I2C can write to define the GPIO status

Bit(s)	Name	Description	Default	Type
[7:4]	*RSVD*	*Reserved (set to default)*	0000b	R
[3:0]	gpio_status<3:0>	0011b: GPIO3 0010b: GPIO2 0001b: GPIO1 0000b: GPIO0	0000b	R/W

Page: 00h
Address: 80h
Register Name: HSD_Timing
Default Value: D3'h
Description: delay in startup and timing diagram

Bit(s)	Name	Description	Default	Type
[7:6]	ton<1:0>	00b:Tswon x1, 01b:Tswon x 256; 10b: Tswon x 512, 11b: Tswon x 1024 (extend the clock cycle number)	11b	R/W
[5:4]	tswon<1:0>	00b:32x 12MHz clock cycles 01b:64x 12MHz clock cycles 10b:128x 12MHz clock cycles 11b: 256x 12MHz clock cycles	01b	R/W
[3:2]	tswoff<1:0>	00b: 32x 12MHz clock cycles 01b: 64x 12MHz clock cycles 10b: 128x 12MHz clock cycles 11b: 256x 12MHz clock cycles	00b	R/W
[1:0]	toff<1:0>	00b: Tswoff x1, 01b: Tswoff x 256; 10b: Tswoff x 512, 11b: Tswoff x 1024 (extend the clock cycle number)	11b	R/W

Page: 00h
Address: 8Eh
Register Name: CP_CTRL
Default Value: 00'h
Description: charge pump control bits

Bit(s)	Name	Description	Default	Type
[7:6]	cl_freq<1:0>	00b: 1MHz 01b: 2MHz 10b: 4MHz 11b: 0.5MHz	00b	R/W
[5:4]	cp_mode<1:0>	00b: 4 slides 01b: 3 slides 10b: 2 slices 11b: 1slice	00b	R/W
[3:2]	cp_drv<1:0>	00b: weak 01b: strong 10b: stronger 11b: ludicrous	00b	R/W
[1]	cp_dis	1b: Disable charge pump, 0b: Enable charge pump	0b	R/W
[0]	allrdy_debouce_dis	1b: 1 Disable debounce compensation in *all_lsd_rdy,* 0b: Enable debounce compensation in *all_lsd_rdy*	0b	R/W

Page: 00h
Address: 93h
Register Name: ALARM_CTRL0
Default Value: A0'h
Description: Alarm ctrl bits 0

Bit(s)	Name	Description	Default	Type
[7:6]	UV_alarm_Vth	Set under-voltage threshold for voltage monitor on main input power) 00b: 3.8V 01b: 4.0V 10b: 4.2V 11b: 4.4V	10b	R/W
[5:4]	OT_Shutdown_threshold	Define the over temperature shutdown threshold 00b: 130C 01b: 140C 10b: 150C 11b: Disable thermal shutdown	10b	R/W
[3:2]	vneg_rdy_vth	Negative voltage ready threshold 00b: -3.9V 01b: -4.4V 10b: -4.9V 11b: -5.4V	00b	R/W
[1:0]	RSVD	Reserved	00b	R

Page: 00h
Address: 94h
Register Name: IIN1_THRESHOLD
Default Value: F8'h
Description: Write the limit threshold of IIN1 reading from ADC, if the MSB of ADC reading is high than this value, issue a alarm bit

Bit(s)	Name	Description	Default	Type
[7:0]	IIN1_THRESHOLD<7:0>	User defined	1111 1000b	R/W

Page: 00h
Address: 95h
Register Name: IIN2_THRESHOLD
Default Value: F8'h
Description: Write the limit theshold of IIN2 reading from ADC, if the MSB of ADC reading is high than this value, issue a alarm bit

Bit(s)	Name	Description	Default	Type
[7:0]	IIN2_THRESHOLD<7:0>	User defined	1111 1000b	R/W

Page: 00h
Address: 96h
Register Name: TEMP1_OT_S_THD
Default Value: F8'h
Description: TEMP_SENSE1 over-temperature alarm threshold. Over-temperature alarm asserts if the internal temperature reading above this value.

Bit(s)	Name	Description	Default	Type
[7:0]	TEMP1_OT_THD<7:0>	User defined	1111 1000b	R/W

Page: 00h
Address: 97h
Register Name: TEMP1_OT_R_THD
Default Value: F0'h
Description: TEMP_SENSE1 over-temperature alarm reset threshold. Over-temperature alarm de-asserts if the internal temperature reading is less than this value.

Bit(s)	Name	Description	Default	Type
[7:0]	TEMP1_OT_R_THD<7:0>	User defined	1111 0000b	R/W

Page: 00h
Address: 98h
Register Name: TEMP2_OT_S_THD
Default Value: F8'h
Description: TEMP_SENSE2 over-temperature alarm threshold. Over-temperature alarm asserts if the internal temperature reading above this value..

Bit(s)	Name	Description	Default	Type
[7:0]	TEMP2_OT_THD<7:0>	User defined	1111 1000b	R/W

Page: 00h
Address: 99h
Register Name: TEMP2_OT_R_THD
Default Value: F0'h
Description: TEMP_SENSE2 over-temperature alarm reset threshold. Over-temperature alarm de-asserts if the internal temperature reading is less than this value..

Bit(s)	Name	Description	Default	Type
[7:0]	TEMP2_OT_R_THD<7:0>	User defined	1111 0000b	R/W

Page: 00h
Address: 9Ah
Register Name: TEMP3_OT_S_THD
Default Value: F8'h
Description: TEMP_SENSE3 over-temperature alarm threshold. Over-temperature alarm asserts if the internal temperature reading above this value.

Bit(s)	Name	Description	Default	Type
[7:0]	TEMP3_OT_THD<7:0>	User defined	1111 1000b	R/W

Page: 00h
Address: 9Bh
Register Name: TEMP3_OT_R_THD
Default Value: F0'h
Description: TEMP_SENSE3 over-temperature alarm reset threshold. Over-temperature alarm de-asserts if the internal temperature reading is less than this value..

Bit(s)	Name	Description	Default	Type
[7:0]	TEMP3_OT_R_THD<7:0>	User defined	1111 0000b	R/W

Page: 00h
Address: 9Ch
Register Name: TEMP4_OT_S_THD
Default Value: F8'h
Description: TEMP_SENSE4 over-temperature alarm threshold. Over-temperature alarm asserts if the internal temperature reading above this value..

Bit(s)	Name	Description	Default	Type
[7:0]	TEMP4_OT_THD<7:0>	User defined	1111 1000b	R/W

Page: 00h
Address: 9Dh
Register Name: TEMP4_OT_R_THD
Default Value: F0'h
Description: TEMP_SENSE4 over-temperature alarm reset threshold. Over-temperature alarm de-asserts if the internal temperature reading is less than this value.

Bit(s)	Name	Description	Default	Type
[7:0]	TEMP4_OT_R_THD<7:0>	User defined	1111 0000b	R/W

Page: 00h
Address: 9Eh
Register Name: TS_VBG_OT_THD
Default Value: F8'h
Description: Voltage bandgap temperature sensor over-temperature alarm threshold. Over-temperature alarm asserts if the internal temperature reading is above this value.

Bit(s)	Name	Description	Default	Type
[7:0]	TS_VBG_OT_S_THD<7:0>	User defined	1111 1000b	R/W

Page: 00h
Address: 9Fh
Register Name: TS_VBG_OT_R_THD
Default Value: F0'h
Description: Voltage bandgap temperature sensor over-temperature alarm reset threshold. Over-temperature alarm de-asserts if the internal temperature reading is less than this value.

Bit(s)	Name	Description	Default	Type
[7:0]	TS_VBG_OT_R_THD<7:0>	User defined	1111 0000b	R/W

Page: 00h
Address: A0h
Register Name: TS_PTAT_OT_THD
Default Value: F8'h
Description: PTAT (Proportional to Ambient Temperature) temperature sensor over-temperature alarm threshold. Over-temperature alarm asserts if the internal temperature reading is above this value.

Bit(s)	Name	Description	Default	Type
[7:0]	TS_PTAT_OT_S_THD<7:0>	User defined	1111 1000b	R/W

Page: 00h
Address: A1h
Register Name: TS_PTAT_OT_R_THD
Default Value: F0'h
Description: PTAT (Proportional to Ambient Temperature) temperature sensor over-temperature alarm reset threshold, Over-temperature alarm de-asserts if the internal temperature reading is less than this value.

Bit(s)	Name	Description	Default	Type
[7:0]	TS_PTAT_OT_R_THD<7:0>	User defined	1111 0000b	R/W

Page: 00h
Address: A2h
Register Name: FAIL_CTRL
Default Value: 20'h
Description: Fail pin Ctrl, in scan and bist mode, always cmos output only

Bit(s)	Name	Description	Default	Type
[7]	alarm_clear	1b: Clear all latched alarms 0b: Normal operation	0b	R/W
[6]	*RSVD*	*Reserved (set to default)*	0b	R
[5]	Fail_out_cmos	1b: Fail pin output type is an open-drain output 0b: Fail pin output type is a CMOS output	1b	R/W
[4]	Fail_flip_polar	1b: Active high logic 0b: Active low logic	0b	R/W
[3:1]	Fail_interrupt_duration	Number of clock cycles of Fail output pin is pulled low in interrupt mode 000b = 12 001b = 24 010b = 36 011b = 48 100b = 60 101b = 72 110b = 84 111b = 96	000b	R/W
[0]	FAIL_PIN_MODE	Controls the FAIL pin behavior 1b:Trigger lock mode 0b: Interrupt mode	0b	R/W

Page: 00h
Address: A3h
Register Name: ALARM_MASK0
Default Value: 00'h
Description: Alarm mask 0 for register Alarm0

Bit(s)	Name	Description	Default	Type
[7]	msk_neg_uv_rt	1b: Mask negative voltage under-voltage alarm 0b: Normal operation	0b	R/W
[6]	msk_lsd1_cl_rt	1b: Mask LSD1 current limit alarm 0b: Normal operation	0b	R/W
[5]	msk_lsd2_cl_rt	1b: Mask LSD2 current limit alarm 0b: Normal operation	0b	R/W
[4]	msk_lsd3_cl_rt	1b: Mask LSD3 current limit alarm 0b: Normal operation	0b	R/W

Bit(s)	Name	Description	Default	Type
[3]	msk_lsd4_cl_rt	1b: Mask LSD4 current limit alarm 0b: Normal operation	0b	R/W
[2]	msk_v1p8d_uv_rt	1b: Mask 1.8V digital supply under-voltage alarm 0b: Normal operation	0b	R/W
[1]	msk_v1p8a_uv_rt	1b: Mask 1.8V analog supply under-voltage alarm 0b: Normal operation	0b	R/W
[0]	msk_uv_alarm_rt	1b: Mask 5V analog supply under-voltage alarm 0b: Normal operation	0b	R/W

Page: 00h
Address: A4h
Register Name: ALARM_MASK1
Default Value: 00'h
Description: Alarm mask 1 for register Alarm_LUT_VOLT (page 02h, Address 43h)

Bit(s)	Name	Description	Default	Type
[7]	msk_lsd4_lut_volt_p	1b: Mask LSD4 Alarm - ALU did not finish at address 63 0b: Normal operation	0b	R/W
[6]	msk_lsd4_lut_volt_n	1b: Mask LSD4 Alarm - ALU did not finish at address 0 0b: Normal operation	0b	R/W
[5]	msk_lsd3_lut_volt_p	1b: Mask LSD3 Alarm - ALU did not finish at address 63 0b: Normal operation	0b	R/W
[4]	msk_lsd3_lut_volt_n	1b: Mask LSD3 Alarm - ALU did not finish at address 0 0b: Normal operation	0b	R/W
[3]	msk_lsd2_lut_volt_p	1b: Mask LSD2 Alarm - ALU did not finish at address 63 0b: Normal operation	0b	R/W
[2]	msk_lsd2_lut_volt_p	1b: Mask LSD2 Alarm - ALU did not finish at address 0 0b: Normal operation	0b	R/W
[1]	msk_lsd1_lut_volt_p	1b: Mask LSD1 Alarm - ALU did not finish at address 63 0b: Normal operation	0b	R/W
[0]	msk_lsd1_lut_volt_p	1b: Mask LSD4 Alarm - ALU did not finish at address 0 0b: Normal operation	0b	R/W

Page: 00h
Address: A5h
Register Name: ALARM_MASK2
Default Value: 03'h
Description: Alarm mask 2 for TEMP_ALARM

Bit(s)	Name	Description	Default	Type
[7]	msk_iin1_cl_lt	1b: Mask latched IIN1 current limit alarm 0b: Normal operation	0b	R/W
[6]	msk_iin2_cl_lt	1b: Mask latched IIN2 current limit alarm 0b: Normal operation	0b	R/W
[5]	msk_TS_VBG_Alarm	1b: Mask latched voltage bandgap temperature sensor alarm 0b: Normal operation	0b	R/W
[4]	msk_TS_PTAT_Alarm	1b: Mask latched PTAT temperature sensor alarm 0b: Normal operation	0b	R/W
[3]	msk_LSD4_TS_Alarm	1b: Mask latched temperature alarm for LSD4 0b: Normal operation	0b	R/W
[2]	msk_LSD3_TS_Alarm	1b: Mask latched temperature alarm for LSD3 0b: Normal operation	0b	R/W
[1]	msk_LSD2_TS_Alarm	1b: Mask latched temperature alarm for LSD2 0b: Normal operation	1b	R/W
[0]	msk_LSD1_TS_Alarm	1b: Mask latched temperature alarm for LSD1 0b: Normal operation	1b	R/W

Page: 00h
Address: A6h
Register Name: ALARM_MASK3
Default Value: 03'h
Description: Alarm mask 3 for Alarm_LUT_TEMP

Bit(s)	Name	Description	Default	Type
[7]	msk_lsd4_lut_volt_p	1b: Mask LSD4 Alarm - ALU did not finish at address 255 0b: Normal operation	0b	R/W
[6]	msk_lsd4_lut_volt_n	1b: Mask LSD4 Alarm - ALU did not finish at address 0 0b: Normal operation	0b	R/W
[5]	msk_lsd3_lut_volt_p	1b: Mask LSD3 Alarm - ALU did not finish at address 255 0b: Normal operation	0b	R/W
[4]	msk_lsd3_lut_volt_n	1b: Mask LSD3 Alarm - ALU did not finish at address 0 0b: Normal operation	0b	R/W
[3]	msk_lsd2_lut_volt_p	1b: Mask LSD2 Alarm - ALU did not finish at address 255 0b: Normal operation	0b	R/W

Bit(s)	Name	Description	Default	Type
[2]	msk_lsd2_lut_volt_p	1b: Mask LSD2 Alarm - ALU did not finish at address 0 0b: Normal operation	0b	R/W
[1]	msk_lsd1_lut_volt_p	1b: Mask LSD1 Alarm - ALU did not finish at address 255 0b: Normal operation	0b	R/W
[0]	msk_lsd1_lut_volt_p	1b: Mask LSD4 Alarm - ALU did not finish at address 0 0b: Normal operation	0b	R/W

Page: 00h
Address: AAh
Register Name: UPLIMIT_LSD1_MSB
Default Value: FF'h
Description: Set the up limit of the DAC code of LSD1, MSB

Bit(s)	Name	Description	Default	Type
[7:0]	UPLIMIT_LSD1<11:4>	User defined	1111 1111b	R/W

Page: 00h
Address: ABh
Register Name: UPLIMIT_LSD2_MSB
Default Value: FF'h
Description: Set the up limit of the DAC code of LSD2, MSB

Bit(s)	Name	Description	Default	Type
[7:0]	UPLIMIT_LSD2<11:4>	User defined	1111 1111b	R/W

Page: 00h
Address: ACh
Register Name: UPLIMIT_LSD12_LSB
Default Value: FF'h
Description: Set the up limit of the DAC code of LSD1 and LSD2, LSB

Bit(s)	Name	Description	Default	Type
[7:4]	UPLIMIT_LSD1<3:0>	User defined	1111b	R/W
[3:0]	UPLIMIT_LSD2<3:0>	User defined	1111b	R/W

Page: 00h
Address: ADh
Register Name: UPLIMIT_LSD3_MSB
Default Value: FF'h
Description: Set the up limit of the DAC code of LSD3, MSB

Bit(s)	Name	Description	Default	Type
[7:0]	UPLIMIT_LSD3<11:4>	User defined	1111 1111b	R/W

Page: 00h
Address: AEh
Register Name: UPLIMIT_LSD4_MSB
Default Value: FF'h
Description: Set the up limit of the DAC code of LSD4, MSB

Bit(s)	Name	Description	Default	Type
[7:0]	UPLIMIT_LSD4<11:4>	User defined	1111 1111b	R/W

Page: 00h
Address: AFh
Register Name: UPLIMIT_LSD34_LSB
Default Value: FF'h
Description: Set the up limit of the DAC code of LSD3 and LSD4, LSB

Bit(s)	Name	Description	Default	Type
[7:4]	UPLIMIT_LSD3<3:0>	User defined	1111b	R/W
[3:0]	UPLIMIT_LSD4<3:0>	User defined	1111b	R/W

Page: 00h
Address: B0h
Register Name: BTLIMIT_LSD1_MSB
Default Value: 00'h
Description: Set the bottom limit of the DAC code of LSD1, MSB

Bit(s)	Name	Description	Default	Type
[7:0]	BTLIMIT_LSD1<11:4>	User defined	0000 0000b	R/W

Page: 00h
Address: B1h
Register Name: BTLIMIT_LSD2_MSB
Default Value: 00'h
Description: Set the bottom limit of the DAC code of LSD2, MSB

Bit(s)	Name	Description	Default	Type
[7:0]	BTLIMIT_LSD2<11:4>	User defined	0000 0000b	R/W

Page: 00h
Address: B2h
Register Name: BTLIMIT_LSD12_LSB
Default Value: 00'h
Description: Set the bottom limit of the DAC code of LSD1 and LSD2, LSB

Bit(s)	Name	Description	Default	Type
[7:4]	BTLIMIT_LSD1<3:0>	User defined	0000b	R/W
[3:0]	BTLIMIT_LSD2<3:0>	User defined	0000b	R/W

Page: 00h
Address: B3h
Register Name: BTLIMIT_LSD3_MSB
Default Value: 00'h
Description: Set the bottom limit of the DAC code of LSD3, MSB

Bit(s)	Name	Description	Default	Type
[7:0]	BTLIMIT_LSD3<11:4>	User defined	0000 0000b	R/W

Page: 00h
Address: B4h
Register Name: BTLIMIT_LSD4_MSB
Default Value: 00'h
Description: Set the bottom limit of the DAC code of LSD4, MSB

Bit(s)	Name	Description	Default	Type
[7:0]	BTLIMIT_LSD4<11:4>	User defined	0000 0000b	R/W

Page: 00h
Address: B5h
Register Name: BTLIMIT_LSD34_LSB
Default Value: 00'h
Description: Set the bottom limit of the DAC code of LSD3 and LSD4, LSB

Bit(s)	Name	Description	Default	Type
[7:4]	BTLIMIT_LSD3<3:0>	User defined	0000b	R/W
[3:0]	BTLIMIT_LSD4<3:0>	User defined	0000b	R/W

Page: 00h
Address: B6h
Register Name: LUT_VOLT_CTRL
Default Value: 08'h
Description: control bit of the LUT voltage

Bit(s)	Name	Description	Default	Type
[7:4]	*RSVD*	*Reserved (set to default)*	0000b	R
[3:0]	LUTVOLT_TEMP_SEL<3:0>	LUT_VOLT_CTRL<3:0>: 0000: TS_VPTAT ->LSD[1:4] 0001: TS_VBG ->LSD[1:4] 0010: TS1 ->LSD[1:4] 0011:TS2 ->LSD[1:4] 0100:TS3 -> LSD[1:4] 0101:TS3 -> LSD2 and LSD4; TS1->LSD1 and LSD3 0110:TS4 -> LSD[1:4] 0111:TS1 -> LSD1 and LSD3, TS2-> LSD2 and LSD4 1000: TS3 -> LSD1 and LSD3, TS4 -> LSD2 and LSD4 1001: TS1->LSD1 and LSD3, TS2=LSD2, TS4=LSD4 1010:TS3->LSD1 and LSD3, TS2=LSD2, TS4=LSD4 1011:TS2->LSD2 and LSD4, TS1=LSD1, TS3=LSD3 1100:TS4->LSD2 and LSD4, TS1=LSD1, TS3=LSD3 1101: TS1->LSD1;TS2->LSD2;TS3->LSD3;TS3->LSD4 1110: TS_PTAT->LSD2 and LSD4; TS1->LSD1 and LSD3 1111:TS_OFFCHIP->LSD[1:4]	1000b	R/W

Page: 00h
Address: B7h
Register Name: I2C_CONTROL
Default Value: 80'h
Description: I2C control, skipped in scan mode(need to confirmed by digital designer)

Bit(s)	Name	Description	Default	Type
[7]	*RSVD*	*Reserved (set to default)*	1b	R
[6:0]	i2c_add_reg	Store the I2C address	000 0000b	R/W

Page: 00h
Address: B8h
Register Name: I2C_ALLCALL
Default Value: 55'h
Description: I2C control, skipped in scan mode(need to confirmed by digital designer)

Bit(s)	Name	Description	Default	Type
[7]	*RSVD*	*Reserved (set to default)*	0b	R
[6:0]	i2c_allcall_adr<6:0>	Store the I2C broadcasting address	101 0101b	R/W

Page: 00h
Address: E0h
Register Name: NVM_BURN_COUNT1
Default Value: 00'h
Description: The non-volatile memory (NVM) burn counter result will automatically increase by 1 when programmed

Bit(s)	Name	Description	Default	Type
[7:0]	NVM_BURN_COUNT<7:0>	Store the NVM burns counter result	0000 0000b	R

Page: 00h
Address: E1h
Register Name: NVM_BURN_COUNT2
Default Value: 00'h
Description: The non-volatile memory burn counter result will automatically increase by 1 when programmed. Reserve the E2h through FFh registers for the non-volatile memory burn function. Keep these registers idle.

Bit(s)	Name	Description	Default	Type
[7:0]	NVM_BURN_COUNT<15:8>	Store the NVM burns counter result	0000 0000b	R

Page: 02h
Address: 00h
Register Name: CHIPID
Default Value: 47'h
Description: Chip ID register.

Bit(s)	Name	Description	Default	Type
[7:0]	CHIPID	MABC11040 Chip ID: (TBD)	0100 0111b	R

Page: 02h
Address: 01h
Register Name: REVID
Default Value: 1F'h
Description: Revision ID register.

Bit(s)	Name	Description	Default	Type
[7:0]	REVID	MABC11040 revision (TBD)	0001 1111b	R

Page: 02h
Address: 02h
Register Name: SOFT_RESET
Default Value: 00'h
Description: Software reset register. Not download from NVM, need to program from Host.

Bit(s)	Name	Description	Default	Type
[7:0]	SOFT_RESET	0000 0000b: Normal operation. 1010 1010b: Self Clearing Reset (16 clock cycles at 12MHz) 0101 01010b: Reset everything without an OTP download	0000 0000b	R/W
NOTES: 1. Writing AAh causes a 16 12MHz clock cycles reset (self clearing) 2. Writing 55h reset everything without download OTP (double check with RF design).				

Page: 02h
Address: 09h
Register Name: I2C_ANA
Default Value: 41'h
Description: RSVD

Bit(s)	Name	Description	Default	Type
[7]	I2C_allcall_dis	0: Part will respond to the broadcast address [Note 1] 1: Part will not respond to the broadcasting address.	0b	R/W
[6:0]	I2c_ana<6:0>	The address from the i2c_add_sel	100 0001b	R
NOTES: 1. Broadcast address is found in Page: 00h, Address: B8h				

Page: 02h
Address: 0Fh
Register Name: CHNL0_MSB
Default Value: 00'h
Description: MSB readback of input channel 0

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_I_LSD_ADJUST<11:4>	Reserved		R

Page: 02h
Address: 10h
Register Name: CHNL0_LSB
Default Value: 00'h
Description: LSB readback of input channel 0

Bit(s)	Name	Description	Default	Type
[7:4]	*RSVD*	*Reserved (set to default)*	0000b	R
[3:0]	Access_ctrl<3:0>	Bit<0/1/2/3>.=1 means password0/1/2/3 is right	0000b	R

Page: 02h
Address: 11h
Register Name: CHNL1_MSB
Default Value: 00'h
Description: MSB readback of input channel 1

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD1_OUTP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 12h
Register Name: CHNL1_LSB
Default Value: 00'h
Description: LSB readback of input channel 1

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD1_OUTP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 13h
Register Name: CHNL2_MSB
Default Value: 00'h
Description: MSB readback of input channel 2

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD2_OUTP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 14h
Register Name: CHNL2_LSB
Default Value: 00'h
Description: LSB readback of input channel 2

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD2_OUTP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 15h
Register Name: CHNL3_MSB
Default Value: 00'h
Description: MSB readback of input channel 3

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD3_OUTP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 16h
Register Name: CHNL3_LSB
Default Value: 00'h
Description: LSB readback of input channel 3

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD3_OUTP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 17h
Register Name: CHNL4_MSB
Default Value: 00'h
Description: MSB readback of input channel 4

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD4_OUTP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 18h
Register Name: CHNL4_LSB
Default Value: 00'h
Description: LSB readback of input channel 4

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD4_OUTP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 19h
Register Name: CHNL5_MSB
Default Value: 00'h
Description: MSB readback of input channel 5

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD1_OUTN<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 1Ah
Register Name: CHNL5_LSB
Default Value: 00'h
Description: LSB readback of input channel 5

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD1_OUTN<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 1Bh
Register Name: CHNL6_MSB
Default Value: 00'h
Description: MSB readback of input channel 6

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD2_OUTN<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 1Ch
Register Name: CHNL6_LSB
Default Value: 00'h
Description: LSB readback of input channel 6

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD2_OUTN<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 1Dh
Register Name: CHNL7_MSB
Default Value: 00'h
Description: MSB readback of input channel 7

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD3_OUTN<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 1Eh
Register Name: CHNL7_LSB
Default Value: 00'h
Description: LSB readback of input channel 7

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD3_OUTN<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 1Fh
Register Name: CHNL8_MSB
Default Value: 00'h
Description: MSB readback of input channel 8

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD4_OUTN<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 20h
Register Name: CHNL8_LSB
Default Value: 00'h
Description: LSB readback of input channel 8

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD4_OUTN<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 27h
Register Name: CHNL12_MSB
Default Value: 00'h
Description: MSB readback of input channel 12

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_IIN1<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 28h
Register Name: CHNL12_LSB
Default Value: 00'h
Description: LSB readback of input channel 12

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_IIN1<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 29h
Register Name: CHNL13_MSB
Default Value: 00'h
Description: MSB readback of input channel 13

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_IIN2<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 2Ah
Register Name: CHNL13_LSB
Default Value: 00'h
Description: LSB readback of input channel 13

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_IIN2<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 2Fh
Register Name: CHNL16_MSB
Default Value: 00'h
Description: MSB readback of input channel 16

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD4_TEMP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 30h
Register Name: CHNL16_LSB
Default Value: 00'h
Description: LSB readback of input channel 16

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD4_TEMP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 31h
Register Name: CHNL17_MSB
Default Value: 00'h
Description: MSB readback of input channel 17

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD3_TEMP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 32h
Register Name: CHNL17_LSB
Default Value: 00'h
Description: LSB readback of input channel 17

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD3_TEMP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 33h
Register Name: CHNL18_MSB
Default Value: 00'h
Description: MSB readback of input channel 18

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD2_TEMP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 34h
Register Name: CHNL18_LSB
Default Value: 00'h
Description: LSB readback of input channel 18

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD2_TEMP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 35h
Register Name: CHNL19_MSB
Default Value: 00'h
Description: MSB readback of input channel 19

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD1_TEMP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 36h
Register Name: CHNL19_LSB
Default Value: 00'h
Description: LSB readback of input channel 19

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD1_TEMP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 39h
Register Name: CHNL21_MSB
Default Value: 00'h
Description: MSB readback of input channel 21

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_EXT_VNEG<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 3Ah
Register Name: CHNL21_LSB
Default Value: 00'h
Description: LSB readback of input channel 21

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_EXT_VNEG<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 3Fh
Register Name: TEMP_ALARM
Default Value: 00'h
Description: Latched alarm: Temperature sensor status,

Bit(s)	Name	Description	Default	Type
[7]	iin1_cl_lt	Current input 1: Current limit indicator 1b: Current limit reached or exceeded 0b: Normal operation	0b	R
[6]	iin2_cl_lt	Current input 2: Current limit indicator 1b: Current limit reached or exceeded 0b: Normal operation	0b	R
[5]	TS_VBG_Alarm	Latched temperature alarm for TS_VBG 1b: Voltage bandgap temperature sensor threshold reached or exceeded 0b: Normal operation	0b	R
[4]	TS_PTAT_Alarm	Latched temperature alarm for TS_PTAT 1b: PTAT temperature sensor threshold reached or exceeded 0b: Normal operation	0b	R
[3]	LSD4_TS_Alarm	Latched temperature alarm for LSD4 1b: LSD4 temperature sensor threshold reached or exceeded 0b: Normal operation	0b	R
[2]	LSD3_TS_Alarm	Latched temperature alarm for LSD3 1b: LSD3 temperature sensor threshold reached or exceeded 0b: Normal operation	0b	R
[1]	LSD2_TS_Alarm	Latched temperature alarm for LSD2 1b: LSD2 temperature sensor threshold reached or exceeded 0b: Normal operation	0b	R
[0]	LSD1_TS_Alarm	Latched temperature alarm for LSD1 1b: LSD1 temperature sensor threshold reached or exceeded 0b: Normal operation	0b	R

Page: 02h
Address: 40h
Register Name: ALARM0
Default Value: 00'h
Description: Real-time alarm: Device voltage and current status

Bit(s)	Name	Description	Default	Type
[7]	neg_uv_rt	Negative voltage supply under-voltage alarm 1b: Negative voltage supply is not ready 0b: Normal operation	0b	R
[6]	lsd1_cl_rt	LSD1 output current limit alarm 1b: LSD1 output current limit reached or exceeded 0b: Normal operation	0b	R
[5]	lsd2_cl_rt	LSD2 output current limit alarm 1b: LSD2 output current limit reached or exceeded 0b: Normal operation	0b	R
[4]	lsd3_cl_rt	LSD3 output current limit alarm 1b: LSD3 output current limit reached or exceeded 0b: Normal operation	0b	R
[3]	lsd4_cl_rt	LSD4 output current limit alarm 1b: LSD4 output current limit reached or exceeded 0b: Normal operation	0b	R
[2]	v1p8d_uv_rt	Digital 1.8V under-voltage alarm 1b: 1.8V digital supply is too low 0b: Normal operation	0b	R
[1]	v1p8a_uv_rt	Analog 1.8V under-voltage alarm 1b: 1.8V analog supply is too low 0b: Normal operation	0b	R
[0]	undervoltage_alarm_rt	Analog 5V under-voltage alarm 1b: 5V analog supply is too low 0b: Normal operation	0b	R

Page: 02h
Address: 41h
Register Name: ALARM1
Default Value: 00'h
Description: Latched alarm: Device voltage and current status

Bit(s)	Name	Description	Default	Type
[7]	neg_uv_lt	Negative voltage supply under-voltage alarm 1b: Negative voltage supply is not ready 0b: Normal operation	0b	R
[6]	lsd1_cl_lt	LSD1 output current limit alarm 1b: LSD1 output current limit reached or exceeded 0b: Normal operation	0b	R
[5]	lsd2_cl_lt	LSD2 output current limit alarm 1b: LSD2 output current limit reached or exceeded 0b: Normal operation	0b	R
[4]	lsd3_cl_lt	LSD3 output current limit alarm 1b: LSD3 output current limit reached or exceeded 0b: Normal operation	0b	R
[3]	lsd4_cl_lt	LSD4 output current limit alarm 1b: LSD4 output current limit reached or exceeded 0b: Normal operation	0b	R
[2]	v1p8d_uv_lt	Digital 1.8V under-voltage alarm 1b: 1.8V digital supply is too low 0b: Normal operation	0b	R
[1]	v1p8a_uv_lt	Analog 1.8V under-voltage alarm 1b: 1.8V analog supply is too low 0b: Normal operation	0b	R
[0]	undervoltage_alarm_lt	Analog 5V under-voltage alarm 1b: 5V analog supply is too low 0b: Normal operation	0b	R

Page: 02h
Address: 42h
Register Name: ALARM_LUT_TEMP
Default Value: 00'h
Description: realtime(unlatched) version of ALAMR0

Bit(s)	Name	Description	Default	Type
[7]	lsd4_lut_temp_p	0b: Normal operation 1b: ALU did not finish at the address 255 for LSD_TEMP4	0b	R
[6]	lsd4_lut_temp_n	0b: Normal operation 1b: ALU did not finish at the address 0 for LSD_TEMP4	0b	R
[5]	lsd3_lut_temp_p	0b: Normal operation 1b: ALU did not finish at the address 255 for LSD_TEMP3	0b	R
[4]	lsd3_lut_temp_n	0b: Normal operation 1b: ALU did not finish at the address 0 for LSD_TEMP3	0b	R
[3]	lsd2_lut_temp_p	0b: Normal operation 1b: ALU did not finish at the address 255 for LSD_TEMP2	0b	R
[2]	lsd2_lut_temp_n	0b: Normal operation 1b: ALU did not finish at the address 0 for LSD_TEMP2	0b	R
[1]	lsd1_lut_temp_p	0b: Normal operation 1b: ALU did not finish at the address 255 for LSD_TEMP1	0b	R
[0]	lsd1_lut_temp_n	0b: Normal operation 1b: ALU did not finish at the address 0 for LSD_TEMP1	0b	R

Page: 02h
Address: 43h
Register Name: ALARM_LUT_VOLT
Default Value: 00'h
Description: latched version of ALARM0

Bit(s)	Name	Description	Default	Type
[7]	lsd4_lut_volt_p	0b: Normal operation 1b: ALU didn't finish at the address 63 for LSD4_DEL	0b	R
[6]	lsd4_lut_volt_n	0b: Normal operation 1b: ALU didn't finish at the address 0 for LSD4_DEL	0b	R
[5]	lsd3_lut_volt_p	0b: Normal operation 1b: ALU didn't finish at the address 63 for LSD3_DEL	0b	R
[4]	lsd3_lut_volt_n	0b: Normal operation 1b: ALU didn't finish at the address 0 for LSD3_DEL	0b	R
[3]	lsd2_lut_volt_p	0b: Normal operation 1b: ALU didn't finish at the address 63 for LSD2_DEL	0b	R
[2]	lsd2_lut_volt_n	0b: Normal operation 1b: ALU didn't finish at the address 0 for LSD2_DEL	0b	R
[1]	lsd1_lut_volt_p	0b: Normal operation 1b: ALU didn't finish at the address 63 for LSD1_DEL	0b	R
[0]	lsd1_lut_volt_n	0b: Normal operation 1b: ALU didn't finish at the address 0 for LSD1_DEL	0b	R

Page: 02h
Address: 46h
Register Name: OFFCHIP_TEMP_MSB
Default Value: 00'h
Description: Store the calculated off-chip temperature MSB. The expected temperature range of the temperature sensor is -45° to -125°C (RSVD)

Bit(s)	Name	Description	Default	Type
[7:0]	offchip_temp<11:4>	User defined	0000 0000b	R/W

Page: 02h
Address: 47h
Register Name: OFFCHIP_TEMP_LSB
Default Value: 00'h
Description: Store the calculated off-chip temperature LSB. The expected temperature range of the temperature sensor is -45° to -125°C (RSVD)

Bit(s)	Name	Description	Default	Type
[7:4]	offchip_temp<3:0>	User defined	0000b	R/W
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 48h
Register Name: CAL_TS1_MSB
Default Value: 00'h
Description: Store the calculated temperature MSB for the temperature sensor on LSD1

Bit(s)	Name	Description	Default	Type
[7:0]	CAL_TS1<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 49h
Register Name: CAL_TS1_LSB
Default Value: 00'h
Description: Store the calculated temperature LSB for the temperature sensor on LSD1

Bit(s)	Name	Description	Default	Type
[7:4]	CAL_TS1<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved*	0000b	R

Page: 02h
Address: 4Ah
Register Name: CAL_TS2_MSB
Default Value: 00'h
Description: Store the calculated temperature MSB for the temperature sensor on LSD2

Bit(s)	Name	Description	Default	Type
[7:0]	CAL_TS2<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 4Bh
Register Name: CAL_TS2_LSB
Default Value: 00'h
Description: Store the calculated temperature LSB for the temperature sensor on LSD2

Bit(s)	Name	Description	Default	Type
[7:4]	CAL_TS2<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved*	0000b	R

Page: 02h
Address: 4Ch
Register Name: CAL_TS3_MSB
Default Value: 00'h
Description: Store the calculated temperature MSB for the temperature sensor on LSD3

Bit(s)	Name	Description	Default	Type
[7:0]	CAL_TS3<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 4Dh
Register Name: CAL_TS3_LSB
Default Value: 00'h
Description: Store the calculated temperature LSB for the temperature sensor on LSD3

Bit(s)	Name	Description	Default	Type
[7:4]	CAL_TS3<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved*	0000b	R

Page: 02h
Address: 4Eh
Register Name: CAL_TS4_MSB
Default Value: 00'h
Description: Store the calculated temperature MSB for the temperature sensor on LSD4

Bit(s)	Name	Description	Default	Type
[7:0]	CAL_TS4<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 4Fh
Register Name: CAL_TS4_LSB
Default Value: 00'h
Description: Store the calculated temperature LSB for the temperature sensor on LSD4

Bit(s)	Name	Description	Default	Type
[7:4]	CAL_TS4<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved*	0000b	R

Page: 02h
Address: 50h
Register Name: CAL_INT_BG_MSB
Default Value: 00'h
Description: Store the calculated temperature MSB for internal voltage bandgap (VBG) temperature sensor.

Bit(s)	Name	Description	Default	Type
[7:0]	CAL_INT_TS_VBG<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 51h
Register Name: CAL_INT_BG_LSB
Default Value: 00'h
Description: Store the calculated temperature LSB for internal voltage bandgap (VBG) temperature sensor.

Bit(s)	Name	Description	Default	Type
[7:4]	CAL_INT_TS_VBG<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved*	0000b	R

Page: 02h
Address: 52h
Register Name: CAL_INT_PTAT_MSB
Default Value: 00'h
Description: Store the calculated temperature MSB for the internal PTAT temperature sensor.

Bit(s)	Name	Description	Default	Type
[7:0]	CAL_INT_TS_PTAT<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 53h
Register Name: CAL_INT_PTAT_LSB
Default Value: 00'h
Description: Store the calculated temperature LSB for the internal PTAT temperature sensor.

Bit(s)	Name	Description	Default	Type
[7:4]	CAL_INT_TS_PTAT<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved*	0000b	R

Page: 01h
Address: 62h
Register Name: POWER_MSB
Default Value: 00'h
Description: Pre-programmed non-volatile memory location for power level MSB.

Bit(s)	Name	Description	Default	Type
[7:0]	POWER_MSB	Power level MSB	0000 0000b	R/W

Page: 01h
Address: 6Ch
Register Name: VENDOR_CODE
Default Value: 00'h
Description: Pre-programmed non-volatile memory location for interface identification coding

Bit(s)	Name	Description	Default	Type
[7:0]	VENDOR_CODE	Identical to interface identification coding	0000 0000b	R/W

Page: 01h
Address: 6Dh
Register Name: UNI_MOD_TYP_NO1
Default Value: 00'h
Description: Pre-programmed non-volatile memory location for unique software identification

Bit(s)	Name	Description	Default	Type
[7:0]	UNI_MOD_TYP_NO1	Unique software identification	0000 0000b	R/W

Page: 01h
Address: 6Eh
Register Name: UNI_MOD_TYP_NO2
Default Value: 00'h
Description: Pre-programmed non-volatile memory location for unique software identification

Bit(s)	Name	Description	Default	Type
[7:0]	UNI_MOD_TYP_NO2	Unique software identification	0000 0000b	R/W

Page: 01h
Address: 6Fh
Register Name: POWER_LSB
Default Value: 00'h
Description: Pre-programmed non-volatile memory location for power level LSB (Binary value * 0.1W)

Bit(s)	Name	Description	Default	Type
[7:0]	POWER_LSB	Power level LSB (Binary value * 0.1W)	0000 0000b	R/W

Page: 01h
Address: 70h
Register Name: DL_FREQ_LOW1
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	DL_FREQ_LOW1	Binary in MHz, lower address LSB	0000 0000b	R/W

Page: 01h
Address: 71h
Register Name: DL_FREQ_LOW2
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	DL_FREQ_LOW2	Binary in MHz, upper address MSB	0000 0000b	R/W

Page: 01h
Address: 72h
Register Name: DL_FREQ_HIGH1
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	DL_FREQ_HIGH1	Binary in MHz, lower address LSB	0000 0000b	R/W

Page: 01h
Address: 73h
Register Name: DL_FREQ_HIGH2
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	DL_FREQ_HIGH2	Binary in MHz, upper address MSB	0000 0000b	R/W

Page: 01h
Address: 74h
Register Name: CODE_YEAR
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	CODE_YEAR	Binary year -2000	0000 0000b	R/W

Page: 01h
Address: 75h
Register Name: CODE_WEEK
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	CODE_WEEK	Binary week	0000 0000b	R/W

Page: 01h
Address: 76h
Register Name: MODULE_NAME1
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME1	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 77h
Register Name: MODULE_NAME2
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME2	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 78h
Register Name: MODULE_NAME3
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME3	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 79h
Register Name: MODULE_NAME4
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME4	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 7Ah
Register Name: MODULE_NAME5
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME5	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 7Bh
Register Name: MODULE_NAME6
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME6	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 7Ch
Register Name: MODULE_NAME7
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME7	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 7Dh
Register Name: MODULE_NAME8
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME8	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 7Eh
Register Name: MODULE_NAME9
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME9	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 7Fh
Register Name: MODULE_NAME10
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME10	ASCII module name and / or serial number	0000 0000b	R/W

Page: 80h
Address: 00h to 7Fh
Register Name: LUT_TEMP[0:127]
Default Value: 00'h
Description: LUT from -40C ,per 2.5C

Bit(s)	Address	Name	Description	Default	Type
[7:0]	00h-7Fh	LUT_TEMP[0:127] Bit[7:0]	User Defined Look-Up Table Record	0000 0000b	R/W

Page: 81h
Address: 00h to 7Fh
Register Name: LUT_TEMP[128:255]
Default Value: 00'h
Description: LUT from -40C ,per 2.5C

Bit(s)	Address	Name	Description	Default	Type
[7:0]	00h-7Fh	LUT_TEMP[128:255] Bit[7:0]	User Defined Look-Up Table Record	0000 0000b	R/W

Page: 90h
Address: 00h to 3Fh
Register Name: LSD1_VOLT[0:63]
Default Value: 00'h
Description: LSD Channel 1, Record 0 of look-up-table (LUT) for gate voltage. Intended temperature range from -40°C to +125°C

Bit(s)	Address	Name	Description	Default	Type
[7:0]	00h-3F	LSD1_VOLT[0:63] Bit[7:0]	User Defined Look-Up Table Record	0000 0000b	R/W

Page: 91h
Address: 00h to 3Fh
Register Name: LSD2_VOLT[0:63]
Default Value: 00'h
Description: LUT from -40C ,per 2.5C

Bit(s)	Address	Name	Description	Default	Type
[7:0]	00h-3Fh	LSD2_VOLT[0:63] Bit[7:0]	User Defined Look-Up Table Record	0000 0000b	R/W

Page: 92h
Address: 00h to 3Fh
Register Name: LSD3_VOLT[0:63]
Default Value: 00'h
Description: LUT from -40C ,per 2.5C

Bit(s)	Address	Name	Description	Default	Type
[7:0]	00h-3Fh	LSD3_VOLT[0:63] Bit[7:0]	User Defined Look-Up Table Record	0000 0000b	R/W

Page: 93h
Address: 00h to 3Fh
Register Name: LSD4_VOLT[0:63]
Default Value: 00'h
Description: LUT from -40C ,per 2.5C

Bit(s)	Address	Name	Description	Default	Type
[7:0]	00h-3Fh	LSD4_VOLT[0:63] Bit[7:0]	User Defined Look-Up Table Record	0000 0000b	R/W