MACH231-6/7/10/12/15

High-Performance EE CMOS Programmable Logic

DISTINCTIVE CHARACTERISTICS

- 84 Pins in PLCC
- 128 Macrocells
- 6 ns t_{PD} Commercial; 12 ns t_{PD} Industrial
- 133 MHz f_{CNT}
- 64 I/Os; 4 dedicated inputs/clocks; 2 dedicated inputs
- 128 Flip-flops; 4 clock choices
- 8 "PALCE32V16" blocks with buried macrocells
- SpeedLocking™ for guaranteed fixed timing
- Bus-Friendly™ Inputs and I/Os
- Peripheral Component Interconnect (PCI) compliant (-6/-7/-10/-12)
- Programmable power-down mode
- Pin-compatible with the MACH131 and M4-128N

GENERAL DESCRIPTION

The MACH231 is a member of Vantis' high-performance EE CMOS MACH® 1 & 2 device families. This device has approximately twelve times the logic macrocell capability of the popular PALCE22V10 without loss of speed.

The MACH231 consists of eight PAL® blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH231 has two kinds of macrocell: output and buried. The output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH231 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers for use in synchronizing signals and reducing setup time requirements.

Vantis offers software design support for MACH devices through its own development system and device fitters integrated into third-party CAE tools. Platform support extends across PCs, Sun and HP workstations under advanced operating systems such as Windows 3.1, Windows 95 and NT, SunOS and Solaris, and HPUX.

Publication# **19603** Rev: **C**
Amendment/**0** Issue Date: **August 1997**

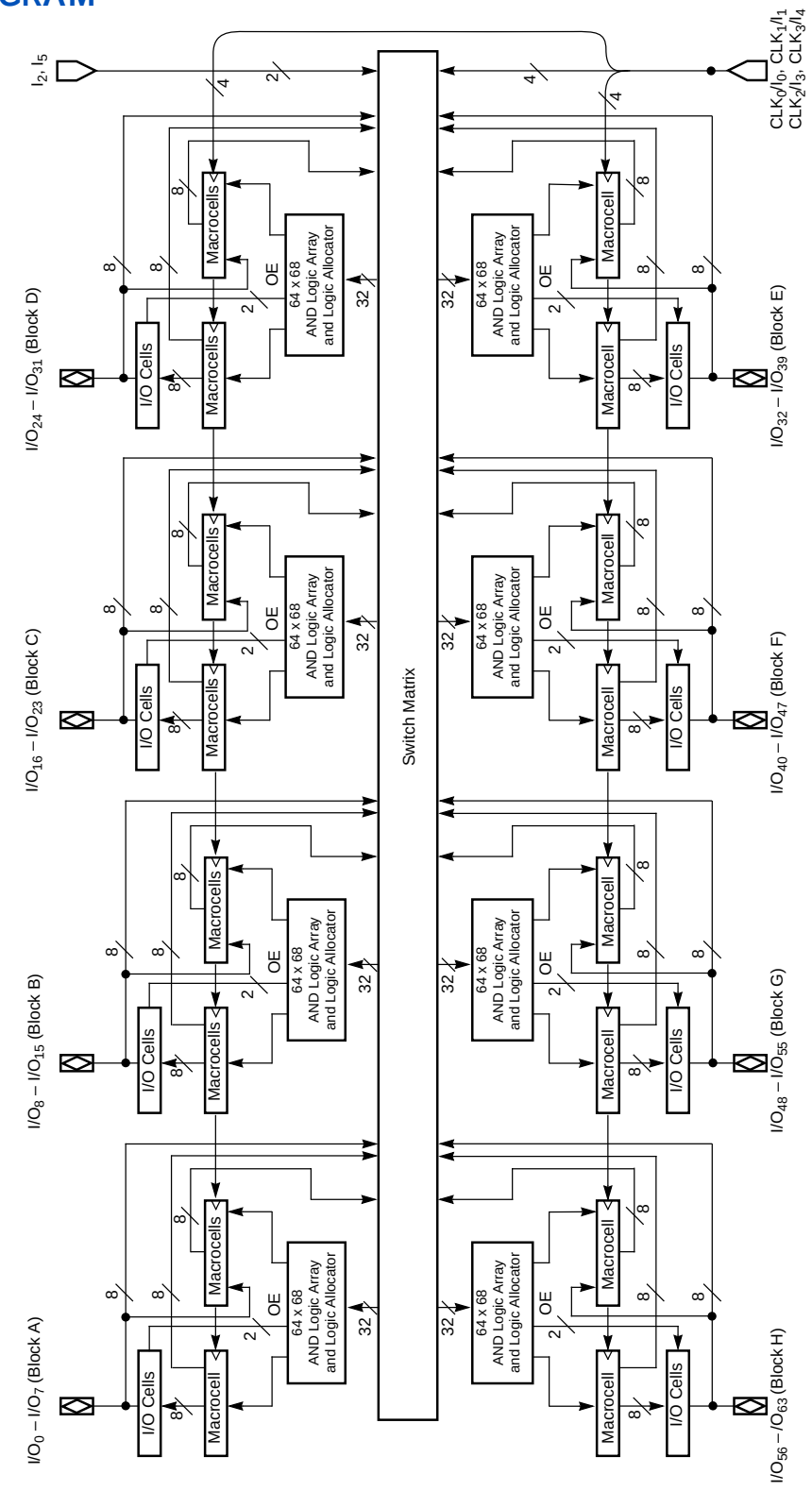
MACHXL® software is a complete development system for the PC, supporting Vantis' MACH devices. It supports design entry with Boolean and behavioral syntax, state machine syntax and truth tables. Functional simulation and static timing analysis are also included in this easy-to-use system. This development system includes high-performance device fitters for all MACH devices.

The same fitter technology included in MACHXL software is seamlessly incorporated into third-party tools from leading CAE vendors such as Synario, Viewlogic, Mentor Graphics, Cadence and MINC. Interface kits and MACHXL configurations are also available to support design entry and verification with other leading vendors such as Synopsys, Exemplar, OrCAD, Synplicity and Model Technology. These MACHXL configurations and interfaces accept EDIF 2.0.0 netlists, generate JEDEC files for MACH devices, and create industry-standard SDF, VITAL-compliant VHDL and Verilog output files for design simulation.

Vantis offers in-system programming support for MACH devices through its MACHPRO® software enabling MACH device programmability through JTAG compliant ports and easy-to-use PC interface. Additionally, MACHPRO generated vectors work seamlessly with HP3070, GenRad and Teradyne testers to program MACH devices or test them for connectivity.

All MACH devices are supported by industry standard programmers available from a number of vendors. These programmer vendors include Advin Systems, BP Microsystems, Data I/O Corporation, Hi-Lo Systems, SMS GmbH, Stag House, and System General.

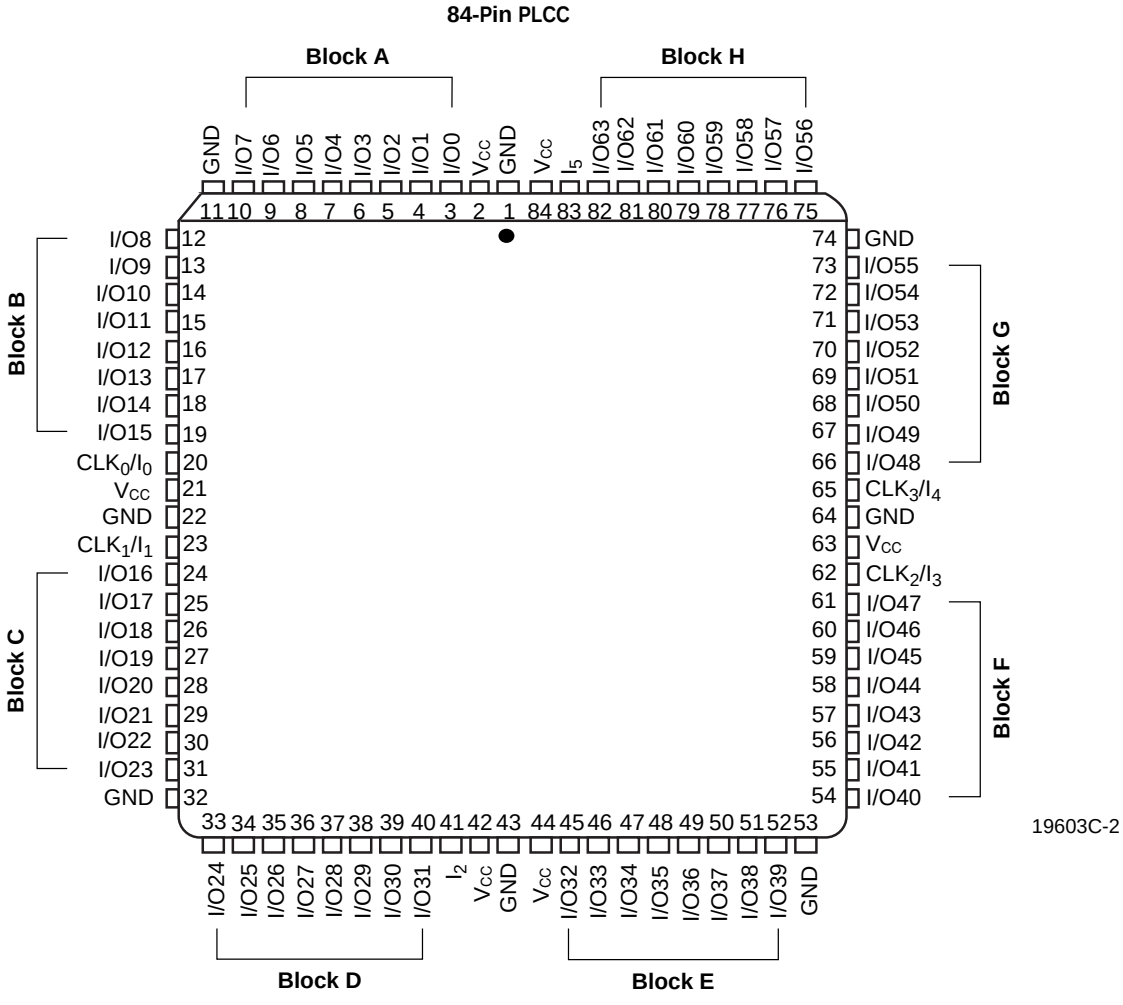
BLOCK DIAGRAM



19603C-1

CONNECTION DIAGRAM

Top View



Note:
Pin-compatible with the MACH131 and M4-128N.

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

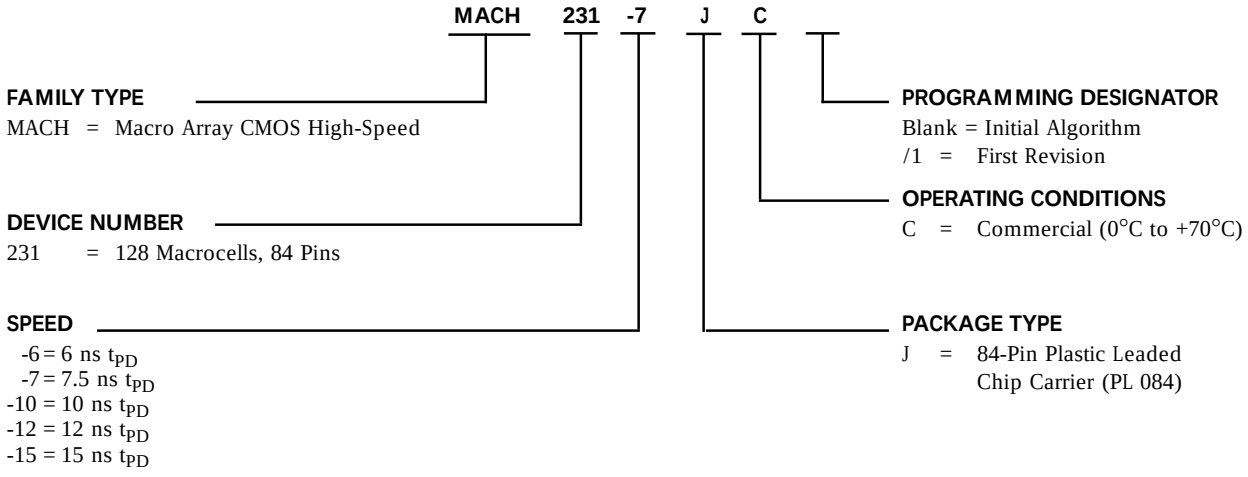
I/O = Input/Output

V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

Vantis programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH231-6	JC
MACH231-7	
MACH231-10	JC/1
MACH231-12	
MACH231-15	

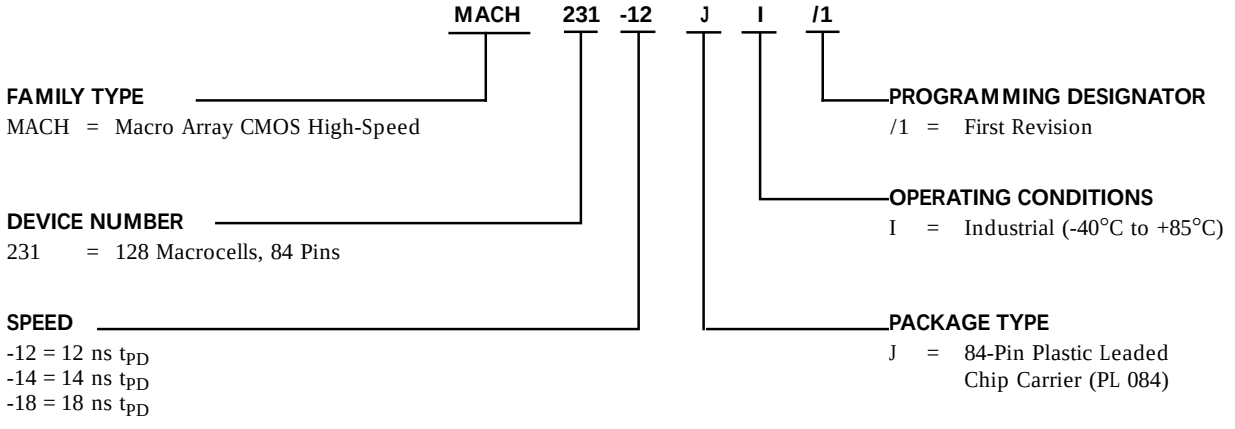
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Industrial Products

Vantis programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH231-12	JI/1
MACH231-14	
MACH231-18	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH231 consists of eight PAL blocks connected by a switch matrix. There are 64 I/O pins and 2 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH231 (Figure 1) contains a 64-product-term logic array, a logic allocator, 8 output macrocells, 8 buried macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 32 inputs. This makes the PAL block look effectively like an independent “PALCE32V16" with 8 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two output enable product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH231 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH231 product-term array consists of 64 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACH231 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Macrocell			Macrocell		
Output	Buried	Available Clusters	Output	Buried	Available Clusters
M_0		C_0, C_1, C_2	M_8		C_7, C_8, C_9, C_{10}
	M_1	C_0, C_1, C_2, C_3		M_9	C_8, C_9, C_{10}, C_{11}
M_2		C_1, C_2, C_3, C_4	M_{10}		$C_9, C_{10}, C_{11}, C_{12}$
	M_3	C_2, C_3, C_4, C_5		M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_4		C_3, C_4, C_5, C_6	M_{12}		$C_{11}, C_{12}, C_{13}, C_{14}$
	M_5	C_4, C_5, C_6, C_7		M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_6		C_5, C_6, C_7, C_8	M_{14}		C_{13}, C_{14}, C_{15}
	M_7	C_6, C_7, C_8, C_9		M_{15}	C_{14}, C_{15}

The Macrocell

The MACH231 has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACH231 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

SpeedLocking for Guaranteed Fixed Timing

The unique MACH 1 & 2 architecture is designed for high performance—a metric that is met in both raw speed, but even more importantly, *guaranteed fixed speed*. Using the design of the central switch matrix, the MACH 231 product offers the SpeedLocking feature, which allows a stable fixed pin-to-pin delay, independent of logic paths, routing resources and design refits for up to 16 product terms per output. Other non-Vantis CPLDs incur serious timing delays as product terms expand beyond their typical 4 or 5 product term limits. Speed *and* SpeedLocking combine for continuous, high performance required in today's demanding designs.

Bus-Friendly Inputs and I/Os

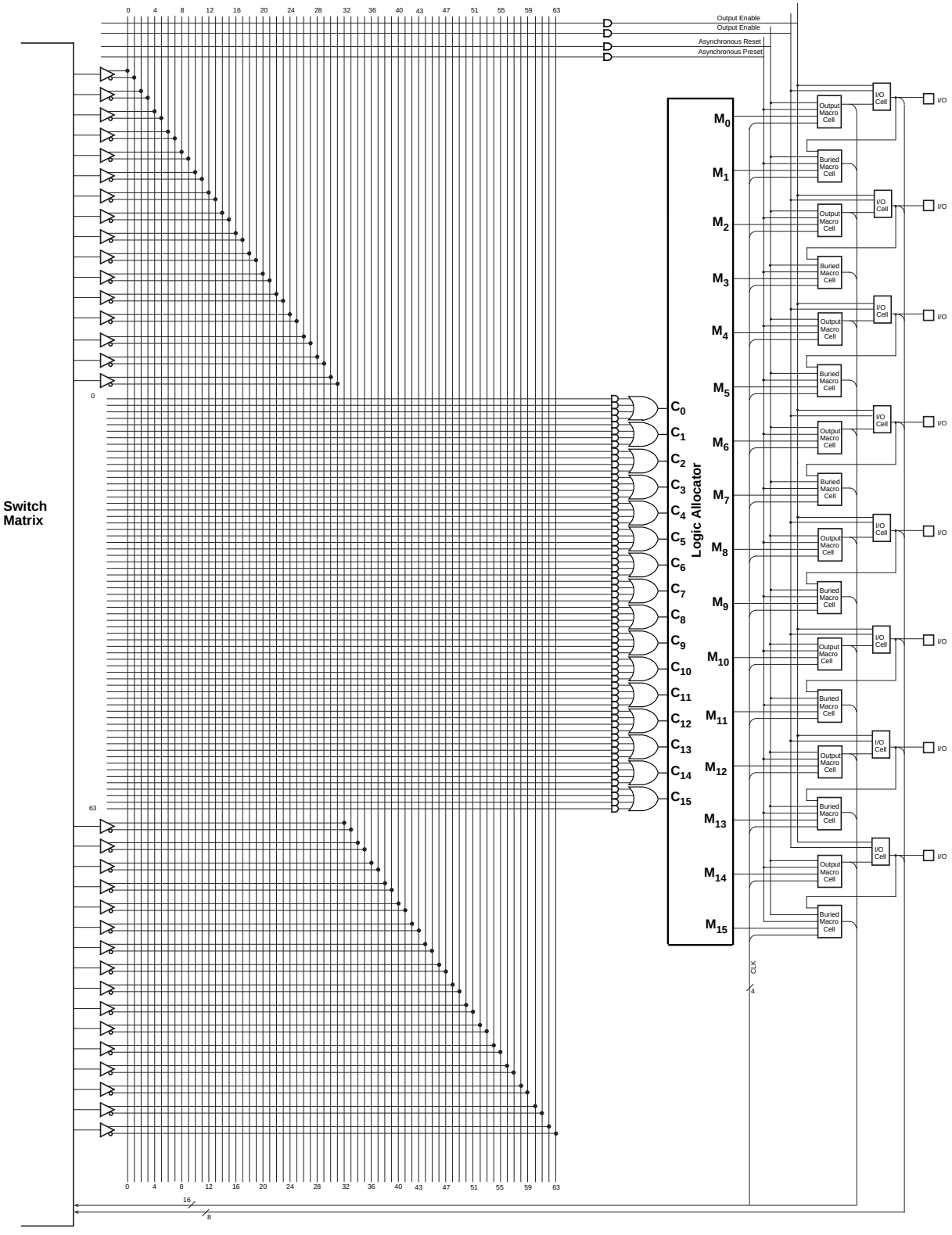
The MACH231 inputs and I/Os include two inverters in series which loop back to the input. This double inversion reinforces the state of the input and pulls the voltage away from the threshold voltage. Unlike a pull-up, this configuration cannot cause contention on a bus. For an illustration of this configuration, please turn to the I/O and Equivalent Schematics section at the end of this data book.

PCI Compliance

The MACH231-6/7/10/12 is fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The MACH231's predictable timing ensures compliance with the PCI AC specifications independent of the design.

Power-Down Mode

The MACH231 features a programmable low-power mode in which individual signal paths can be programmed as low power. These low-power speed paths will be slightly slower than the non-low-power paths. This feature allows speed critical paths to run at maximum frequency while the rest of the paths operate in low power mode resulting in power savings of up to 50%. If all signals in a PAL block are low-power, then total power is reduced further.



19603C-3

Figure 1. MACH231 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +125°C

Device Junction Temperature . . . . . +150°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current
(T_A = 0°C to 70°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –3.2 mA, V_{CC}= Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN}= 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL}(Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL}(Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Static)	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = 5 V, f = 0 MHz, T_A = 25°C (Note 4)		135		mA
	Supply Current (Active)	V_{CC} = 5 V, f = 25 MHz, T_A = 25°C (Note 4)		150		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = V_{CC} - 0.5$ V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-6		-7		-10		-12		-15		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output					6		7.5		10		12		15	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	5		5.5		6.5		7		10		ns
				T-type	6		6.5		7.5		8		11		ns
t_H	Register Data Hold Time				0		0		0		0		0		ns
t_{CO}	Clock to Output					4		5		6.5		8		10	ns
t_{WL}	Clock Width			LOW	2.5		3		4		6		6		ns
t_{WH}				HIGH	2.5		3		4		6		6		ns
f_{MAX}	Maximum Frequency	External Feedback	$1/(t_S + t_{CO})$	D-type	111		95		77		66.7		50		MHz
				T-type	100		87		72		62.5		47.6		MHz
		Internal Feedback (f_{CNT})		D-type	166		133		100		76.9		66.6		MHz
				T-type	150		125		91		71.4		62.5		MHz
		No Feedback			200		166.7		125		83.3		83.3		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				5		5.5		6.5		7		10		ns
t_{HL}	Latch Data Hold Time				0		0		0		0		0		ns
t_{GO}	Gate to Output					5		6		7.5		8.5		11	ns
t_{GWL}	Gate Width LOW				2		3		4		6		6		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					9		9.5		14		14.5		17	ns
t_{SIR}	Input Register Setup Time				1.5		2		2		2		2		ns
t_{HIR}	Input Register Hold Time				1.5		2		2.5		2.5		2.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					10		11		15.5		16		18	ns
t_{ICS}	Input Register Clock to output Register Setup			D-type	8		9		11		12		15		ns
				T-type	9		10		12		13		16		ns
t_{WICL}	Input Register Clock Width			LOW	2.5		3		4		6		6		ns
t_{WICH}				HIGH	2.5		3		4		6		6		ns
f_{MAXIR}	Maximum Input Register Frequency				200		166.7		125		83.3		83.3		MHz
t_{SIL}	Input Latch Setup Time				1.5		2		2		2.5		2.5		ns
t_{HIL}	Input Latch Hold Time				1.5		2		2.5		3		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					11		12		17		17		20	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					13		14		18		19.5		22	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	-6		-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate	7		7.5		10		10.5		12		ns
t_{IGS}	Input Latch Gate to Output Latch Setup	9		10		11		13.5		16		ns
t_{WIGL}	Input Latch Gate Width LOW	2		3		4		6		6		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		11		12.5		16		17		19	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		9		9.5		13		16		20	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	4		5		10		12		15		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	4		5		7.5		8		10		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		9		9.5		13		16		20	ns
t_{APW}	Asynchronous Preset Width (Note 1)	4		5		10		12		15		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	4		5		7.5		8		10		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		9		9.5		10		12		15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		9		9.5		10		12		15	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)		9		10		10		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		6		7		7		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		2		3		3		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		9		10		10		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit for test conditions.*
3. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +125°C

Device Junction Temperature . . . . . +150°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current
(T_A = -40°C to +85°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Notes 3, 5)	–30		–160	mA
I_{CC}	Supply Current (Static)	V_{CC} = 5 V, T_A = 25°C, f = 0 MHz (Note 4)		135		mA
	Supply Current (Active)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 4)		150		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled and reset.*
5. *This parameter is not 100% tested, but evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, TA = 25°C f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-12		-14		-18		Unit
					Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					12		14		18	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	8		8.5		12		ns
				T-type	9		10		13.5		ns
t_H	Register Data Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					8		10		12	ns
t_{WL}	Clock Width			LOW	6		7.5		7.5		ns
t_{WH}				HIGH	6		7.5		7.5		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	62.5		54		41		MHz
				T-type	58.8		50		39		MHz
		Internal Feedback (f_{CNT})		D-type	83.3		61.5		53		MHz
				T-type	76.9		57		44		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		66.5		66.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				8		8.5		12		ns
t_{HL}	Latch Data Hold Time				0		0		0		ns
t_{GO}	Gate to Output (Note 3)					10		12		13.5	ns
t_{GWL}	Gate Width LOW				6		7.5		7.5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					14		17		20.5	ns
t_{SIR}	Input Register Setup Time				2.5		2.5		2.5		ns
t_{HIR}	Input Register Hold Time				3		3		3.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					17		18		22	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	12		14.5		18		ns
				T-type	13		16		19.5		ns
t_{WICL}	Input Register Clock Width			LOW	6		7.5		7.5		ns
t_{WICH}				HIGH	6		7.5		7.5		ns
f_{MAXIR}	Maximum Input Register Frequency		$1/(t_{WICL} + t_{WICH})$		83.3		66.5		66.5		MHz
t_{SIL}	Input Latch Setup Time				2.5		2.5		2.5		ns
t_{HIL}	Input Latch Hold Time				3		3		3.5		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

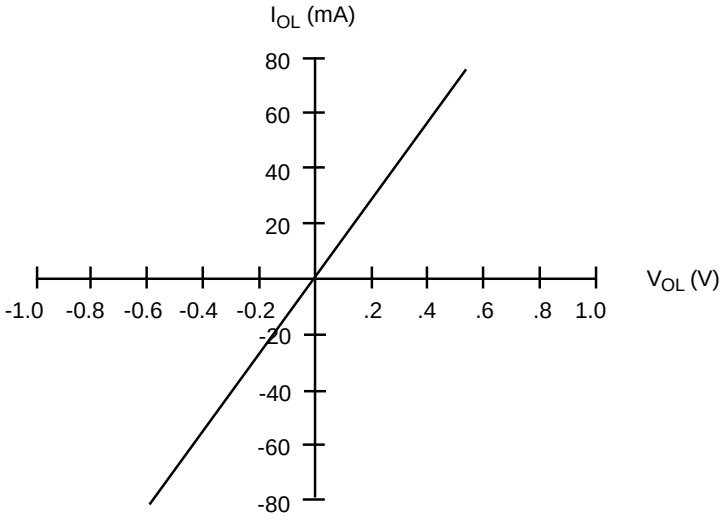
Parameter Symbol	Parameter Description	-12		-14		-18		Unit
		Min	Max	Min	Max	Min	Max	
t_{IGO}	Input Latch Gate to Combinatorial Output		19		20.5		24	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch		21		23		26.5	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate	10.5		11		14.5		ns
t_{IGS}	Input Latch Gate to Output Latch Setup	13.5		16		19.5		ns
t_{WIGL}	Input Latch Gate Width LOW	6		7.5		7.5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		17		19.5		23	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		19.5		19.5		24	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	12		14.5		18		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	10		10		12		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		19.5		19.5		24	ns
t_{APW}	Asynchronous Preset Width (Note 1)	12		14.5		18		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	10		10		12		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 1)		12		15		18	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 1)		12		15		18	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)		10		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		7		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		3		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		10		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *If a signal is powered down, this parameter must be added to its respective high-speed parameter.*

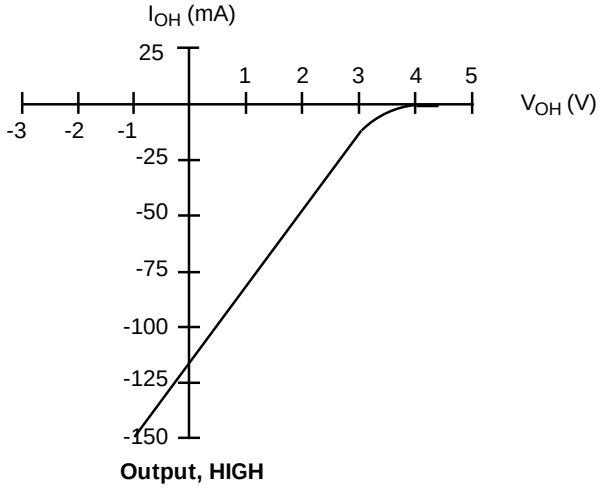
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



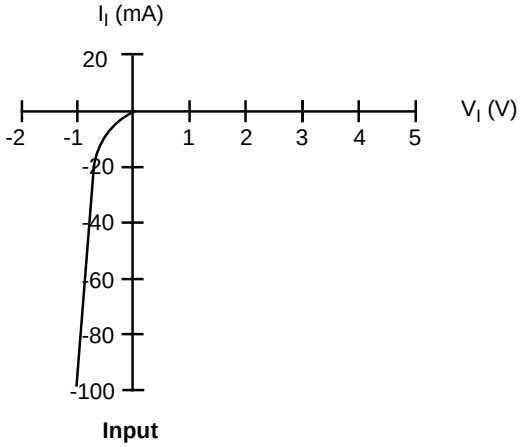
Output, LOW

19603C-4



Output, HIGH

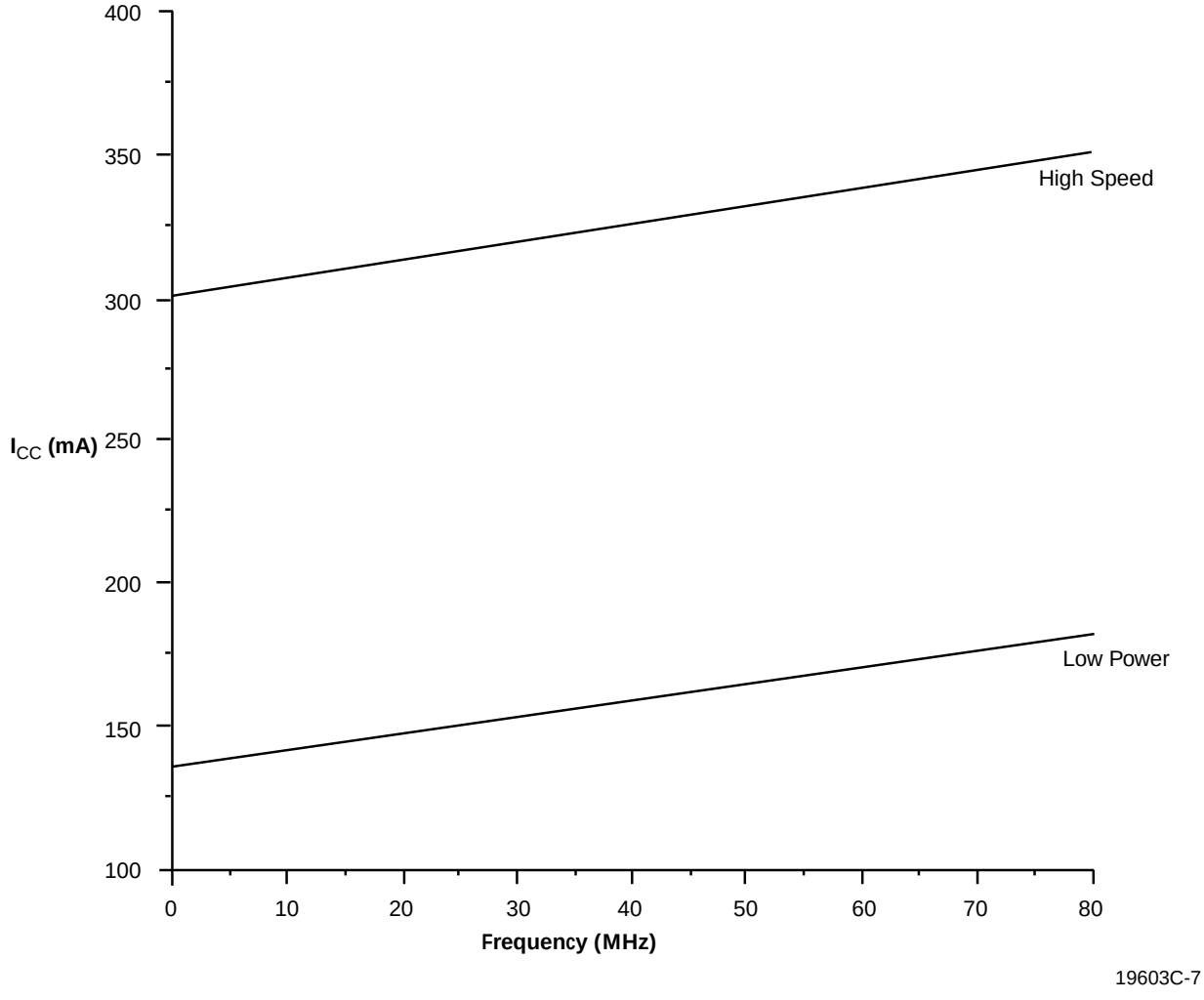
19603C-5



Input

19603C-6

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

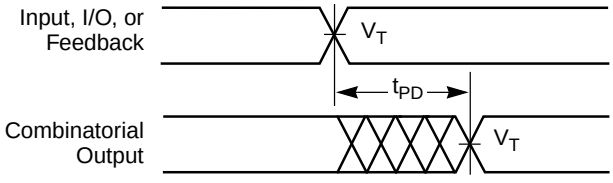
Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Units
θ_{jc}	Thermal impedance, junction to case		5	°C/W
θ_{ja}	Thermal impedance, junction to ambient		20	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	17	°C/W
		400 lfpm air	14	°C/W
		600 lfpm air	12	°C/W
		800 lfpm air	10	°C/W

Plastic θjc Considerations

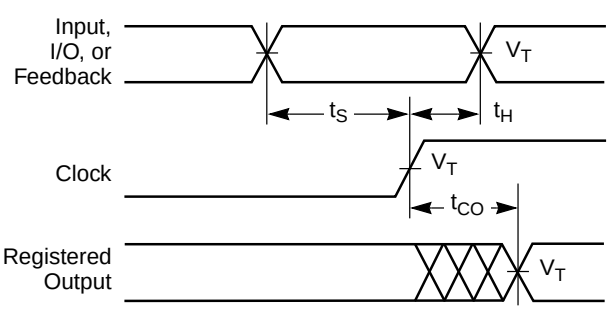
The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

SWITCHING WAVEFORMS



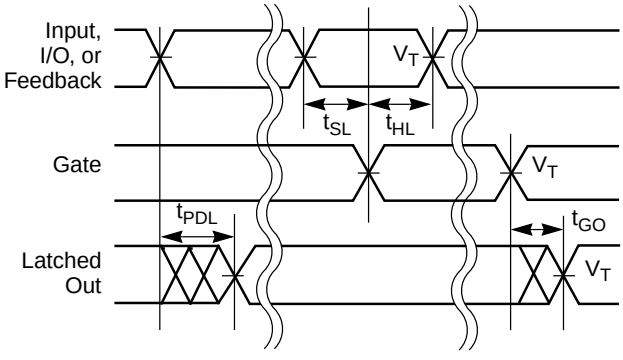
19603C-8

Combinatorial Output



19603C-9

Registered Output



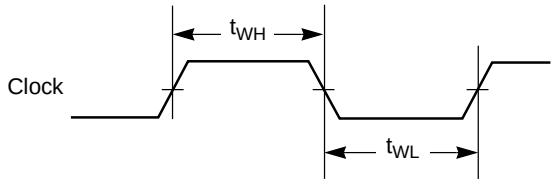
19603C-10

Latched Output

Notes:

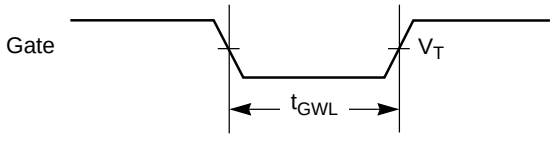
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



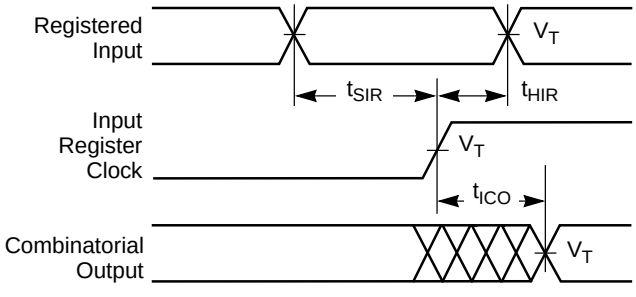
19603C-11

Clock Width



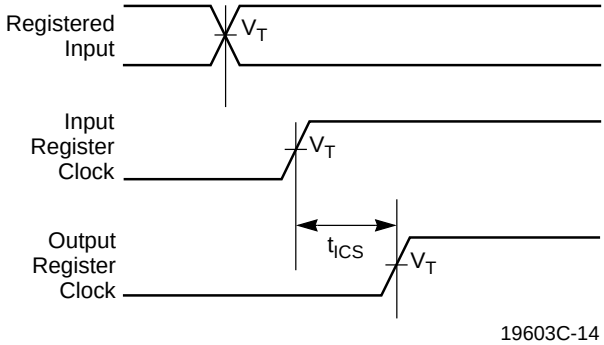
19603C-12

Gate Width



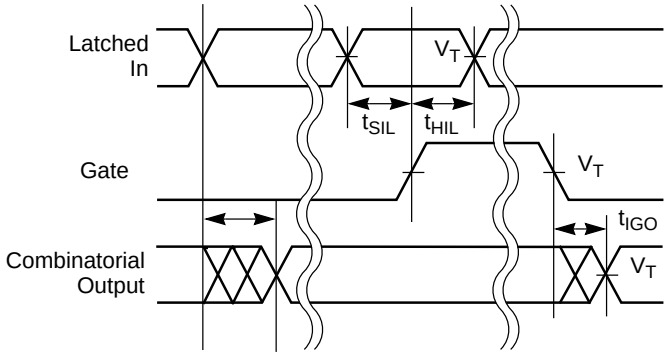
19603C-13

Registered Input



19603C-14

Input Register to Output Register Setup



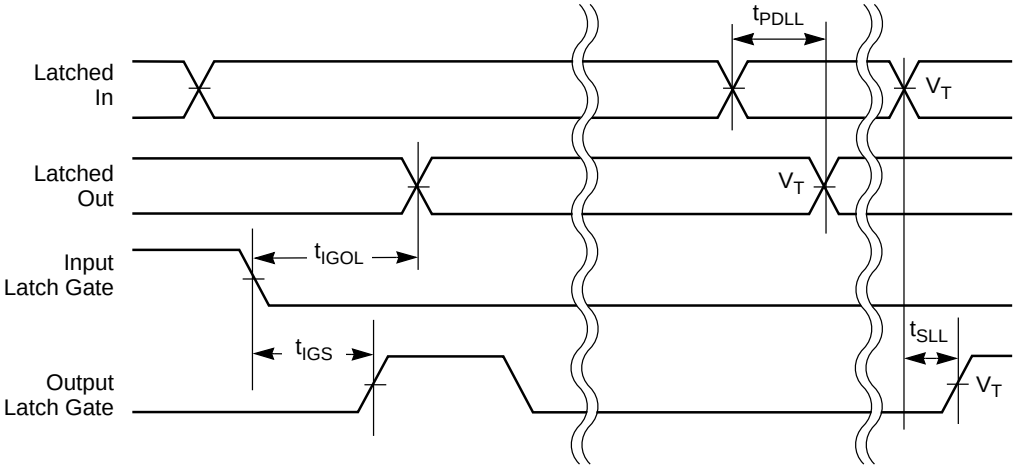
19603C-15

Latched Input

Notes:

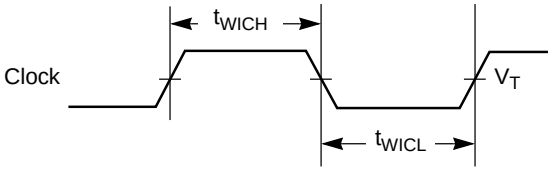
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



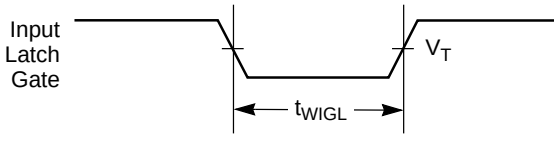
19603C-16

Latched Input and Output



19603C-17

Input Register Clock Width



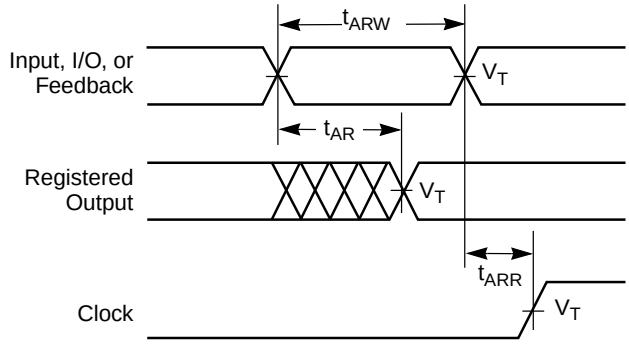
19603C-18

Input Latch Gate Width

Notes:

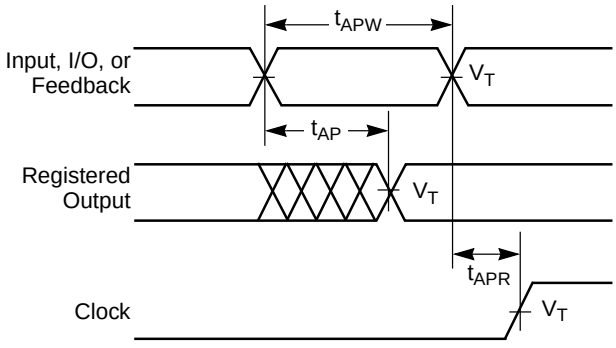
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



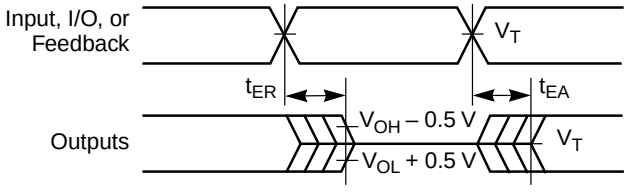
19603C-19

Asynchronous Reset



19603C-20

Asynchronous Preset



19603C-21

Output Disable/Enable

Notes:

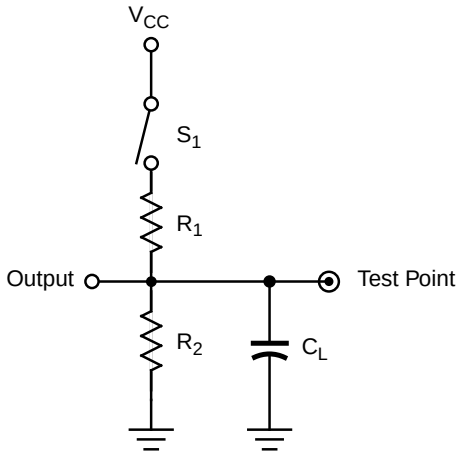
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



19603C-22

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	35 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

**Switching several outputs simultaneously should be avoided for accurate measurement.*

f_{MAX} PARAMETERS

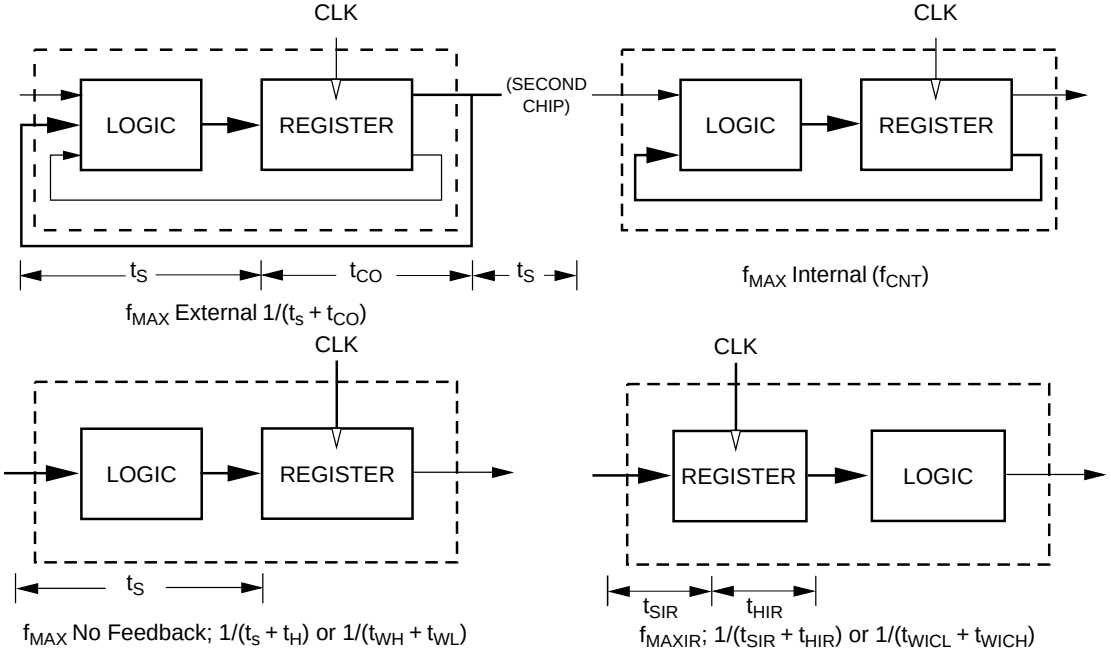
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design; therefore, this parameter is sometimes called "$f_{CNT.}$"

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."

For devices with input registers, one additional f_{MAX} parameter is specified: f_{MAXIR}. Because this involves no feedback, it is calculated the same way as f_{MAX} no feedback. The minimum period will be limited either by the sum of the setup and hold times ($t_{SIR} + t_{HIR}$) or the sum of the clock widths ($t_{WICL} + t_{WICH}$). The clock widths are normally the limiting parameters, so that f_{MAXIR} is specified as $1/(t_{WICL} + t_{WICH})$. Note that if both input and output registers are used in the same path, the overall frequency will be limited by t_{ICS}. All frequencies except f_{MAX} internal are calculated from other measured AC parameters. f_{MAX} internal is measured directly.



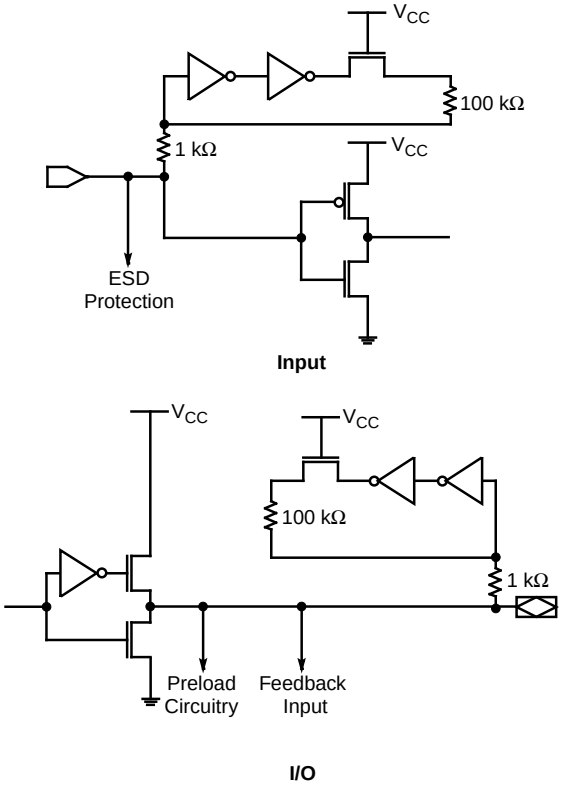
ENDURANCE CHARACTERISTICS

The MACH families are manufactured using Vantis' advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

Endurance Characteristics

Parameter Symbol	Parameter Description		Units	Test Conditions
t_{DR}	Min Pattern Data Retention Time	10	Years	Max Storage Temperature
		20	Years	Max Operating Temperature
N	Max Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



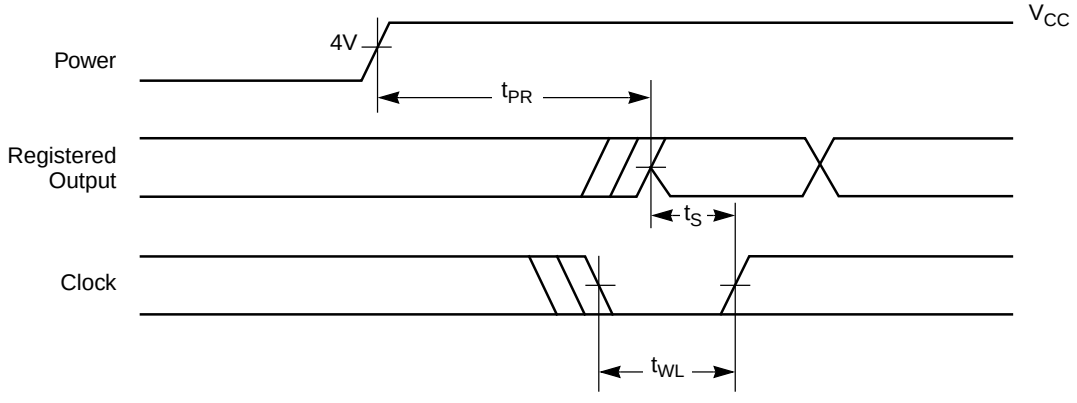
19603C-23

POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-Up Reset Time	10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



19603C-24

Power-Up Reset Waveform

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the local Vantis sales office.

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Vantis Corporation P.O. Box 3755 920 DeGuigne Drive Sunnyvale, CA 94088 (408) 732-0555 or 1(888) 826-8472 (VANTIS2) http://www.vantis.com	MACHXL Software Vantis-ABEL Software Vantis-Synario Software
Aldec, Inc. 3 Sunset Way, Suite F Henderson, NV 89014 (702) 456-1222 or (800) 487-8743	ACTIVE-CAD
Cadence Design Systems 555 River Oaks Pkwy San Jose, CA 95134 (408) 943-1234 or (800) 746-6223	PIC Designer Concept/Composer Synergy Leapfrog/Verilog-XL
Exemplar Logic, Inc. 815 Atlantic Avenue, Suite 105 Alameda, CA 94501 (510) 337-3700	Leonardo™ Galileo™
Logic Modeling 19500 NW Gibbs Dr. P.O. Box 310 Beaverton, OR 97075 (800) 346-6335	SmartModel® Library
Mentor Graphics Corp. 8005 S.W. Boeckman Rd. Wilsonville, OR 97070-7777 (800) 547-3000 or (503) 685-7000	Design Architect, PLDSynthesis™ II Autologic II Synthesizer, QuickSim Simulator, QuickHDL Simulator
MicroSim Corp. 20 Fairbanks Irvine, CA 92718 (714) 770-3022	MicroSim Design Lab PLogic, PLSyn
MINC Inc. 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (800) 755-FPGA or (719) 590-1155	PLDesigner-XL™ Software
Model Technology 8905 S.W. Nimbus Avenue, Suite 150 Beaverton, OR 97008 (503) 641-1340	V-System/VHDL
OrCAD, Inc. 9300 S.W. Nimbus Avenue Beaverton, OR 97008 (503) 671-9500 or (800) 671-9505	OrCAD Express
Synario® Design Automation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL™ Synario™ Software

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Synopsys 700 E. Middlefield Rd. Mountain View, CA 94040 (415) 962-5000 or (800) 388-9125	FPGA or Design Compiler (Requires MINC PLDesigner-XL™) VSS Simulator
Synplicity, Inc. 624 East Evelyn Ave. Sunnyvale, CA 94086 (408) 617-6000	Synplify
Teradyne EDA 321 Harrison Ave. Boston, MA 02118 (800) 777-2432 or (617) 422-2793	MultiSIM Interactive Simulator LASAR
VeriBest, Inc. 6101 Lookout Road, Suite A Boulder, CO 80301 (800) 837-4237	VeriBest PLD
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 873-8439 or (508) 480-0881	Viewdraw, ViewPLD, Viewsynthesis Speedwave Simulator, ViewSim Simulator, VCS Simulator
MANUFACTURER	**TEST GENERATION SYSTEM**
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 881-8821	ATGEN™ Test Generation Software
iNt GmbH Busenstrasse 6 D-8033 Martinsried, Munich, Germany (87) 857-6667	PLDCheck 90

Vantis is not responsible for any information relating to the products of third parties. The inclusion of such information is not a representation nor an endorsement by Vantis of these products.

APPROVED PROGRAMMERS (subject to change)

For more information on the products listed below, please consult the local Vantis sales office.

MANUFACTURER	PROGRAMMER CONFIGURATION
Advin Systems, Inc. 1050-L East Duane Ave. Sunnyvale, CA 940 86 (408) 243-7000 or (800) 627-2456 BBS (408) 737-9200 Fax (408) 736-2503	Pilot-U40 Pilot-U84 MVP
BP Microsystems 1000 N. Post Oak Rd., Suite 225 Houston, TX 77055-7237 (800) 225-2102 or (713) 688-4600 BBS (713) 688-9283 Fax (713) 688-0920	BP1200 BP1400 BP2100 BP2200
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 426-1045 or (206) 881-6444 BBS (206) 882-3211 Fax (206) 882-1043	UniSite™ Model 2900 Model 3900 AutoSite
Hi-Lo Systems 4F, No. 2, Sec. 5, Ming Shoh E. Road Taipei, Taiwan (886) 2-764-0215 Fax (886) 2-756-6403 or Tribal Microsystems / Hi-Lo Systems 44388 South Grimmer Blvd. Fremont, CA 94538 (510) 623-8859 BBS (510) 623-0430 Fax (510) 623-9925	ALL-07 FLEX-700
SMS GmbH Im Grund 15 88239 Wangen Germany (49) 7522-97280 Fax (49) 7522-972850 or SMS USA 544 Weddell Dr. Suite 12 Sunnyvale, CA 94089 (408) 542-0388	Sprint Expert Sprint Optima Multisite
Stag House Silver Court Watchmead, Welwyn Garden City Herfordshire UK AL7 1LT 44-1-707-332148 Fax 44-1-707-371503	Stag Quazar

MANUFACTURER	PROGRAMMER CONFIGURATION
System General 1603A South Main Street Milpitas, CA 95035 (408) 263-6667 BBS (408) 262-6438 Fax (408) 262-9220 or 3F, No. 1, Alley 8, Lane 45 Bao Shing Road, Shin Diau Taipei, Taiwan (886) 2-917-3005 Fax (886) 2-911-1283	Turpro-1 Turpro-1/FX Turpro-1/TX

APPROVED ADAPTER MANUFACTURERS

MANUFACTURER	PROGRAMMER CONFIGURATION
California Integration Coordinators, Inc. 656 Main Street Placerville, CA 95667 (916) 626-6168 Fax (916) 626-7740	MACH/PAL Programming Adapters
Emulation Technology, Inc. 2344 Walsh Ave., Bldg. F Santa Clara, CA 95051 (408) 982-0660 Fax (408) 982-0664	Adapt-A-Socket® Programming Adapters

APPROVED ON-BOARD ISP PROGRAMMING TOOLS

MANUFACTURER	PROGRAMMER CONFIGURATION
Corelis, Inc. 12607 Hidden Creek Way, Suite H Cerritos, California 70703 (310) 926-6727	JTAGPROG™
Vantis Corporation P.O. Box 3755 920 DeGuigne Drive Sunnyvale, CA 94088 (408) 732-0555 or 1(888) 826-8472 (VANTIS2) http://www.vantis.com	MACHPRO®

PHYSICAL DIMENSIONS

PL 084

84-Pin Plastic Leaded Chip Carrier (measured in inches)