tyco Electronics

MACOM

# PCS LNA/Downconverter 1800-2000 MHz

MADCSM0012 V2

## Features

- Highly Integrated LNA and Downconverter
- 3mm 16-Lead PQFN
- Operates over 2.7 V to 5 V Supply Voltage
- Low Noise Figure: 2.3 dB Typical
- High Input Intercept Point: -9 dBm Typical
- Continuous Current Control Downconverter
- Low LO Drive Level: -10 dBm

## Description

M/A-COM's MADCSM0012 integrated downconverter combines a low noise amplifier, a RF amplifier, a downconverting mixer, an IF amplifier, and LO buffer amplifier. The MADCSM0012 is packaged in a low cost 3mm 16-Lead PQFN with an exposed pad for improved high frequency grounding.

M/A-COM designed the MADCSM0012 for handsets requiring wide dynamic range and low power consumption. By application of a suitable control voltage to pin 6, the linearity of the device can be controlled in real time to keep the current as low as possible

The MADCSM0012 is fabricated using M/A-COM's 0.5-micron low noise E/D GaAs MESFET process. The process features full passivation for increased performance and reliability.

## Ordering Information[1]

| Part Number | Package |
|---|---|
| MADCSM0012 | Bulk Packaging |
| MADCSM0012TR | Tape and Reel (1K Reel) |
| MADCSM0012SMB | Sample Test Board |

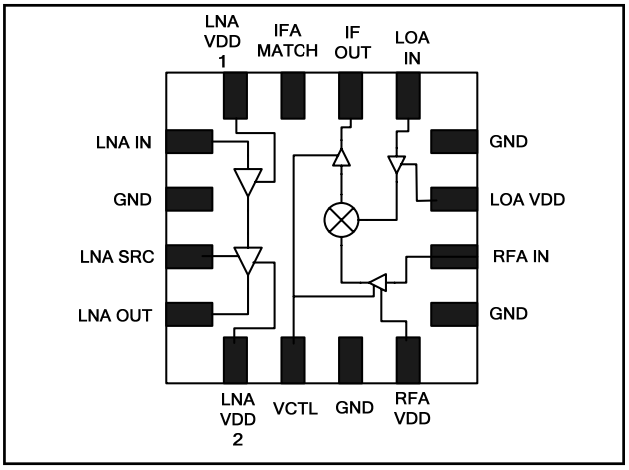
1. Reference Application Note M513 for reel size information.

## Absolute Maximum Ratings [2,3]

| Parameter | Absolute Maximum |
|---|---|
| Voltage | 6 V |
| Input Power | 0 dBm |
| Operating Temperature | -30°C to +85°C |
| Storage Temperature | -65°C to +150°C |

2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. M/A-COM does not recommend sustained operation near these survivability limits.

## Functional Block Diagram




## Pin Configuration

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | LNA IN | Input to LNA; RF matching required |
| 2 | GND | DC and RF Ground |
| 3 | LNA SRC | Source of LNA output stage FET. RF bypassing required. Off-chip resistor may be used to increase IIP3 |
| 4 | LNA OUT | 50 Ohm LNA output; DC Blocked |
| 5 | LNA $V_{DD2}$ | LNA second stage supply voltage; RF bypassing required |
| 6 | $V_{CTL}$ | Downconverter bias control. 0 to 3.0 V allowed |
| 7 | GND | DC and RF Ground |
| 8 | RFA $V_{DD}$ | RFA supply voltage; RF bypassing required |
| 9 | GND | DC and RF Ground |
| 10 | RFA IN | 50 Ohm RFA Input; DC Blocked |
| 11 | LOA $V_{DD}$ | LOA supply voltage; RF bypassing required |
| 12 | GND | DC and RF Ground |
| 13 | LOA IN | Local oscillator input (-10 to –5 dBm) |
| 14 | IF OUT | IF Output of downconverter; IF matching required |
| 15 | IFA MATCH | IF matching between mixer and IFA; required an inductor to ground |
| 16 | LNA $V_{DD1}$ | LNA first stage supply voltage; RF bypassing required |



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Visit www.macom.com for additional data sheets and product information.

## Electrical Specifications - Korean Band PCS: Test Conditions: $V_{DD}$ = 3.0 V, RF = 1855 MHz, IF = 210 MHz, LO = 1645 MHz, LO = -10 dBm, $T_A$ = 25°C

### Low Noise Amplifier

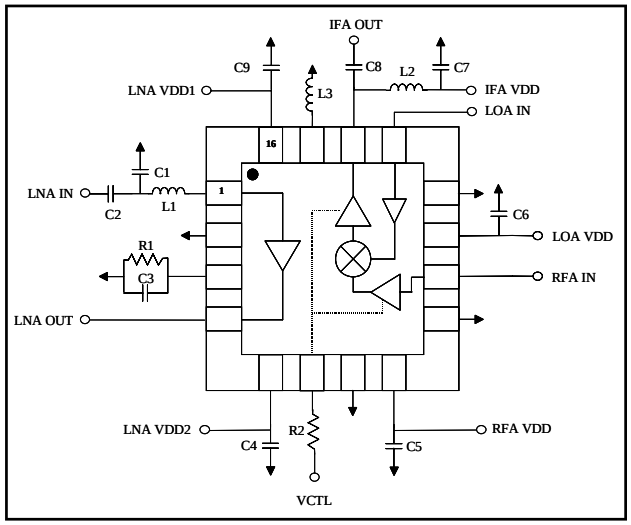
| Parameter | Test Conditions | Units | Min | Typ | Max |
|---|---|---|---|---|---|
| Gain | — | dB | — | 15 | — |
| Noise Figure | — | dB | — | 1.35 | — |
| VSWR In/Out | — | Ratio | — | 2:1 | — |
| Input IP3 | — | dBm | — | 6 | — |
| Idd | — | mA | — | 15 | — |

### Cascaded LNA/Downconverter [4]

| Parameter | Test Conditions | Units | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| Conversion Gain | $V_{CTL}$ = 3.0 V<br>$V_{CTL}$ = 1.0 V | dB<br>dB | 22.5<br>— | 25<br>21 | 27.5<br>— |
| Noise Figure | $V_{CTL}$ = 3.0 V | dB | — | 2.3 | 3.2 |
| Input IP3 | RF Input = -30 dBm, $V_{CTL}$ = 3.0V | dBm | -11 | -9 | — |
| Isolation | LO to RF, $V_{CTL}$ = 3.0 V<br>LO to IF, $V_{CTL}$ = 3.0 V<br>RF to IF, $V_{CTL}$ = 3.0 V | dB<br>dB<br>dB | —<br>—<br>— | 50<br>31<br>18 | —<br>—<br>— |
| $I_{DD}$ | $V_{CTL}$ = 3.0 V | mA | — | 25 | 37 |

4. Complete cascaded measurements taken with 3 dB pad between LNA output and Downconverter input (RFA IN).

### Sample Board Schematic




### External Circuitry Parts List (Korean Band PCS)

| Part | Value | Case Size | Purpose |
|---|---|---|---|
| C1 | 10 pF | 0402 | LNA Input Matching |
| C2 | 1.2 pF | 0402 | LNA Input Matching |
| C3 | 0.1 µF | 0402 | LNA Source Bypass |
| C4, C5, C6, C9 | 0.1 µF | 0402 | RF Bypass |
| C7 | 0.1 µF | 0402 | IF Bypass |
| C8 | 6.8 pF | 0402 | IF Matching |
| L1 | 6.2 nH | 0603 | LNA Matching |
| L2 | 47 nH | 0603 | IF Output Matching |
| L3 | 120 nH | 0603 | IF Mixer Matching |
| R1 | — | 0603 | Optional Resistor to increase LNA IIP3 |
| R2 | 3010 Ω | 0603 | Voltage Control Resistor |





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## Operating Instructions

M/A-COM's MADCSM0012 is a highly integrated MMIC LNA/downconverter for operation in the 1800-2000 MHz PCS frequency band. The downconverter provides exceptional RF performance while consuming low DC current and is packaged in a low cost plastic package. It is ideal for lightweight battery operated portable radio systems.

The MADCSM0012 consists of an LNA, RFA, single-ended mixer and single-ended IF output buffer as shown in the block diagram. Surface mount resistors, inductors and capacitors are used in conjunction with the LNA/downconverter to optimize the trade-offs among performance, tunability and ease of use. The sample board schematic shows the LNA/downconverter and required off-chip components.

The input of the LNA is matched externally with a series inductor (L1) and a shunt capacitor (C1) to provide a low loss match to the optimum noise impedance in the band of interest. A high Q inductor such as Coilcraft's 0402CS series must be used if the specified noise figures are to be achieved. The series capacitor, C2, is a DC blocking and input matching capacitor. The LNA is nominally biased with 15 mA to give an input IP3 of +6 dBm. An external resistor, R1, may be used to increase the LNA bias current and thus increase the IP3. An external image reject filter is required between the LNA output and RFA input to prevent downconversion of noise at the image frequency to the IF. This filter should have a 50-ohm input and output impedance.

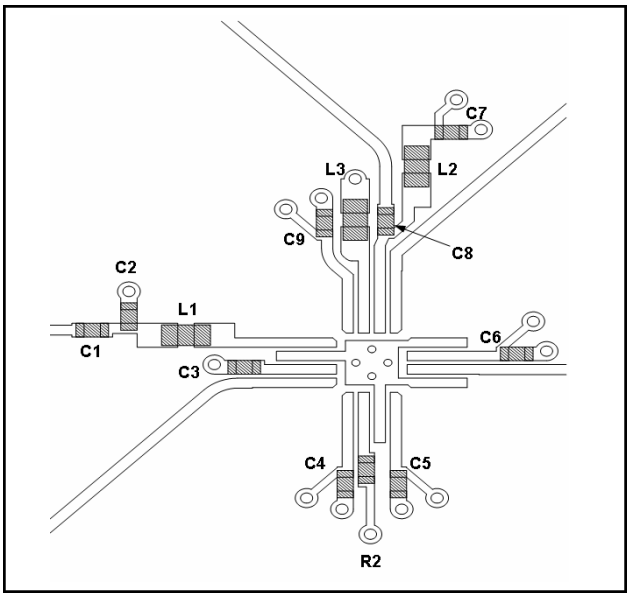
The mixer is a single-ended floating FET mixer that provides exceptional linearity and isolation with low loss and no DC current. An off-chip inductor, L3, is required to match the output of the mixer to the input of the IF buffer amplifier. The case size of L3 is typically 0603 but if more gain is needed, use a 0805 case size.

The IF output port is the open drain of the IF buffer amplifier. This allows maximum flexibility of the intermediate frequency and also IF filter. A matching network such as that shown herein can be used to match to 50 ohms from the output impedance of the buffer to the input impedance of the filter at the 210 MHz intermediate frequency. The inductor also acts as a choke for the DC supply line. Elements L2 and C8 provide the necessary impedance transformation.

The LO input port is matched on-chip to 50 ohms. An LO buffer amplifier amplifies the -10 dBm input signal to the level required to drive the mixer. Performance is optimum with a drive level of -7 dBm.

All DC supply lines must be properly bypassed at RF frequencies to obtain optimum performance and at lower frequency to maintain unconditional stability. Capacitors C4, C5, C6, C7 and C9 are RF bypass capacitors for the LNA, RFA and LOA. The value and placement of these capacitors is critical in determining the frequency response of these amplifiers. Capacitor C3 is a source bypass capacitor for the second stage of the low noise amplifier. The placement of this capacitor will affect the gain of the LNA. For best performance, all the RF bypass capacitors should be placed as close to the device as possible.

## Recommended PCB Configuration





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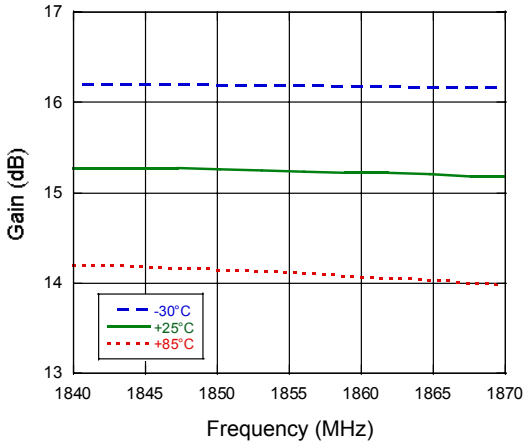
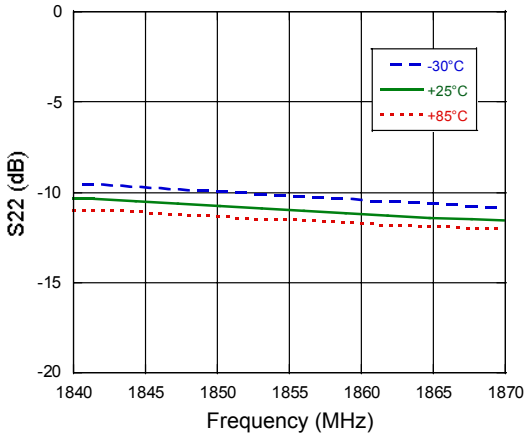
## Typical Performance Curves vs. Temperature

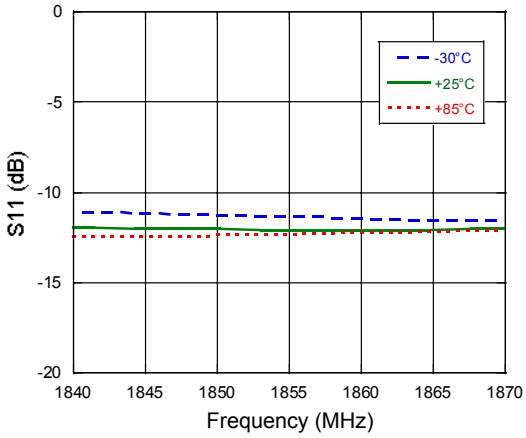
### *LNA Gain*



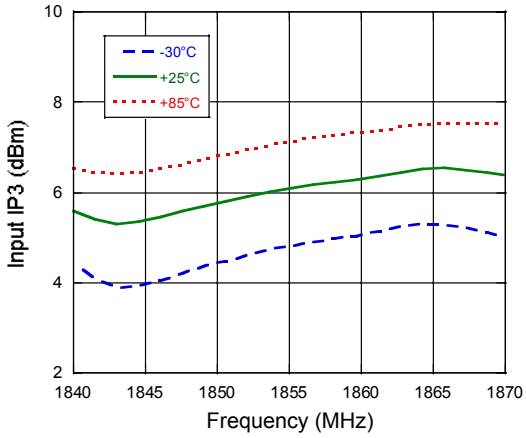

### *LNA Output Return Loss*



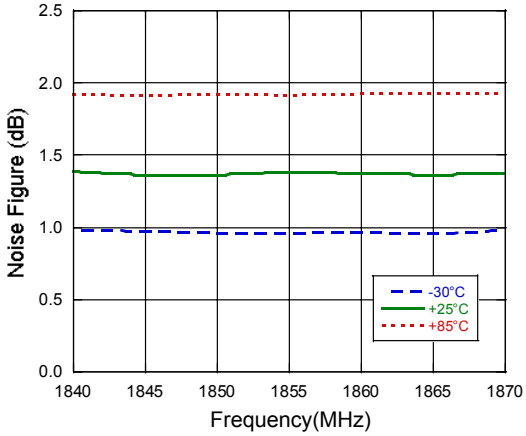

### *LNA Input Return Loss*



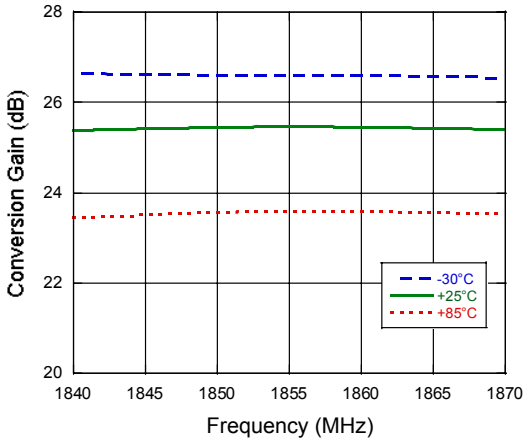

### *LNA Input IP3*




### *LNA Noise Figure*




### *Full Chain Conversion Gain*









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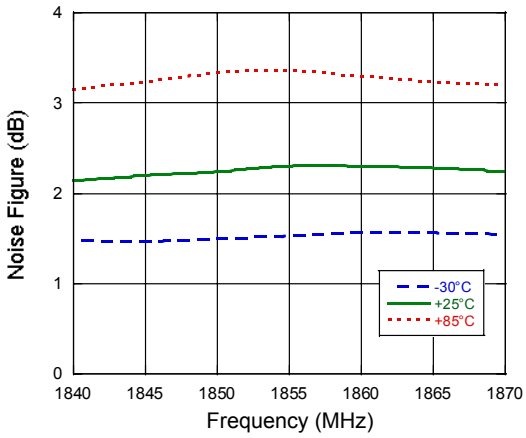
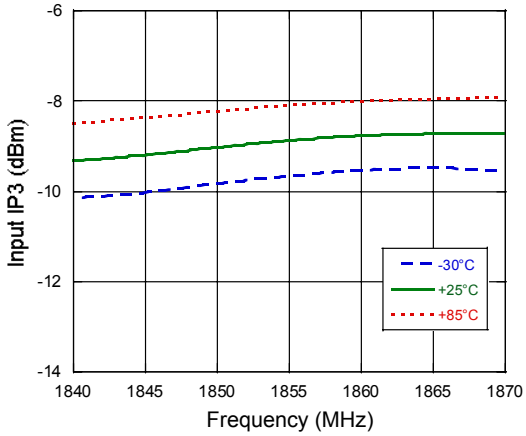
## Typical Performance Curves vs. Temperature

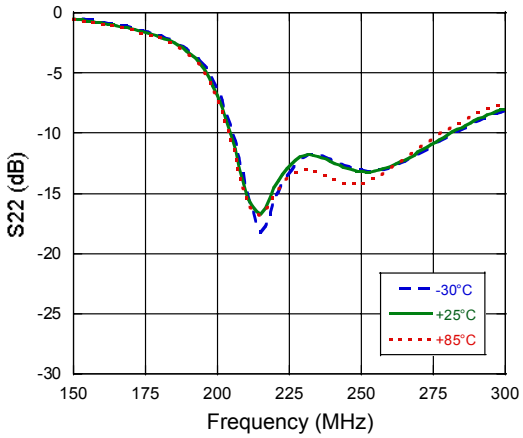
***Full Chain Noise Figure***



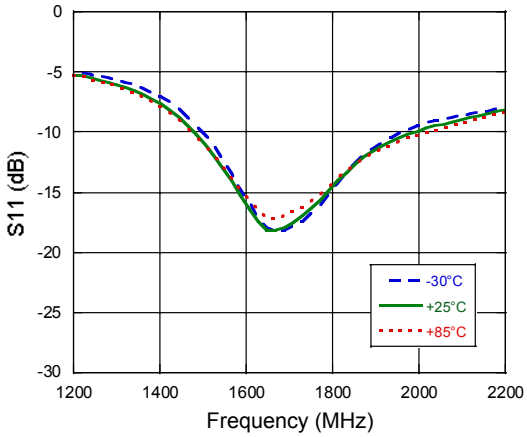

***Full Chain Input IP3***



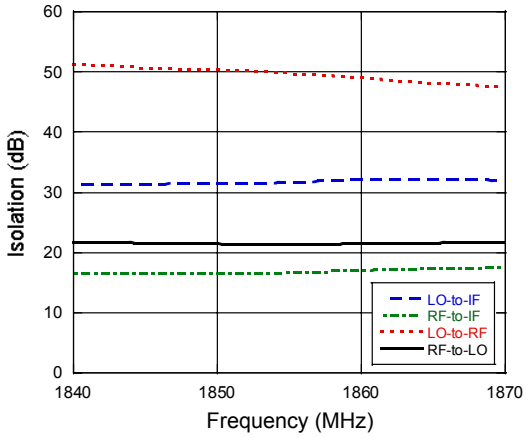

***Full Chain IF Return Loss***



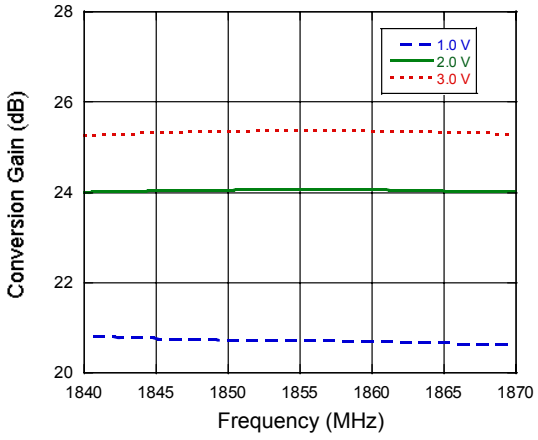

***Full Chain LO Return Loss***




***Full Chain Port to Port Isolation***




***Full Chain Conversion Gain vs. $V_{CTL}$***





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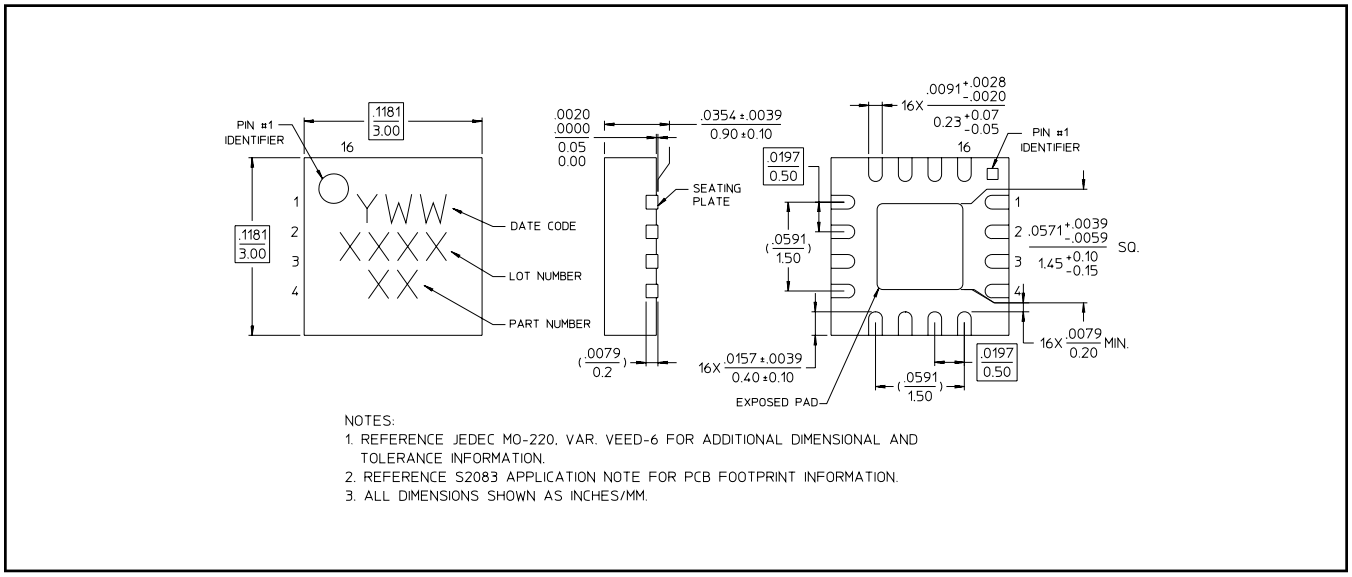
## 3mm 16-Lead PQFN†




†Meets JEDEC moisture sensitivity level 1 requirements.

## Handling Procedures

Please observe the following precautions to avoid damage:

## Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.





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