

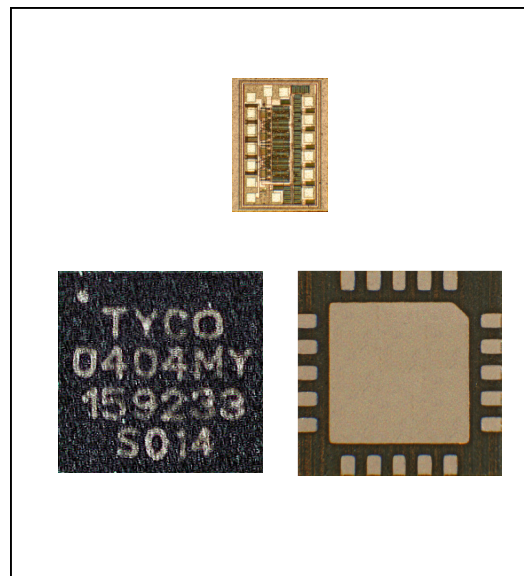
Quad Bias Driver for GaAs FET and PIN Diode Switches

MADRMA0001 & 2
MADR-007690-DR0002

Description The MADRMA0001 family of quad bias drivers can either be configured to translate TTL signals into the negative voltages required for GaAs FET switches or attenuators or they can be used to produce up to ± 40 mA per channel for biasing series or shunt PIN diode switches. Each channel contains Inverting and Non-Inverting Outputs for logic flexibility. Designed with high-speed CMOS technology, the drivers achieve high performance with very low power dissipation.

Features

- Propagation Delay less than 25 nS
 - Complementary Outputs
 - High positive and negative output currents
 - True TTL Inputs
 - Low Quiescent Power Dissipation
 - Available in DIE and QFN-20 Surface Mount Package formats
 - Available in Pb-free RoHS compliant package or Sn/Pb plated package for Military applications (No Pure Sn)
- MADRMA0001: Die
 - MADRMA0002: QFN-20, Tin Plating (Sn, 100%)
 - MADR-007690-DR0002: QFN-20, Tin-Lead Plating (Sn/Pb, 85%/15%)



AC & DC Characteristics Over Guaranteed Operating Temperature Range

| Symbol | Parameter | Test Conditions | Units | Min | Typ | Max |
|--------------------|----------------------------------|--------------------------------------------------|----------|-----------------|-----|----------------|
| V_{IH} | Input HIGH Voltage | | V | 2.0 | — | V_{CC} |
| V_{IL} | Input LOW Voltage | | V | -0.8 | — | 0.8 |
| V_{OH} | Output HIGH Voltage | No Load | V | $V_{OPT} - 0.1$ | — | - |
| V_{OL} | Output LOW Voltage | No Load | V | — | — | $V_{EE} + 0.1$ |
| I_{IN} | Input Current | $V_{IN} = V_{CC}$ or GND | μA | -20 | 0 | 20 |
| R_{out} | Output Resistance | | Ω | | 40 | 60 |
| I_{OH} | DC Output Current – HIGH | Set by external resistors, R2 or R3 | mA | | | 40 |
| I_{OL} | DC Output Current – LOW | Set by external resistors, R2 or R3 | mA | | | -40 |
| I_{CC} | Quiescent Supply Current | $V_{CC} = \text{Max}$, $V_{in} = V_{CC}$ or GND | μA | — | — | 400 |
| T_{PHL}, T_{PLH} | Propagation Delay | -40°C to $+85^{\circ} \text{C}$ | nS | — | 15 | 25 |
| T_{THL}, T_{TLH} | Output Transition Time | -40°C to $+85^{\circ} \text{C}$ | nS | — | 3 | 6 |
| | Delay Skew, Output A to Output B | -40°C to $+85^{\circ} \text{C}$ | nS | — | 3 | 6 |
| | Minimum Pulse Width | | nS | 30 | | |
| | Maximum PRF | | MHz | | | 15 |

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Absolute Maximum Ratings

| Parameter | Absolute Maximum |
|-----------------------|----------------------------|
| V_{CC} | - .5V to + 6.0 V |
| V_{EE} | - 6.0 V to 0.0 V |
| V_{OPT} | Equal to V_{CC} |
| $V_{CC} - V_{EE}$ | 12 V |
| V_{IN} | -0.5 V to $V_{CC} + 0.5$ V |
| V_{OUT} | V_{EE} to V_{CC} |
| I _{in} | ± 25 mA |
| I _{out} | ± 50 mA |
| Storage Temperature | -65°C to +150°C |
| Operating Temperature | -40°C to +85°C |

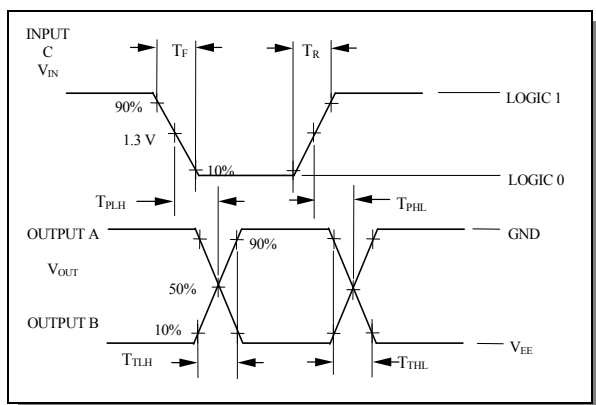
Note: The TTL interface is a CMOS structure. Without V_{CC} applied, the input will be low impedance. Once V_{CC} is applied, the driver will function as specified without latching-up.

Guaranteed Input Operating Ranges

| Symbol | Parameter | Unit | Min | Typical | Max |
|-----------|---------------------------------------------|------|------|---------|----------|
| V_{CC} | Positive DC Supply | V | 4.5 | 5.0 | 5.5 |
| V_{EE} | Negative DC Supply | V | -5.5 | -5.0 | -4.5 |
| V_{OPT} | Output DC Supply | V | 0.0 | | V_{CC} |
| T_A | Operating Temperature | °C | -40 | | +85 |
| TTL Input | Rise or Fall Time 10% to 90%, 90% to 10% | nS | — | | 500 |

Note: All voltages are relative to GND.

Switching Waveforms

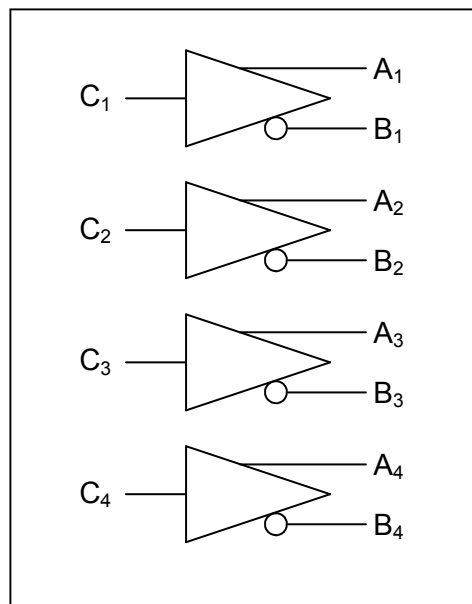


Note: See Switching Wave Forms for the definition of the switching terms. Supplies must be by-passed with .01 μ F Capacitors. Unused inputs must be tied to Ground

Truth Table

| Input - C_X | Outputs - A_X | Output - B_X |
|---------------|-----------------|----------------|
| 0 | V_{EE} | V_{OPT} |
| 1 | V_{OPT} | V_{EE} |

Logic Diagram

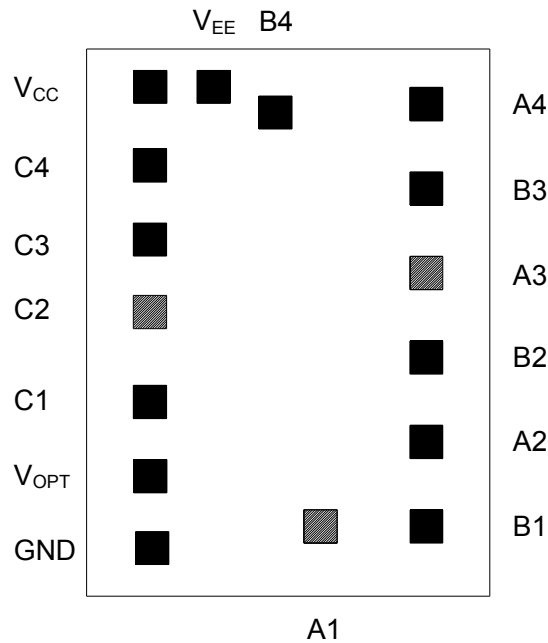


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MADRMA0001 Outline:

While die pad and package pin numbers are different, the functions remain the same. The back of the die is internally connected to V_{EE}. It must remain isolated from other voltages.



Die Size: 48 x 64 mils
Die Thickness: 10 mils max

Assembly Instructions:

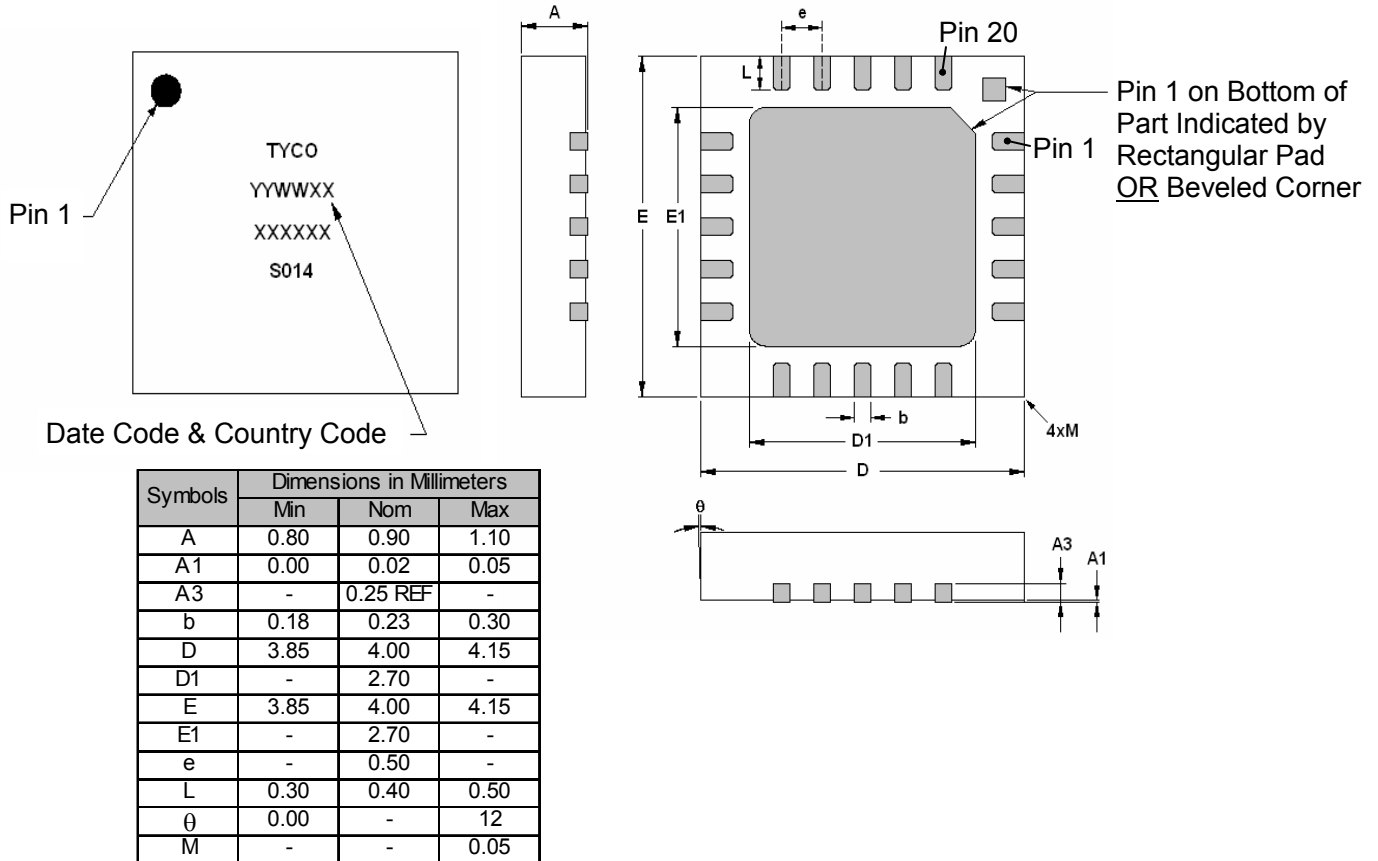
Die attach: Use non-conductive epoxy.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds.

Quad Bias Driver for GaAs FET and PIN Diode Switches

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MADRMA0002 / MADR-007690-DR0002 Outline:



Pin Configuration (QFN-20)

| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|-----|----------|-----|----------|-----|-----------------|-----|------------------|
| 1 | GND | 6 | A2 | 11 | A4 | 16 | C4 |
| 2 | N/C | 7 | B2 | 12 | B4 | 17 | C3 |
| 3 | N/C | 8 | N/C | 13 | V _{EE} | 18 | C2 |
| 4 | A1 | 9 | A3 | 14 | N/C | 19 | C1 |
| 5 | B1 | 10 | B3 | 15 | V _{CC} | 20 | V _{OPT} |

Note: The center paddle on the back of the package should be left floating. The paddle does not require a thermal or electrical connection.

Ordering Information

| Part Number | Description | Available Packaging |
|--------------------|--------------------------|---------------------------------------|
| MADRMA0001 | Die | Waffle Pack (100 or 400 die per pack) |
| MADRMA0002 | QFN-20, Tin Plating | Bulk or Tape & Reel (1K Reel) |
| MADR-007690-DR0002 | QFN-20, Tin-Lead Plating | Bulk or Tape & Reel (1K Reel) |

Note: Packaging choices will be noted as a service line item on any quotation or sales order.

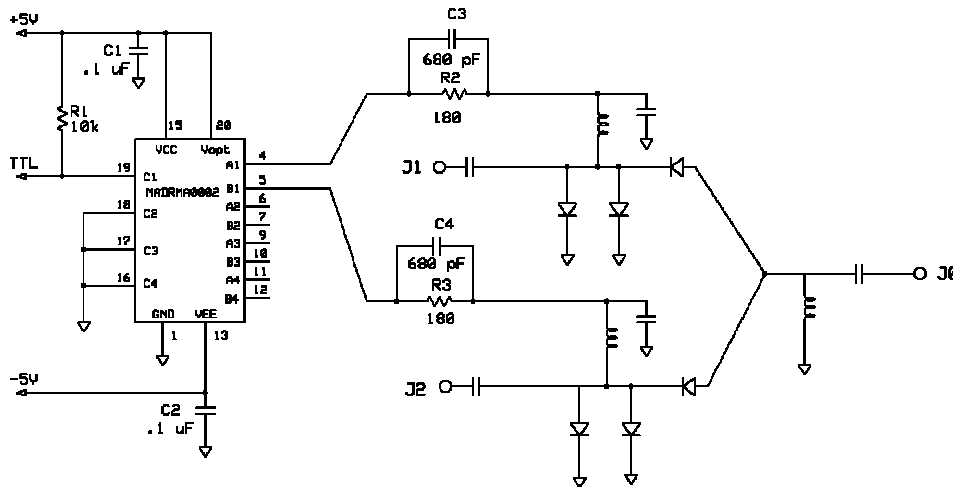
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Application Information

- The input logic voltage (V_{in}) cannot exceed the positive supply (V_{cc}) by more than 0.5 V nor go below GND by more than 0.5 V.
- The input current should not exceed ± 25 mA.
- This device should be treated as any TTL CMOS circuit. Pull-up/down resistors should tie to V_{cc} or GND. Non-used inputs must be tied to GND. Decoupling caps (0.1 uF) should be used on V_{cc} and V_{ee}, and the output current should be limited to ± 40 mA.
- Logic “0” sets J0 to J1 to low loss state
- Limiting Resistors (R2, R3) set for +/- 20 mA output current
- The value of the limiting resistors (R2, R3) is determined by the following: $R1 = [(V_{cc} - V_{diode})/I_{desired}] - R_{out}$

Driving PIN Diode Switches:



Driving FET Switches:

