Datasheet - MAP3242

4-channel LED Driver for High Brightness LEDs

General Description

MAP3242 is a 4-channel LED driver optimized for LED backlight application targeting mid and large size LCD module. MAP3242 uses the boost MOSFET externally and 4-channel current sources internally for driving high brightness White LEDs.

MAP3242 has 65V absolute Max. rating FB pins and input voltage is ranged from 8.5V ~ 36V and max LED current is 240mA per channel.

MAP3242 features internal soft-start and 2.5% LED current accuracy including matching between channels

MAP3242 has various protections like output over-voltage, adjustable LED short, LED open, open schottky diode and UVLO.

MAP3242 has initial open FB detection function to not boost the output voltage to OVP level except LED open event.

MAP3242 is available 28 leads HSOP, 20 leads SOIC and E-TSSOP with Halogen-free (fully RoHS compliant).

Features

- 8.5V to 36V Input Voltage Range
- Drive up to 4 Channels
- 65V FB Pin Voltage
- 0.8V Min Headroom Voltage @ 150mA
- 240mA Output Current per Channel
- ±2.5% Current Accuracy
- Initial Open FB Detection Function
- Programmable Boost Switching Frequency (100KHz ~ 500KHz)
- LED Current Set by both PWM and External DC Voltage
- Boost Over Current Protection
- Output Over Voltage Protection
- Adjustable LED Short Protection
- LED Open Protection
- Schottky Diode Open Protection
- UVLO

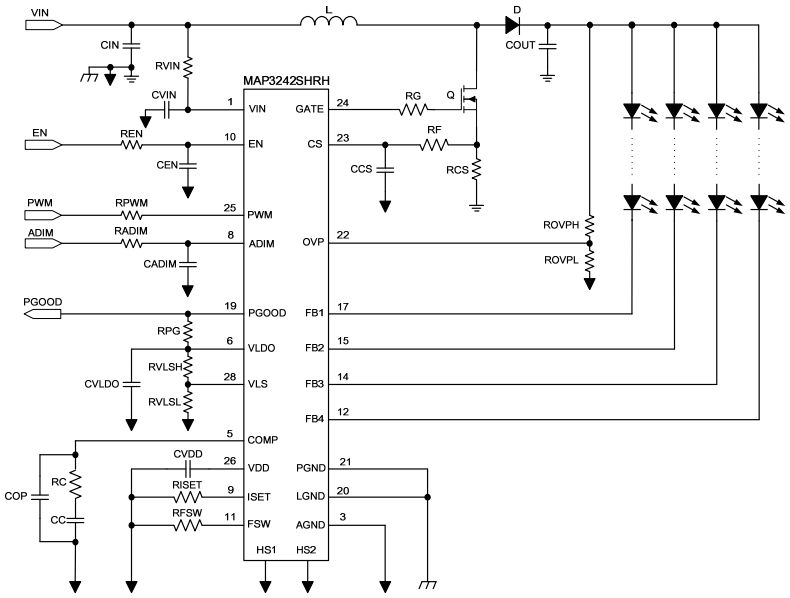
Applications

- High Brightness white LED backlighting for LCD TVs and monitors
- General LED lighting applications

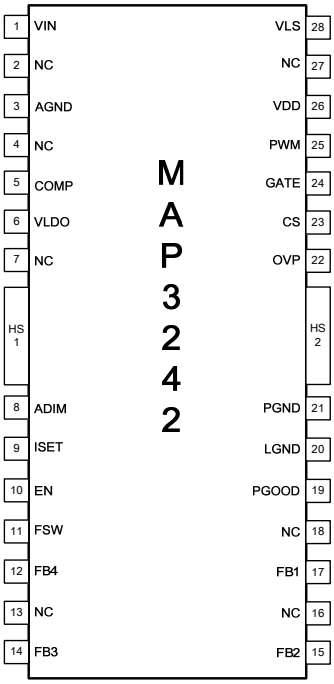
Ordering Information

Part Number	Top Marking	Ambient Temperature Range	Package	RoHS Status
MAP3242SHRH	MAP3242	-40℃ to +85℃	28Leads HSOP	Halogen Free
MAP3242SIRH	MAP3242	-40℃ to +85℃	20Leads SOIC	Halogen Free
MAP3242TERH	MAP3242	-40℃ to +85℃	20Leads E-TSSOP	Halogen Free

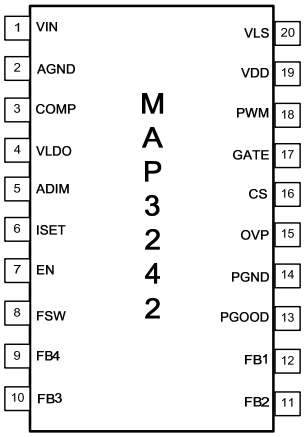
Typical Application



Pin Configuration

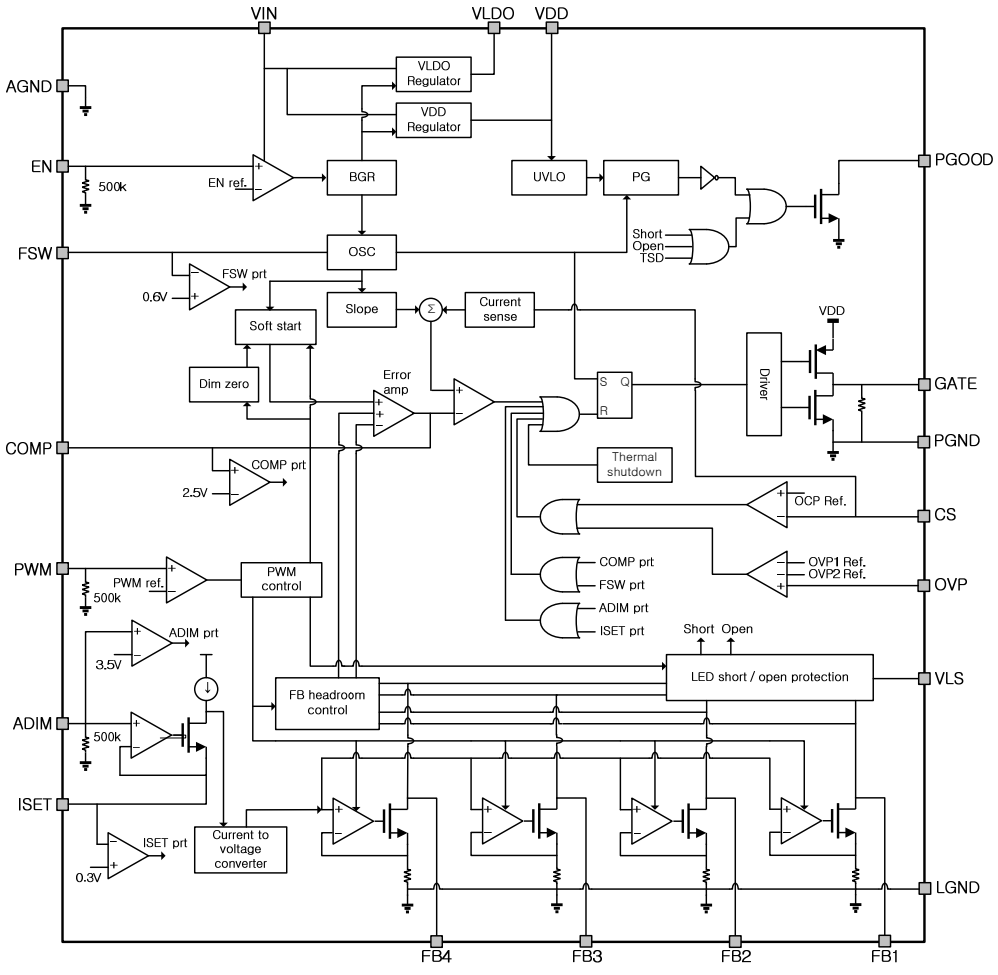


HSOP-28L



SOIC/ETSSOP-20L

Functional Block Diagram



Pin Description

Name	28leads HSOP	20leads E-TSSOP	20leads SOIC	Description
VIN	**1**	**1**	**1**	Power supply input. Need external input capacitor.
AGND	**3**	**2**	**2**	Analog ground
COMP	**5**	**3**	**3**	Internal error amplifier compensation (Note 1)
VLDO	**6**	**4**	**4**	Internal 5V Regulator Output. Need external capacitor to stabilize the regulator
ADIM	**8**	**5**	**5**	Setting for LED current thru external DC voltage
ISET	**9**	**6**	**6**	Setting for LED current reference resistor (Note2)
EN	**10**	**7**	**7**	Enable. Active High.
FSW	**11**	**8**	**8**	Setting for booster switching frequency (Note 3)
FB4	**12**	**9**	**9**	LED current sink for Ch4
FB3	**14**	**10**	**10**	LED current sink for Ch3
FB2	**15**	**11**	**11**	LED current sink for Ch2
FB1	**17**	**12**	**12**	LED current sink for Ch1
PGOOD	**19**	**13**	**13**	Power Good status open drain output (Normal : Open, Protection : Internal GND)
LGND	**20**	**-**	**-**	LED current sink ground
PGND	**21**	**14**	**14**	Power ground
OVP	**22**	**15**	**15**	Output Over voltage sense (Note 4)
CS	**23**	**16**	**16**	External boost current sense (Note 5)
GATE	**24**	**17**	**17**	Gate driver output for external boost MOSFET
PWM	**25**	**18**	**18**	PWM signal input for dimming (Note 6)
VDD	**26**	**19**	**19**	Internal 10V Regulator Output. Need external capacitor to stabilize the regulator
VLS	**28**	**20**	**20**	Setting for LED short detection level thru external DC voltage
-	**2, 4, 7, 13, 16, 18, 27**	**-**	-	No connection
-	**HS1, 2**	**-**	-	Connect to GND for heat-sinking purpose (Note 7)
-	**-**	**Exposed PAD**	-	Connect to GND by multiple vias for heat-sinking purpose (Note 7)

Note 1: Connect external capacitor and resistor to COMP pin. Refer to a typical application diagram
Note 2: The resistor value on ISET pin controls the full scale level of sink current on FB- pins. Do not leave this pin open.
Note 3: Connect external resistor to set the oscillator frequency from 100kHz to 500kHz
Note 4:.Connect center node of resistive voltage divider from output to ground. Refer to a typical application diagram
Note 5: Connect external resistor to PGND to sense the external power MOSFET drain current
Note 6: This external PWM signal is used for brightness control
Note 7: Not connected internally.

Absolute Maximum Ratings(Note 1)

Symbol	Parameter	Min	Max	Unit
V_{VIN}	Supply Voltage	-0.3	40	V
V_{GATE}	Gate Driver Output	-0.3	14	V
$V_{VDD,}$	VDD pin	-0.3	14	V
V_{EN}, V_{CS}, V_{VLDO} ,V_{PWM}, V_{COMP}, V_{OVP}, V_{VLS}, $V_{ISET,}$ $V_{PGOOD,}$ $V_{FSW,}$ V_{ADIM}	EN, CS, VLDO, PWM, COMP, OVP, VLS, ISET, PGOOD, FSW, ADIM pin	-0.3	6	V
$V_{FB1~4}$	LED Current Sink Pin	-0.3	65	V
$I_{FB1~4}$	LED Current Sink Pin		240	mA
T_{PAD}	Soldering Lead/ Pad Temperature 10sec		300	°C
T_J	Junction Temperature	-40	+150	°C
T_S	Storage Temperature	-65	+150	°C
ESD	HBM on All Pins (Note 2)	-2000	+2000	V
	MM on All Pins (Note 3)	-200	+200	

Note 1: Stresses beyond the above listed maximum ratings may damage the device permanently. Operating above the recommended conditions for extended time may stress the device and affect device reliability. Also the device may not operate normally above the recommended operating conditions. These are stress ratings only.
Note 2: ESD tested per JESD22A-114.
Note 3: ESD tested per JESD22A-115.

Recommended Operating Conditions (Note 1)

Parameter		Min	Max	Unit
V_{VIN}	Supply Input Voltage	8.5	36	V
$I_{FB1~4}$	LED Current Sink Pin	90	240	mA
$V_{FB1~4}$	LED Current Sink Pin		65	V
T_A	Ambient Temperature (Note 2)	-40	+85	°C

Note 1: Normal operation of the device is not guaranteed if operating the device over outside range of recommended conditions.
Note 2: The ambient temperature may have to be derated if used in high power dissipation and poor thermal resistance conditions.

Package Thermal Resistance (Note 1)

Parameter		θJA	θJC	Unit
MAP3242SHRH	28 Leads HSOP	45.1	28.7	℃/W
MAP3242SIRH	20 Leads SOIC	68.5	36.3	℃/W
MAP3242TERH	20 Leads E-TSSOP	64.1	9.3	℃/W

Note 1: Multi-layer PCB based on JEDEC standard (JESD51-7)

Electrical Characteristics

Unless noted, V_{IN} = 12V, C_{IN} = 1.0μF, and typical values are tested at T_A = 25°C.

Parameter		Test Condition	Min	Typ	Max	Unit
General Input Output						
V_{VIN}	Input Voltage Range		8.5		36	V
I_Q	Quiescent Current	Driving FBs at Min. setting with no load		5	10	mA
I_{SD}	Ground Pin Current in Shutdown	V_{IN} = 12V, V_{EN} = 0V No Load Current on FB-		40		μA
V_{EN}	Logic Input Level on EN pin	V_{EN_L} : Logic Low			0.8	V
		V_{EN_H} : Logic High	2.2			
R_{EN}	Pull-down resistor on EN pin		250	500		kΩ
V_{UVLO}	Under Voltage Lockout Threshold Voltage on VDD pin	Release UVLO		7.0	7.5	V
		Hysteresis		1.0		
Oscillator						
f_{SW}	Internal Oscillator Frequency	R_{FSW}=250 kΩ	180	200	220	kHz
		R_{FSW}=100 kΩ	425	500	575	
D_{max}	Max. Duty Cycle		85	90		%
Reference						
V_{VLDO}	5V LDO Voltage	V_{IN} > 15V, No load current	4.75	5	5.25	V
I_{VLDO}	5V LDO Source Current	V_{IN} > 15V, No load current	10			mA
V_{VDD}	LDO Voltage for Gate Driver	V_{IN} > 15V, No load current	8.5	10	11.5	V
Protection						
T_{SD}	Thermal Shutdown Temperature	Shutdown Temperature		150		°C
		Hysteresis, ΔT_{SD}		25		
V_{OVP}	Over-Voltage Threshold on OVP pin	Rising Over-Voltage Limit on OVP pin	2.35	2.5	2.65	V
		Hysteresis, ΔV_{OVP}		0.1		
V_{LED_SHORT}	LED Short Protection Threshold on FB pins	V_{VLS}=1V		5		V
		V_{VLS}=3V		15		
t_{SCP}	LED Short Protection Time	f_{SW}=500kHz (Note 1, 2)		8.192		ms
V_{CS}	Boost Over Current Protection Threshold on CS pin		0.57	0.6	0.63	V
V_{OPEN}	LED Open Protection Threshold on FB pins	I_{LED}=90mA		0.09		V
		I_{LED}=240mA		0.24		
$V_{SBDOPEN}$	SBD Open Protection Threshold on OVP pin	(Note 1)		0.1		V
LED Current Sink Regulator						
$V_{FB1\sim4}$	Min. FB1~FB4 Voltage	I_{LED}=150mA, V_{ADIM}=1.5V		0.8		V
I_{FB}	Current Accuracy	I_{LED}=120mA, V_{ADIM}=1.2V			±2.5	%
I_{FB_max}	Current Sink Max. Current	V_{ADIM}=2.4V			240	mA
$I_{FB\_leakage}$	Current Sink Leakage Current	V_{PWM}=0V			5	uA
V_{ADIM}	ADIM Input Voltage Range		0.9		2.4	V
R_{ADIM}	Pull-down Resistor on ADIM pin		250	500		kΩ
PWM Interface						
f_{PWM}	PWM Dimming Frequency		0.1		2.0	kHz
V_{PWM}	Logic Input Level on PWM pin	V_{PWM_L} : Logic Low			0.8	V
		V_{PWM_H} : Logic High	2.2			
t_{ON_MIN}	Min. On-Time (Note 1)	f_{SW}=100kHz			30	us
R_{PWM}	Pull-down Resistor on PWM pin		250	500		kΩ
Boost MOSFET GATE Driver						
V_{GATE}	Gate Drive Voltage	V_{IN} > 15V	8.5	10	11.5	V
I_{SOURCE}	Gate Source Current	V_{IN} > 15V, V_{GATE} = 0.9* V_{VDD}	20			mA
I_{SINK}	Gate Sink Current	V_{IN} > 15V, V_{GATE} = 0.1* V_{VDD}	20			mA
t_{RISE}	Gate Output Rising Time	Gate load : 10Ω / 1nF		0.1	0.5	us
t_{FALL}	Gate Output Falling Time	Gate load : 10Ω / 1nF		0.1	0.5	us

Electrical Characteristics(Continued)

Parameter		Test Condition	Min	Typ	Max	Unit
Soft Start						
t_{SS}	Soft Start Time	f_{SW}=200kHz (Note 1)		8.5	13	ms
PGOOD Output(Open Drain)						
R_{PGOOD}	Internal PGOOD resistance	V_{PGOOD}=1V		50	200	Ω

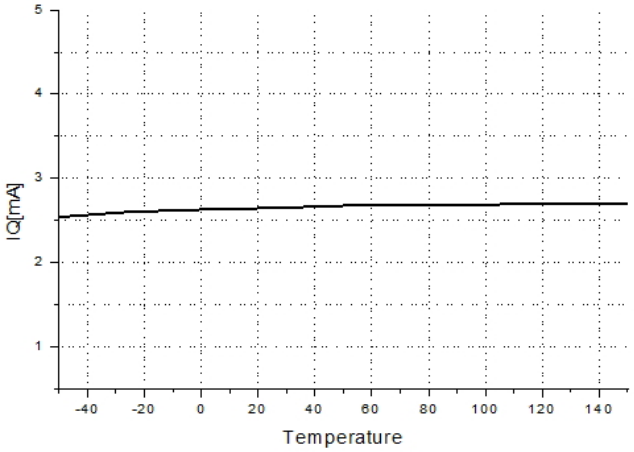
Note 1: These parameters, although guaranteed by design, are not tested in mass production.

Note 2: $tscp = \frac{1}{fsw} \times 4096$

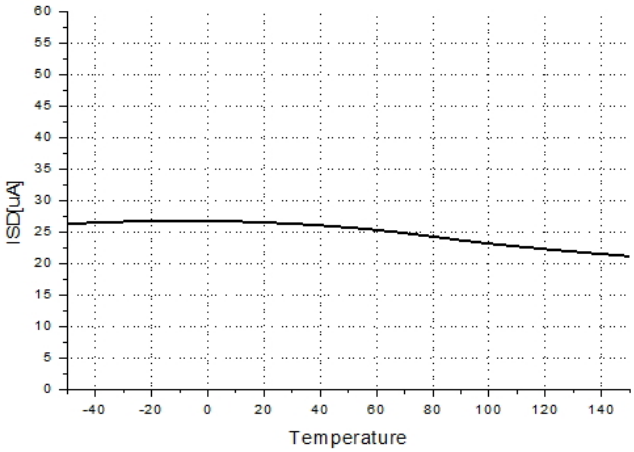
Typical Operating Characteristics

Unless otherwise noted, V_{IN} = 24V, Cin=220uF, Cout=100uF, RISET=10kΩ, RFSW=250kΩ and T_A = 25°C.

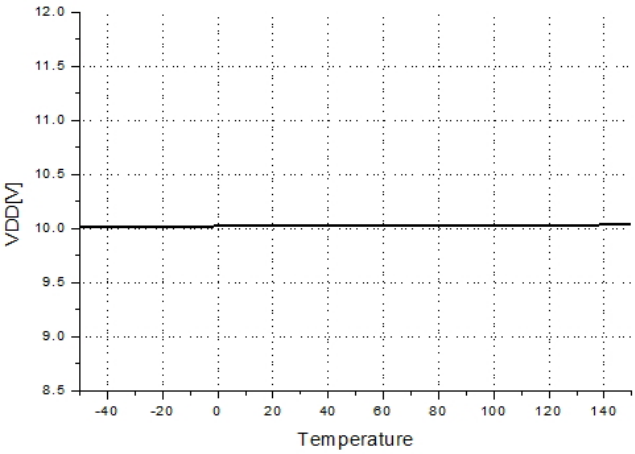
Temp. vs. I_Q



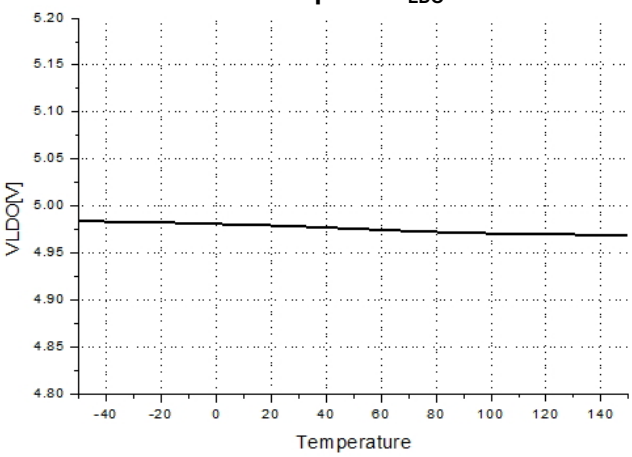
Temp. vs. I_{SD}



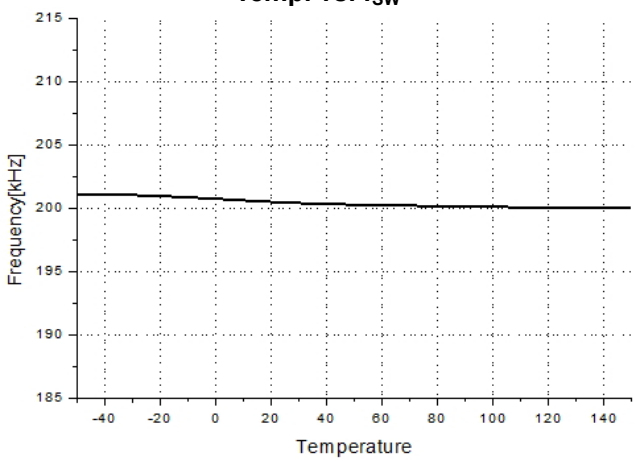
Temp. vs. V_{DD}



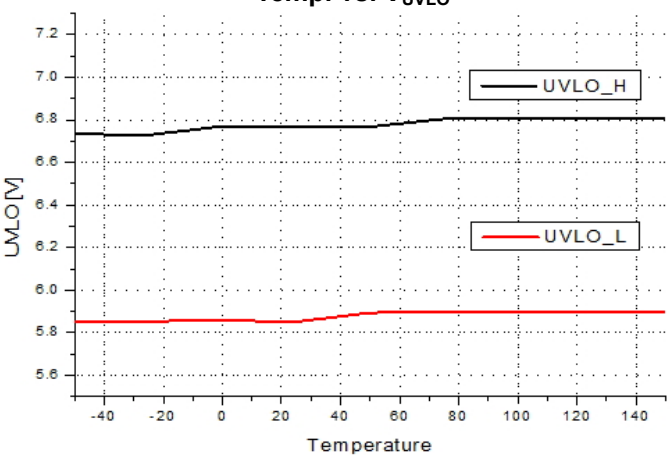
Temp. vs. V_{LDO}



Temp. vs. f_{SW}



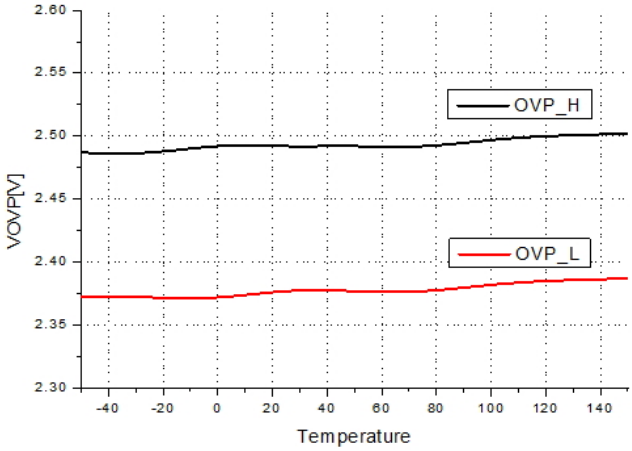
Temp. vs. V_{UVLO}



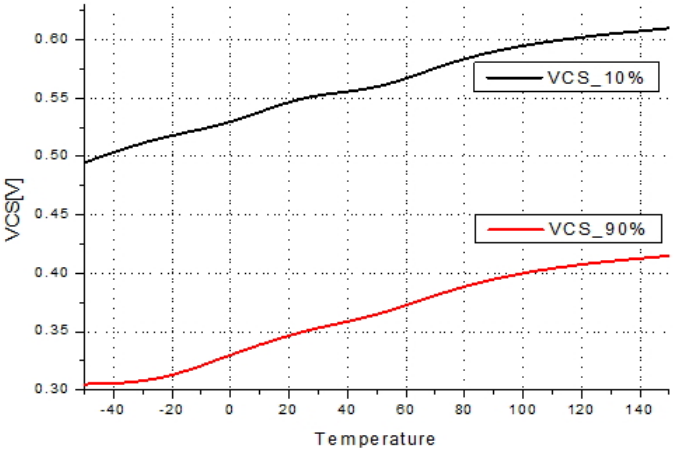
Typical Operating Characteristics

Unless otherwise noted, V_{IN} = 24V, Cin=220uF, Cout=100uF, RISET=10kΩ, RFSW=250kΩ and T_A = 25°C.

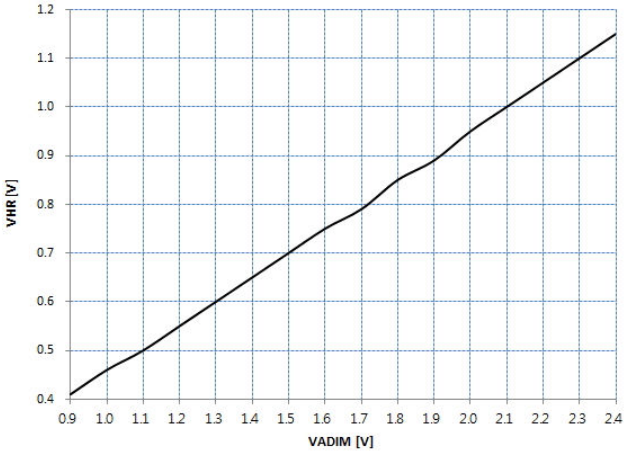
Temp. vs. V_{OVP}



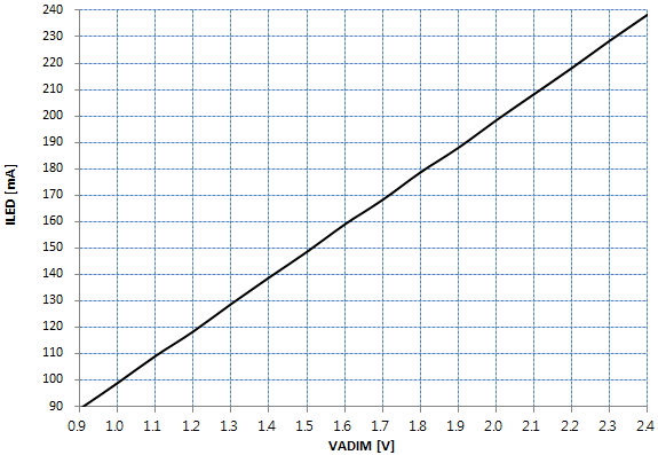
Temp. vs. V_{CS}



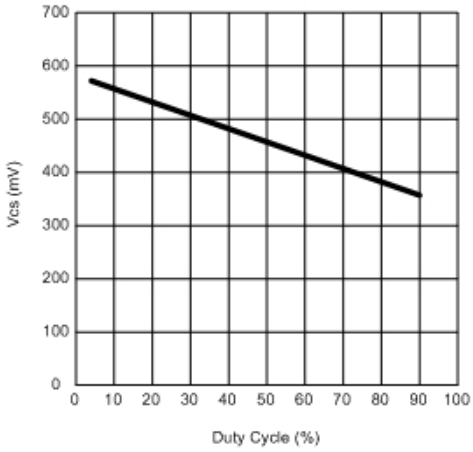
V_{ADIM}. vs. Min. V_{FB}(Headroom)



V_{ADIM}. vs. I_{LED}



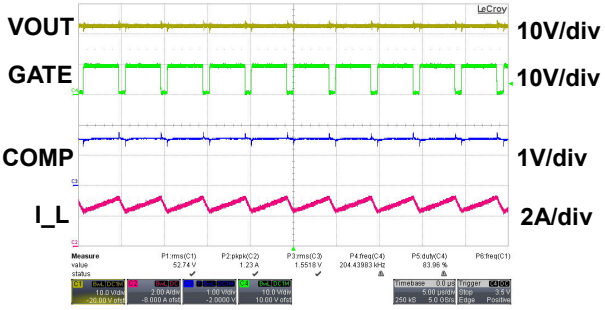
Duty Cycle. vs. V_{CS}



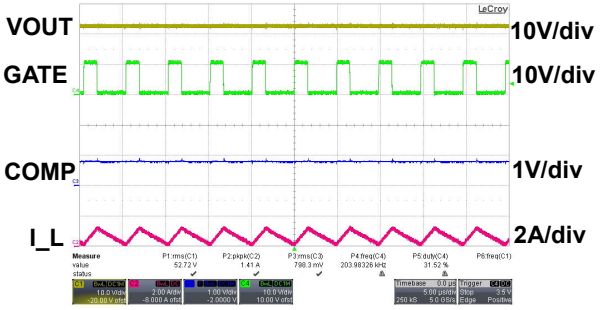
Typical Operating Characteristics

Unless otherwise noted, V_{IN} = 24V, Cin=220uF, Cout=100uF, RISET=10kΩ, RFSW=250kΩ and T_A = 25°C.

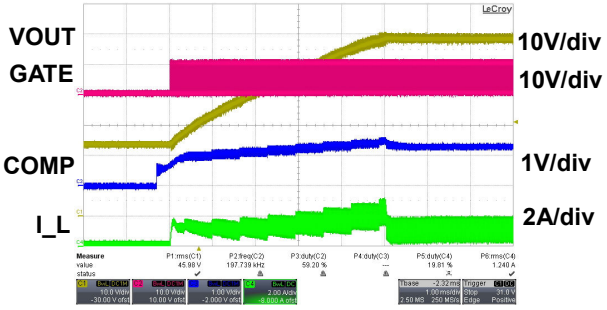
CCM Operation



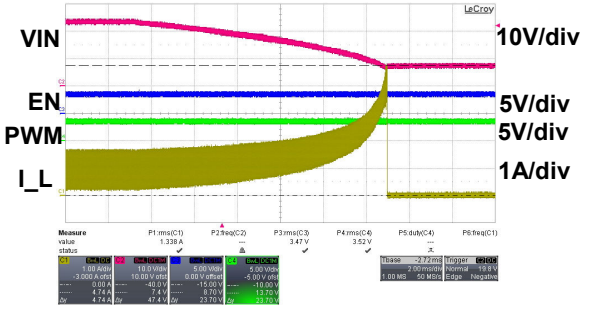
DCM Operation



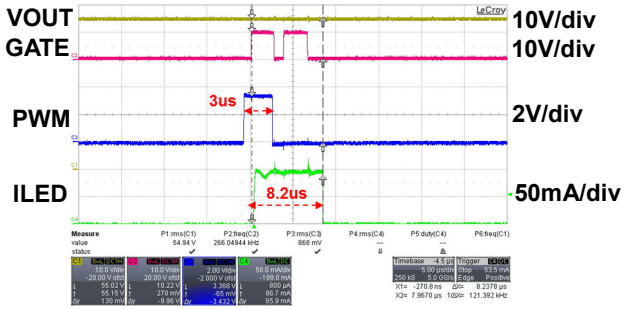
Turn-on(Soft-start)



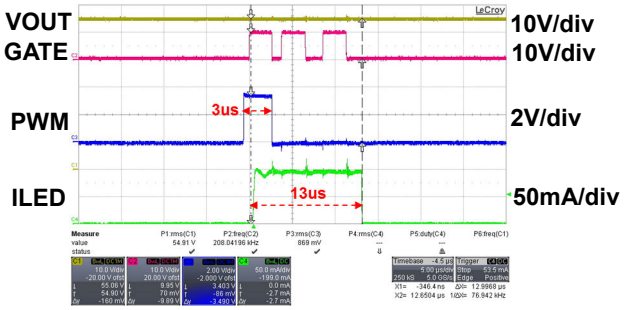
Turn-off



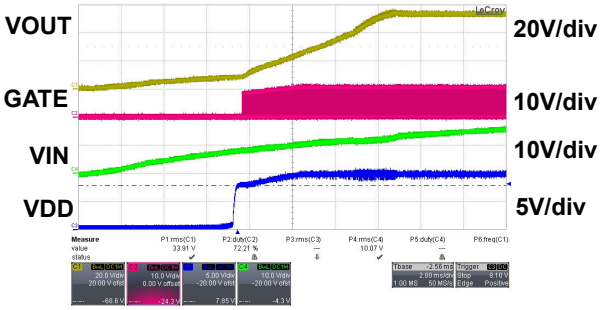
Min. Dimming(2 Clock)



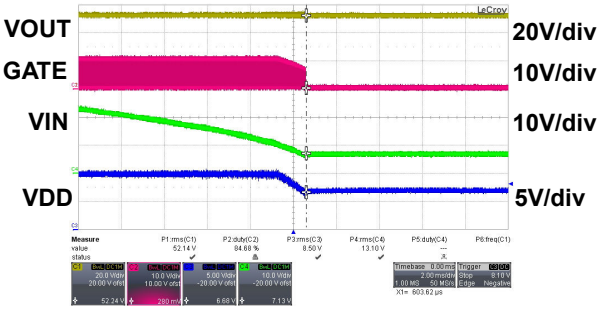
Min. Dimming(3 Clock)



UVLO Release



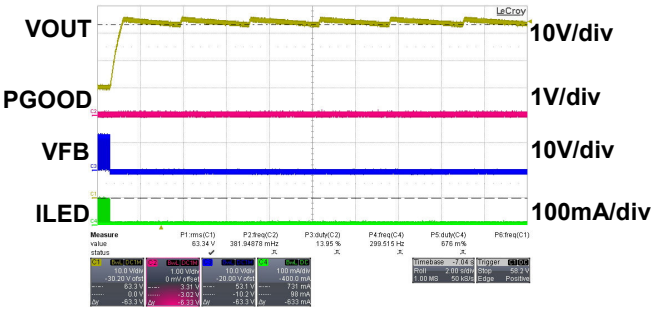
UVLO Lockout



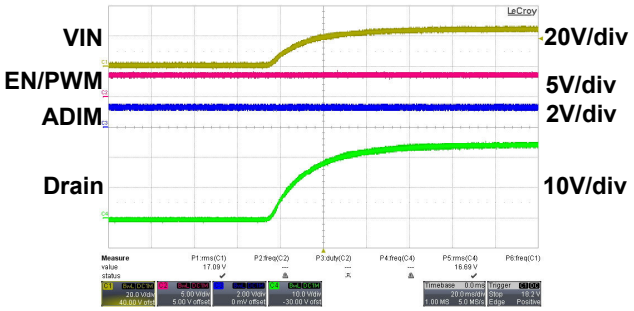
Typical Operating Characteristics

Unless otherwise noted, V_{IN} = 24V, Cin=220uF, Cout=100uF, RISET=10kΩ, RFSW=250kΩ and T_A = 25°C.

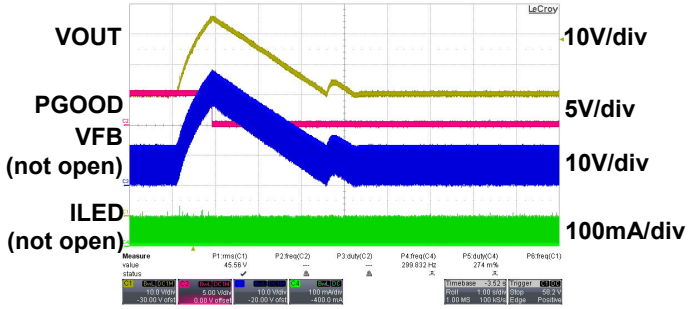
Over-Voltage Protection(LED all open)



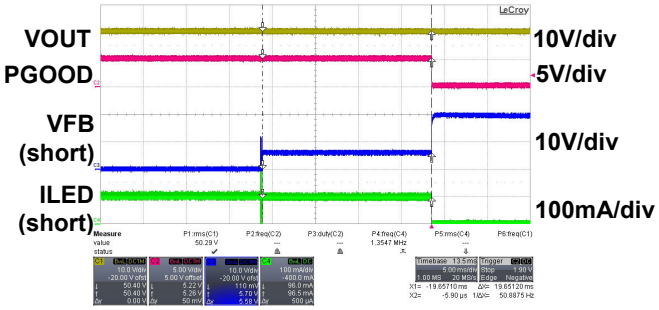
SBD Open Protection



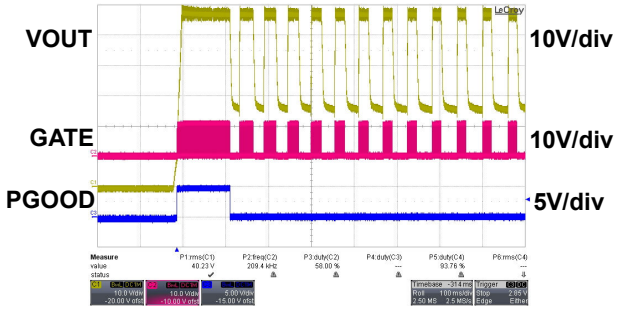
LED Open Protection



LED Short Protection



Thermal Shutdown



Application Information

CURRENT MODE BOOST SWITCHING CONTROLLER OPERATION

The MAP3242 employs current mode control boost architecture that has a fast current sense loop and a slow voltage feedback loop. Such architecture achieves a fast transient response that is essential for the LED backlight application.

DYNAMIC HEADROOM CONTROL

The MAP3242 features a proprietary Dynamic Headroom Control circuit that detects the lowest voltage from any of the FB1-FB4 pins. This lowest channel voltage is used as the feedback signal for the boost controller. Since all LED stacks are connected in parallel to the same output voltage, the other FB pins will have a higher voltage, but the regulated current source circuit on each channel will ensure that each channel has the same current.

INTERNAL 5V/10V REGULATOR

The MAP3242 has built-in 5V LDO regulator to supply internal analog and logic blocks. The LDO is powered up when the EN pin is Logic High. A 2.2uF bypass capacitor is required on the VLDO pin for stable operation of the LDO.

A 10V LDO is used to drive external MOSFET connected to the GATE pin. A 2.2uF bypass capacitor is required on the VDD pin for stable operation of the LDO.

DIMMING SCHEME

The brightness control of the LEDs is performed by a pulse-width modulation of the channel current. When a PWM signal is applied to the PWM pin, the current generators are turned on and off mirroring the PWM pin behavior.

When PWM signal stays at low level (<0.8V) for a long time, the MAP3242 turns off the boost circuitry, but internal circuit is enabled so the MAP3242 increases the output voltage promptly.

If the on-time of inputted PWM signal is less than 3 fsw clock, the MAP3242 controls the Min. on-time of output PWM by 2 or 3 fsw clock to prevent abnormal turn-off or opreation. For example,

fsw=100kHz -> t_{ON_MIN} =20us to 30us
fsw=500kHz -> t_{ON_MIN} =4us to 6us

PARALLEL OPERATION

Even the MAP3242 has 4 channels and 240mA LED current capability per channel, 2 channels and 480mA application can be supported by tying 2FBs into 1ch, so the LED current capability can be increased to 480mA.

LED CURRENT ADJUSTMENT

The MAP3242 sets the LED current through the voltage level on the ADIM pin. ADIM pin voltage vs. LED current is as following table. A 10kΩ/1% resistor must be connected between the ISET pin and ground.

ADIM Voltage [V]	LED Current [mA]
0.9	90
1.0	100
1.2	120
1.4	140
1.6	160
1.8	180
2.0	200
2.2	220
2.4	240

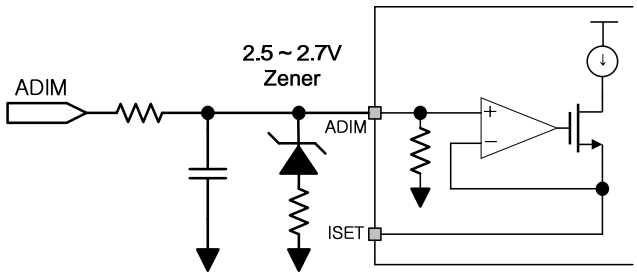
The relationship between ADIM pin voltage, RISET value and LED current is defiend by following equation.

$$I_{LED}[mA] = \frac{V_{ADIM}[V]}{R_{ISET}[k\Omega]} \times 1000$$

The MAP3242 offers protection functions to limit excess LED current increase at abnormall ISET and ADIM pin voltage. If the ADIM or ISET pin voltage is at following conditions abnormally, the MAP3242 turns off the GATE output and internal LED current sink MOSFETs.

V_ISET ≤ 0.3V
V_ADIM ≥ 3.5V

Some application need to decrease LED current further at abnormal pin voltage. In this case, a 2.5 ~ 2.7V zener clamp is recommendable on the ADIM pin like following circuit.



BOOST SWITCHING FREQUENCY

The switching frequency of the MAP3242 should be programmed between 100kHz and 500kHz by an external resistor connected between the FSW pin and ground. Do not leave this pin open. The approximate operating boost switching frequency can be calculated by following equation.

$$f_{SW}[MHz] = \frac{50}{R_{FSW}[k\Omega]}$$

If the FSW pin voltage is decreaed to below or equal to 0.6V abnormally the MAP3242 turns off the GATE output to protect excess switching frequency increase.

START-UP

(1) The MAP3242 has soft-start circuitry internally and the soft-start time(tss) is typical 8.5ms.

(2) ***'Initial Open FB Detection Function'***
There can be exist applications which do not use all the FB pins(4 channel). Conventional multi-channel LED drivers boost the output voltage to OVP level to check open FB(s).
The MAP3242 detects unused FB(s) and excludes corresponding FB(s) automatically from headroom control before start-up. ***The unused FB(s) must be conntected to GND.*** This ensures the output voltage is not boosted to OVP level at start-up. If the unused FB(s) are not connected to GND, the output voltage is boosted up to OVP level like conventional boost LED driver.

These features significantly reduce the start-up current and prevent abnormal operation at start-up.

PGOOD OUTPUT

The PGOOD pin is at its high-impedance state when no error is detected. However, if any of following exists, PGOOD pin goes into low-impedance state.

(1) LED open protection
(2) LED short protection
(3) Thermal shutdown

The PGOOD pin can be cleared by recycling the EN pin or applying a complete power-on-reset (POR).

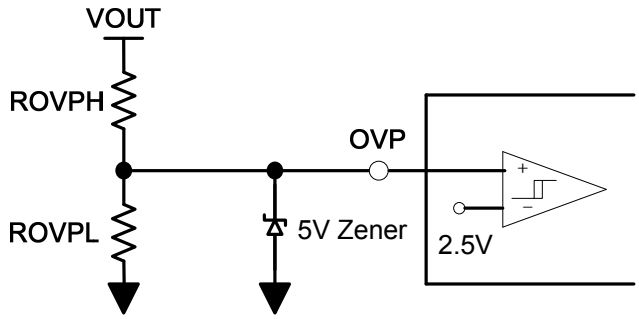
UNDER VOLTAGE LOCKOUT

If the input voltage falls below the UVLO level of typical 7V on the VDD pin, the device will stop switching and be reset. Operation will restart when the VDD pin voltage rises Min. 1V hysteresis over the lock-out threshold. This ensures fail-safe operation when the input voltage falls below Min. VIN voltage of IC.

OUTPUT OVER VOLTAGE PROTECTION

To protect the boost converter when the load is open or the output voltage becomes excessive for any reason, the MAP3242 features a dedicated overvoltage feedback input. The OVP pin is connected to the center tap of a resistive voltage-divider from the high voltage output. When the OVP pin voltage exceeds typical 2.5V, a comparator turns off the external power MOSFET. This switch is re-enabled after the OVP pin voltage drops typical 100mV hysteresis below the protection threshold. This over voltage protection feature ensures the boost converter fail-safe operation when the LED channels are disconnected from the output.

A 5V zener diode is recommendable to avoid pin damage when the RVOPL resistor is open abnormally.



The OVP voltage of output voltage can be calculated by following equation.

$$V_{OUT\_OVP}[V] = 2.5 \times (1 + \frac{R_{OVPH}}{R_{OVPL}})$$

SBD OPEN PROTECTION

When OVP pin voltage is less than 0.1V, the MAP3242 turns off the GATE output.

This protects the driver from damage if the output schottky diode is open(defective or poor solder contact).

BOOST OVER-CURRENT PROTECTION

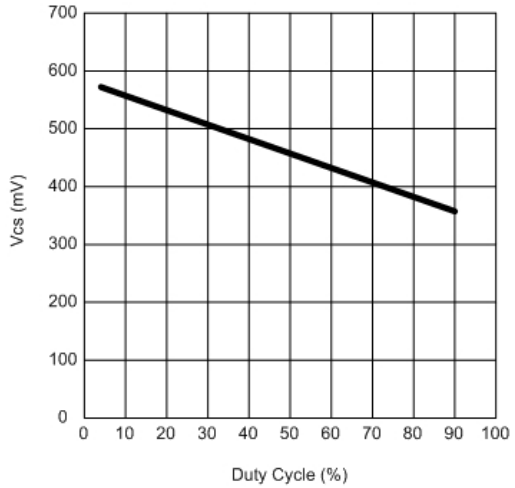
The MAP3242 features Over-Current Protection (OCP) by sensing CS pin voltage. This CS pin is used for inductor current sensing for current mode control as well.

If the CS pin voltage exceeds typical 0.6V, the MAP3242 turns off the GATE output.

The internal OCP sensing voltage decreases with increase of gate duty-cycle due to internal slope compensation which ensures stable CCM operation.

Following graph shows the relationship between gate duty-cycle and internal OCP sensing typical voltage.

Vcs vs. Duty Cycle



$$VCS\_OCP\_TYP.[V] = -0.21255D + 0.56125$$

RCS Setting Procedure

(1) Choose boost inductor value

Once the LED current, the input and output voltage and the switching frequency are fixed, the inductance value defining the boundary between DCM and CCM opreation can be calculated as;

$$L_B[H] = \frac{R_O \times D \times (1-D)^2}{2 \times f_{SW}}$$

where, Ro=Vout/Iout

(2) Find peak inductor current at selected boost inductance

$$I_{L\_peak\_DCM} = \frac{V_{IN} \times D}{f_{SW} \times L}$$

$$I_{L\_peak\_CCM} = I_{IN(OVP)} + \frac{V_{IN} \times D}{2 f_{SW} \times L}$$

The RCS value should be choosen that the output voltage can be boosted up to OVP level. And the Iout value should be considered with Max. 3 channel because the OVP is occurred LED open event only. Thus,

$$I_{IN(OVP)}[A] = \frac{V_{OUT\_OVP} \times I_{OUT} \times (N_{FB} - 1)}{\eta \times V_{IN}}$$

η : effieincy

N_{FB} : The number of using channel

(3) Find typical VCS_OCP value at given D

$$VCS\_OCP\_TYP.[V] = -0.21255D + 0.56125$$

(4) Find RCS value

In order to avoid touching the current limit during normal operation, the voltage across the current sensing resistor Rcs should be less than 80% of the worst case current limit voltage.

$$R_{CS}[\Omega] = 0.8 \times \frac{V_{CS\_OCP\_TYP}}{I_{L\_peak}}$$

Example

Vin=24V, Vout_ovp=65V, η=90%, ILED/ch=100mA, LED string=4X18, fsw=200kHz

(1) Choose boost inductor value

$$L_B = \frac{R_O \times D \times (1-D)^2}{2 \times f_{SW}} = 37[\mu H]$$

In this case, choosed inductance value is 47uH for CCM operation.

(2) Find peak inductor current

$$I_{IN(OVP)} = \frac{V_{OUT\_OVP} \times I_{LED/CH} \times (4-1)}{\eta \times V_{IN}} = 0.9[A]$$

$$I_{L\_peak\_CCM} = I_{IN(OVP)} + \frac{V_{IN} \times D}{2 f_{SW} \times L} = 1.61[A]$$

(3) Find typical VCS_OCP value at given D

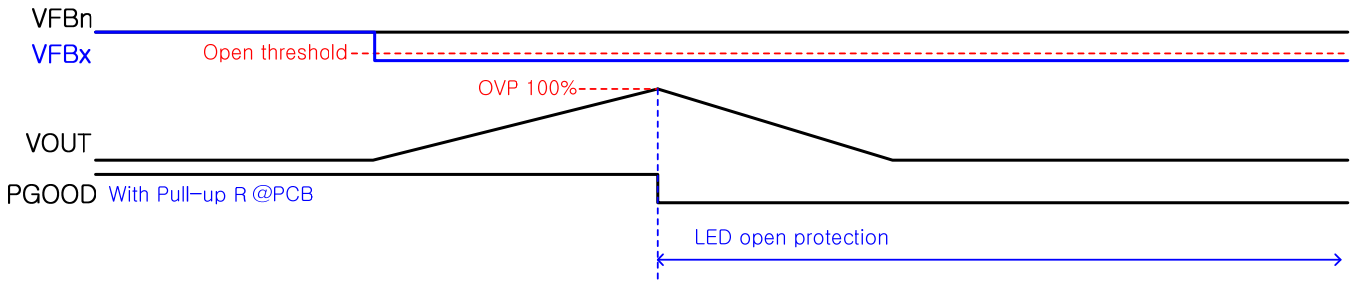
$$VCS\_OCP\_TYP = -0.21255D + 0.56125 = 0.443[V]$$

(4) Find RCS value

$$R_{CS} = 0.8 \times \frac{V_{CS\_OCP\_TYP}}{I_{L\_peak}} = 0.22[\Omega]$$

MX provides '***Design spreadsheet for MAP3242 Ver0.1***' for ease external componts calculation.

LED OPEN PROTECTION



In case the voltage on any of LED current sink pins (FB1~4) is below LED open protection threshold due to LED open during normal operation, the output voltage is boosted up to 100% of OVP level and the MAP3242 automatically excludes the corresponding channel and remaining string(s) will continue operation.

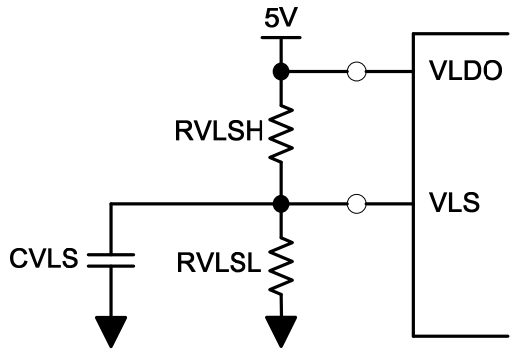
The protection status is latched and the PGOOD pin goes into low impedance state. The PGOOD pin can be cleared by recycling the EN pin or applying a complete power-on-reset(POR).

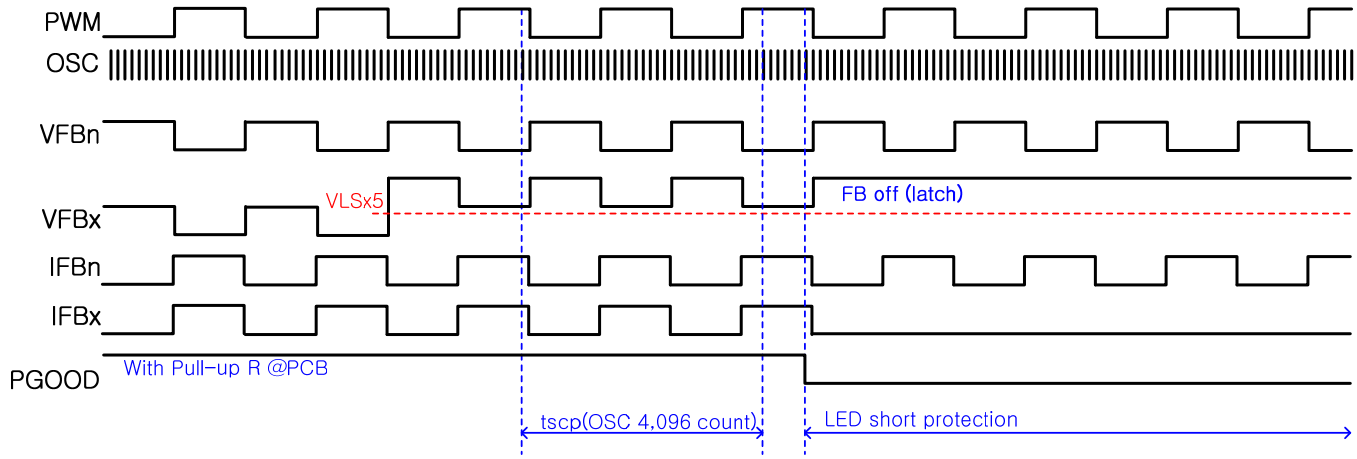
LED SHORT PROTECTION

The MAP3242 can set LED short detection voltage through adjusting VLS pin voltage. Input voltage range of VLS pin is from 1V to 3V and LED short detection voltage on the FB pins is determined by following equation.

$$V_{LED\_SHORT}[V] = 5 \times V_{VLS}$$

Following is a typical application circuit. More than 1nF capacitor is recommendable to bypass spike noise.





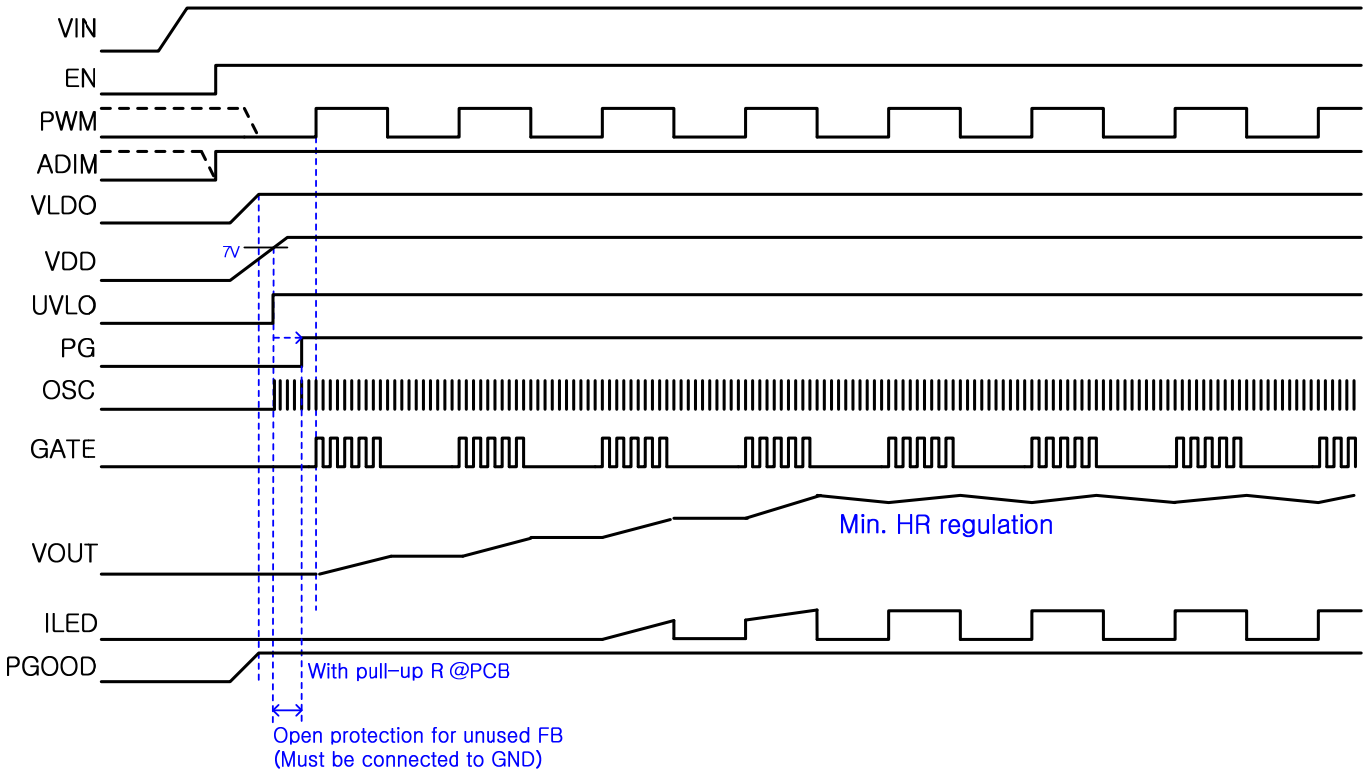
If the voltage at any of the FB1-4 pins exceeds LED short detection voltage due to LED short during normal operation and persists for tscp, the MAP3242 automatically turns off the corresponding channel and remaining channel(s) will continue operation.

The protection status is latched and the PGOOD pin goes into low impedance state. The PGOOD pin can be cleared by recycling the EN pin or applying a complete power-on-reset(POR).

When LED(s) is(are) open on any channel, the output voltage is boosted up to 100% of OVP level and this can cause abnormal LED short protection due to high FB voltage. To avoid this abnormal operation, the MAP3242 disables the LED short protection function with related to Min. FB voltage conditions.

Min. VFB ≥ 2.60V => LED short protection disable
Min. VFB ≤ 2.15V => LED short protection enable

OPERATION TIMING CHART



Each of capacitors which is connected on VLDO and VDD pin begins charing after EN is turned-on and ADIM voltage is set-up. Once the VDD voltage reaches typical 7V, the internal UVLO is released. The MAP3242 checks the initial open FB(s) and excludes corresponding FB(s) from headroom control before internal PG signal is set up. ***The unused FB(s) must be connected to GND.*** Internal controller starts boosting with first PWM input and performs soft-start. After soft-start is end or during soft-start period, the output voltage is boosted up to regulation voltage(total forward voltage of LED bar + FB Voltage) without touching OVP level and the controller performs headroom control.

The PGOOD output becomes valid after the VLDO capacitor is fully charged after EN is turned-on. It depens on the capacitance of VLDO capacitor. It is recommeded that the PGOOD valid time be taken about 1ms after EN is turned-on.

The MAP3242 boosts the output voltage only in condition that VIN is applied and EN, PWM and ADIM is turned-on. And there is no limitation with regard to turn-on sequence. But in case that VIN(input voltage of booster) is applied lastly after EN, PWM and ADIM is turned-on, the start-up current is increased because the output voltage is boosted from 0V.

If the PWM signal remains logic low for over than 16.4ms(1/fsw * 8192) at 500kHz boost switching frequency during normal operation, the controller regards it as dim-zero condition. Because of discharge of output capacitor through the OVP sensing resistors during the dim-zero time, the output voltage getting declined. The MAP3242 performs soft-start as soon as PWM signal rises to boost the output voltage rapidly.

The controller stops switching right after EN is turned-off.

EXTERNAL COMPONENTS SELECTION

Inductor

The inductor value should be decided before system design. Because the selection of the inductor affects the operating mode of CCM(Continuous Conduction Mode) or DCM(Discontinuous Conduction Mode).

The inductance value defining the boundary between DCM and CCM opreation can be calculated as;

$$L_B[H] = \frac{R_O \times D \times (1-D)^2}{2 \times f_{SW}}$$

where, Ro=Vout/Iout

In CCM operation, inductor size should be bigger, even though the ripple current and peak current of inductor can be small. In DCM operation, even ripple current and peak current of inductor should be large while the inductor size can be smaller.

The inductor DC current or input current can be calculated as following equations.

$$I_{IN}[A] = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}}$$

η – Efficiency of the boost converter

Then the duty ratio is,

$$D = \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D}$$

V_D – Forward voltage drop of the output rectifying diode

When the boost converter runs in DCM (L < L_B), it takes the advantages of small inductance and quick transient response. The inductor peak current is,

$$I_{L\_peak\_DCM} = \frac{V_{IN} \times D}{f_{SW} \times L}$$

The converter will work in CCM if L > L_B, generally the converter has higher efficiency under CCM and the inductor peak current is,

$$I_{L\_peak\_CCM} = I_{IN} + \frac{V_{IN} \times D}{2 f_{SW} \times L}$$

Boost MOSFET

The critical parameters for selection of a MOSFET are:

1. Maximum drain current rating, $I_{D(MAX)}$
2. Maximum drain to source voltage, $V_{DS(MAX)}$
3. On-resistance, $R_{DS(ON)}$
4. Gate source chareg Q_{GS} and gate drain chare Q_{GD}
5. Total gate charge, Q_G

The maximum current through the power MOSFET happens when the input voltage is minimum and the output power is maximum. The maximum RMS current through the MOSFET is given by;

$$I_{RMS(MAX)} = I_{IN(MAX)} \times \sqrt{D_{MAX}}$$

The off-state voltage of the MOSFET is approximately equal to the output voltage plus the diode V_f. Therefore, $V_{DS(MAX)}$ of the MOSFET must be rated higher than the maximum output voltage(OVP voltage).

The power losses in the MOSFET can be separated into conduction losses and switching losses. The conduction loss, Pcond, is the I2R loss across the MOSFET. The conduction loss is given by;

$$P_{COND} = R_{DS(ON)} \times {I_{RMS}}^2 \times k$$

where k is the temperature coefficient of the MOSFET.

The switching loss is related to Q_{GD} and Q_{GS1} which determine the commutation time. Q_{GS1} is the charge between the threshold voltage and the plateau voltage when a driver charges the gate, which can be read in the chart of V_{GS} vs. Q_G of the MOSFET datasheet. Q_{GD} is the charge during the plateau voltage. These two parameters are needed to estimate the turn on and turn off loss.

$$P_{SW} = \frac{Q_{GS1} \times R_G}{V_{DR} - V_{TH}} \times V_{DS} \times I_{IN} \times f_{SW} + \frac{Q_{GD} \times R_G}{V_{DR} - V_{PLT}} \times V_{DS} \times I_{IN} \times f_{SW}$$

where V_{TH} is the threshold voltage, V_{PLT} is the plateau voltage, R_G is the gate resistance, V_{DS} is the drain-source voltage, V_{DR} is the drive voltage

The total gate charge, Q_G, is used to calculate the gate drive loss. The expression is

$$P_{DR} = Q_G \times V_{DR} \times f_{SW}$$

Fast switching MOSFETs can cause noise spikes which may affect performance. To reduce these spikes a drive resistor can be placed between GATE pin and the MOSFET gate.

Output Rectifying Diode

Schottky diodes are the ideal choice for MAP3242 due to their low forward voltage drop and fast switching speed. Make sure that the diode has a voltage rating greater that the possible maximum output voltage. The diode conducts current only when the power switch is turned off.

Input Capacitor

In boost converter, input current flows continuously into the inductor; AC ripple component is only proportional to the rate of the inductor charging, thus, smaller value input capacitors may be used. Ensure the voltage rating of the input capacitor is suitable to handle the full supply range.

A capacitor with low ESR should be chosen to minimize heating effects and improve system efficiency.

Output Capacitor

The output capacitor acts to smooth the output voltage and supplies load current directly during the conduction phase of the power switch. Output ripple voltage consists of the discharge of the output capacitor during the FET ton period and the voltage drop due to load current flowing through the ESR of the output capacitor. The ripple voltage is shown in following equation.

$$\Delta V_{OUT} = \frac{I_{OUT} \times D}{C_{OUT} \times f_{SW}} + I_{OUT} \times ESR$$

Assume a ceramic capacitor is used. The minimum capacitance needed for a given ripple can be estimated by following equation.

$$C_{OUT} = \frac{(V_{IN} - V_{OUT}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times \Delta V_{OUT}}$$

Loop Compensation

The MAP3242 controls in current mode. Current mode easily achieves compensation by consisting simple single pole from double pole that LC filer makes at voltage mode. In general, crossover frequency is selected from 1/3 ~ 1/6 range of the switching frequency. If fc is large, there is possibility of oscillation to occur, although time response gets better.

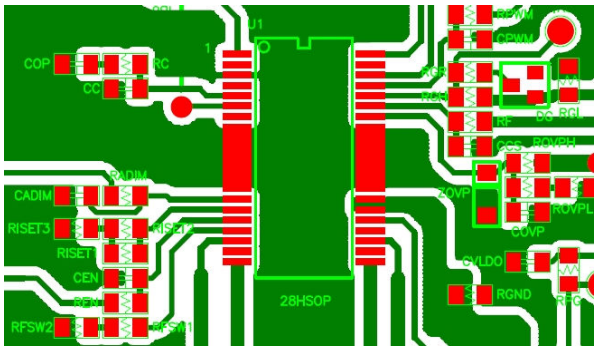
On the other hand, if fc is small, time response will be bad, while it has improved stability, which may cause over shoot or under shoot in abnormal condition.

Layout Consideration

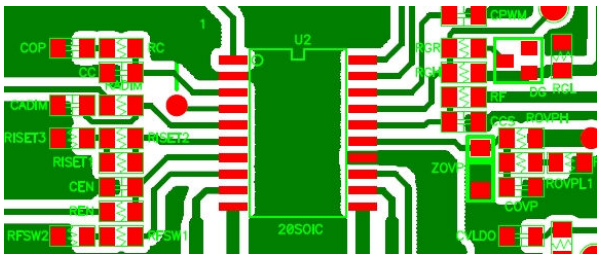
A gate drive signal output from GATE pin becomes noise source, which may cause malfunction of IC due to cross talk if placed by the side of an analog line. It is recommended to avoid placing the output line especially by the side of CS, ADIM, ISET, FSW, OVP, COMP, VLS pins as far as possible.

All the GND of MAP3242, AGND, PGND and LGND(HSOP), are totally seperated internally. For GND layout, it is the best that all the GNDs are seperated to improve noise immunity and avoid unstability. If layout difficulty is high, the second best is tying PGND and LGND(HSOP) and seperating AGND. Followings are GND layout rules for each package.

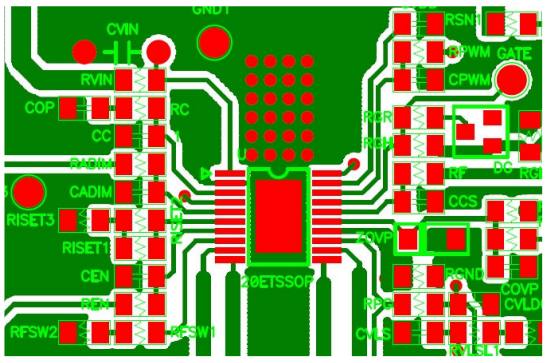
(1) HSOP
- Tie PGND/LGND and seperate AGND
- Heak sink pins(HS1, HS2) shoud be tied to AGND



(2) SOIC
- Separate AGND and PGND



(3) ETSSOP
- Separate AGND and PGND
- Exposed pad shoud be tied to AGND with multiple vias



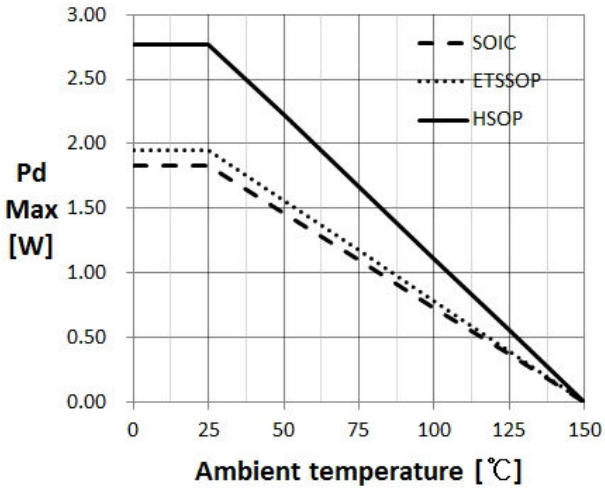
Thermal Consideration

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$Pd_{(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the MAP3242 packages, the derating curve in following graph allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

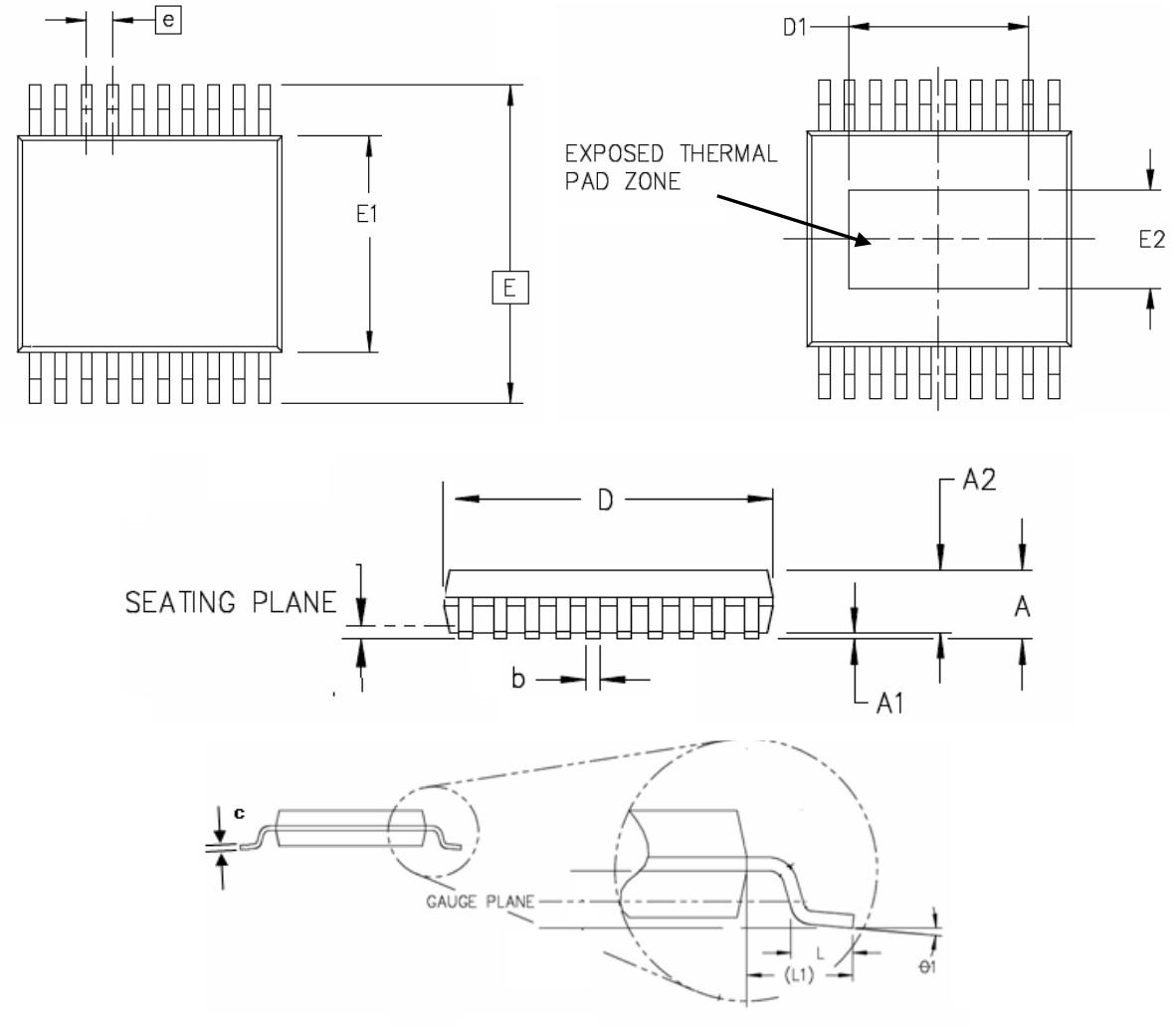


For a typical application, the operation power of the IC can be calculated roughly by;

$$Pd = (V_{IN} \times I_{IN}) + (V_{FB1} \times I_{FB1} + \bullet\bullet\bullet + V_{FB4} \times I_{FB4}) \times D_{PWM}$$

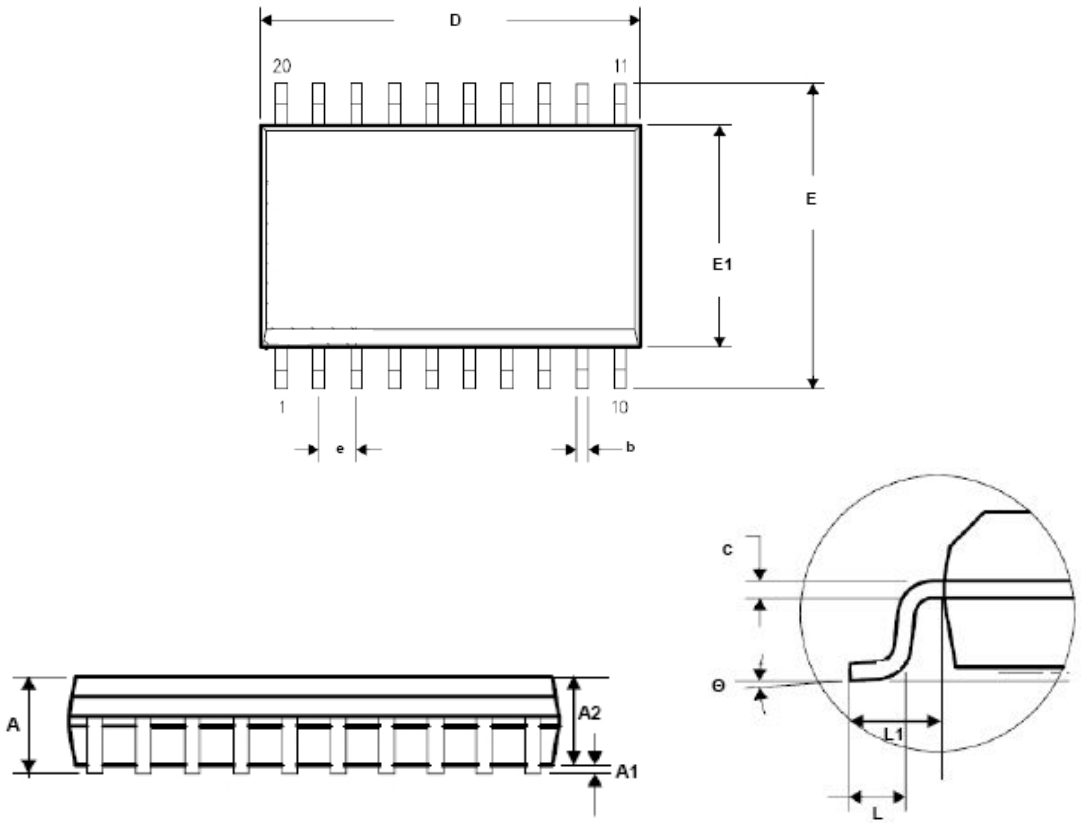
where V_{IN} represents the input voltage at the VIN pin of the IC and I_{IN} represents the current flow into the VIN pin of the IC. D_{PWM} is duty cycle of PWM input signal.

Physical Dimensions



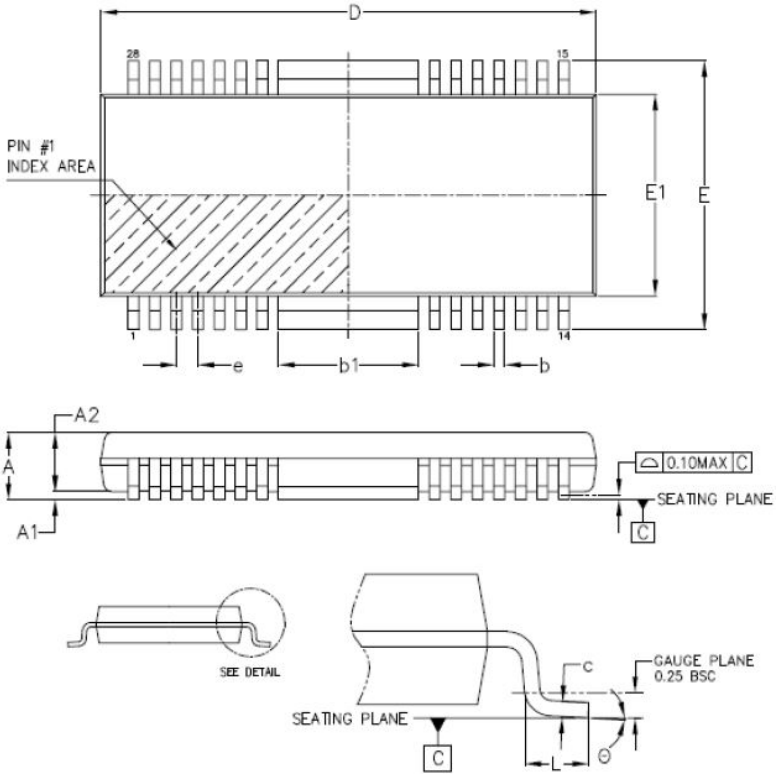
20 Leads E-TSSOP

Symbol	Dimension		
	Min	Norm	Max
A			1.20
A1	0.00		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40		6.60
D1	2.20		
E	6.40 BSC		
E1	4.30		4.50
E2	1.50		
e	0.65 BSC		
L	0.45		0.75
L1	1.00 REF		
θ	0°		8°



20 Leads SOIC

Symbol	Dimension		
	Min	Norm	Max
A			2.65
A1	0.05		0.30
A2	2.05		2.40
b	0.31		0.51
c	0.20		0.33
D	12.54		13.00
E			
E1	7.30		7.70
e		1.27 BSC	
L	0.40		1.27
L1		1.40 REF	
ɵ	0°		8°



28 Leads HSOP

Symbol	Dimension [mm]		
	Min	Nom	Max
A	-	-	2.75
A1	0.00	-	0.30
A2	2.05	-	2.55
b	0.23	-	0.50
b1	5.00	-	5.30
c	0.20	-	0.36
D	17.85	-	18.29
E	10.00	-	10.65
E1	7.30	-	7.70
e	0.80 BSC		
L	0.40	-	1.27
θ	0°	-	8°

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Datasheet Revision History

Date	Version	Changes
2012-04-02	Version 0.0	Initial release
2012-07-11	Version 0.1	Change : ILED Min/Max spec. 50mA~200mA to 90mA~240m - Page 1, 4, 5, 7 Change : ILED accuracy condition spec. I_{LED}=100mA, V_{ADIM}=1.2V to I_{LED}=120mA, V_{ADIM}=1.2V – Page 5 Change : ADIM input voltage spec. 0.6~2.4V to 0.9~2.4V – Page 5, 7 Change : RISET value. 12kΩ to 10 kΩ - Page 7 Change : Min. on-time(t_{ON_MIN}) spec. 15us to 30us – Page 5 Change : Soft-start scheme(Remove OVP60% control) – Page 8, 11 Addition : Abnormal pin voltage protection functions – Page 4, 5 Addition : Power sequence comment – Page 11 Addition : RCS setting detail guide – Page 9 Addition : Boost MOSFET selection guide – Page 12 Addition : PCB layout detail consideration – Page 13 Addition : Thermal consideration – Page 14
2012-09-21	Version 1.0	**<Final Release>** Change : I_{SD}(Shutdown current) spec. Max. 40uA to Typ. 40uA – Page 5 Change : Thermal resistance – Page 4 MAP3242SIRH : Θja - 54℃/W to 68.5℃/W Θjc - 26℃/W to 36.3℃/W MAP3242TERH : Θja - 43℃/W to 64.1℃/W Θjc - 4℃/W to 9.3℃/W Change : Thermal consideration – Page 18 Addition : MAP3242SHRH thermal resistance – Page 4 Addition : PGOOD internal resistance, R_{PGOOD} – Page 6 Addition : Typical operating characteristics – Page 7. 8. 9. 10
2013-06-13	Version 1.1	Change : HSOP28 package dimension – Page 21