Datasheet - MAP3512

2-CH Average Current Control Buck Controller for LED Backlight

General Description

MAP3512 is a 2 channel average-mode current control buck controller for LED backlight application. It does not require an additional dimming MOSFET and utilizes constant off-time control and average current control feedback without external loop compensation or high-side current sensing.

MAP3512 features ±1% CS voltage accuracy and has dedicated analog dimming input up to 3V. It can be powered from 8.5V ~ 18V supply.

MAP3512 provides MOSFET DS short detection(FLT output), SCP, ODP and UVLO.

MAP3512 is available 16 leads SOIC with Halogen-free (fully RoHS compliant).

Features

- 8.5V to 18V Input Voltage Range
- Average-Mode Current Control
- Programmable Constant Off-time
- Up to 3V Analog Dimming Input
- ±1% CS Voltage Accuracy
- Direct PWM Dimming Input
- Fault Output(MOSFET Drain-Source Short)
- Short Circuit Protection
- Over-Duty Protection
- UVLO
- 16 Leads SOIC Package with Halogen-free

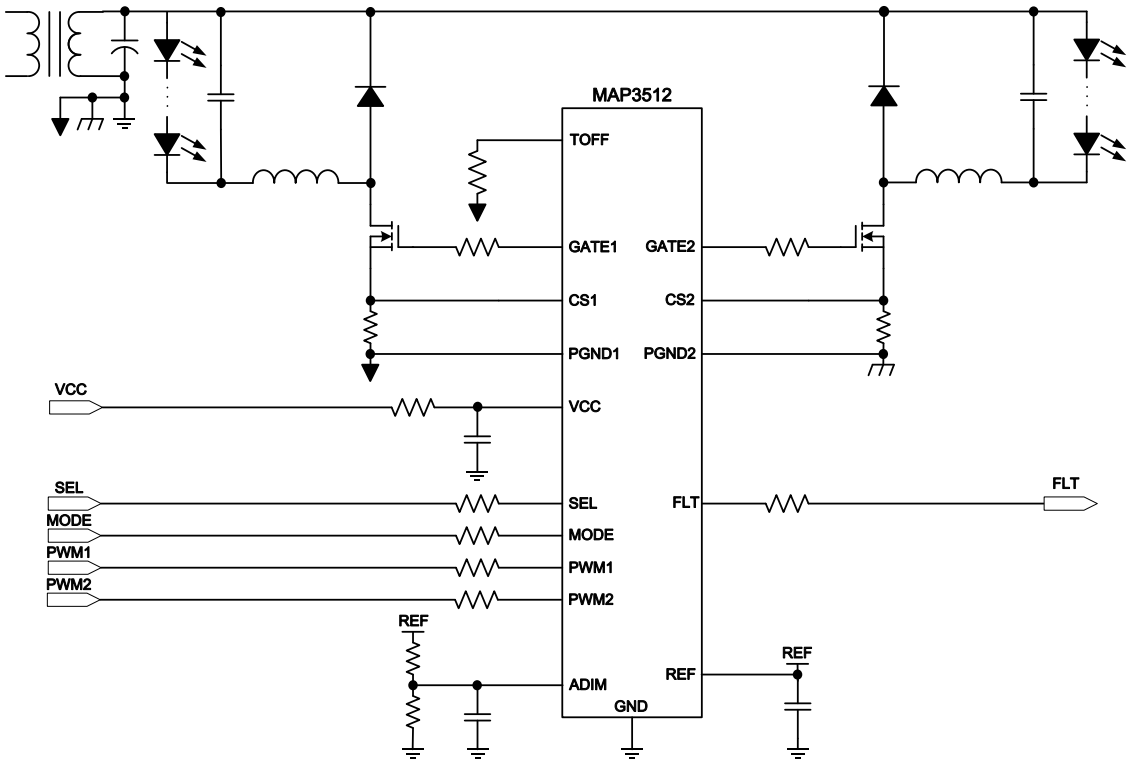
Applications

- High Brightness white LED backlighting for LCD TVs
- General LED lighting applications

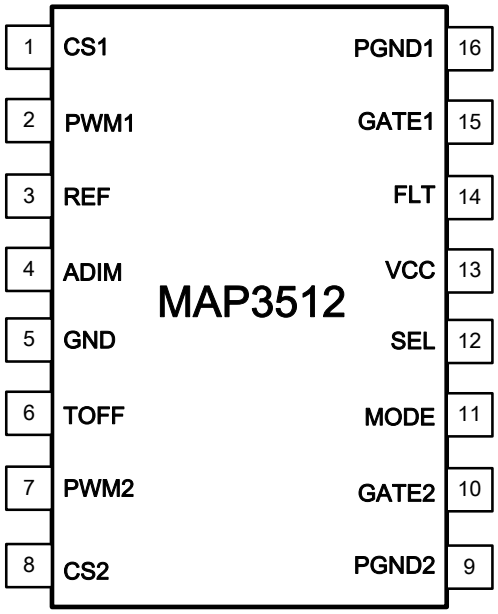
Ordering Information

Part Number	Top Marking	Ambient Temperature Range	Package	RoHS Status
MAP3512SIRH	MAP3512	-40℃ to +85℃	16Leads SOIC	Halogen Free

Typical Application



Pin Configuration



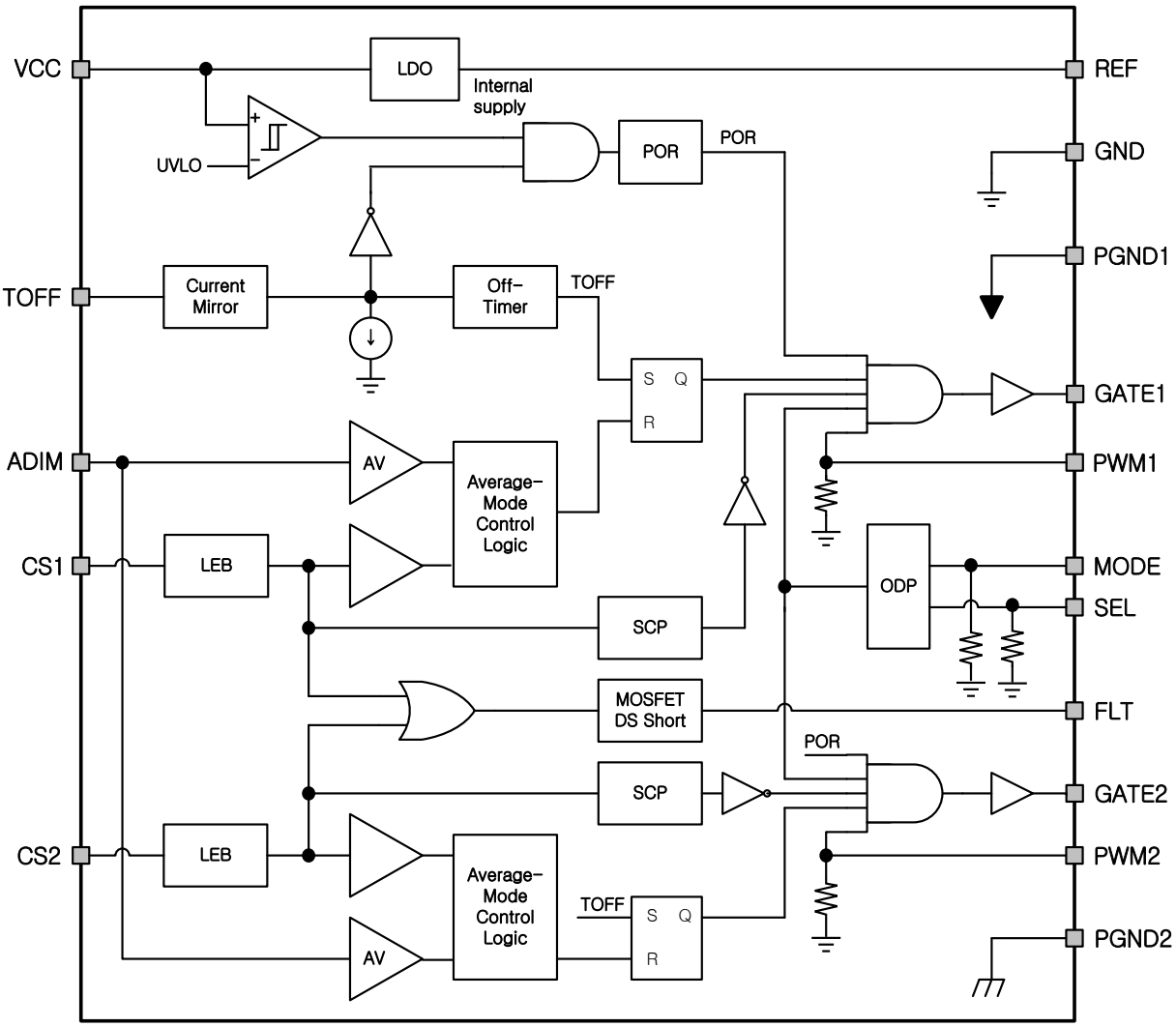
SOIC-16L

Pin Description

8leads SOIC	Name	Description
1	CS1	External current sense for CH1(Note 1).
2	PWM1	PWM signal input for CH1.
3	REF	Internal 5V regulator output. Need 1uF or more external bypass capacitor.
4	ADIM	Setting for LED current thru external DC voltage
5	GND	Ground
6	TOFF	Setting for GATE off-time(Note 2)
7	PWM2	PWM signal input for CH2.
8	CS2	External current sense for CH2(Note 3).
9	PGND2	Power GND for CH2
10	GATE2	GATE driver output to drive external NMOSFET for CH2
11	MODE	Enable logic input for Over-Duty protection. Default logic 'Low' (Note 4)
12	SEL	Logic input for selecting OD1 or OD2 protection. Default logic 'Low' (Note 5)
13	VCC	Power supply input. Need external bypass capacitor
14	FLT	Fault Output
15	GATE1	GATE driver output to drive external NMOSFET for CH1
16	PGND1	Power GND for CH1

Note 1: Connect external resistor to PGND1 to sense the external power MOSFET source current as shown in typical application
Note 2: Connect external resistor to GND to set GATE off-time as shown in typical application
Note 3: Connect external resistor to PGND2 to sense the external power MOSFET source current as shown in typical application
Note 4: Logic 'H' → ODP disable, Logic 'L' or floating → ODP enable
Note 5: Logic 'H' → OD1 protection, Logic 'L' or floating → OD2 protection

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Min	Max	Unit
V_{VCC}, V_{GATE1}, V_{GATE2},V_{PWM1}, V_{PWM2}, V_{MODE}, V_{SEL}	VCC, GATE1, GATE2, PWM1, PWM2, MODE, SEL pins Voltage	-0.3	20	V
V_{CS1}, V_{CS2}, V_{TOFF}, V_{ADIM}, V_{FLT}	CS1, CS2, TOFF, ADIM, FLT pins Voltage	-0.3	5	V
V_{REF}	REF pin Voltage	-0.3	5.5	V
T_{PAD}	Soldering Lead/ Pad Temperature 10sec		300	°C
T_J	Junction Temperature	-40	+150	°C
T_S	Storage Temperature	-65	+150	°C
ESD	HBM on All Pins (Note 2)	-2000	+2000	V
	MM on All Pins (Note 3)	-200	+200	

Note 1: Stresses beyond the above listed maximum ratings may damage the device permanently. Operating above the recommended conditions for extended time may stress the device and affect device reliability. Also the device may not operate normally above the recommended operating conditions. These are stress ratings only.
Note 2: ESD tested per JESD22A-114.
Note 3: ESD tested per JESD22A-115.

Recommended Operating Conditions (Note 1)

Parameter		Min	Max	Unit
V_{Vcc}	Supply Input Voltage	8.5	18.0	V
V_{ADIM}	ADIM Input Range	0.5	3.0	V
T_A	Ambient Temperature (Note 2)	-40	+85	°C

Note 1: Normal operation of the device is not guaranteed if operating the device over outside range of recommended conditions.
Note 2: The ambient temperature may have to be derated if used in high power dissipation and poor thermal resistance conditions.

Package Thermal Resistance (Note 1)

Parameter		θJA	θJC	Unit
MAP3512SIRH	16 Leads SOIC	65.1	25.3	℃/W

Note 1: Multi-layer PCB based on JEDEC standard (JESD51-7)

Electrical Characteristics

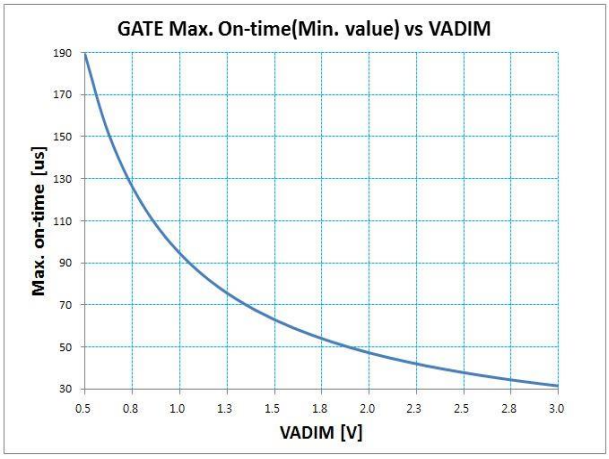
Unless noted, V_{VCC} = 12V, C_{VCC} = 1.0μF, and typical values are tested at T_A = 25°C.

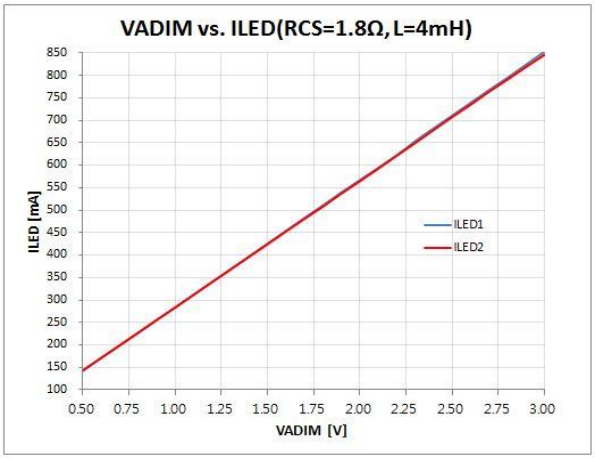
Parameter		Test Condition	Min	Typ	Max	Unit
Supply						
V_{VCC}	Input Voltage Range		8.5		18	V
I_Q	Quiescent Current	V_{PWM} = 5V, V_{CS} = 0V		3.4		mA
V_{UVLO}	Under Voltage Lockout Threshold Voltage on VCC pin	Release threshold(rising V_{VCC})	7.5	8.0	8.5	V
		Lockout hysteresis(falling V_{VCC})	0.5	1.0	1.5	
Reference						
V_{REF}	Voltage on REF pin	I_{REF} = 1mA	4.95	5.00	5.05	V
OFF Timer						
t_{OFF}	GATE1/2 Off-time	R_{TOFF}=52kΩ	4.5	5.0	5.5	us
		R_{TOFF}=104kΩ	9	10	11	
t_{ON_MIN}	Min. On-Time			300		ns
t_{ON_MAX}	Max. On-Time	V_{ADIM} = 3V		37		us
t_{OFF_MIN}	Min. Off-Time			1.2	1.5	us
D_{MAX}	Max. Duty Cycle	V_{ADIM} = 3V, t_{OFF}=1.2us		97		%
GATE Driver						
I_{SOURCE}	GATE1/2 Source Current	$V_{GATE1/2}$ = 0V,	400			mA
I_{SINK}	GATE1/2 Sink Current	$V_{GATE1/2}$ = V_{VCC}=12V	800			mA
t_{RISE}	GATE1/2 Output Rising Time	$C_{GATE1/2}$=1nF, V_{VCC} = 12V		50	85	ns
t_{FALL}	GATE1/2 Output Falling Time	$C_{GATE1/2}$=1nF, V_{VCC} = 12V		25	45	ns
Current Sense & Dimming						
V_{ADIM}	ADIM Input Voltage Range		0.5		3.0	V
A_V	VADIM to CS1/2 Voltage Ratio			0.5075		V/V
$V_{CS1/2}$	CS1/2 Voltage	V_{ADIM} = 0.5V	0.2512		0.2563	V
		V_{ADIM} = 3.0V	1.5073		1.5377	
t_{LEB}	Leading Edge Blanking Time			300		ns
Logic Interface						
$V_{PWM1/2}$	Logic Input Level on PWM1/2 pins	$V_{PWM1/2\_L}$: Logic Low			0.8	V
		$V_{PWM1/2\_H}$: Logic High	2.0			
$R_{PWM1/2}$	Pull-down Resistor on PWM1/2 pins	$V_{PWM1/2}$ = 4V	50	100	150	kΩ
V_{MODE}	Logic Input Level on MODE pin	V_{MODE_L} : Logic Low			0.8	V
		V_{MODE_H} : Logic High	2.0			
R_{MODE}	Pull-down Resistor on MODE pin	V_{MODE} = 4V	50	100	150	kΩ
V_{SEL}	Logic Input Level on SEL pin	V_{SEL_L} : Logic Low			0.8	V
		V_{SEL_H} : Logic High	2.0			
R_{SEL}	Pull-down Resistor on SEL pin	V_{SEL} = 4V	50	100	150	kΩ
Protection						
A_{VSCP}	V_{ADIM} to SCP Voltage Ratio	0.5 <= V_{ADIM} <= 2.5V		1.7		V/V
V_{SCP}	SCP Detection Threshold Voltage on CS1/2 pins	V_{ADIM} = 0.5V	0.8075	0.8500	0.8925	V
		V_{ADIM} = 1.0V	1.6150	1.7000	1.7850	
		V_{ADIM} = 2.5V	4.0375	4.2500	4.4625	
t_{DELAY}	SCP Delay Time			300		ns
$t_{RESTART}$	Restart Time			1		ms
V_{SCPDS}	MOSFET DS Short Detection Threshold Voltage on CS1/2 pins	V_{ADIM} = 0.5V (Note 1, 2)		0.25		V
		V_{ADIM} = 2.5V (Note 1, 2)		1.25		
V_{FLT}	FLT pin High Voltage		4.5		5	V
D_{OD1}	Protection Duty for OD1		55	57	59	%
D_{OD2}	Protection Duty for OD2		35	37	39	%
t_{OD}	Auto-Restart time for OD1/2	V_{MODE} = GND or Floating		200		ms

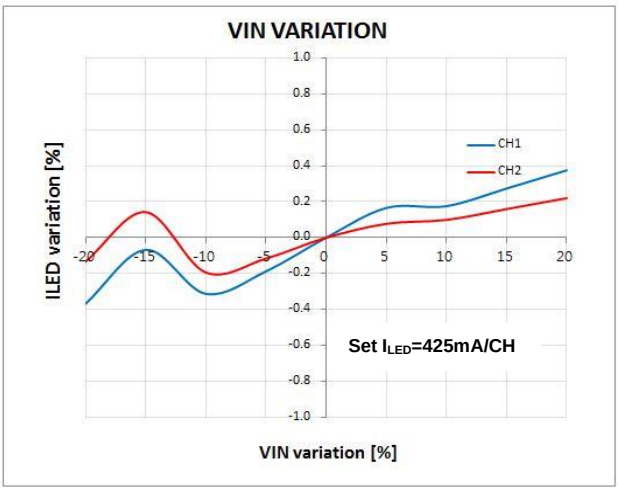
Note 1: These parameters, although guaranteed by design, are not tested in mass production.
Note 2: At start-up(V_{VCC} >= V_{UVLO} release threshold) or V_{PWMx} = Logic 'High' at running

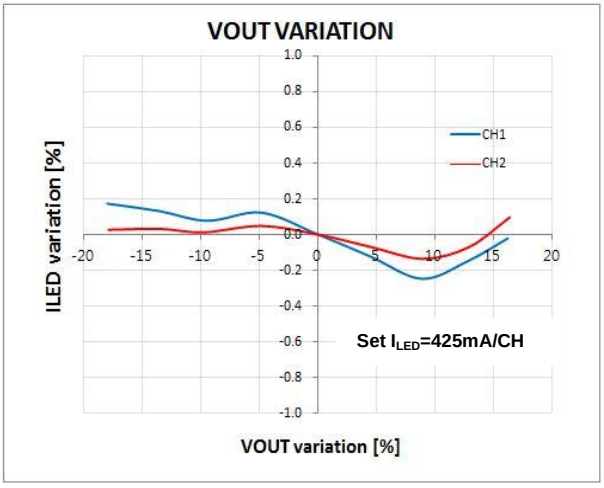
Typical Operating Characteristics

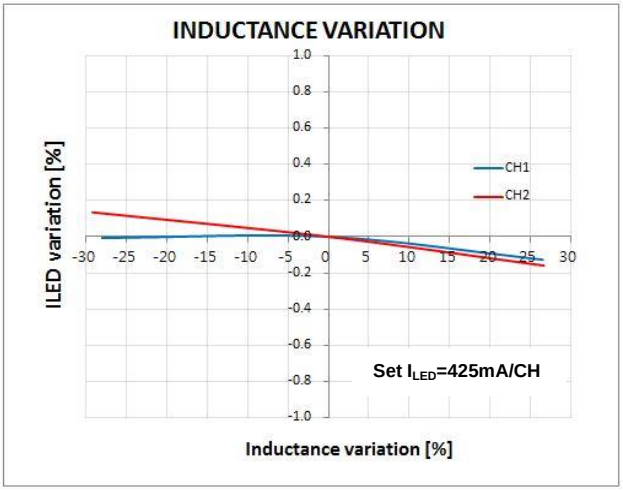
Unless otherwise noted, V_{VCC} = 12V and T_A = 25°C.

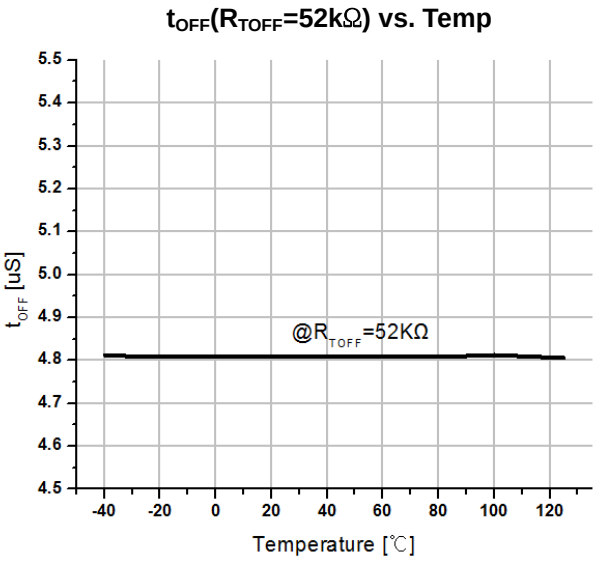








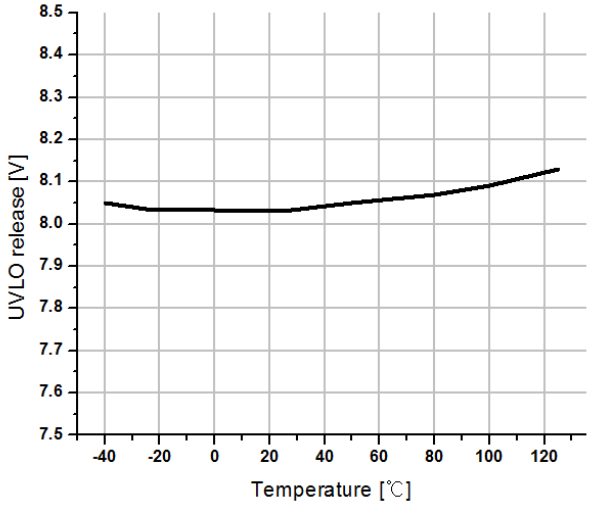




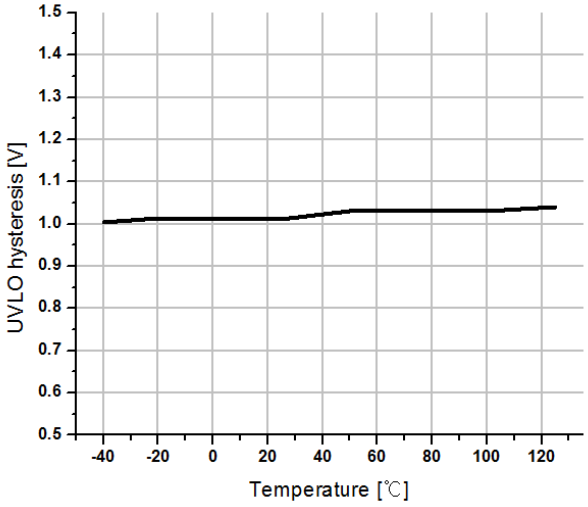
Typical Operating Characteristics

Unless otherwise noted, V_{VCC} = 12V and T_A = 25°C.

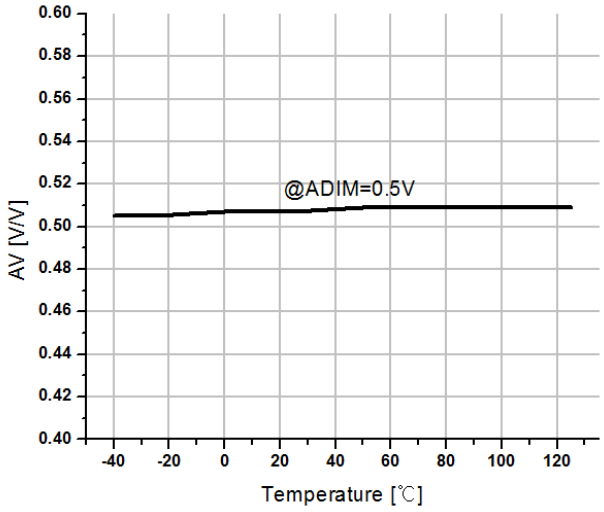
$V_{UVLO(RELEASE)}$ vs. Temp



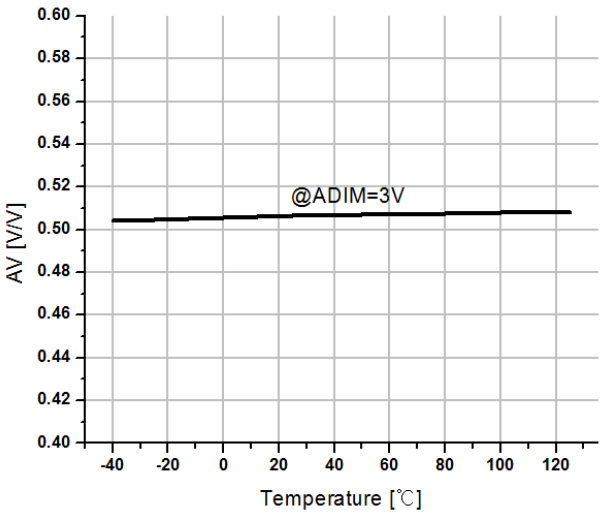
$V_{UVLO(HYS)}$ vs. Temp.



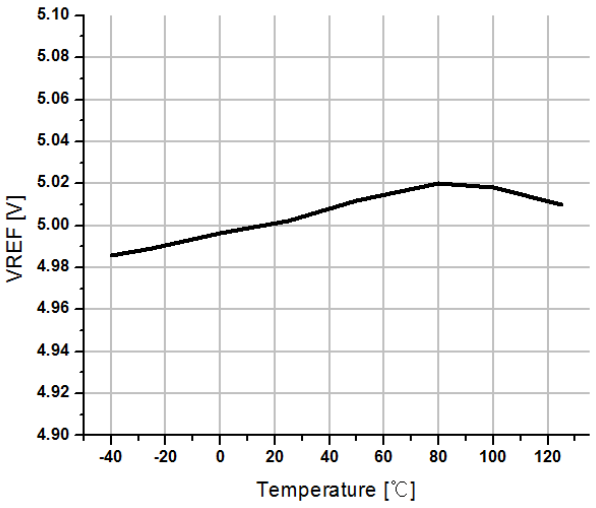
A_V(V_{ADIM}=0.5V) vs. Temp



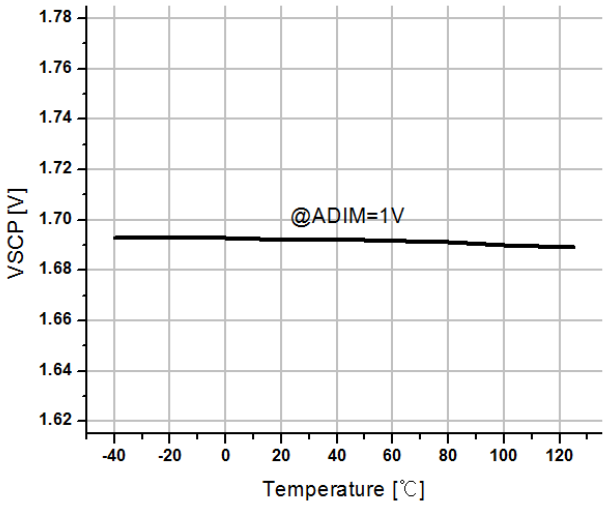
A_V(V_{ADIM}=3.0V) vs. Temp



V_{REF} vs. Temp



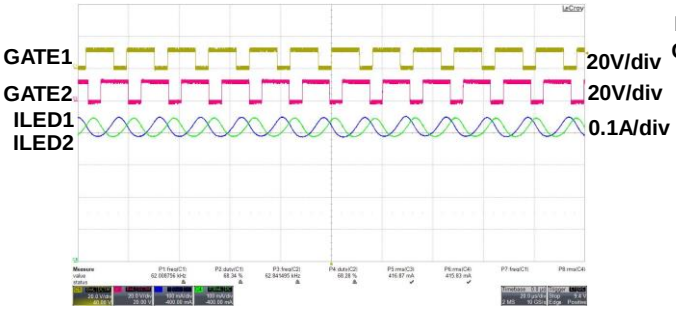
V_{SCP}(V_{ADIM}=1V) vs. Temp



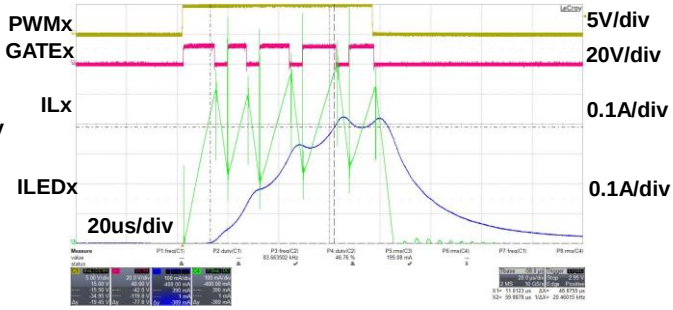
Typical Operating Characteristics

Unless otherwise noted, V_{VCC} = 12V and T_A = 25°C.

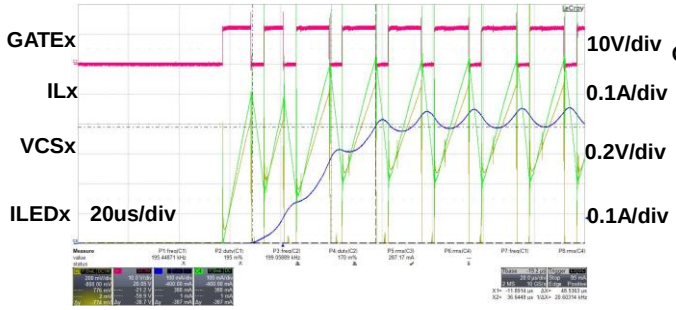
Constant Current Control



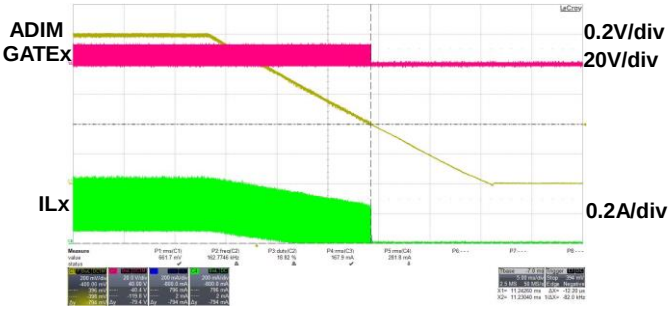
Min. Dimming(C_{OUT}=330nF)



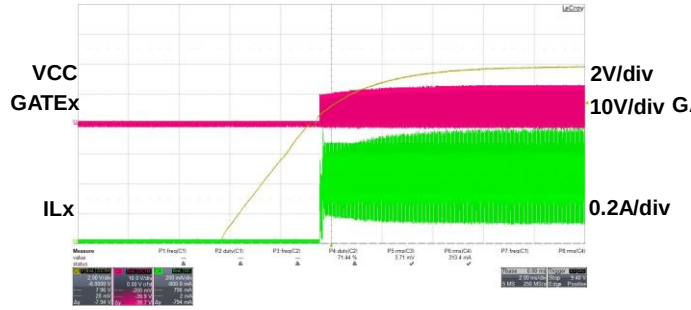
Soft-start(C_{OUT}=330nF)



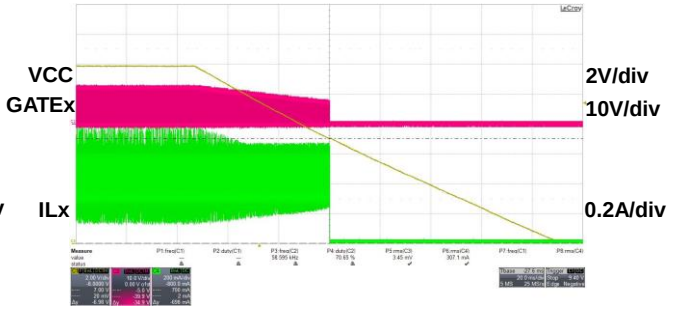
V_{ADIM} Off



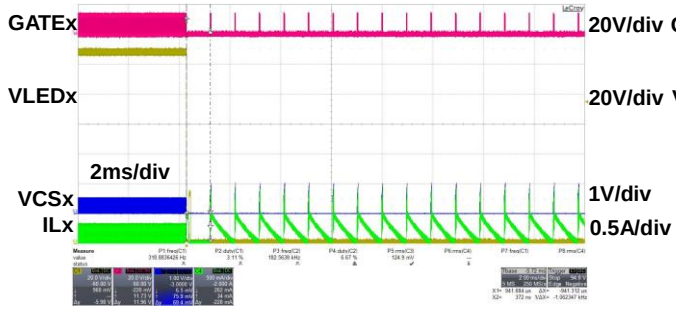
UVLO Release



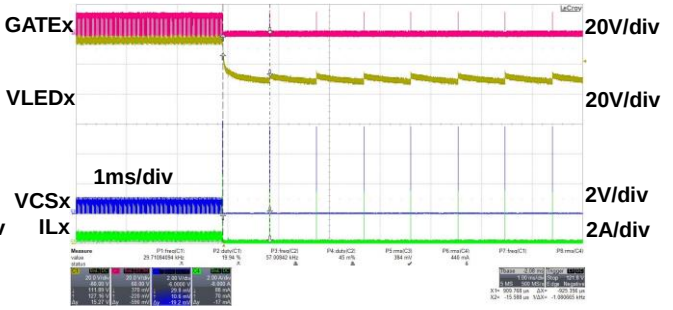
UVLO Lockout



SCP(LED All Short)



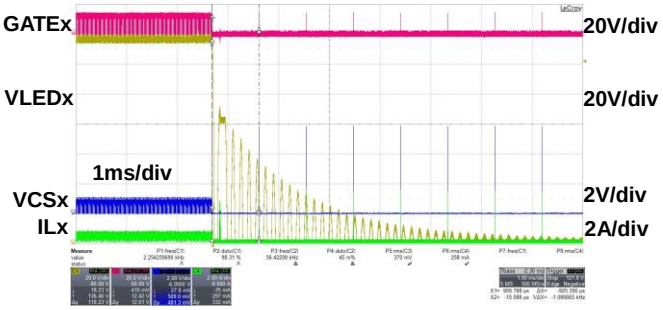
SCP(Inductor Short)



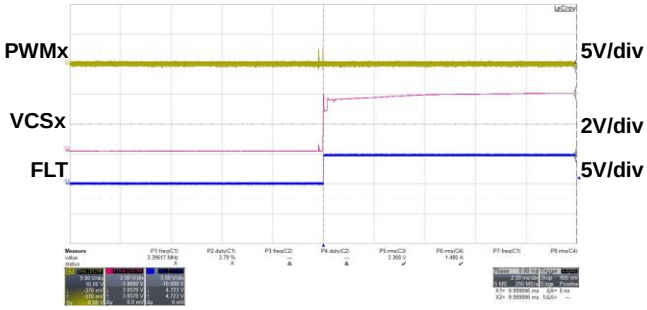
Typical Operating Characteristics

Unless otherwise noted, V_{VCC} = 12V and T_A = 25°C.

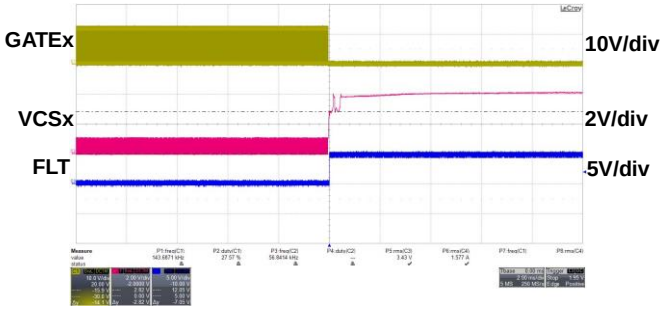
SCP(Catch Diode Short)



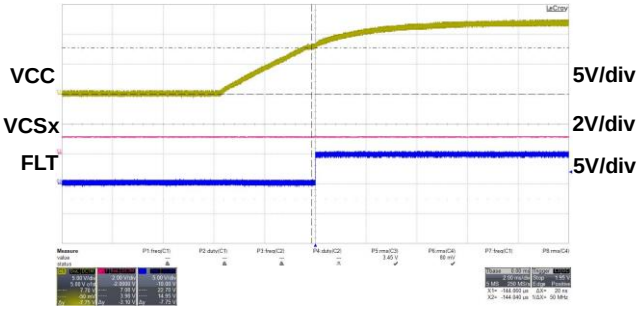
FLT Output(@ PWM Off @ Running)



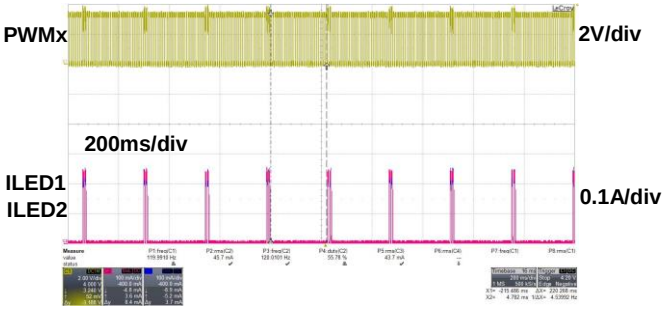
FLT Output(@ PWM On @ Running)



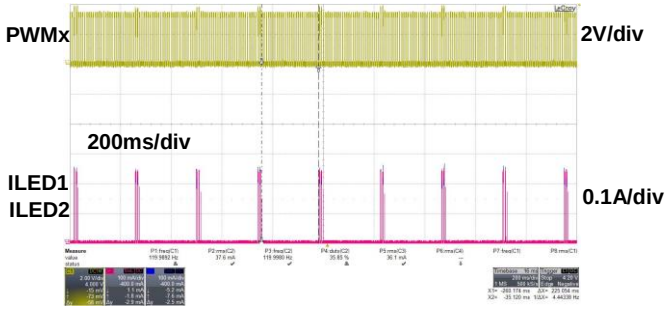
FLT Output(@ PWM On or Off @ Start-up)



OD1 Protection



OD2 Protection



Functional Description

GENERAL DESCRIPTION

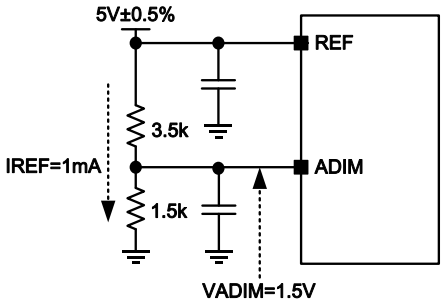
The MAP3512 is a 2-channel low-side single switch control, constant off-time buck controller optimized to LED backlight applications. The IC employs unique average-mode current control architecture which provides precise LED current accuracy. It does not require any external loop compensation or high side current sensing.

The IC operates at continuous conduction mode to reduce output ripple, thus small output capacitor is available. The off time is user adjustable through the selection of an external resistor, this allows the design to be optimized for a given switching frequency range and supports wide range of input voltages.

5V REFERENCE & UVLO

The MAP3512 has a 5V internal LDO to supply internal circuit and provide reference voltage for ADIM voltage input. This LDO is powered up when the VCC voltage rises to UVLO release threshold.

To maintain ±1% voltage accuracy, the current flowing through the resistor divider should be 1mA. It is recommended to use total 5kΩ resistors as shown in following circuit.



If the voltage on the VCC pin falls below UVLO lockout threshold, the device turns-off the GATE output and be reset. This ensures fail-safe operation for VCC input voltage falling.

An 1uF or more bypass capacitor is required on the REF pin for stable operation.

PWM DIMMING

The brightness control of the LEDs is performed by a pulse-width modulation. The GATE output is valid only at PWM on period. This means that the GATE maintains off-state as long as PWM signal is logic low.

Care should be taken to test at low PWM duty-cycle because the output capacitor can affect rising and falling time of LED current due to its charging and discharging time.

RCS SETTING

The current sense resistor value is calculated by following equation.

$$R_{CS} = \frac{0.5075 \times V_{ADIM}}{I_{LED}} [\Omega]$$

RTOFF SETTING

The off-time of the GATE driver is programmed by an external resistor connected between the TOFF pin and ground. Do not leave this pin open. The off-time is calculated by following equation.

$$R_{TOFF} = \frac{0.4 \times t_{OFF}[us] \times 1000}{38.4} [k\Omega]$$

OVER-DUTY PROTECTION

The MAP3512 provides over-duty protection for PWM inputs in case the MODE pin is logic ‘LOW’ or floated. In general, this status is 3D mode in TV applications.

The logic status on the SEL pin decides the protection duty of PWM inputs as following table.

	Available Duty	Duty Protection
OD1	Up to 55%	ODP over 56%
OD2	Up to 35%	ODP over 36%

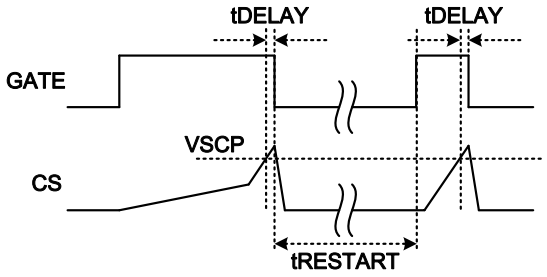
Following table summarizes the relationship between MODE, SEL pins and ODP.

Input	HIGH	LOW or FLOATING
MODE	2D	3D
SEL	OD1	OD2

At the ODP status, the MAP3512 rechecks the protection status at every 200ms. If the error is removed, the IC status will be automatically recovered.

SCP

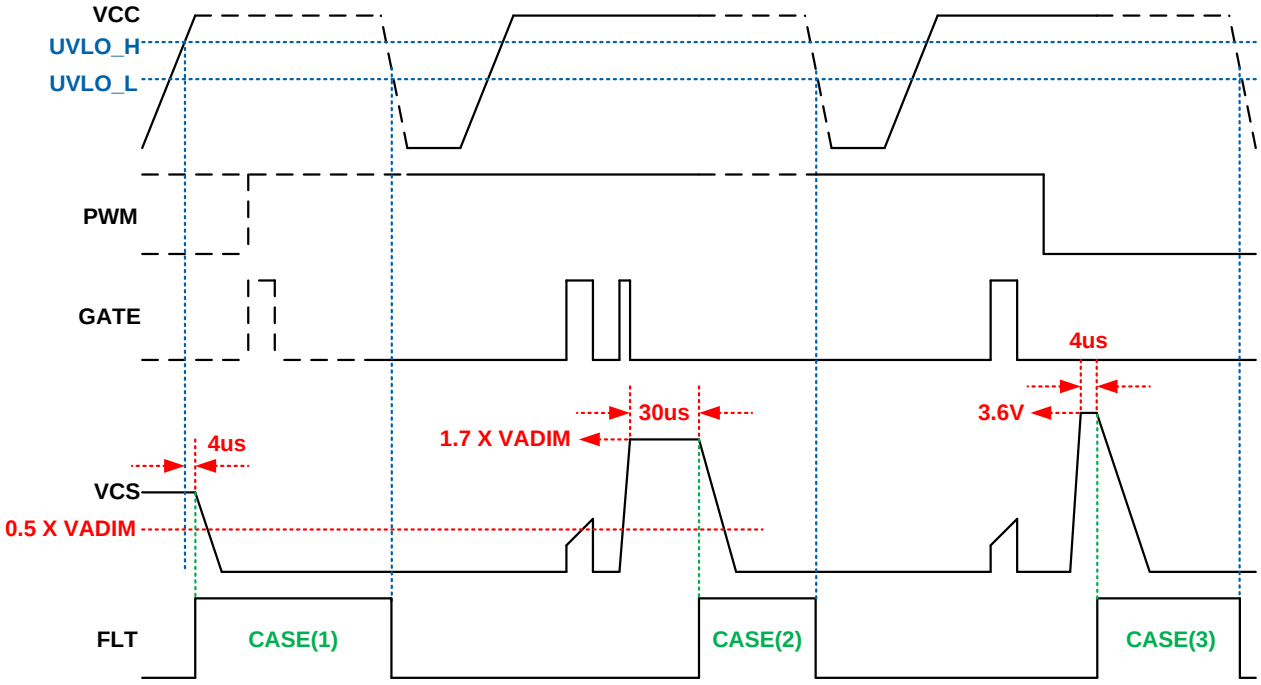
If the CS voltage rises V_{SCP} during normal operation, the MAP3512 turns-off the GATE output after t_{DELAY}(typ. 300ns) time. The auto-restart time is typ. 1ms($t_{RESTART}$). This protects for hard instantaneous short such as catch diode, inductor or LED bar short.



MOSFET D-S Short Detection & FLT Output

In case the following drain-source short events of external MOSFET occur, the FLT pin goes to logic HIGH state immediately. This shuts off the whole system power supply. The protection status is latched and can be cleared by applying a complete power-on-reset(POR).

CASE(1) : At start-up - Regardless of PWM logic state, if VCS is equal or over than 0.5*VADIM and last over 4us. FLT pin voltage goes HIGH level before the first GATE output if PWM is logic HIGH state.
CASE(2) : At dimming(PWM=logic HIGH) - At first, SCP will be occured. Even though the GATE is off-state by SCP, if the CS voltage is equal or over than 1.7*VADIM and last over 30us.
CASE(3) : At other condition(PWM=logic LOW) - If the CS voltage is equal or over than 3.6V and lasts over 4us.



The FLT pin is at logic low state when no error is detected.

External Components Selection

Inductor

In order to achieve accurate constant current output, the MAP3512 is required to operate in Continuous Conduction Mode (CCM) under all operating conditions. In general, the magnitude of the inductor ripple current should be kept as small as possible. If the PCB size is not limited, higher inductance values result in better accuracy of the output current. However, in order to minimize the physical size of the circuit, an inductor with minimum physical outline should be selected such that the converter always operates in CCM and the peak inductor current does not exceed the saturation current limit of the inductor.

The Min. inductance(boundary inductance) which guarantees CCM operation can be calculated as;

$$\Delta I_{LB} = 2I_{OUT}$$

$$L_{MIN} = \frac{V_{OUT}}{\Delta I_{LB}} \times t_{OFF} = \frac{V_{OUT} \times (1-D)}{2 \times I_{OUT} \times f_{SW}}$$

The ripple current through chosen inductor is as following equation;

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}}$$

For example, in case V_{IN}=175V, V_{OUT}=135V, I_{OUT}(I_{LED})=425mA, f_{SW}=50kHz and target ripple current=300mA;

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{135}{175} = 0.77$$

$$L_{MIN} = \frac{V_{OUT} \times (1-D)}{2 \times I_{OUT} \times f_{SW}} = \frac{135 \times (1-0.77)}{2 \times 0.425 \times 50 \times 10^3} = 0.73[mH]$$

The ripple current at L_{MIN} is 2*I_{OUT}=850[mA] and this is too large to use.

For target ripple current(ΔI_L=300mA);

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}} = \frac{(175-135) \times 0.77}{0.3 \times 50 \times 10^3} = 2.05[mH]$$

In this case, the chosen conventional inductor is 2mH/1A.

MOSFET

The power MOSFET is chosen based on maximum stress voltage, maximum peak MOSFET current, total power losses, maximum allowed operating temperature and the driver capability of the MAP3512.

Maximum stress voltage on the power MOSFET (drain-source voltage) for this buck converter is equal to the input voltage. The power MOSFET must be selected with some voltage margin. For example, if the input voltage is maximally 400 V, then maximum drain-source voltage should be 450 V or higher.

Maximum peak MOSFET current was selected in order to calculate the inductor size. Also in this case, the power MOSFET must be chosen with some current margin.

The power losses in the MOSFET can be separated into conduction losses and switching losses. The conduction loss, P_{COND}, is the I2R loss across the MOSFET. The conduction loss is given by;

$$P_{COND} = R_{DS(ON)} \times I_{RMS}{}^2 \times k$$

Where, k is the temperature coefficient of the MOSFET.

The switching loss is related to Q_{GD} and Q_{GS1} which determine the commutation time. Q_{GS1} is the charge between the threshold voltage and the plateau voltage when a driver charges the gate, which can be read in the chart of V_{GS} vs. Q_G of the MOSFET datasheet. Q_{GD} is the charge during the plateau voltage. These two parameters are needed to estimate the turn on and turn off loss.

$$P_{SW} = \frac{Q_{GS1} \times R_G}{V_{DR} - V_{TH}} \times V_{DS} \times I_{IN} \times f_{SW} + \frac{Q_{GD} \times R_G}{V_{DR} - V_{PLT}} \times V_{DS} \times I_{IN} \times f_{SW}$$

where V_{TH} is the threshold voltage, V_{PLT} is the plateau voltage, R_G is the gate resistance, V_{DS} is the drain-source voltage, V_{DR} is the drive voltage

The total gate charge, Q_G, is used to calculate the gate drive loss. The expression is

$$P_{DR} = Q_G \times V_{DR} \times f_{SW}$$

Fast switching MOSFETs can cause noise spikes which may affect performance. To reduce these spikes a drive resistor can be placed between GATE pin and the MOSFET gate.

Catch Diode

The catch diode is chosen based on its maximum stress voltage, its maximum peak current and total power losses. The power losses are lower for a larger duty cycle and vice-versa, because the diode is opened (connected) during off-time.

Maximum voltage stress across the diode is equal to the input voltage V_{IN}, and therefore the power diode must be selected with some voltage margin. For example, if the input voltage is maximally 400 V, then maximum repetitive peak reverse voltage (V_{RRM}) should be 450 V or higher.

Maximum peak diode current is selected in order to calculate the inductor size. Also in this case, the catch diode must be selected with some current margin.

The voltage drop across the diode in a conducting state is primarily responsible for the losses in the diode. The power dissipated by the diode can be calculated as the product of the forward voltage and the output load current for the time that the diode is conducting. The switching losses which occur at the transitions from conducting to non-conducting states are very small compared to conduction losses and are usually ignored. The power dissipated by the catch diode is given by:

$$P_D = V_D \times I_O \times (1 - D)$$

Where, V_D is the forward voltage drop of the catch diode.

Input Capacitor

Select the input capacitor to ensure that the input voltage ripple is within a desired range (1% to 5% of the input bus voltage). The input capacitor is usually electrolytic and its ESR dominates its impedance.

A 4.7μF to 22μF electrolytic capacitor will usually suffice.

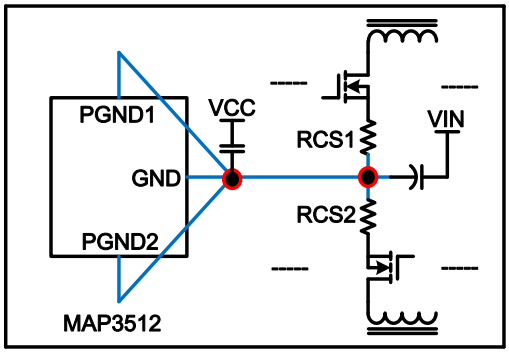
Output Capacitor

Selecting a suitable capacitor can reduce LED current ripple and increase LED life-time. Note that having too large of a capacitance will cause the LED current to respond slowly. The typical value of the capacitor is 0.33μF.

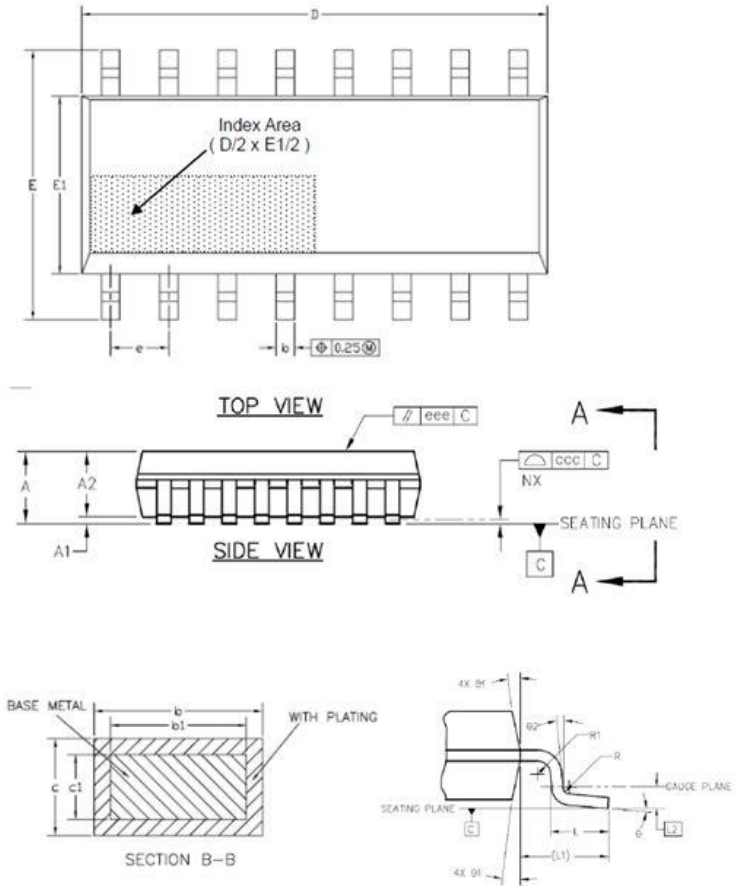
PCB LAYOUT GUIDE

A gate drive signal outputs from GATE1 and GATE2 pins become noise source, which may cause malfunction of IC due to cross talk if placed by the side of an analog line. It is recommended to avoid placing the output line especially by the side of CS1, CS2, ADIM and TOFF pins as far as possible.

For GND layout, PGND1, PGND2 and GND pins should be connected as Y-connection from the VCC capacitor GND and the GNDs of current sense resistors should be separated and tied at input capacitor GND as following figure to improve noise immunity and avoid cross-talk between channels.



Physical Dimensions



Symbol	Min	Nom	Max
A	-	-	1.80
A1	0.05	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
b1	0.28	-	0.48
C	0.10	-	0.30
c1	0.10	-	0.23
D	9.70	-	10.10
E	5.70	-	6.30
E1	3.75	-	4.15
e	1.14	1.27	1.40
L	0.40	-	1.27
L1	1.04 REF		
L2	0.25 BSC		
R	0.07	-	-
R1	0.07	-	-
θ	0°	-	8°
θ1	0°	-	15°

16 **Leads SOIC**

MagnaChip Semiconductor Ltd.
891, Daechi-Dong, Kangnam-Gu, Seoul, 135-738 Korea
Tel : 82-2-6903-3451 / Fax : 82-2-6903-3668 ~9
www.magnachip.com

Datasheet Revision History

Date	Version	Changes
2014-11-07	Version 1.0	Initial release
2015-07-03	Version 1.1	<Change> REF pin voltage Max. rating : 5V → 5.5V – Page 4