Preliminary Datasheet - MAP3702

600kHz 1-CH White LED Driver for Mobile Backlight

General Description

MAP3702 is an 1-channel LED driver optimized for LED backlight application targeting mobile LCD module.

MAP3702 uses 40V absolute Max. rating boost MOSFET internally and input voltage is ranged from 2.7V ~ 5.5V. The boost converter runs at 600kHz fixed switching frequency. The default LED current is set by external resistor and the feedback voltage is regulated up to 200mV.

Two dimming controls are available; 32 dimming steps using the SWIRE interface and filtered-PWM control.

MAP3702 has various protections like over-current, output over-voltage protection for open-LED faults, thermal shutdown and UVLO.

MAP3702 is available 2mm X 2mm 6 leads DFN package with Halogen-free (fully RoHS compliant).

Features

- 2.7V to 5.5V input voltage range
- 37V open LED protection
- Up to 90% Efficiency
- 600kHz switching frequency
- Internal boost MOSFET
- 200mV reference voltage with 2% accuracy
- Flexible 32-steps single-wire digital and filtered-PWM brightness control
- Bulilt-in soft-start
- UVLO
- Thermal shutdown
- 2mmX 2mm 6-pin DFN package

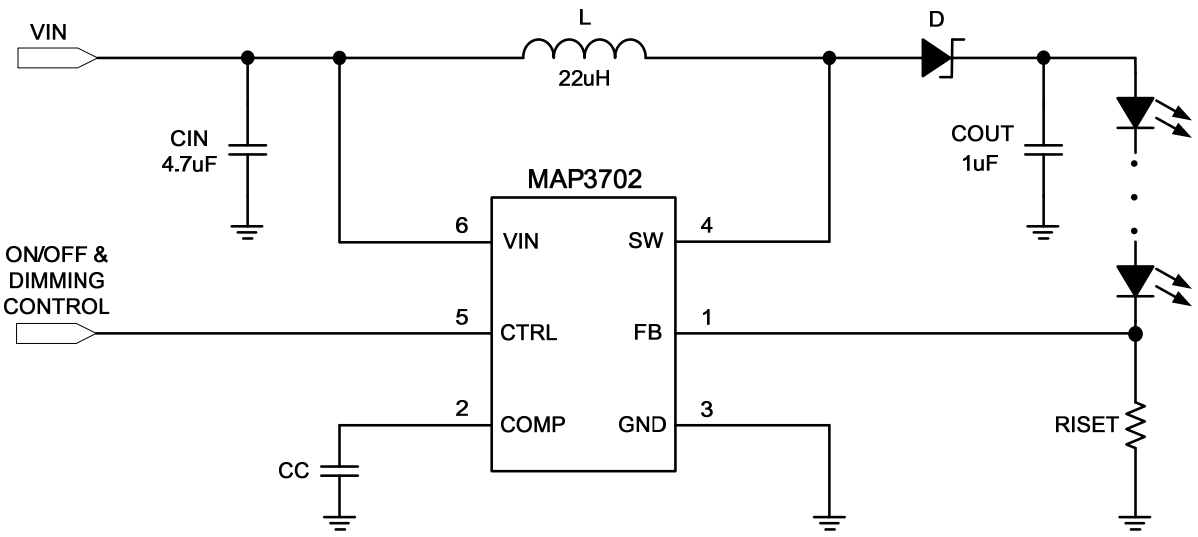
Applications

- Mobile hansets
- Tablets
- Dititial still cameras(DSC)

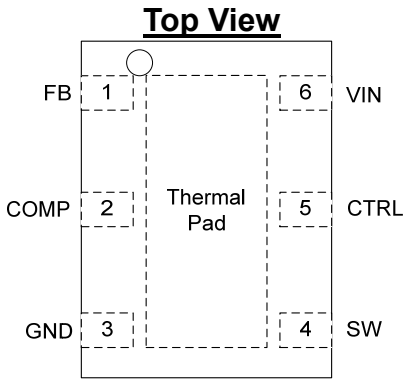
Ordering Information

Part Number	Top Marking	Ambient Temperature Range	Package	RoHS Status
MAP3702DFRH	MAP3702	-40℃ to +85℃	2.0mmX2.0mm DFN	Halogen Free

Typical Application



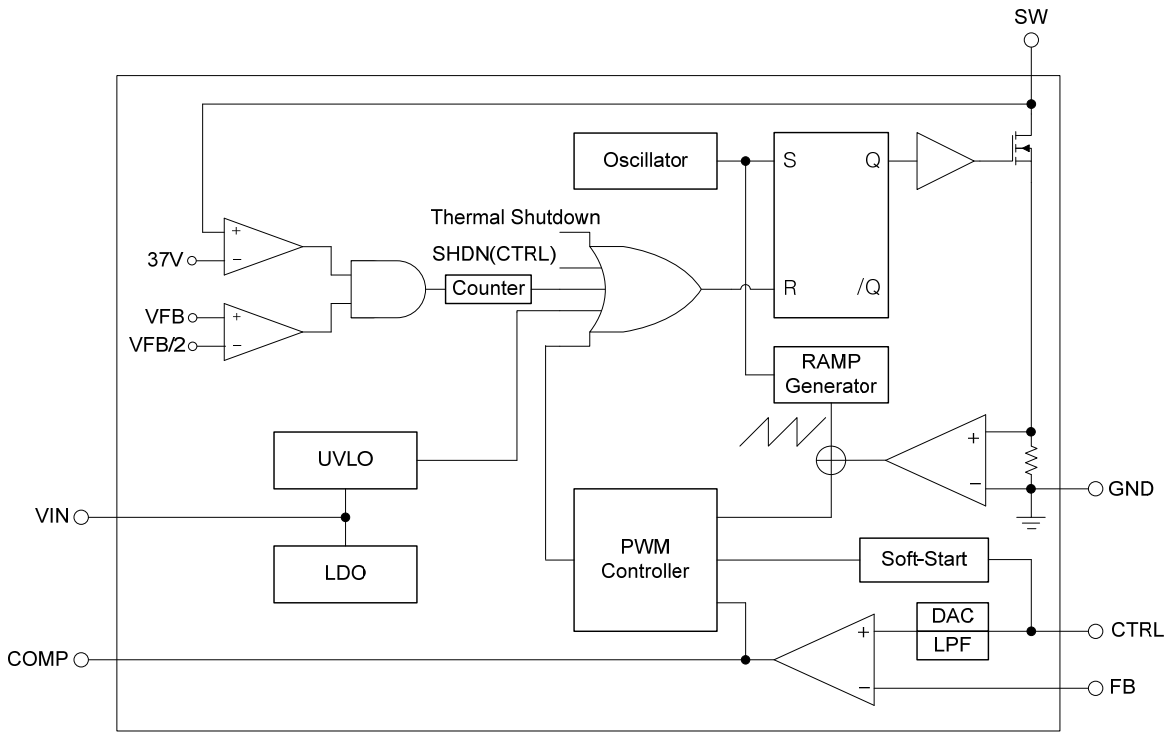
Pin Configuration



Pin Description

Name	No.	Description
FB	**1**	Feedback pin for LED current. Connect an 1% sense resistor from FB to GND.
COMP	**2**	Output of internal error amplifier. Connect an external capacitor to compensate the converter.
GND	**3**	Ground
SW	**4**	Internal boost MOSFET drain. Connect power inductor and Schottky diode as seen in typical application diagram
CTRL	**5**	Multi-functional pin which can be used for enable/shutdown control, SWIRE digital and filtered-PWM dimming.
VIN	**6**	Power supply input. Need external input capacitor.
Thermal Pad	**-**	Connected to Ground by multiple vias for Heat-sinking Purposes. Not connected internally.

Functional Block Diagram



Absolute Maximum Ratings(Note 1)

Symbol	Parameter	Min	Max	Unit
V_{VIN}	Supply Voltages on VIN pin	-0.3	5.5	V
V_{CTRL}	Voltages on CTRL pin	-0.3	5.5	V
V_{FB}, V_{COMP}	Voltage on FB and COMP pin	-0.3	3	V
V_{SW}	Voltage on SW pin	-0.3	40	V
T_J	Operating Junction Temperature Range	-40	150	℃
T_S	Storage Temperature Range	-65	150	℃
ESD	HBM on All Pins (Note 2)	-2000	+2000	V
	MM on All Pins (Note 3)	-200	+200	

Note 1: Stresses beyond the above listed maximum ratings may damage the device permanently. Operating above the recommended conditions for extended time may stress the device and affect device reliability. Also the device may not operate normally above the recommended operating conditions. These are stress ratings only.
Note 2: ESD tested per JESD22A-114.
Note 3: ESD tested per JESD22A-115.

Recommended Operating Conditions (Note 1)

Parameter		Min	Max	Unit
V_{VIN}	Supply Input Voltage	2.7	5.5	V
V_{OUT}	Output Voltage	VIN	38	V
f_{PWM}	PWM dimming input frequency	5	100	kHz
T_A	Ambient Temperature (Note 2)	-40	+85	°C

Note 1: Normal operation of the device is not guaranteed if operating the device over outside range of recommended conditions.
Note 2: The ambient temperature may have to be derated if used in high power dissipation and poor thermal resistance conditions.

Package Thermal Resistance (Note 1)

Parameter	θJA	Unit
2mm X 2mm 6 leads DFN	88.8	℃/W

Note 1: Measured on JESD51-7, Multi-layer PCB with multiple vias.

Electrical Characteristics

Unless noted, V_{IN} = 3.6V, C_{IN} = 4.7μF, and typical values are tested at T_A = 25°C.

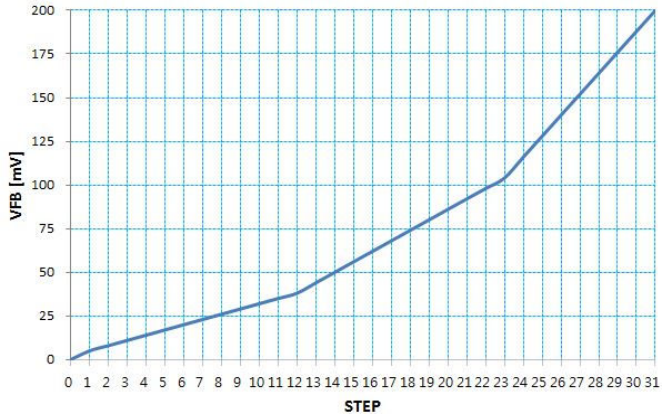
Parameter		Test Condition	Min	Typ.	Max	Unit
General Input Output						
V_{VIN}	Input Voltage Range on VIN pin		2.7		5.5	V
I_Q	Operating Quiescent Current	PWM switching with no load			1.8	mA
I_{GND}	Ground Pin Current in Shutdown	V_{CTRL}=GND, V_{VIN} = 4.2 V			1	uA
V_{CTRL}	Logic Input Level on CTRL pin	V_{CTRL_L} : Logic Low			0.4	V
		V_{CTRL_H} : Logic High	1.2			
R_{CTRL}	Pull-down Resistor on CTRL pin		400	800	1600	kΩ
t_{SHDN}	Shutdown Pulse Width on CTRL pin	CTRL pin Logic High to Low	2.0			ms
t_{WIN}	SWIRE Detection Window Time	Measured from CTRL pin High	1			ms
t_{DET}	SWIRE Detection Time	CTRL pin Logic Low	260			us
t_{DELAY}	SWIRE Detection Delay		100			us
t_{START_DELAY}	Start-up Delay Time, Both SWIRE and Filtered-PWM mode	(Note 1)		4		ms
V_{UVLO}	UVLO Threshold Voltage on VIN pin	Lockout Voltage		2.2	2.52	V
		Hysteresis		100		mV
Oscillator and Power Switch						
$R_{DS(ON)}$	N-channel MOSFET on-resistance	V_{VIN} = 3.6 V		0.3	0.6	Ω
		V_{VIN} = 3.0 V			0.7	
I_{LEAK}	N-channel MOSFET Leakage Current	V_{SW} = 35 V, T_A = 25°C			1	uA
f_{SW}	Oscillator Frequency	3.0V ≤ V_{VIN} ≤ 5.5V	500	600	700	kHz
D_{MAX}	Max. Duty Cycle on SW pin	V_{FB} = 100 mV	90	93		%
T_{min_on}	Min. ON Pulse Width on SW pin			40		ns
FB Voltage Control						
V_{FB}	Voltage Feedback Regulation Voltage	V_{FB} = 200 mV	196	200	204	mV
		V_{FB} = 50 mV	47	50	53	
		V_{FB} = 20 mV	17	20	23	
t_{STEP}	V_{FB} Ramp-up Time	Between Each step, f_{SW} = 1.2MHz		213		us
I_{SINK}	COMP pin Sink Current			100		uA
I_{SOURCE}	COMP pin Source Current			100		uA
G_{EA}	Error Amplifier Transconductance		400	550	700	umho
R_{EA}	Error Amplifier Output Resistance			1.4		MΩ
f_C	Error Amplifier Crossover Frequency	C_{COMP}=5pF		3.18		MHz
t_{FB}	V_{FB} Filter Time Constant (Note 1)			180		us
Protection						
I_{LIM}	N-Channel MOSFET Current Limit	D = D_{MAX}	0.56	0.7	0.84	A
I_{LIM_START}	Start-up Current Limit	D = D_{MAX}		0.4		A
t_{LIM_START}	Time Step for Start-up Current Limit			5		ms
V_{OVP}	Open LED Protection Threshold on SW pin		35.5	37		V
T_{SD}	Thermal Shutdown Temperature	Shutdown Temperature		160		℃
		Hysteresis, ΔT_{SD}		15		
SWIRE Timing						
t_{START}	Start Time of Program Stream		2			us
t_{EOS}	End Time of Program Stream		2		360	us
t_{H_LB}	High Time Low bit	Logic 0	2		180	us
t_{L_LB}	Low Time Low bit	Logic 0	2* t_{H_LB}		360	us
t_{H_HB}	High Time High bit	Logic 1	2* t_{L_HB}		360	us
t_{L_HB}	Low Time High bit	Logic 1	2		180	
V_{ACKNL}	Acknowledge Output Voltage Low	Open drain, R_{pullup} =15 kΩ to VIN			0.4	V
$t_{VALACKN}$	Acknowledge Valid Time				2	us
tACKN	Duration of Acknowledge Condition				616	us

Note 1: These parameters, although guaranteed by design, are not tested in mass production.

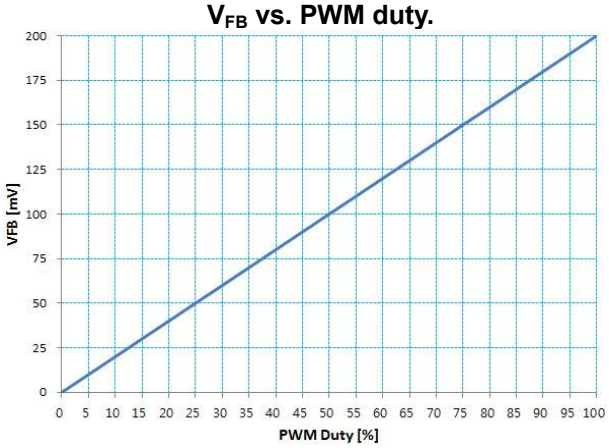
Typical Operating Characteristics

Unless otherwise noted, V_{IN} = 3.6V, Cin=4.7uF, Cout=1uF, RISET=10Ω and T_A = 25°C.

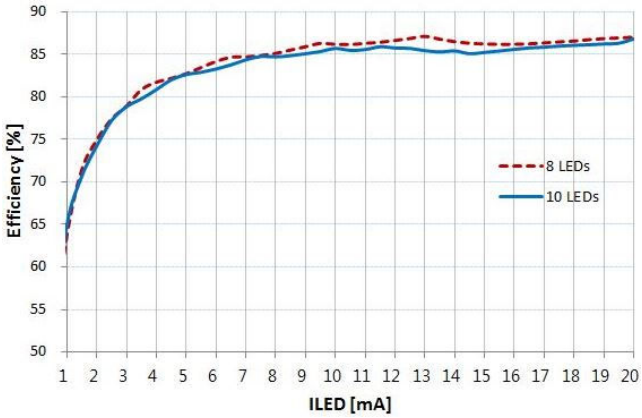
V_{FB} vs. STEP



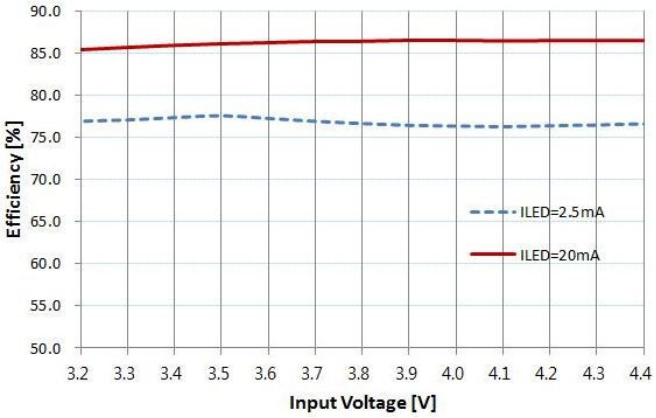
V_{FB} vs. PWM duty.



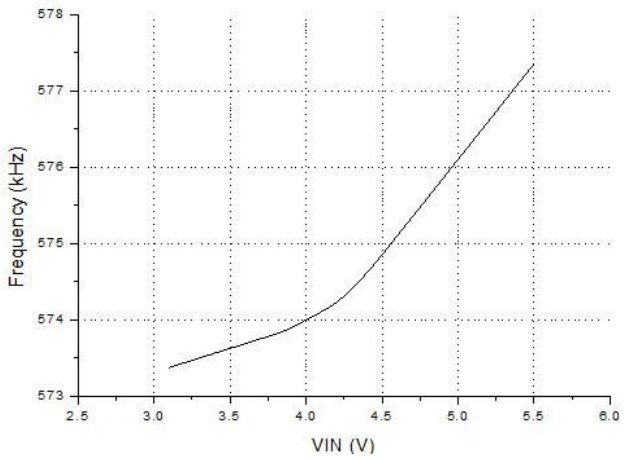
Efficiency vs. LED Current



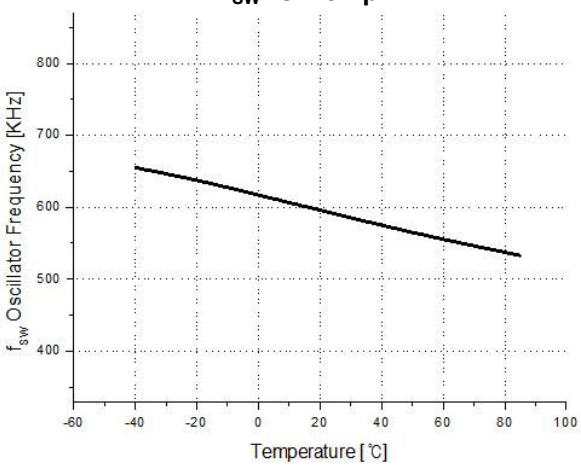
Efficiency vs. V_{IN}(10 LEDs)



f_{SW} vs. V_{IN}



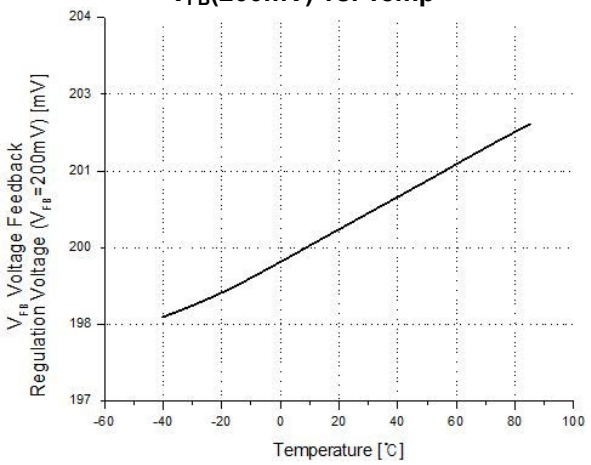
f_{SW} vs. Temp



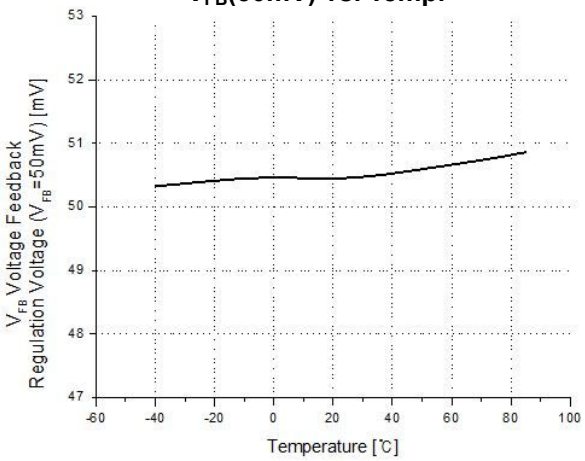
Typical Operating Characteristics

Unless otherwise noted, V_{IN} = 3.6V, Cin=4.7uF, Cout=1uF, RISET=10Ω and T_A = 25°C.

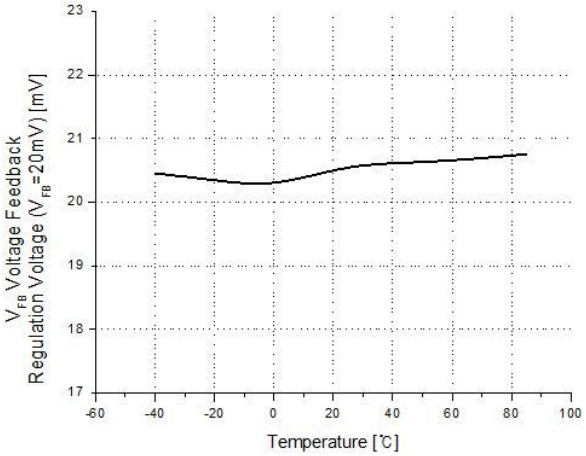
V_{FB}(200mV) vs. Temp



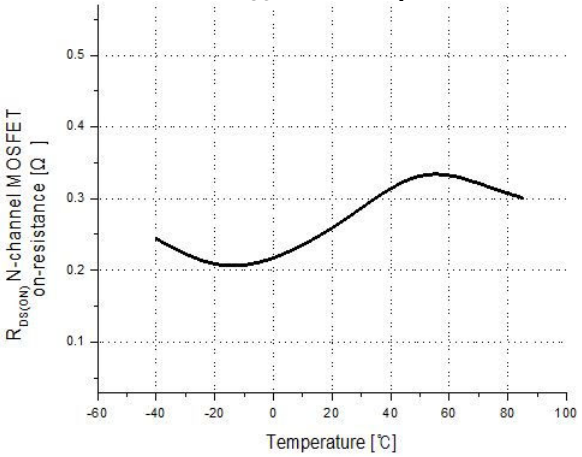
V_{FB}(50mV) vs. Temp.



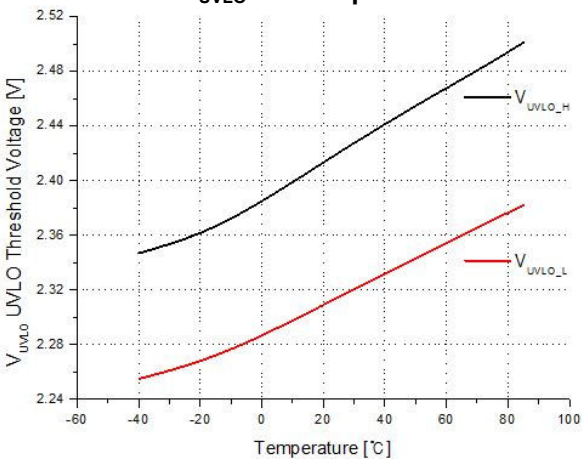
V_{FB}(20mV) vs. Temp



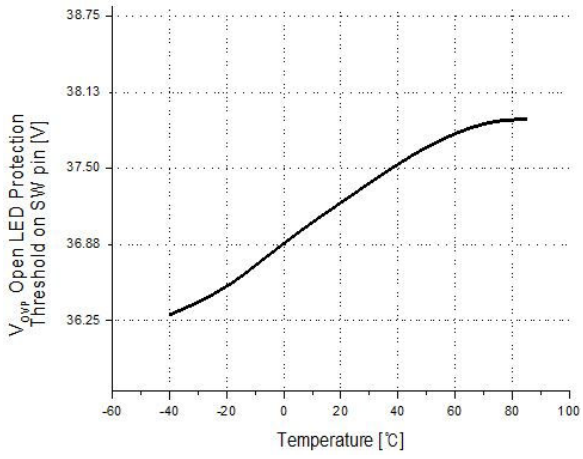
R_{DSON}. vs. Temp



V_{UVLO} vs. Temp



V_{OVP} vs. Temp



Typical Operating Characteristics

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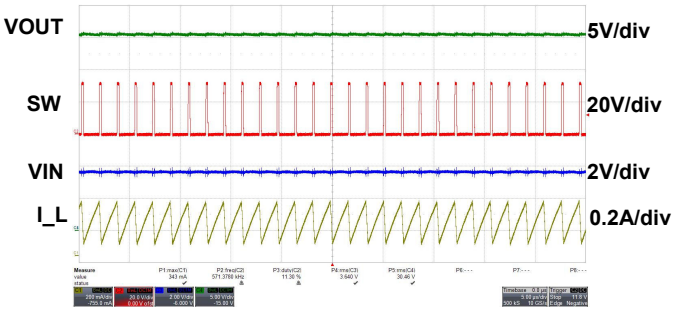
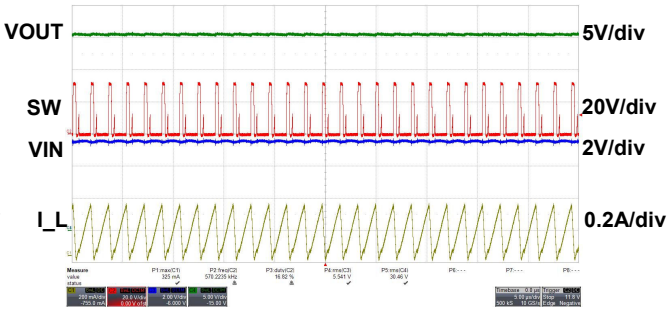
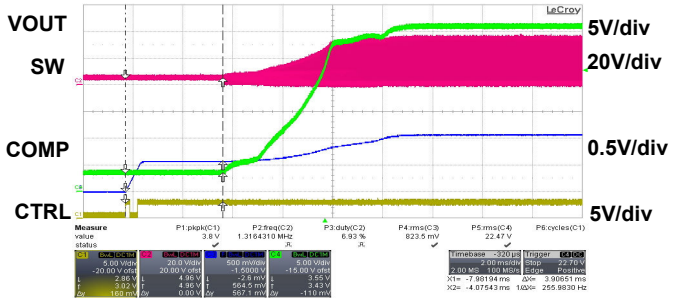
CCM Operation



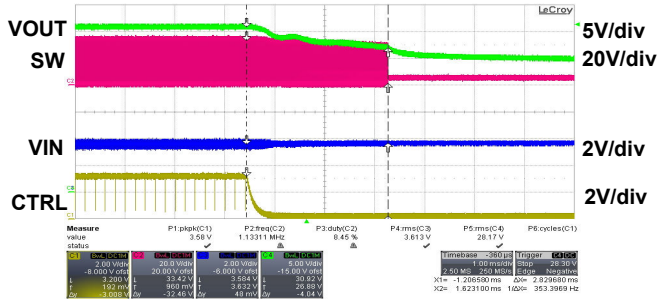
DCM Operation



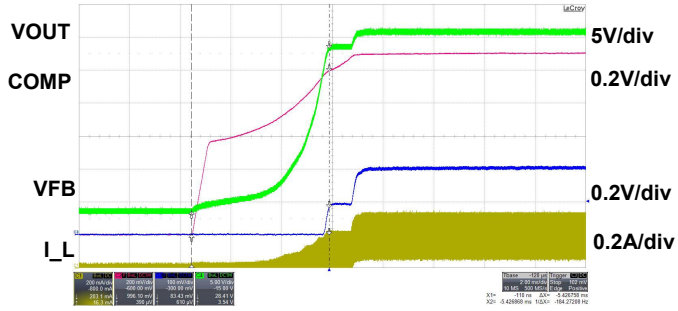
Turn-on(Soft-start)



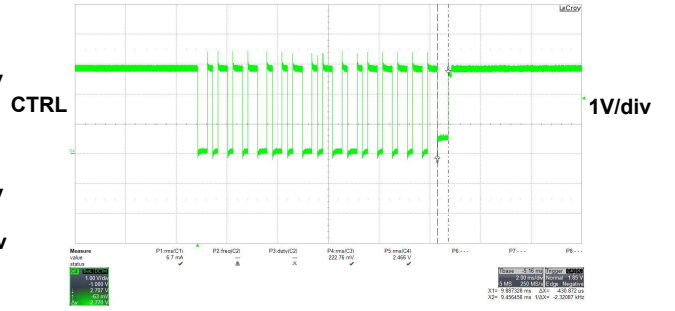
Turn-off(Shutdown)



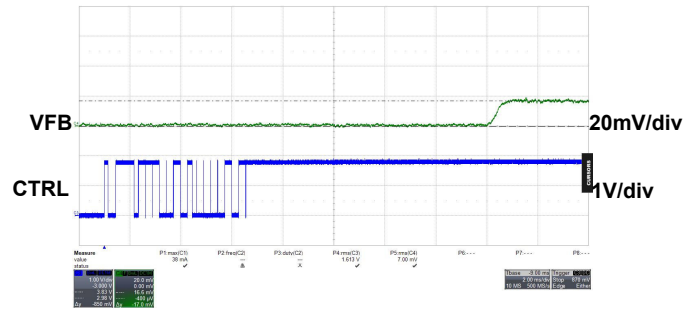
STEP0 to STEP31



Acknowledge



Enter SWIRE Mode



Typical Operating Characteristics

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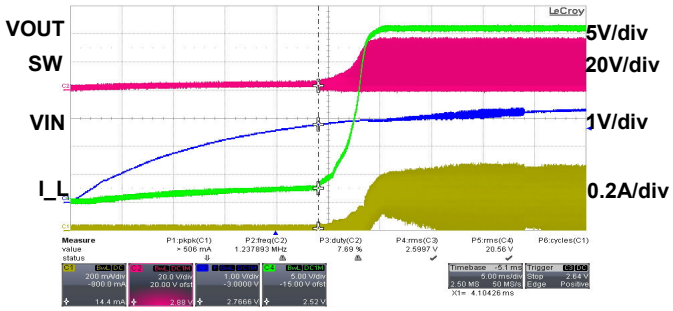
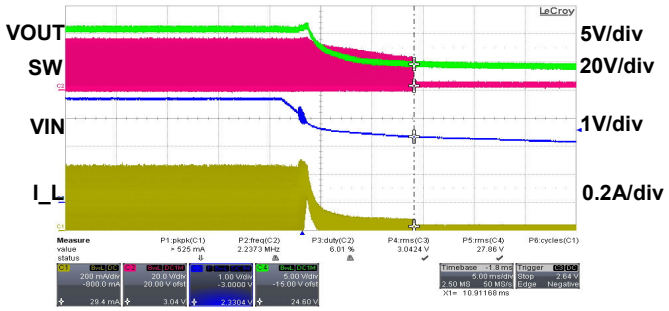
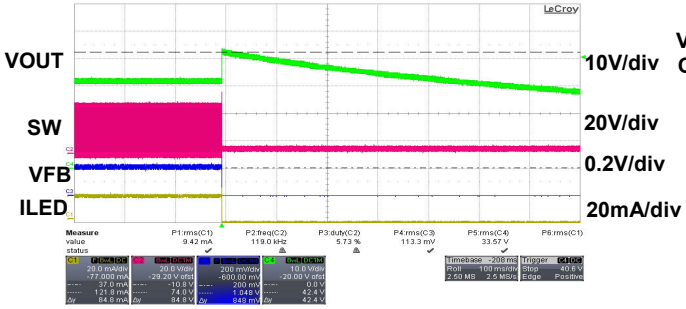
UVLO Release



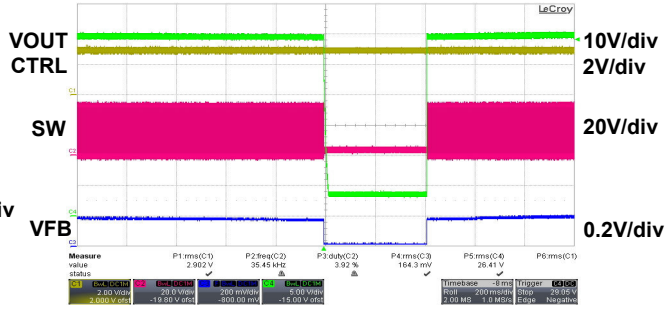
UVLO Lockout



Open LED Protection



Thermal Shutdown



Application Information

CURRENT MODE BOOST SWITCHING CONVERER OPERATION

The MAP3702 employs current mode control boost architecture that has a fast current sense loop and a slow voltage feedback loop. Internal slope compensation feature ensures stable CCM operation.
Such architecture achieves a fast transient response that is essential for the LED backlight application.

SOFT-START

The MAP3702 has following two soft-start circuitry internally to smooth start-up and reduce the start-up current.

(1) After the device is enabled, the FB pin voltage ramps to the reference voltage(200mV) in 32 steps, each step takes 213μs.
(2) After the COMP voltage ramps, for the first 5msec, the current limit of the internal boost MOSFET is set to typ. 0.4A.

LED CURRENT SETTING

The FB pin voltage can be regulated up to 200mV. Max. LED current value is programmed by external current sense resistor in series with the LED string and calculated by following equation.
To reduce LED current tolerance, 1% resistor should be used.

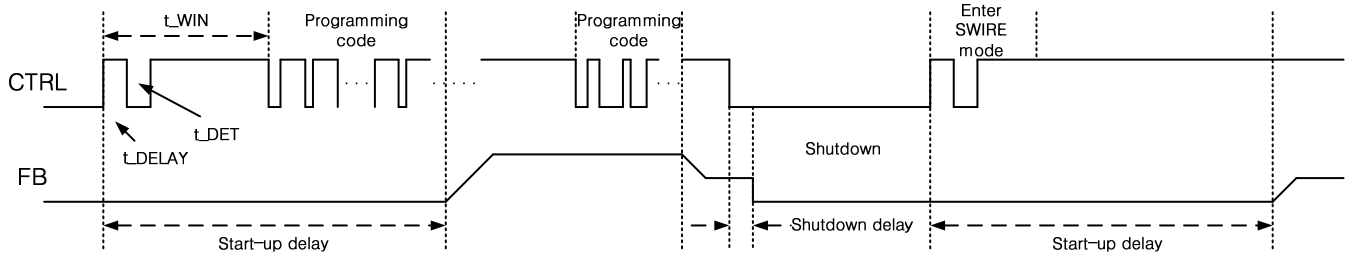
$$I_{LED} = \frac{V_{FB}}{R_{ISET}}$$

DIMMING MODE SELECTION

The MAP3702 offers two dimming modes, filtered-PWM and the SWIRE digital dimming. The CTRL pin is used for the control input for both dimming modes. The MAP3702 checks the dimming mode each time the device is enabled. The default mode is filtered-PWM dimming. To enter SWIRE mode, the following digital pattern must be applied to the CTRL pin every time the MAP3702 starts from the shutdown mode.

(1) Pull CTRL pin high to enable the MAP3702 and to start the SWIRE detection window.
(2) After the SWIRE detection delay (t_{DELAY}, min. 100μs) ends, the CTRL should be low for more than the SWIRE detection time (t_{DET}, min. 260μs).
(3) The CTRL pin should be low for more than SWIRE detection time before the SWIRE detection window (t_{WIN}, min. 1msec) ends. The SWIRE detection window starts from the first CTRL pin low to high transition.

Once the above 3 conditions are met, the MAP3702 enters the SWIRE mode immediately. The SWIRE communication can start before the detection window ends. Once the dimming mode is selected, it cannot be changed without another start up. This means the IC needs to be shutdown by pulling the CTRL low for more than 2.0ms and restarts to change dimming mode. When the IC enters shutdown mode, the MAP3702 memorizes the latest FB voltage(the latest programming code) before shutdown and when re-enters the SWIRE mode, the MAP3702 outputs the memorized FB voltage otherwise new programming code is applied.



SWIRE DIGITAL DIMMING

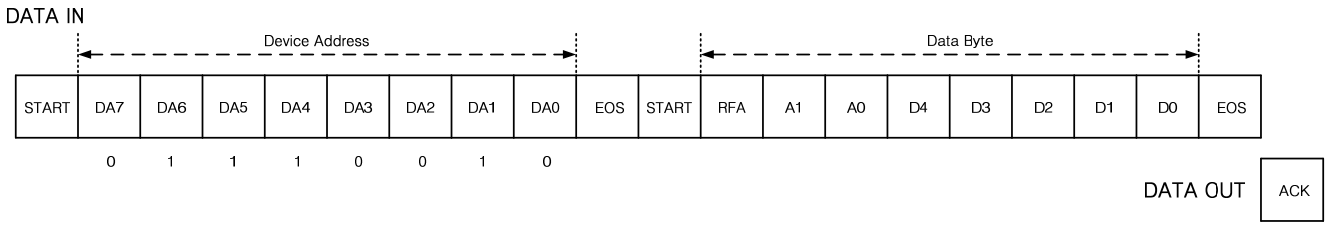
The 32-steps digital dimming can be achieved by the SWIRE interface through CTRL pin. Because it does not require a PWM signal on the CTRL pin all the time, power consumption in the host processor can be saved and it makes the battery life longer. The processor can enter idle mode if available.

The MAP3702 can program the target FB voltage to any of 32-steps with single command by the SWIRE interface. The step increment increases with the voltage to produce pseudo logarithmic curve for the brightness step. See following table for the FB voltage steps. The default step is full scale(VFB=200mV) when the device is first enabled. The programming code is stored in the internal register and will not be changed by pulling CTRL low for more than 2.0ms and then re-enabling the IC by taking CTRL high. A power reset clears the register value and reset it to default.

Step	D4	D3	D2	D1	D0	FB Voltage [mV]
0	0	0	0	0	0	0
1	0	0	0	0	1	5
2	0	0	0	1	0	8
3	0	0	0	1	1	11
4	0	0	1	0	0	14
5	0	0	1	0	1	17
6	0	0	1	1	0	20
7	0	0	1	1	1	23
8	0	1	0	0	0	26
9	0	1	0	0	1	29
10	0	1	0	1	0	32
11	0	1	0	1	1	35
12	0	1	1	0	0	38
13	0	1	1	0	1	44
14	0	1	1	1	0	50
15	0	1	1	1	1	56
16	1	0	0	0	0	62
17	1	0	0	0	1	69
18	1	0	0	1	0	74
19	1	0	0	1	1	80
20	1	0	1	0	0	86
21	1	0	1	0	1	92
22	1	0	1	1	0	98
23	1	0	1	1	1	104
24	1	1	0	0	0	116
25	1	1	0	0	1	128
26	1	1	0	1	0	140
27	1	1	0	1	1	152
28	1	1	1	0	0	164
29	1	1	1	0	1	176
30	1	1	1	1	0	188
31	1	1	1	1	1	200

SWIRE INTERFACE PROTOCOL

The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor. The protocol consists of a device specific address byte and a data byte. The device specific address byte is fixed to 72 hex. The data byte consists of five bits for information, two address bits, and the RFA bit. The RFA bit set to high indicates the *Request for Acknowledge* condition. The Acknowledge condition is only applied if the protocol was received correctly. The SWRIE interface can automatically detect bit rates between 1.7kBit/sec and up to 160kBit/sec.



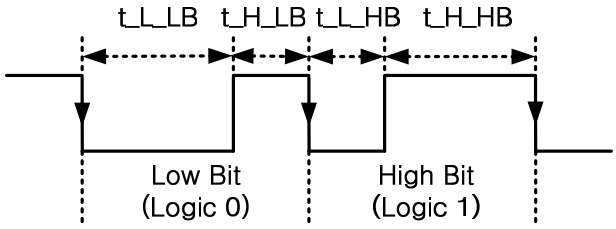
Byte	bit no.	Name	Transmission Direction	Description	Byte	bit no.	Name	Transmission Direction	Description
Device Address (72 HEX)	7	DA7	IN	0(MSB)	Data	7	RFA	IN	RFA(Note 1)
	6	DA6		1		6	A1		0(Address)
	5	DA5		1		5	A0		0(Address)
	4	DA4		1		4	D4		Data bit 4
	3	DA3		0		3	D3		Data bit 3
	2	DA2		0		2	D2		Data bit 2
	1	DA1		1		1	D1		Data bit 1
	0	DA0		0(LSB)		0	D0		Data bit 0
							ACK	OUT	(Note 2)

Note 1. Request For Acknowledge, If High, acknowledge is applied by device
Note 2. Acknowledge condition active 0, this condition will only be applied in case RFA bit is set. Open drain output. Line needs to be pulled high by the host with a pull-up resistor. This feature can only be used if the master has an open drain output stage. In case of a push-pull output stage acknowledge condition may not be requested.

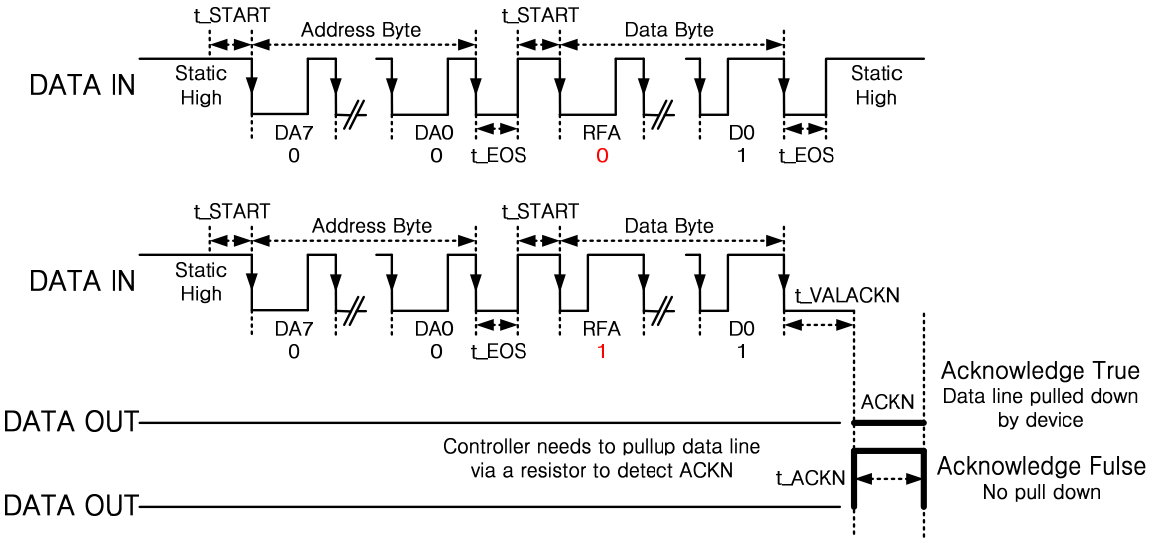
The bit detection is based on a Logic Detection scheme, where the criterion is the relation between logic low time and logic high time.

Low Bit: t_{L_LB}(Low time Low bit) > 2*t_{H_LB}(High time Low bit)
High Bit: t_{H_HB}(High time High bit) > 2*t_{L_HB}(Low time High bit)

The bit detection starts with a falling edge on the CTRL pin and ends with the next falling edge.



All bits are transmitted MSB first and LSB last. Following figures show the protocol without acknowledge request (bit RFA = 0) and with acknowledge (bit RFA = 1) request. Prior to both bytes, device address byte and data byte, a start condition must be applied. For this, the CTRL pin must be pulled high for at least t_{START}(2µs) before the bit transmission starts with the falling edge. If the CTRL pin is already at a high level, no start condition is needed prior to the device address byte. The transmission of each byte is closed with an End Of Stream(EOS) condition for at least t_{EOS}(2µs).



The acknowledge condition is only applied if:

- Acknowledge is requested by a set RFA bit.
- The transmitted device address matches with the device address of the device.
- 16 bits is received correctly.

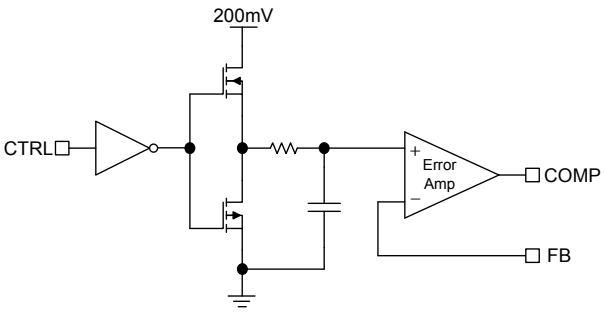
If the device turns on the internal ACKN-MOSFET and pulls the CTRL pin low for the time t_{ACKN}, which is max. 616µs then the acknowledge condition is valid after an internal delay time $t_{VALACKN}$. This means that the internal ACKN-MOSFET is turned on after $t_{VALACKN}$, when the last falling edge of the protocol was detected. The master controller keeps the line low in this period. The master device can detect the acknowledge condition with its input by releasing the CTRL pin after $t_{VALACKN}$ and read back a logic 0. The CTRL pin can be used again after the acknowledge condition ends.

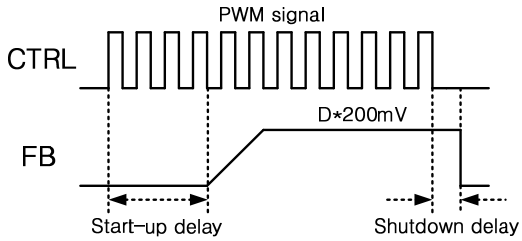
Note that the acknowledge condition may only be requested if the master device has an open drain output. For a push-pull output stage, the use a series resistor in the CRTL line to limit the current to 500µA is recommended to for such cases as:

- accidently requested acknowledge, or
- to protect the internal ACKN-MOSFET.

FILTERED-PWM DIMMING

The MAP3702 offers a filtered-PWM dimming through PWM signal input on the CTRL pin.





The MAP3702 chops up the internal 200mV reference voltage at the duty cycle of the input PWM signal. The pulse signal is then filtered by an internal low pass filter. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for dimming, only the LED DC current is modulated, which is often referred as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control.

The relationship between the duty cycle of input PWM signal and FB voltage is given by following equation.

$$V_{FB} = D \times 200mV$$

where, D is duty cycle of input PWM signal.

The input PWM frequency is ranged from 5kHz to 100kHz. The requirement of minimum dimming frequency comes from the SWIRE detection delay and detection time specification in the dimming mode selection.

SHUTDOWN

The MAP3702 enters shutdown mode when the CTRL voltage is logic low for more than 2.0ms. During shutdown, the input supply current for the device is less than 1uA(max). Although the internal boost MOSFET does not switch in shutdown, there is still a DC current path between the input and the LEDs through the inductor and schottky diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown.

UNDER VOLTAGE LOCKOUT

If the input voltage falls below the UVLO level of typical 2.2V, the device will stop switching and be reset. Operation will restart when the input voltage rises typ. 100mV hysteresis over the lock-out threshold. This ensures fail-safe operation when the input voltage falls below min. VIN voltage of IC.

OPEN LED PROTECTION

Open LED protection circuitry prevents IC damage as the result of LED disconnection. The MAP3702 monitors the voltage at the SW pin during each switching cycle. The controller turns off the boost MOSFET and shuts down the IC when the SW voltage exceeds V_{OVP} threshold and persists for 8 switching clock cycles.

As a result, the output voltage falls to the level of the input supply. The device remains in shutdown mode until it is enabled by toggling the CTRL pin or complete power-on-reset(POR).

The product of the number of external series LEDs and each LED's maximum forward voltage plus the 200mV reference voltage should be not exceed the 35.5V(Min. OVP threshold).

EXTERNAL COMPONENTS SELECTION

Inductor

The inductor value should be decided before system design. Because the selection of the inductor affects the operating mode of CCM(Continuous Conduction Mode) or DCM(Discontinuous Conduction Mode).

The inductance value defining the boundary between DCM and CCM operation can be calculated as;

$$L_B[H] = \frac{R_O \times D \times (1-D)^2}{2 \times f_{SW}}$$

where, Ro=Vout/Iout

In CCM operation, inductor size should be bigger, even though the ripple current and peak current of inductor can be small. In DCM operation, even ripple current and peak current of inductor should be large while the inductor size can be smaller.

The inductor DC current or input current can be calculated as following equations.

$$I_{IN}[A] = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}}$$

η – Efficiency of the boost converter

Then the duty ratio is,

$$D = \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D}$$

V_D – Forward voltage drop of the output rectifying diode

When the boost converter runs in DCM (L < L_B), it takes the advantages of small inductance and quick transient response. The inductor peak current is,

$$I_{L\_peak\_DCM} = \frac{V_{IN} \times D}{f_{SW} \times L}$$

The converter will work in CCM if L > L_B, generally the converter has higher efficiency under CCM and the inductor peak current is,

$$I_{L\_peak\_CCM} = I_{IN} + \frac{V_{IN} \times D}{2 f_{SW} \times L}$$

Output Rectifying Diode

Schottky diodes are the ideal choice for MAP3702 due to their low forward voltage drop and fast switching speed. Make sure that the diode has a voltage rating greater that the possible maximum output voltage. The diode conducts current only when the power switch is turned off.

Input Capacitor

In boost converter, input current flows continuously into the inductor; AC ripple component is only proportional to the rate of the inductor charging, thus, smaller value input capacitors may be used. Ensure the voltage rating of the input capacitor is suitable to handle the full supply range.

A capacitor with low ESR should be chosen to minimize heating effects and improve system efficiency.

Output Capacitor

The output capacitor acts to smooth the output voltage and supplies load current directly during the conduction phase of the power switch. Output ripple voltage consists of the discharge of the output capacitor during the FET ton period and the voltage drop due to load current flowing through the ESR of the output capacitor. The ripple voltage is shown in following equation.

$$\Delta V_{OUT} = \frac{I_{OUT} \times D}{C_{OUT} \times f_{SW}} + I_{OUT} \times ESR$$

Assume a ceramic capacitor is used. The minimum capacitance needed for a given ripple can be estimated by following equation.

$$C_{OUT} = \frac{(V_{IN} - V_{OUT}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times \Delta V_{OUT}}$$

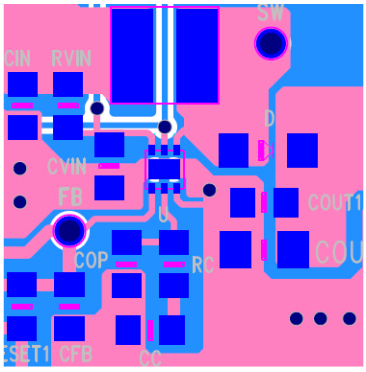
Loop Compensation

The MAP3702 controls in current mode. Current mode easily achieves compensation by consisting simple single pole from double pole that LC filer makes at voltage mode. A 220nF ceramic capacitor is suitable for most applications.

Layout Consideration

Due to fast-switching waveforms and high-current paths, careful PCB board layout is required. When laying out a board, minimize trace lengths between the IC and the inductor, diode, input capacitor, output capacitor, and FB resistor. Keep noisy traces, such as the SW node trace, away from FB. Place the input capacitor and VIN pin bypass capacitor as close to the IC as possible.

Make sure the ground bump connected to the printed circuit board with large copper area for better thermal dissipation.



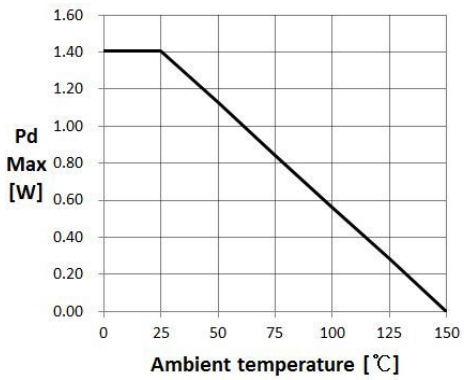
Thermal Consideration

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

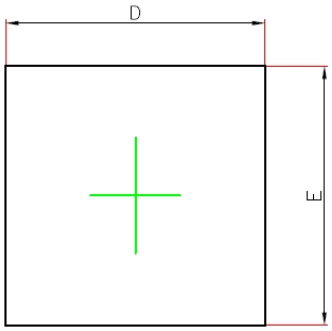
$$Pd_{(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where, $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

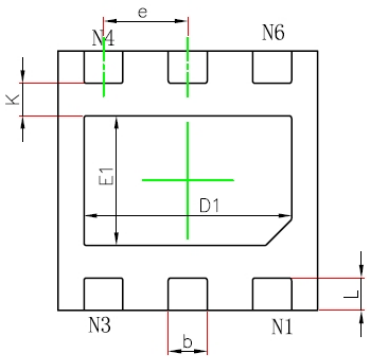
The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the MAP3702 package, the derating curve in following graph allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.



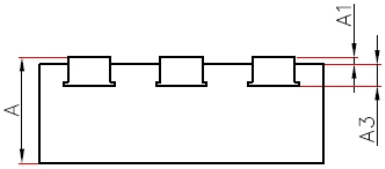
Physical Dimensions



TOP VIEW



BOTTOM VIEW



SIDE VIEW

2mm X 2mm 6 leads DFN

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.110REF.		0.005REF.	
D	1.924	2.076	0.076	0.082
E	1.924	2.076	0.076	0.082
D1	1.500	1.700	0.059	0.067
E1	0.900	1.100	0.035	0.043
k	0.2MIN		0.008	
b	0.250	0.350	0.010	0.014
e	0.650TYP.		0.026TYP.	
L	0.174	0.326	0.007	0.013

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Datasheet Revision History

Date	Version	Changes
2012-08-10	Version 0.0	Initial release
2012-11-26	Version 0.1	<Change> Shutdown current(I_{GND}) : TBD to 1uA – Page4 N-ch MOSFET leakage current(I_{LEAK}) : TBD to 1uA – Page4 OLP scheme(remove V_{OVP_FB}) – Page4, 9 Remove FB input bias current spec(I_{FB}) – Page4 Compensation capacitor value : 220nF to TBD – Page10 <Addition> Oscillator frequency(f_{SW}) condition : 3.0V ≤ V_{VIN} ≤ 5.5V – Page4 Start-up delay time(t_{START_DELAY}) – Page4 Layout consideration – Page10
2012-12-07	Version 0.2	<Change> ESD ratings – Page 3 HBM : ±3000V to ±2000V MM : ±300V to ±200V
2013-05-16	Version 1.0	<Change> Package thermal resistance(θ_{JA}) : TBD to 88.8℃/W – Page 3 Operating quiescent current(I_Q) : TBD to 1.8mA – Page 4 Shutdown pulse width on CTRL pin(t_{SHDN}) : 2.5ms to 2.0ms – Page 4, 9, 10, 13 Oscillator frequency(f_{SW}) : Min. -> TBD to 500kHz, Max. -> TBD to 700kHz – Page 4 Error amplifier transconductance(G_{EA}) : 170/310/470 to 400/550/700 umho – Page 4 Duration of acknowledge condition(t_{ACKN}) : Max. 512us to Max. 616us – Page 4, 12 Boost compensation capacitor value : TBD to 220nF – Page 14 <Addition> Typical operating characteristics – Page 5 ~ 8 Thermal consideration – Page 14
2013-06-28	Version 1.1	<Change> Part name : MAP3702QNRH to MAP3702DFRH – Page 1 Package name : QFN to DFN – Page 1, 3, 15