

RF Power Field Effect Transistor LDMOS, 1800 — 2000 MHz, 60W, 26V

5/24/04

Preliminary

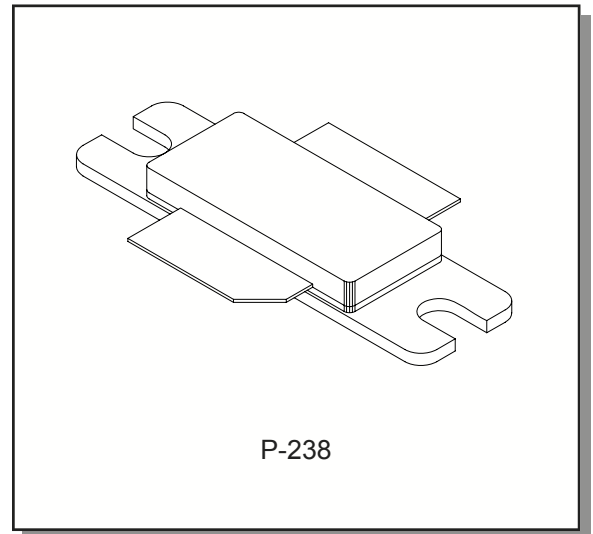
MAPLST1820-060CF

Features

Designed for base station applications in the 1805-1880MHz or 1930-1990MHz Frequency Band. Suitable for GSM, EDGE, TDMA, CDMA, and multi-carrier amplifier applications

- Typical EDGE performance @ 1880MHz, 26V, Idq=900mA:
 - Output Power: 30W
 - Power Gain: 13dB (typ.)
 - Efficiency: 35% (typ.)

Package Style



Maximum Ratings

Parameter	Symbol	Rating	Units
Drain—Source Voltage	V_{DSS}	65	V_{dc}
Gate—Source Voltage	V_{GS}	+20, -20	V_{dc}
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	206	W
Storage Temperature	T_{STG}	-40 to +150	$^\circ C$
Junction Temperature	T_J	+200	$^\circ C$

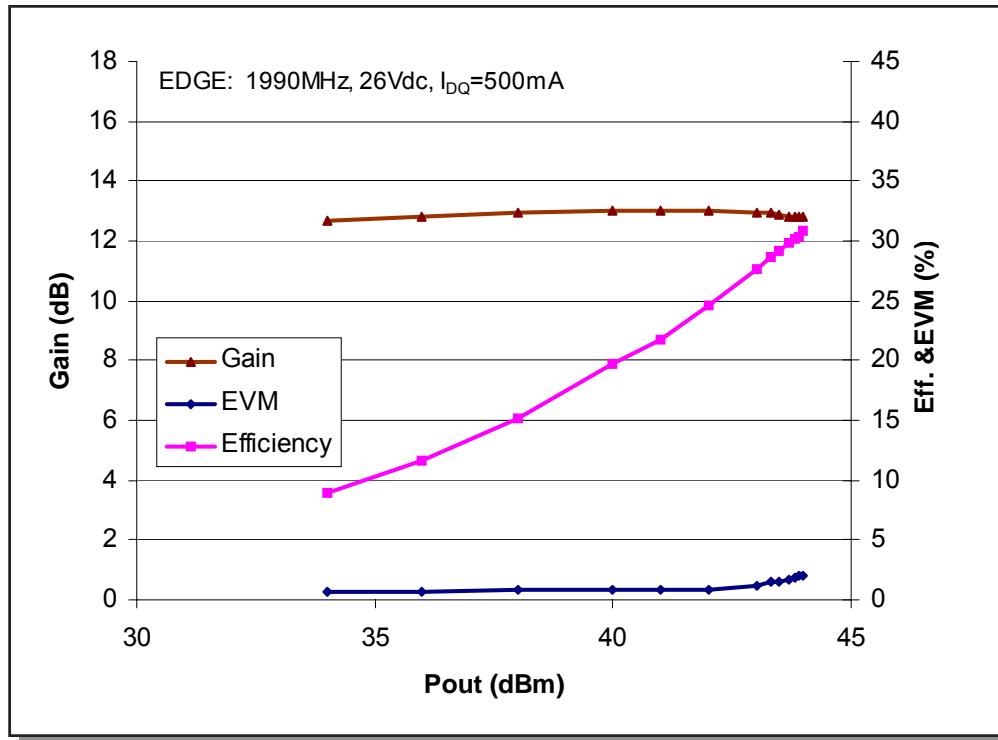
Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.85	$^\circ C/W$

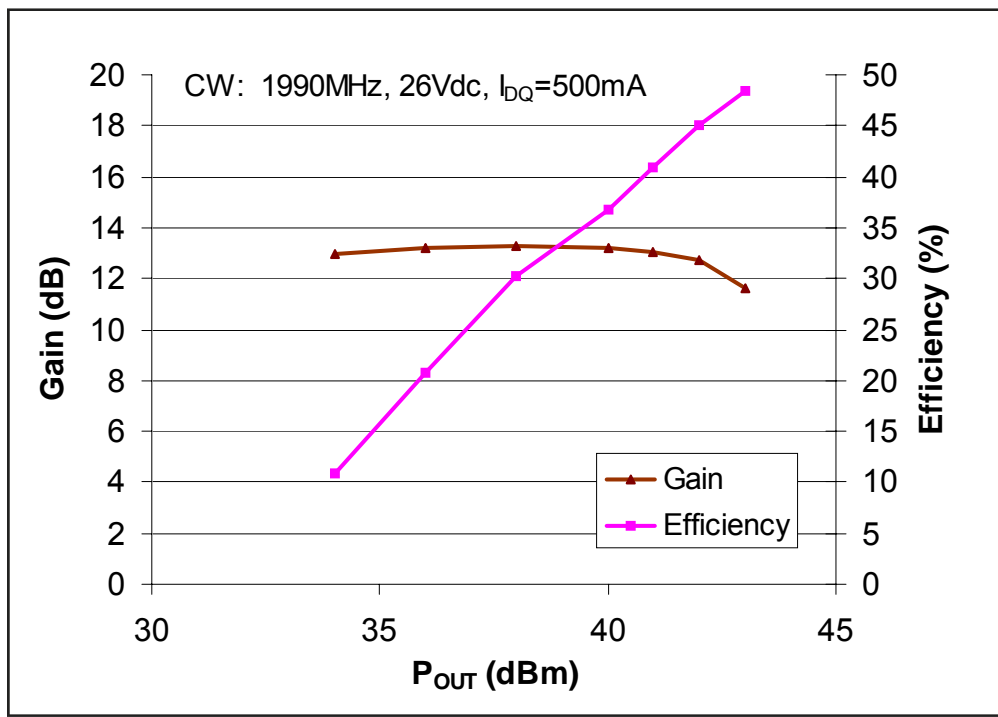
NOTE—**CAUTION**—MOS devices are susceptible to damage from electrostatic charge. Precautions in handling and packaging MOS devices should be observed.

Preliminary

Characteristic	Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS @ 25°C					
Drain-Source Breakdown Voltage ($V_{GS} = 0$ Vdc, $I_D = 100$ μ Adc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 26$ Vdc, $V_{GS} = 0$)	I_{DSS}	—	—	10	μ Adc
Gate—Source Leakage Current ($V_{GS} = 5$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	—	1	μ Adc
Gate Threshold Voltage ($V_{DS} = 26$ Vdc, $I_d = 60$ mA)	$V_{GS(th)}$	2	—	5	Vdc
Gate Quiescent Voltage ($V_{DS} = 26$ Vdc, $I_d = 500$ mA)	$V_{DS(on)}$	3	—	4	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_d = 1$ A)	$V_{DS(on)}$	—	0.40	—	Vdc
Forward Transconductance ($V_{GS} = 10$ Vdc, $I_d = 1$ A)	Gm	—	2.4	—	S
DYNAMIC CHARACTERISTICS @ 25°C					
Reverse Transfer Capacitance ($V_{DS} = 26$ Vdc, $V_{GS} = 0$, $f = 1$ MHz)	C_{rss}	—	3.0	—	pF
RF FUNCTIONAL TESTS @ 25°C (In M/A-COM Test Fixture)					
Common-Source Amplifier Gain ($V_{DS} = 26$ Vdc, $I_{DQ} = 500$ mA, $f = 1880$ MHz, $P_{OUT} = 60$ W)	G_p	—	12	—	dB
Drain Efficiency ($V_{DS} = 26$ Vdc, $I_{DQ} = 500$ mA, $f = 1880$ MHz, $P_{OUT} = 60$ W)	EFF (η)	—	48	—	%
Input Return Loss ($V_{DS} = 26$ Vdc, $I_{DQ} = 500$ mA, $f = 1880$ MHz, $P_{OUT} = 60$ W)	IRL	—	-10	—	dB
Output VSWR Tolerance ($V_{DS} = 26$ Vdc, $I_{DQ} = 500$ mA, $f = 1880$ MHz, $P_{OUT} = 60$ W, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

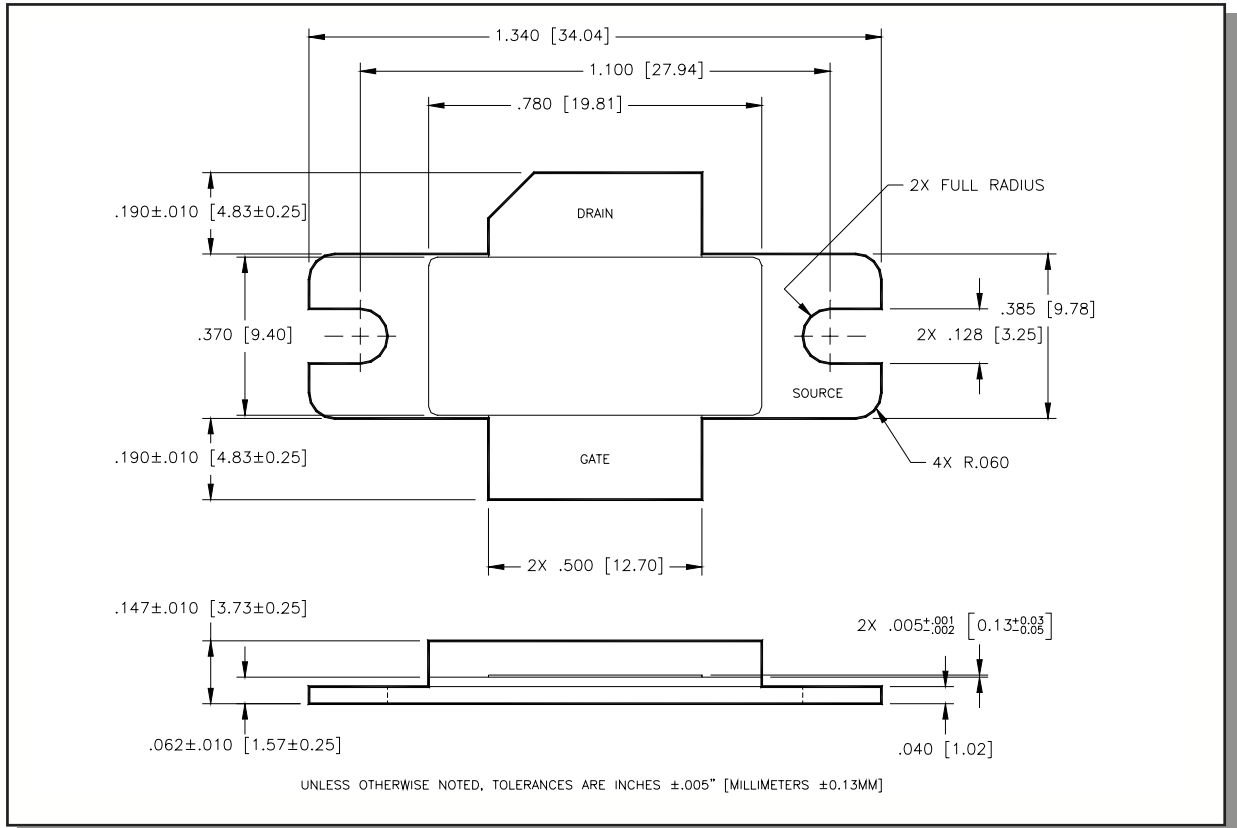


Graph 1. EDGE: Gain, Efficiency and Error Vector Magnitude vs. Output Power



Graph 2. CW: Gain and Efficiency vs. Output Power

Package Dimensions



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