MACOM

RF Power Field Effect Transistor
LDMOS, 2110 — 2170 MHz, 15W, 28V

8/20/03

Preliminary

MAPLST2122-015CF

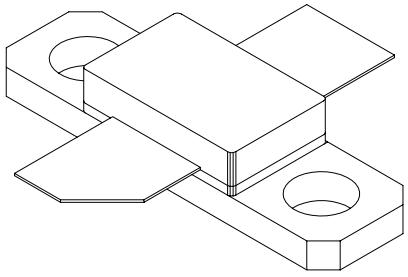
Features

Designed for W-CDMA base station applications in the 2.1 to 2.2 GHz Frequency Band. Suitable for TDMA, CDMA, and multicarrier power amplifier applications.

- 15W Output Power at P_{1dB} (CW)
- 12dB Minimum Gain at P_{1dB} (CW)

- W-CDMA Typical Performance: ($28V_{DC}$, -45dBc ACPR, 5MHz offset, 4.096MHz BW)
  - Output Power: 2.2W (typ.)
  - Gain: 13dB (typ.)
  - Efficiency: 17% (typ.)
- 10:1 VSWR Ruggedness (CW @ 15W, 28V, 2110MHz)

Package Style



MAPLST2122-015CF

Maximum Ratings

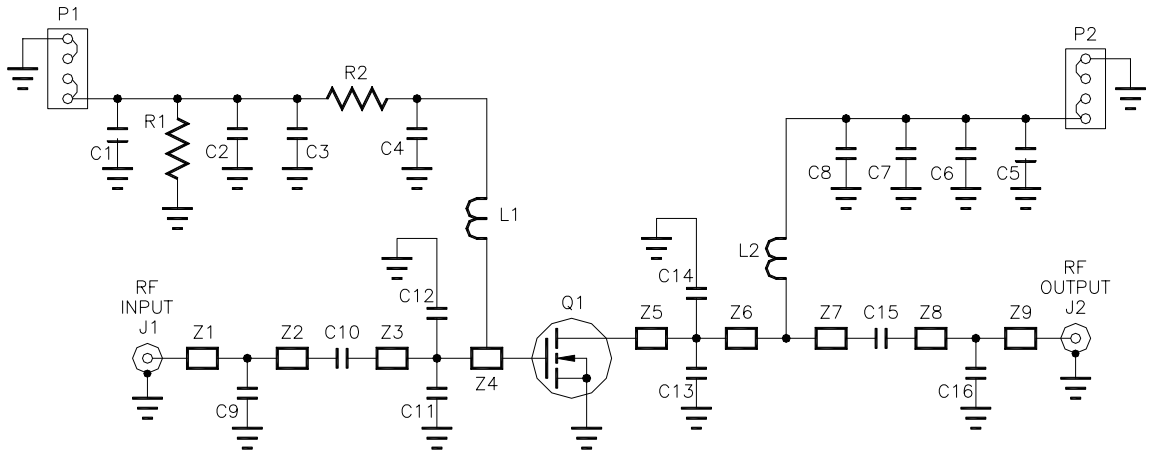
Parameter	Symbol	Rating	Units
Drain—Source Voltage	V_{DSS}	65	V_{dc}
Gate—Source Voltage	V_{GS}	20	V_{dc}
Total Power Dissipation @ T_C = 25 °C	P_D	54.7	W
Storage Temperature	T_{STG}	-40 to +150	°C
Junction Temperature	T_J	+200	°C

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\Theta JC}$	3.2	°C/W

NOTE—**CAUTION**—MOS devices are susceptible to damage from electrostatic charge. Precautions in handling and packaging MOS devices should be observed.

Characteristic	Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS @ 25ºC					
Drain-Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 20 µAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1	µAdc
Gate—Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	µAdc
Gate Threshold Voltage (V_{ds} = 28 Vdc, I_d = 1 mA)	$V_{GS(th)}$	2.5	3.0	4.0	Vdc
Gate Quiescent Voltage (V_{ds} = 28 Vdc, I_d = 250 mA)	$V_{DS(Q)}$	2.5	3.5	4.5	Vdc
Drain-Source On-Voltage (V_{gs} = 10 Vdc, I_d = 1 A)	$V_{DS(on)}$	—	0.2	—	Vdc
Forward Transconductance (V_{gs} = 10 Vdc, I_d = 1 A)	Gm	—	1.0	—	S
DYNAMIC CHARACTERISTICS @ 25ºC					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	0.9	—	pF
RF FUNCTIONAL TESTS @ 25ºC (In M/A-COM Test Fixture) (2)					
Two-Tone Common-Source Amplifier Power Gain (V_{DS} = 28 Vdc, P_{OUT} = 15 W PEP. I_{DQ} = 150 mA, f1 = 2170.0 MHz, f2 = 2170.1 MHz)	G_{ps}	12	12.8	—	dB
Two-Tone Drain Efficiency (V_{DS} = 28 Vdc, P_{OUT} = 15 W PEP. I_{DQ} = 150 mA, f1 = 2170.0 MHz, f2 = 2170.1 MHz)	EFF (η)	—	32	—	%
Two-Tone Third Order Intermod (V_{DS} = 28 Vdc, P_{OUT} = 15 W PEP. I_{DQ} = 150 mA, f1 = 2170.0 MHz, f2 = 2170.1 MHz)	IMD	—	-30	—	dBc
Input Return Loss (V_{DS} = 28 Vdc, P_{OUT} = 15 W PEP. I_{DQ} = 150 mA, f1 = 2170.0 MHz, f2 = 2170.1 MHz)	IRL	—	-12	—	dB
Two-Tone Common-Source Amplifier Power Gain (V_{DS} = 28 Vdc, P_{OUT} = 15 W PEP. I_{DQ} = 150 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz)	G_{ps}	12	12.8	—	dB
Two-Tone Drain Efficiency (V_{DS} = 28 Vdc, P_{OUT} = 15 W PEP. I_{DQ} = 150 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz)	EFF (η)	—	32	—	%
Two-Tone Third Order Intermod (V_{DS} = 28 Vdc, P_{OUT} = 15 W PEP. I_{DQ} = 150 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz)	IMD	—	-30	—	dBc
Input Return Loss (V_{DS} = 28 Vdc, P_{OUT} = 15 W PEP. I_{DQ} = 150 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz)	IRL	—	-12	-10	dB
Output VSWR Tolerance (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 250 mA, f = 2110 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			



C1,C5	Tantalum Electrolytic Surface Mt. Cap., 100 µF	L1	Inductor, 8 nH, CoilCraft A03T
C2,C6	Ceramic Chip Capacitor, 0.1 µF	L2	Inductor, 18.5 nH, CoilCraft A05T
C3,C7	Ceramic Chip Capacitor, 1000 pF	P1,P2	Connector, AMP 640457-4
C4,C8,C10,C15	Chip Capacitor, 8.2 pF ATC100B	Q1	Transistor, MAPLST2122-015WF
C9	Chip Capacitor, 1.5 pF ATC100B	R1	Chip Resistor (0805), 100k Ohm
C11,C12	Chip Capacitor, 0.1 pF ATC100B	R2	Chip Resistor (0805), 1K Ohm
C13,C14	Chip Capacitor, 0.7 pF ATC100B	PC Board	Taconix (TLX-8) Woven Glass Teflon
C16	Chip Capacitor, 0.5 pF ATC100B		Teflon .031" Thick, Er=2.55, 1 Oz Copper
Z1-Z9	Distributed Microstrip Element		Both Sides
J1,J2	SMA Connector, Omni Spectra 2052-5636-02		

Figure 1. 2110—2170 MHz Test Fixture Schematic

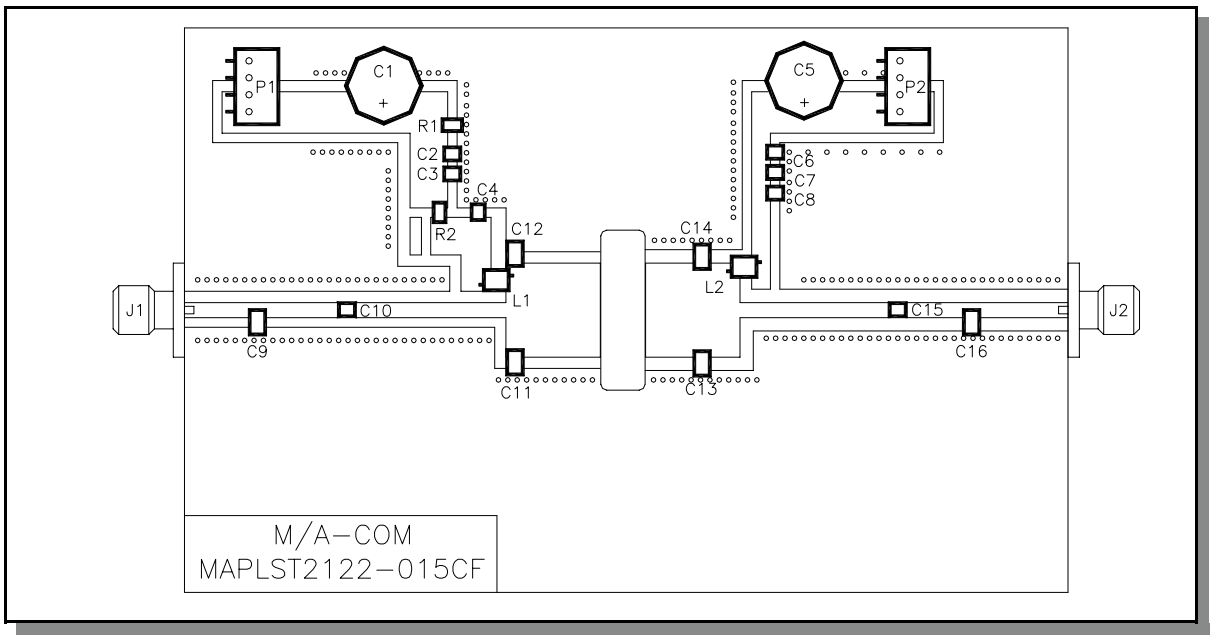
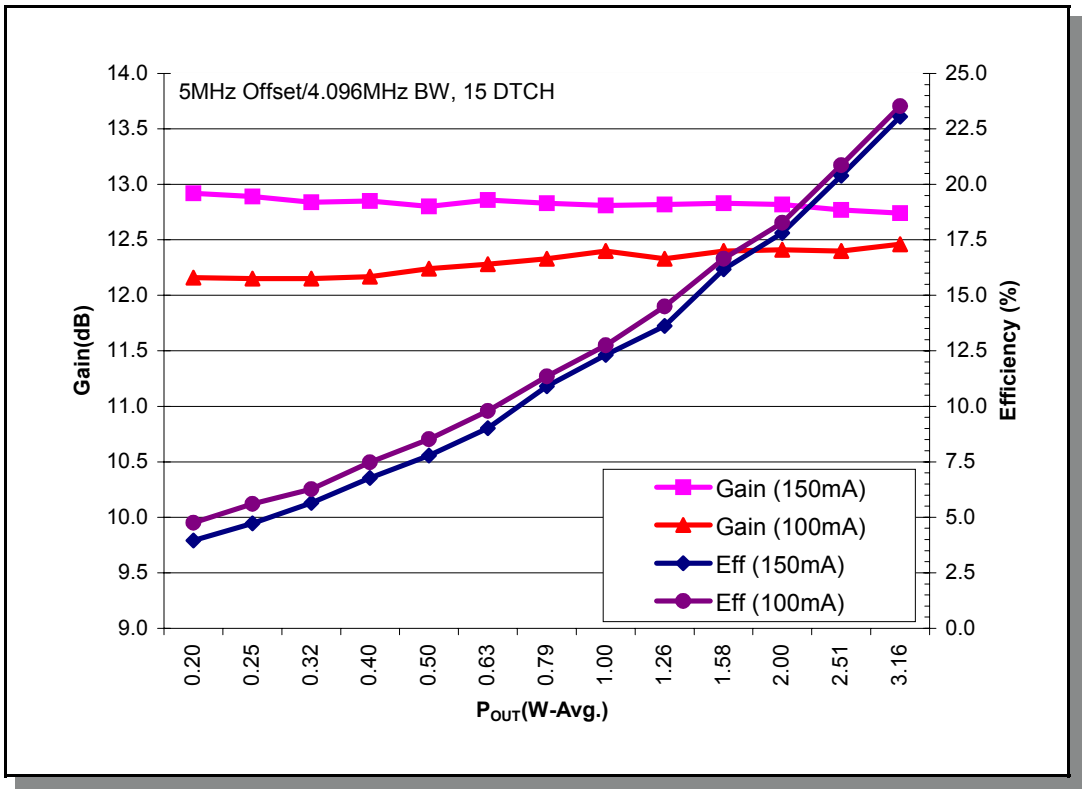
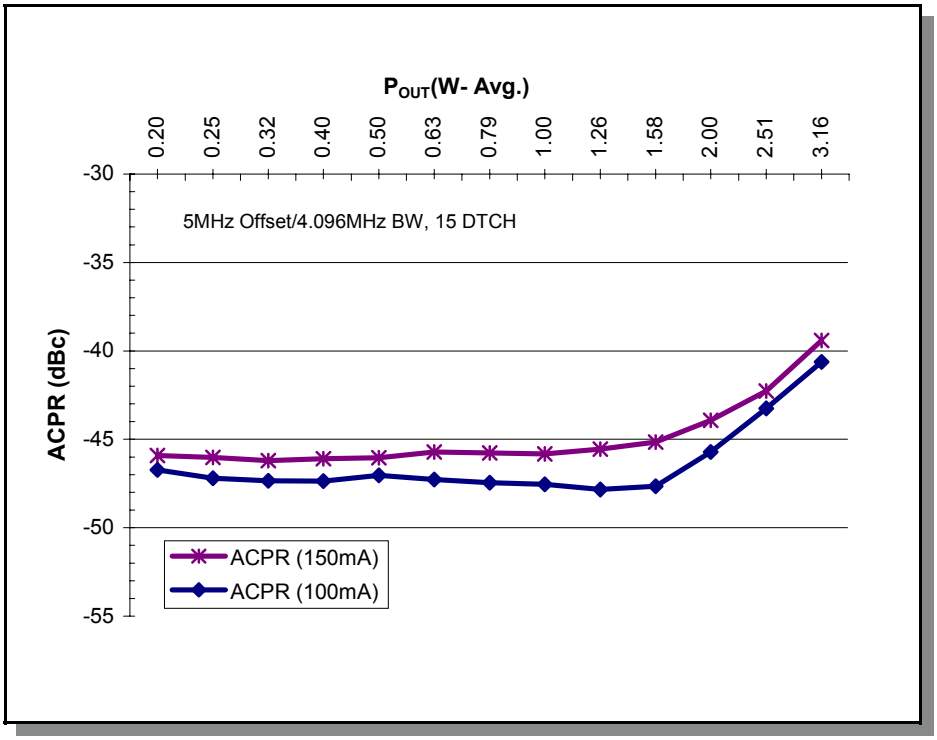


Figure 2. 2110—2170 MHz Test Fixture Component Layout

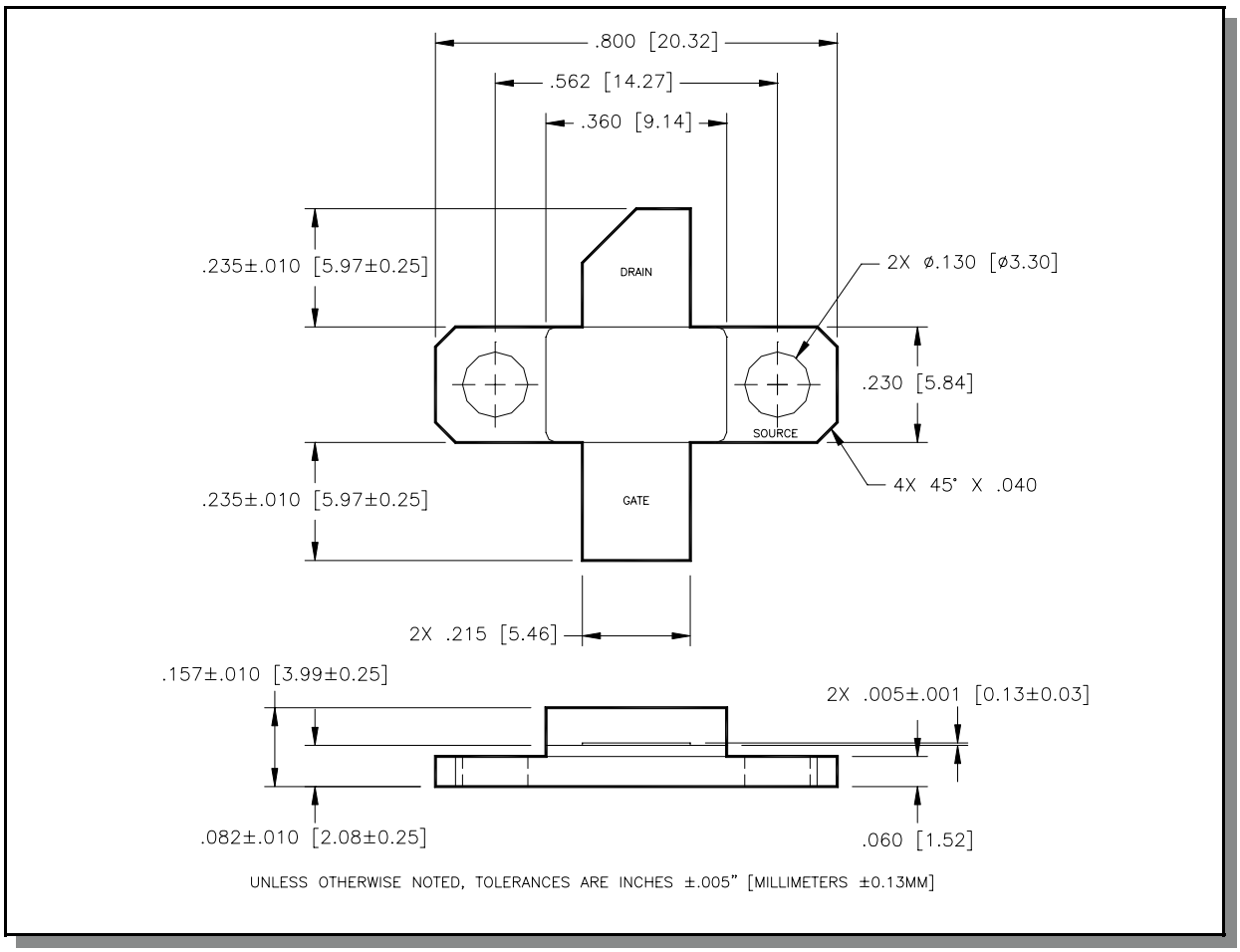


Graph 1. W-CDMA Power Gain and Drain Efficiency vs. Output Power



Graph 2. W-CDMA Adjacent Channel Power Ratio vs. Output Power

Package Dimensions



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