19-3985; Rev 3; 11/08

EVALUATION KIT AVAILABLE

Automatic RF MESFET Amplifier Drain-Current Controllers

General Description

The MAX11014/MAX11015 set and control bias conditions for dual MESFET power devices found in point-to-point communication and other microwave base stations. The MAX11014 integrates complete dual analog closed-loop drain-current controllers for Class A MESFET amplifier operation, while the MAX11015 targets Class AB operation. Both devices integrate SRAM lookup tables (LUTs) that can be used to store temperature and drain-current compensation data.

Each device includes dual high-side current-sense amplifiers to monitor the MESFET drain currents through the voltage drop across the sense resistors in the 0 to 625mV range. External diode-connected transistors monitor the MESFET temperatures while an internal temperature sensor measures the local die temperature of the MAX11014/MAX11015. The internal DAC sets the voltages across the current-sense resistors by controlling the GATE voltages. The internal 12-bit SAR ADC digitizes internal and external temperature, internal DAC voltages, current-sense amplifier voltages, and external GATE voltages. Two of the 11 ADC channels are available as general-purpose analog inputs for analog system monitoring.

The MAX11014's gate-drive amplifier functions as an integrator for the Class A drain-current control loop while the MAX11015's gate-drive amplifier functions with a gain of -2 for Class AB applications. The current-limited gate-drive amplifier can be fast clamped to an external voltage independent of the digital input from the serial interface. Both the MAX11014 and the MAX11015 include self-calibration modes to minimize error over time, temperature, and supply voltage.

The MAX11014/MAX11015 feature an internal reference and can operate from separate ADC and DAC external references. The internal reference provides a well-regulated, low-noise +2.5V reference for the ADC, DAC, and temperature sensors. These integrated circuits operate from a 4-wire 20MHz SPI™-/MICROWIRE™-compatible or 3.4MHz I²C-compatible serial interface (pin-selectable). Both devices operate from a +4.75V to +5.25V analog supply (2.8mA typical supply current), a +2.7V to +5.25V digital supply (1.5mA typical supply current), and a -4.5V to -5.5V negative supply (1.1mA supply current). The MAX11014/MAX11015 are available in a 48-pin thin QFN package specified over the -40°C to +105°C temperature range.

Features

- ♦ **Dual Drain-Current-Sense Gain Amplifier**
  - **Preset Gain of 4**
  - **±0.5% Accuracy for Sense Voltages Between 75mV and 625mV (MAX11014)**
- ♦ **Common-Mode Sense-Resistor Voltage Range**
  - **0.5V to 11V (MAX11014)**
  - **5V to 32V (MAX11015)**
- ♦ **Low-Noise Output GATE Bias with ±10mA GATE Drive**
- ♦ **Fast Clamp and Power-On Reset**
- ♦ **12-Bit DAC Controls MESFET GATE Voltage**
- ♦ **Internal Temperature Sensor/Dual Remote Diode Temperature Sensors**
- ♦ **Internal 12-Bit ADC Measures Temperature and Voltage**
- ♦ **Pin-Selectable Serial Interface**
  - **3.4MHz I²C-Compatible Interface**
  - **20MHz SPI-/MICROWIRE-Compatible Interface**

Ordering Information

PART	PIN-PACKAGE	AMPLIFIER
MAX11014BGTM+	48 Thin QFN-EP**	Class A
MAX11015BGTM+*	48 Thin QFN-EP**	Class AB

+ Denotes a lead-free package.
**Future product—contact factory for availability.*
***EP = Exposed pad.*
***Note:** All devices are specified over the -40°C to +105°C operating temperature range.*

Pin Configuration and Typical Operating Circuit appear at end of data sheet.

Applications

Cellular Base-Station RF MESFET Bias Controllers
Point-to-Point or Point-to-Multipoint Links
Industrial Process Control

SPI is a trademark of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

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ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +6V
DV_{DD} to DGND.....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
AV_{SS} to AGND .....-0.3V to -6V
RCS1+, RCS1-, RCS2+, RCS2- to $GATEV_{SS}$ (MAX11014) .....-0.3V to +13V
RCS1+, RCS1-, RCS2+, RCS2- to AGND (MAX11015) .....-0.3V to +34V
RCS1- to RCS1+.....-6V to +0.3V
RCS2- to RCS2+.....-6V to +0.3V
$GATEV_{SS}$ to AGND.....+0.3V to -6V
GATE1, GATE2 to AGND .....($GATEV_{SS}$ - 0.3V) to (AV_{DD} + 0.3V)
DV_{DD} to AV_{DD}.....-0.3V to (AV_{DD} + 0.3V)
All Other Analog Inputs to AGND .....-0.3V to (AV_{DD} + 0.3V)
PGAOUT1, PGAOUT2 to AGND .....-0.3V to (AV_{DD} + 0.3V)
SCLK/SCL, DIN/SDA, $\overline{CS}$/A0, N.C./A2, $\overline{CNVST}$, OPSAFE1, OPSAFE2 to DGND.....-0.3V to (DV_{DD} + 0.3V)
DOUT/A1, SPI/$\overline{I2C}$, ALARM, BUSY to DGND .....-0.3V to (DV_{DD} + 0.3V)
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C) 48-Pin Thin QFN (derate 27.0mW/°C above +70°C).....2162.2mW
Operating Temperature Range .....-40°C to +105°C
Storage Temperature Range .....-60°C to 150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{GATEVSS}$ = V_{AVSS} = -5.5V to -4.75V, V_{AVDD} = +4.75V to +5.25V, V_{DVDD} = +2.7V to V_{AVDD}, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REFADC} = C_{REFDAC} = 0.1µF, $V_{OPSAFE1}$ = $V_{OPSAFE2}$ = 0, V_{RCS1+} = V_{RCS2+} = +5V, C_{FILT1} = C_{FILT3} = 1nF, C_{FILT2} = C_{FILT4} = 1nF, V_{AGND} = V_{DGND} = 0, V_{ADCIN0} = V_{ADCIN1} = 0, $V_{ACLAMP1}$ = $V_{ACLAMP2}$ = -5V, T_J = T_{MIN} to T_{MAX}, unless otherwise noted. All typical values are at T_J = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT-SENSE AMPLIFIER (Note 1)						
Common-Mode Input Voltage Range	V_{RCS_+}	MAX11014	0.5		11.0	V
		MAX11015	5		32	
Common-Mode Rejection Ratio	CMRR	0.5V < V_{RCS_+} < 11V for the MAX11014		90		dB
		5V < V_{RCS_+} < 32V for the MAX11015		90		
Input-Bias Current	I_{RCS+}	V_{SENSE} < 100mV over the common-mode range			200	µA
	I_{RCS-}				±2	
Full-Scale Sense Voltage	V_{SENSE}	V_{SENSE} = V_{RCS_+} - V_{RCS_-}			625	mV
Sense Voltage Range		To within ±0.5% accuracy	75		625	mV
		To within ±2% accuracy	20		625	
		To within ±20% accuracy	2		625	
Total Current Set Error		V_{SENSE} = 75mV		±0.1	±0.5	%
Current-Sense Settling Time	t_{HSCS}	Settles to within ±0.5% of final value		< 25		µs
Saturation Recovery Time		Settles to within ±0.5% accuracy, from V_{SENSE} = 1.875V		< 45		µs
CLASS AB INPUT CHANNEL						
Untrimmed Offset				19		Bits
Offset Temperature Coefficient				0		Bits/°C
Gain				4		
Gain Error				0.1		%

ELECTRICAL CHARACTERISTICS (continued)

($V_{GATEVSS}$ = V_{AVSS} = -5.5V to -4.75V, V_{AVDD} = +4.75V to +5.25V, V_{DVDD} = +2.7V to V_{AVDD}, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REFADC} = C_{REFDAC} = 0.1µF, $V_{OPSAFE1}$ = $V_{OPSAFE2}$ = 0, V_{RCS1+} = V_{RCS2+} = +5V, C_{FILT1} = C_{FILT3} = 1nF, C_{FILT2} = C_{FILT4} = 1nF, V_{AGND} = V_{DGND} = 0, V_{ADCIN0} = V_{ADCIN1} = 0, $V_{ACLAMP1}$ = $V_{ACLAMP2}$ = -5V, T_J = T_{MIN} to T_{MAX}, unless otherwise noted. All typical values are at T_J = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLASS AB OUTPUT CHANNEL						
Untrimmed Offset		(Note 1)		50		µV
Offset Temperature Coefficient				0		mV/°C
Gain				-2		
Gain Error				0.1		%
GATE-DRIVE AMPLIFIER/INTEGRATOR						
Output Gate-Drive Voltage Range (Note 2)	V_{GATE}	I_{GATE} = -1mA	$V_{GATEVSS}$ + 1			V
		I_{GATE} = +1mA		-0.15	-4	mV
		I_{GATE} = -10mA	$V_{GATEVSS}$ + 1.2			V
		I_{GATE} = +10mA		-1	-20	mV
Gate Voltage Settling Time—MAX11015	t_{GATE}	Settles to within ±0.5% of final value, R_S = 50 , C_{GATE} = 15µF, see GATE Output Resistance vs. GATE Voltage in the *Typical Operating Characteristics*		1.1		ms
Output Capacitive Load (Note 3)	C_{GATE}	No series resistance, R_S = 0	0		0.5	nF
		R_S = 500	0	15,000		
Gate Voltage Noise		RMS noise, 1kHz to 1MHz		250		nV/√Hz
Maximum Power-On Transient		C_{LOAD} = 1nF		±100		mV
Output Short-Circuit Current Limit	I_{SC}	Sinking or sourcing		±25		mA
Output Safe Switch On-Resistance	R_{OPSW}	Clamp GATE1 to ACLAMP1, GATE2 to ACLAMP2 (Note 4)			3.6	k
ADC DC ACCURACY						
Resolution			12			Bits
Differential Nonlinearity	DNL_{ADC}				±2	LSB
Integral Nonlinearity	INL_{ADC}	(Note 5)			±2	LSB
Offset Error				±2	±4	LSB
Gain Error		(Note 6)		±2	±4	LSB
Gain Temperature Coefficient				±0.4		ppm/°C
Offset Temperature Coefficient				±0.4		ppm/°C
Channel-to-Channel Offset Matching				±0.1		LSB
Channel-to-Channel Gain Matching				±0.1		LSB

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ELECTRICAL CHARACTERISTICS (continued)

($V_{GATEVSS}$ = V_{AVSS} = -5.5V to -4.75V, V_{AVDD} = +4.75V to +5.25V, V_{DVDD} = +2.7V to V_{AVDD}, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REFADC} = C_{REFDAC} = 0.1µF, $V_{OPSAFE1}$ = $V_{OPSAFE2}$ = 0, V_{RCS1+} = V_{RCS2+} = +5V, C_{FILT1} = C_{FILT3} = 1nF, C_{FILT2} = C_{FILT4} = 1nF, V_{AGND} = V_{DGND} = 0, V_{ADCIN0} = V_{ADCIN1} = 0, $V_{ACLAMP1}$ = $V_{ACLAMP2}$ = -5V, T_J = T_{MIN} to T_{MAX}, unless otherwise noted. All typical values are at T_J = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC DYNAMIC ACCURACY (1kHz sine-wave input, -0.5dB from full scale, 94.4ksps)						
Signal-to-Noise Plus Distortion	SINAD			70		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-84		dB
Spurious-Free Dynamic Range	SFDR			86		dB
Intermodulation Distortion	IMD	f_{IN1} = 9.9kHz, f_{IN2} = 10.2kHz		76		dB
Full-Power Bandwidth		-3dB point		1		MHz
Full-Linear Bandwidth		S / (N + D) > 68dB		100		kHz
ADC CONVERSION RATE						
Power-Up Time	t_{PU}	External reference		0.8		µs
		Internal reference		50		
Acquisition Time (Note 3)	t_{ACQ}	GATE_ and sense voltage measurements	40			µs
		All other measurements	1.5			
Conversion Time	t_{CONV}	Internally clocked			6.5	µs
Aperture Delay				30		ns
ADCIN1, ADCIN2 INPUTS						
Input Range	$V_{ADCIN\_}$	Relative to AGND (Note 7)	0		V_{REFADC}	V
Input Leakage Current		$V_{ADCIN\_}$ = 0V or V_{AVDD}		±0.01	±1	µA
Input Capacitance	$C_{ADCIN\_}$			34		pF
TEMPERATURE MEASUREMENTS						
Internal Sensor Measurement Error		T_J = +25°C		±0.25		°C
		T_J = -40°C to +85°C (Note 3)		±1.0	±2.5	
		T_J = -40°C to +105°C (Note 3)		±1.0	±3.5	
External Sensor Measurement Error (Note 8)		T_J = +25°C		±1.0		°C
		T_J = -40°C to +105°C		±3		
Temperature Resolution				0.125		°C/LSB
External Diode Drive			3.26		75.00	µA
External Temperature Sensor Drive Current Ratio				16.6		
INTERNAL REFERENCE						
Reference Output Voltage		V_{REFADC} = V_{REFDAC}, T_J = +25°C	+2.490	+2.500	+2.510	V
Reference Output Temperature Coefficient				±15		ppm/°C
Reference Output Impedance				6.5		kΩ
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = +5V ±5%		-83		dB

ELECTRICAL CHARACTERISTICS (continued)

($V_{GATEVSS}$ = V_{AVSS} = -5.5V to -4.75V, V_{AVDD} = +4.75V to +5.25V, V_{DVDD} = +2.7V to V_{AVDD}, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REFADC} = C_{REFDAC} = 0.1µF, $V_{OPSAFE1}$ = $V_{OPSAFE2}$ = 0, V_{RCS1+} = V_{RCS2+} = +5V, C_{FILT1} = C_{FILT3} = 1nF, C_{FILT2} = C_{FILT4} = 1nF, V_{AGND} = V_{DGND} = 0, V_{ADCIN0} = V_{ADCIN1} = 0, $V_{ACLAMP1}$ = $V_{ACLAMP2}$ = -5V, T_J = T_{MIN} to T_{MAX}, unless otherwise noted. All typical values are at T_J = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCES						
REFADC Input Voltage Range	V_{REFADC}		+1.0		V_{AVDD}	V
REFADC Input Current	I_{REFADC}	V_{REFADC} = +2.5V, f_{SAMPLE} = 178ksps		60		µA
		Acquisition/between conversions		±0.01		
REFDAC Input Voltage Range	V_{REFDAC}		+0.50		+2.52	V
REFDAC Input Current				26		µA
DAC DC ACCURACY						
Resolution			12			Bits
Integral Nonlinearity	INL_{DAC}	Measured at FILT_		±1		LSB
Differential Nonlinearity	DNL_{DAC}	Measured at FILT_, guaranteed monotonic		±0.4	±1	LSB
POWER SUPPLIES						
Analog Supply Voltage	V_{AVDD}		+4.75		+5.25	V
Digital Supply Voltage	V_{DVDD}		+2.7		AV_{DD}	V
Negative Supply Voltage	$V_{GATEVSS}$, V_{AVSS}	$V_{GATEVSS}$ = V_{AVSS}	-5.50		-4.75	V
Analog Supply Current	I_{AVDD}	V_{AVDD} = +5.25V		2.8	5	mA
Digital Supply Current	I_{DVDD}	V_{DVDD} = +5.25V		1.5	5	mA
Negative Supply Current	$I_{GATEVSS}$ + I_{AVSS}	$V_{GATEVSS}$ = V_{AVSS} = -5.5V		1.1	1.7	mA
Analog Shutdown Current		V_{AVDD} = +5.25V		0.8		µA
Digital Shutdown Current		V_{DVDD} = +5.25V		0.2		µA
Negative Shutdown Current		$V_{GATEVSS}$ = V_{AVSS} = -5.5V		0.6		µA
SERIAL-INTERFACE SUPPLIES						
Input Voltage	V_{IL}				0.3 x DV_{DD}	V
	V_{IH}		0.7 x DV_{DD}			
Input Hysteresis	V_{HYS}			0.05 x DV_{DD}		V
Output Low Voltage	V_{OL}	BUSY: I_{SINK} = 0.5mA; DOUT, ALARM: I_{SINK} = 3mA			0.4	V
Output High Voltage	V_{OH}	SPI/$\overline{I2C}$ = DV_{DD}; BUSY: I_{SOURCE} = 0.5mA; DOUT, ALARM: I_{SOURCE} = 2mA	DV_{DD} - 0.5V			V
Input Current	I_{IN}			±0.01	±10	µA
Input Capacitance	C_{IN}			5		pF

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SPI-INTERFACE TIMING CHARACTERISTICS

(Note 9) (See Figure 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}		40			ns
SCLK High Time	t_{CH}		16			ns
SCLK Low Time	t_{CL}		16			ns
DIN to SCLK Rise Setup Time	t_{DS}		10			ns
DIN to SCLK Rise Hold Time	t_{DH}		0			ns
SCLK Fall to DOUT Transition	t_{DO}	C_L = 30pF			20	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DV}	C_L = 30pF (Note 3)			40	ns
$\overline{CS}$ Rise to DOUT Disable	t_{TR}	C_L = 30pF (Note 10)			40	ns
$\overline{CS}$ Rise or Fall to SCLK Rise	t_{CSS}		10			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}	(Note 3)	40			ns
Last SCLK Rise to $\overline{CS}$ Rise	t_{CSH}	(Note 3)	0			ns

I²C-INTERFACE SLOW-/FAST-MODE TIMING CHARACTERISTICS

(Note 9) (See Figure 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) for START Condition	$t_{HD;STA}$	After this period, the first clock pulse is generated	0.6			µs
Setup Time for a Repeated START Condition	$t_{SU;STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU;DAT}$		100			ns
Data Hold Time	$t_{HD;DAT}$	(Note 11)	0		0.9	µs
SDA, SCL Rise Time, Receiving	t_R	(Notes 3, 12)	0		300	ns
SDA, SCL Fall Time, Receiving	t_F	(Notes 3, 12)	0		300	ns
SDA Fall Time, Transmitting	t_F	(Notes 3, 12, 13)	20 + 0.1 x C_B		250	ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B	(Notes 3, 14)			400	pF
Pulse Width of Spikes Suppressed By the Input Filter	t_{SP}	(Note 15)			50	ns

I²C-WIRE-INTERFACE HIGH-SPEED-MODE TIMING CHARACTERISTICS

(Note 9) (See Figure 3.)

PARAMETER	SYMBOL	CONDITIONS	C_B = 100pF max		C_B = 400pF		UNITS
			MIN	MAX	MIN	MAX	
Serial Clock Frequency	f_{SCL}		0	3.4	0	1.7	MHz
Setup Time (Repeated) START Condition	$t_{SU;STA}$		160		160		ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160		160		ns
SCL Pulse-Width Low	t_{LOW}		160		320		ns
SCL Pulse-Width High	t_{HIGH}		60		120		ns
Data Setup Time	$t_{SU;DAT}$		10		10		ns
Data Hold Time	$t_{HD;DAT}$	(Note 11)	0	70	0	150	ns
SCL Rise Time	t_{RCL}	(Note 3)	10	40	20	80	ns
SCL Rise Time, After a Repeated START Condition and After an Acknowledge Bit	t_{RCL1}	(Note 3)	10	80	20	160	ns
SCL Fall Time	t_{FCL}	(Note 3)	10	40	20	80	ns
SDA Rise Time	t_{RDA}	(Note 3)	10	80	20	160	ns
SDA Fall Time	t_{FDA}	(Note 3)	10	80	20	160	ns
Setup Time for STOP Condition	$t_{SU;STO}$		160		160		ns
Capacitive Load for Each Bus Line	C_B	(Note 14)		100		400	pF
Pulse Width of Spikes Suppressed By the Input Filter	t_{SP}	(Note 15)	0	10	0	10	ns

MISCELLANEOUS TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Time to Wait After a Write Command Before Reading Back Data from the Same Location	t_{RDBK}	(Note 16)		1		µs
$\overline{CNVST}$ Active-Low Pulse Width in ADC Clock Mode 01	t_{CNV01}	(Note 3)	20			ns
$\overline{CNVST}$ Active-Low Pulse Width in ADC Clock Mode 11 to Initiate a Temperature Conversion	t_{CNV11}	(Note 3)	20			ns
$\overline{CNVST}$ Active-Low Pulse Width in ADC Clock Mode 11 for ADCIN1/2 Acquisition	t_{ACQ11A}	(Note 3)	1.5			µs
ADC Power-Up Time (External Reference)	t_{APUEXT}			0.8		µs
ADC Power-Up Time (Internal Reference)	t_{APUINT}			50		µs
DAC Power-Up Time (External Reference)	t_{DPUEXT}			2		µs
DAC Power-Up Time (Internal Reference)	t_{DPUINT}			50		µs
Acquisition Time (Internally Timed in ADC Clock Modes 00 or 01)	t_{ACQ}				0.6	µs
Conversion Time (Internally Clocked)	t_{CONV}				6.5	µs
Delay to Start of Conversion Time	t_{CONVW}	(Note 17)		1		µs
Temperature Conversion Time (Internally Clocked)	t_{CONVT}			30		µs

MISCELLANEOUS TIMING CHARACTERISTICS (continued)

Note 1: All current-sense amplifier specifications are tested after a current-sense calibration (valid when drain current = 0mA). See RCS Error vs. GATE Current in the *Typical Operating Characteristics*. The calibration is valid only at one temperature and supply voltage and must be repeated if either the temperature or supply voltage changes.

Note 2: The hardware configuration register's CH_OCM1 and CH_OCM0 bits are set to 0. See Table 10a. The max specification is limited by tester limitations.

Note 3: Guaranteed by design. Not production tested.

Note 4: At power-on reset, the output safe switch is closed. See the *ALMHCFG (Read/Write)* section.

Note 5: Integral nonlinearity is the deviation of the analog value at any code from its theoretical value after the gain and offset errors have been calibrated out.

Note 6: Offset nulled.

Note 7: Absolute range for analog inputs is from 0 to V_{AVDD}.

Note 8: Device and sensor at the same temperature. Verified by the current ratio (see the *Temperature Measurements* section).

Note 9: All timing specifications referred to V_{IH} or V_{IL} levels.

Note 10: D_{OUT} goes into tri-state mode after the $\overline{CS}$ rising edge. Keep $\overline{CS}$ low long enough for the DOUT value to be sampled before it goes to tri-state.

Note 11: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.

Note 12: t_R and t_F measured between 0.3 x DV_{DD} and 0.7 x DV_{DD}.

Note 13: C_B = total capacitance of one bus line in pF. For bus loads between 100pF and 400pF, the timing parameters should be linearly interpolated.

Note 14: An appropriate bus pullup resistance must be selected depending on board capacitance. For more information, refer to the I^2C documentation on the Philips website.

Note 15: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

Note 16: When a command is written to the serial interface, it is passed to the internal oscillator clock to be executed. There is a small synchronization delay before the new value is written to the appropriate register. If the user attempts to read the new value back before t_{RDBK}, no harm will be caused to the data, but the read command may not yet show the new value.

Note 17: This is the minimum time from the end of a command before $\overline{CNVST}$ should be asserted. The time allows for the data from the preceding write to arrive and set up the chip in preparation for the $\overline{CNVST}$. The time need only be observed when the write affects the ADC controls. Failure to observe this time may lead to incorrect conversions (for example, conversion of the wrong ADC channel).

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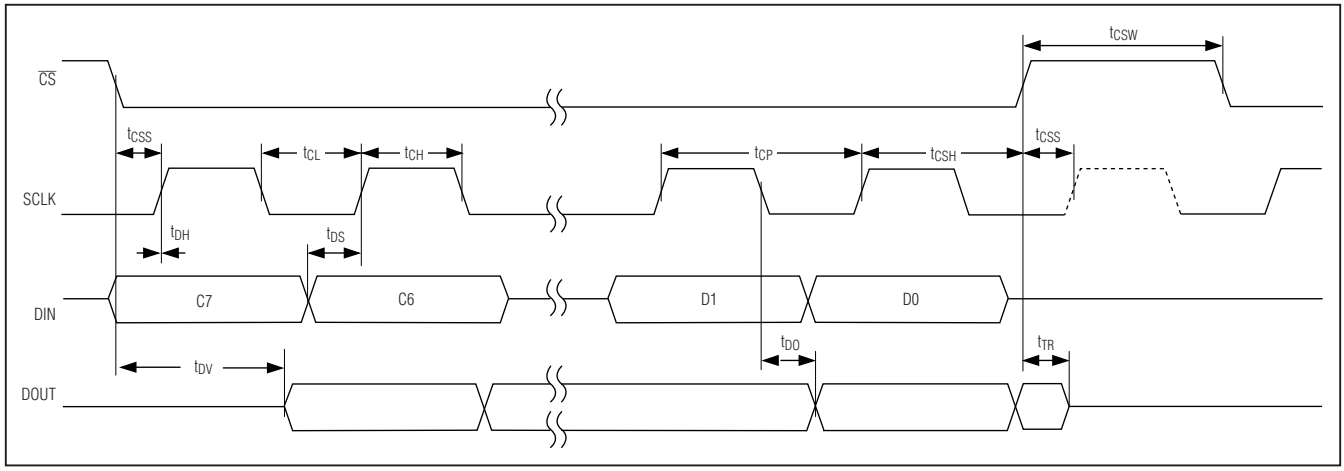


Figure 1. SPI Serial-Interface Timing Diagram

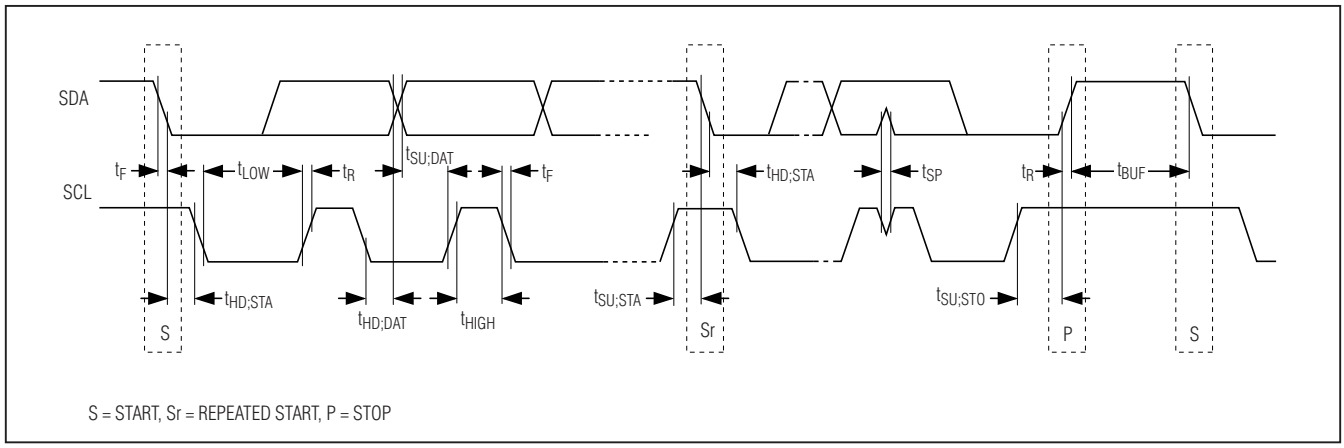


Figure 2. Slow-/Fast-Speed Timing Diagram

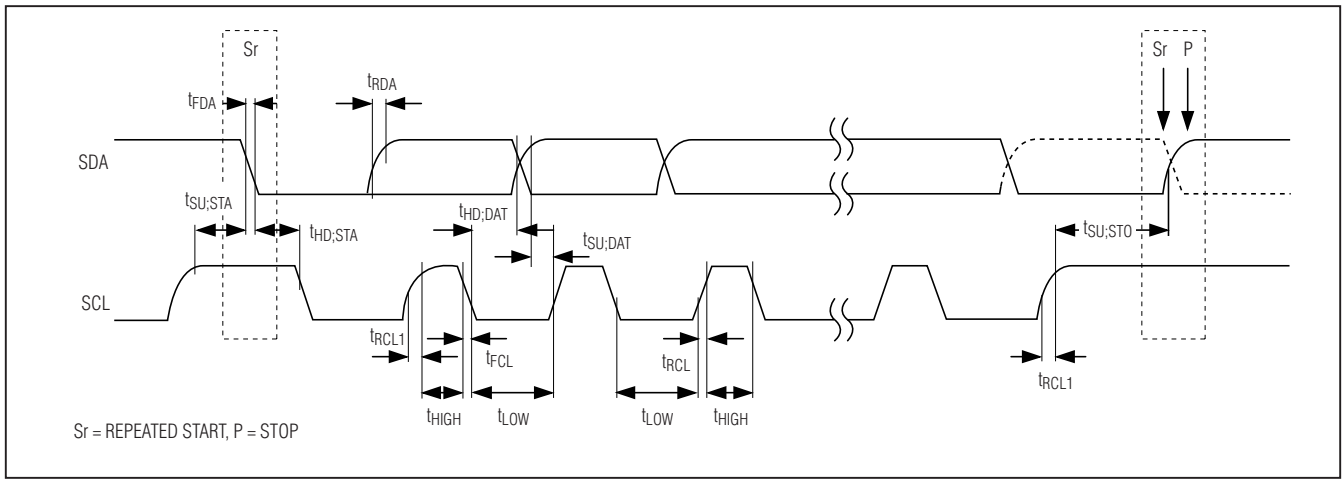
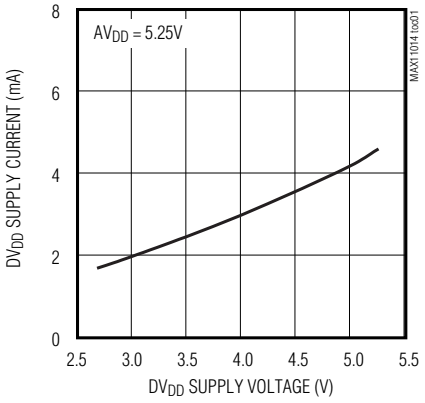


Figure 3. High-Speed Timing Diagram

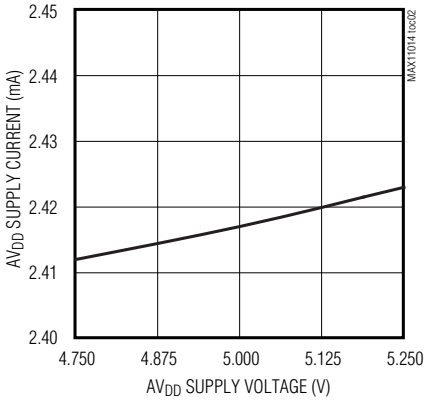
Typical Operating Characteristics

($V_{GATEVSS}$ = -5.5V; V_{AVDD} = V_{DVDD} = +5V, $GATEV_{SS}$ = AV_{SS} = -5V, external V_{REFADC} = +2.5V; external V_{REFDAC} = +2.5V; C_{REF} = 0.1µF; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

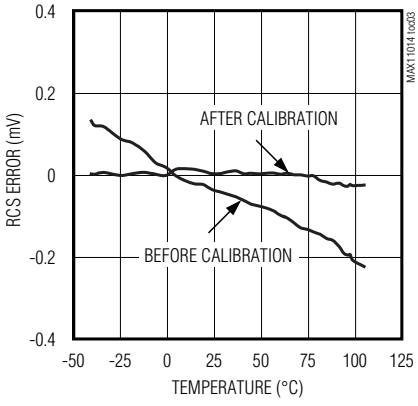
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



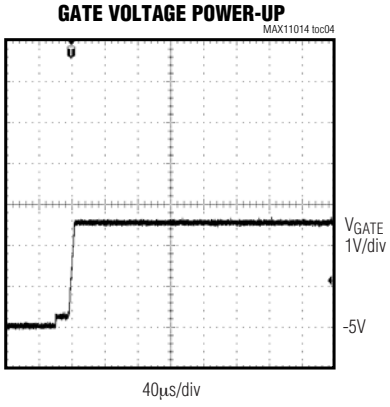
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



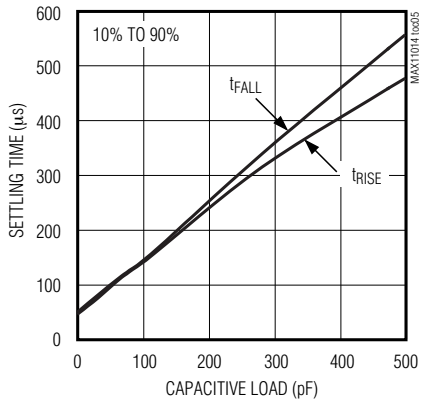
RCS ERROR vs. TEMPERATURE



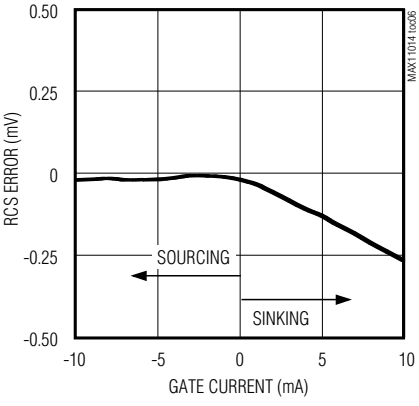
GATE VOLTAGE POWER-UP



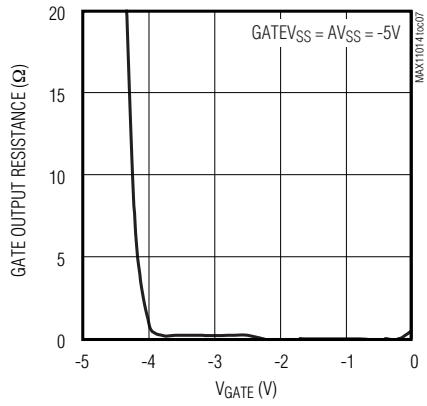
FILT1/FILT3 SETTLING TIME vs. FILT1/FILT3 CAPACITIVE LOAD



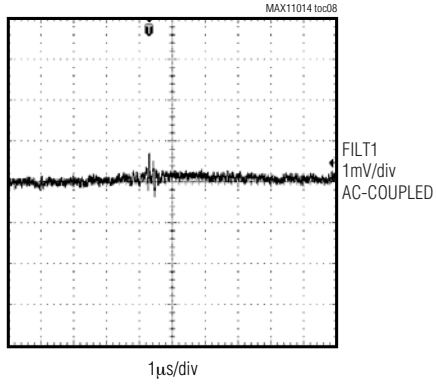
RCS ERROR vs. GATE CURRENT



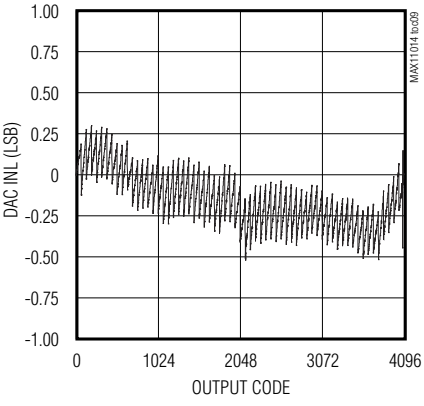
GATE OUTPUT RESISTANCE vs. GATE VOLTAGE



GLITCH IMPULSE



DAC INTEGRAL NONLINEARITY vs. OUPUT CODE

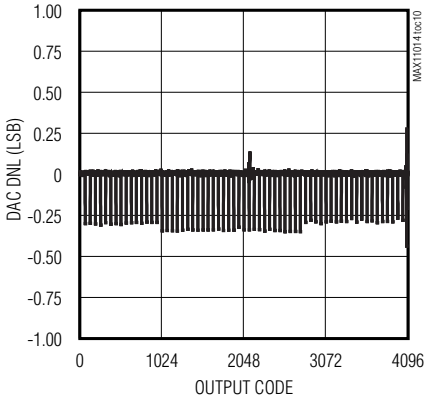


Automatic RF MESFET Amplifier Drain-Current Controllers

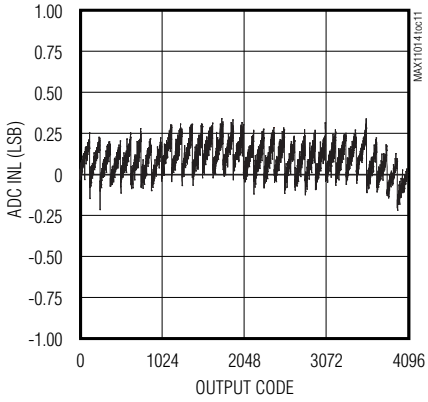
Typical Operating Characteristics (continued)

($V_{GATEVSS}$ = -5.5V; V_{AVDD} = V_{DVDD} = +5V, $GATEV_{SS}$ = AV_{SS} = -5V, external V_{REFADC} = +2.5V; external V_{REFDAC} = +2.5V; C_{REF} = 0.1µF; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

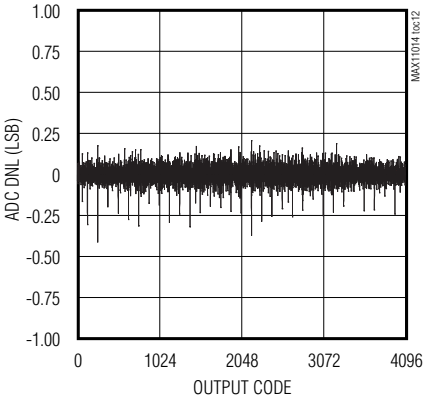
DAC DIFFERTIAL NONLINEARITY vs. OUTPUT CODE



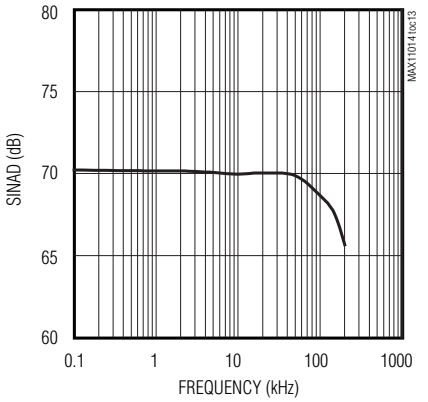
ADC INTEGRAL NONLINEARITY vs. OUTPUT CODE



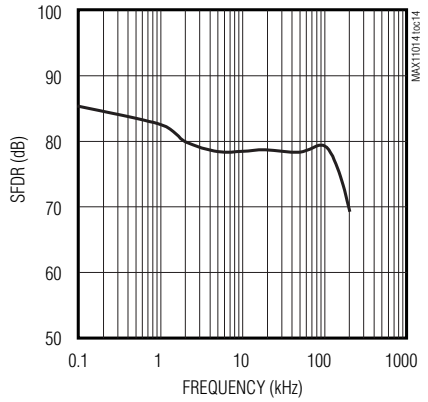
ADC DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



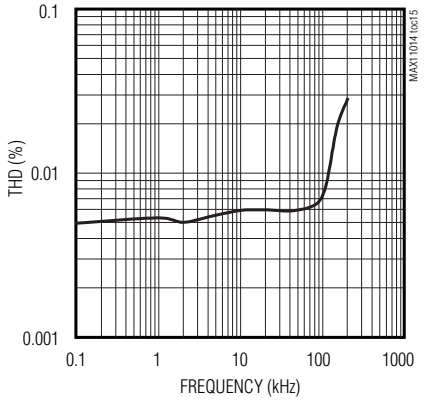
ADC SINAD vs. FREQUENCY



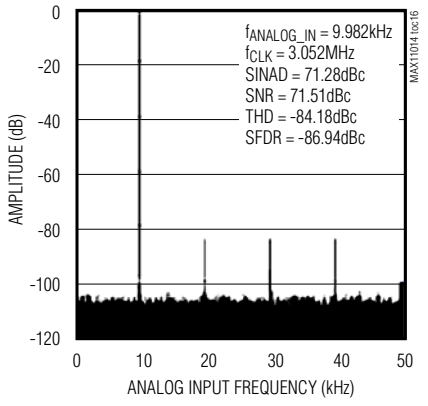
ADC SFDR vs. FREQUENCY



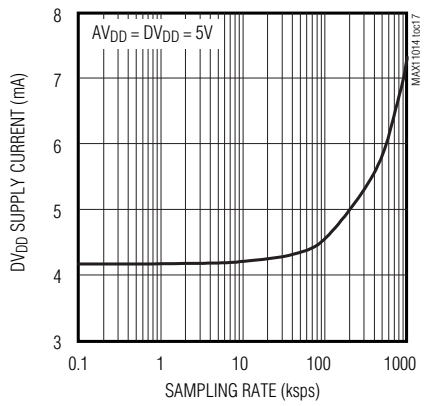
ADC TOTAL HARMONIC DISTORTION vs. FREQUENCY



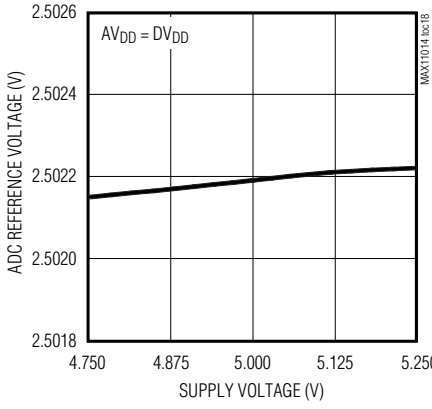
ADC FFT PLOT



DIGITAL SUPPLY CURRENT vs. SAMPLING RATE



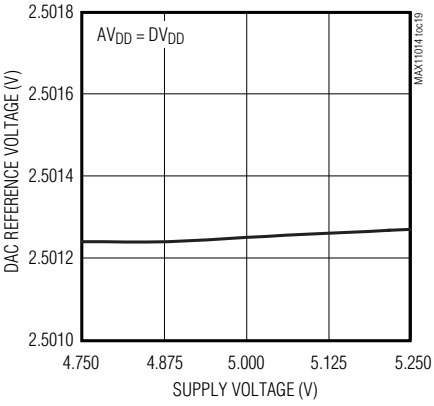
ADC INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



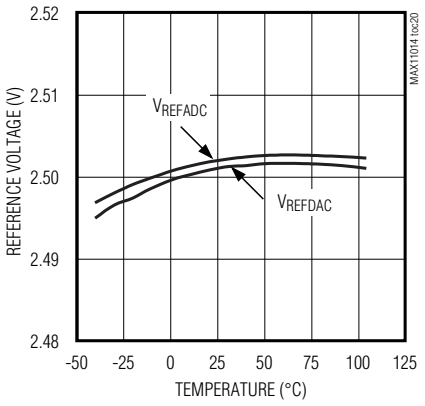
Typical Operating Characteristics (continued)

($V_{GATEVSS}$ = -5.5V; V_{AVDD} = V_{DVDD} = +5V, $GATEV_{SS}$ = AV_{SS} = -5V, external V_{REFADC} = +2.5V; external V_{REFDAC} = +2.5V; C_{REF} = 0.1µF; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

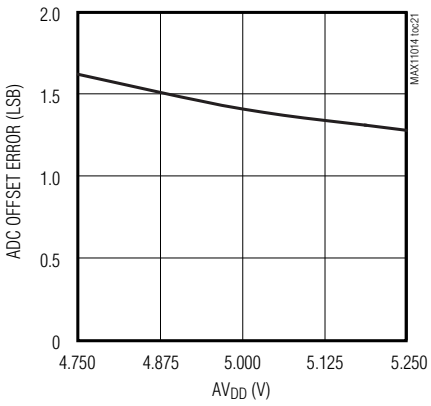
DAC INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



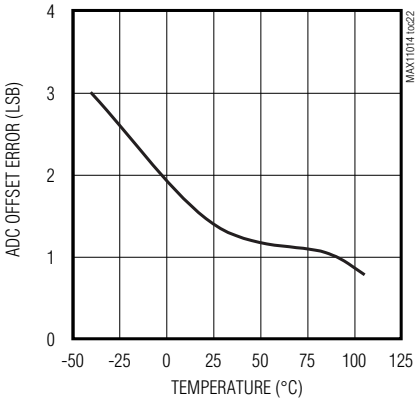
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



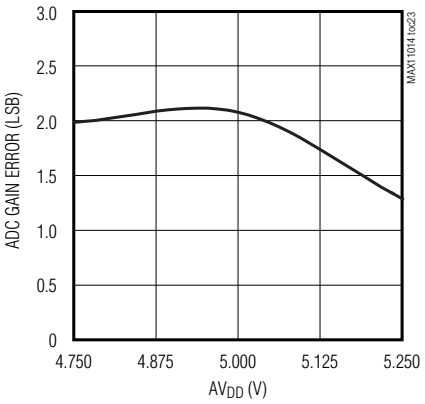
ADC OFFSET ERROR vs. ANALOG SUPPLY VOLTAGE



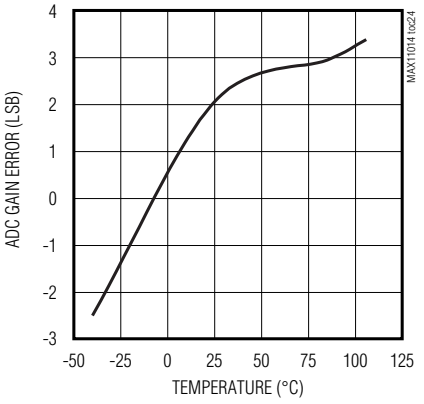
ADC OFFSET ERROR vs. TEMPERATURE



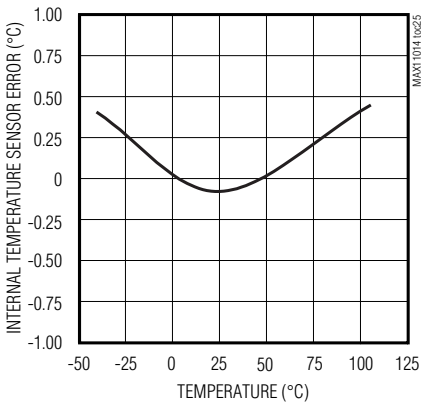
ADC GAIN ERROR vs. ANALOG SUPPLY VOLTAGE



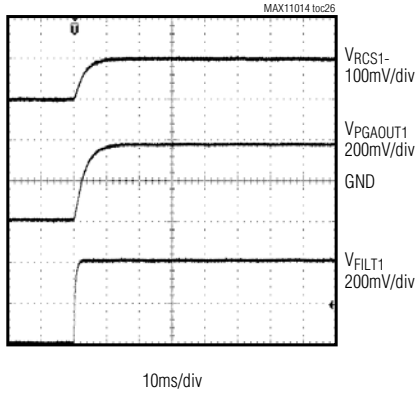
ADC GAIN EROR vs. TEMPERATURE



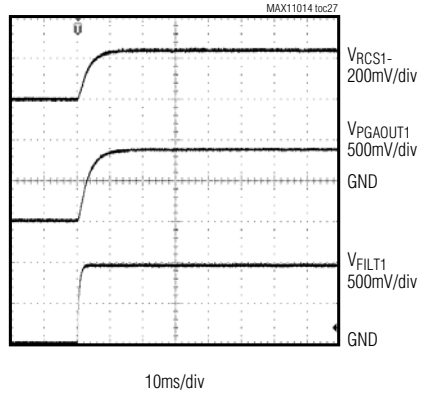
INTERNAL TEMPERATURE SENSOR ERROR vs. TEMPERATURE



0 TO 100mV V_{SENSE} TRANSIENT RESPONSE



0 TO 250mV V_{SENSE} TRANSIENT RESPONSE



Automatic RF MESFET Amplifier Drain-Current Controllers

Pin Description

PIN	NAME	FUNCTION
1	DIN/SDA	Serial Data Input. Data is latched into the serial interface on the rising edge of SCLK in SPI mode. Connect a pullup resistor to SDA in I^2C mode.
2	DOUT/A1	Serial Data Output in SPI Mode/Address Select 1 in I^2C Mode. Data transitions on the falling edge of SCLK. DOUT is high impedance when $\overline{CS}$ is high. Connect A1 to DV_{DD} or DGND to set the device address to I^2C mode.
3	ADCIN1	Analog Input 1
4	ADCIN2	Analog Input 2
5	DXN1	Remote-Diode Current Sink. Connect the emitter of a base-emitter junction remote npn transistor to DXN1.
6	DXP1	Remote-Diode Current Source. Connect DXP1 to the base/collector of a remote temperature-sensing npn transistor. **Do not leave DXP1 open**; connect to DXN1 if no remote diode is used.
7	DXN2	Remote-Diode Current Sink. Connect the emitter of a base-emitter junction remote npn transistor to DXN2.
8	DXP2	Remote-Diode Current Source. Connect DXP2 to the base/collector of a remote temperature-sensing npn transistor. **Do not leave DXP2 open**; connect to DXN2 if no remote diode is used.
9	REFDAC	DAC Reference Input/Output. Connect a 0.1µF capacitor to AGND in external reference mode. See the *HCFG (Read/Write)* section.
10	REFADC	ADC Reference Input/Output. Connect a 0.1µF capacitor to AGND in external reference mode. See the *HCFG (Read/Write)* section.
11, 27	AV_{DD}	Positive Analog Supply Voltage. Set AV_{DD} between +4.75V and +5.25V. Bypass with a 1µF and a 0.1µF capacitor in parallel to AGND.
12, 26	AGND	Analog Ground
13	ACLAMP2	MESFET2 External Clamping Voltage Input
14	GATE2	MESFET2 Gate Connection. See the *Gate-Drive Amplifiers* section.
15	$GATEV_{SS}$	Gate-Drive Amplifier Negative Power-Supply Input. Set $GATEV_{SS}$ between -4.75V and -5.5V. Connect externally to AV_{SS}. Bypass with a 1µF and a 0.1µF capacitor in parallel to AGND.
16, 28, 29, 34–37	N.C.	No Connection. Not internally connected.
17	ACLAMP1	MESFET1 External Clamping Voltage Input
18	GATE1	MESFET1 Gate Connection. See the *Gate-Drive Amplifiers* section.
19	FILT1	Channel 1 Filter 1 Input. See Figures 5 and 6.
20	FILT2	Channel 1 Filter 2 Input. See Figures 5 and 6.
21	FILT3	Channel 2 Filter 3 Input. See Figures 5 and 6.
22	FILT4	Channel 2 Filter 4 Input. See Figures 5 and 6.
23	PGAOUT1	Channel 1 Amplifier Voltage Output. See the *PGAOUT Outputs* section and Figures 5 and 6.
24	PGAOUT2	Channel 2 Amplifier Voltage Output. See the *PGAOUT Outputs* section and Figures 5 and 6.
25	AV_{SS}	Negative Analog Supply Voltage. Set AV_{SS} between -4.75V and -5.5V. Connect externally to $GATEV_{SS}$. Bypass with a 1µF and a 0.1µF capacitor in parallel to AGND.

Pin Description (continued)

PIN	NAME	FUNCTION
30	RCS2+	Channel 2 Current-Sense-Resistor Connection. Connect to the external supply powering channel 2's MESFET drain, in the range of +0.5V to +11V (MAX11014) or +5V to +32V (MAX11015). Bypass with a 1µF and a 0.1µF capacitor in parallel to AGND. If unused, connect to RCS1+.
31	RCS2-	Channel 2 Current-Sense-Resistor Connection. Connect to the channel 2 MESFET drain. Decouple as required by the application. If unused, connect to RCS2+.
32	RCS1-	Channel 1 Current-Sense-Resistor Connection. Connect to the channel 1 MESFET drain. Decouple as required by the application. If unused, connect to RCS1+.
33	RCS1+	Channel 1 Current-Sense-Resistor Connection. Connect to the external supply powering channel 1's MESFET drain, in the range of +0.5V to +11V (MAX11014) or +5V to +32V (MAX11015). Bypass with a 1µF and a 0.1µF capacitor in parallel to AGND. If unused, connect to RCS2+.
38	OPSAFE1	Operating Safe Channel 1 Input. Set OPSAFE1 high to clamp GATE1 to ACLAMP1 for fast protection of enhancement FET power transistors.
39	OPSAFE2	Operating Safe Channel 2 Input. Set OPSAFE2 high to clamp GATE2 to ACLAMP2 for fast protection of enhancement FET power transistors.
40	BUSY	BUSY Output. BUSY asserts high under certain conditions when the device is busy. See the *BUSY Output* section.
41	DV_{DD}	Digital Supply Voltage. Set DV_{DD} between +2.7V and AV_{DD}. Bypass with a 1µF and a 0.1µF capacitor in parallel to DGND.
42	DGND	Digital Ground
43	$\overline{CNVST}$	Active-Low Conversion Start Input. Set $\overline{CNVST}$ low to begin a conversion in clock modes 01 and 11. Connect $\overline{CNVST}$ to DV_{DD} when issuing conversion commands through the serial interface.
44	ALARM	ALARM Output. ALARM asserts when the temperature or voltage measurements exceed their preset high or low thresholds.
45	$\overline{CS}$/A0	Chip-Select Input in SPI Mode/Address Select 0 in I^2C Mode. $\overline{CS}$ is an active-low input. When $\overline{CS}$ is low, the serial interface is enabled. When $\overline{CS}$ is high, DOUT is high impedance. Connect A0 to DV_{DD} or DGND to set the device address in I^2C mode.
46	SPI/$\overline{I2C}$	SPI-/I^2C-Interface Select Input. Connect SPI/$\overline{I2C}$ to DV_{DD} to select SPI mode. Connect SPI/$\overline{I2C}$ to DGND to select I^2C mode.
47	N.C./A2	No Connection in SPI Mode/Address Select 2 in I^2C Mode. Connect A2 to DV_{DD} or DGND to set the device address in I^2C mode.
48	SCLK/SCL	Serial Clock Input. Clocks data in and out of the serial interface. (Duty cycle must be 40% to 60%.) Connect a pullup resistor to SCL in I^2C mode. See Table 10 for details on programming the clock mode.
—	EP	Exposed Pad. Connect to AGND and a large copper plane to meet power dissipation specifications. Do not use as a ground connection.

Automatic RF MESFET Amplifier Drain-Current Controllers

Detailed Description

The MAX11014/MAX11015 set and monitor the bias conditions for dual MESFET power devices found in cellular base stations and point-to-point microwave links. The internal DAC sets the voltage across the current-sense resistor by controlling the GATE voltage. These devices integrate a 12-bit ADC to measure voltage, internal and external temperature, and communicate through a 4-wire 20MHz SPI-/MICROWIRE-compatible serial interface or 2-wire 3.4MHz I^2C-compatible serial interface (pin-selectable).

The MAX11014/MAX11015 operate from an internal +2.5V reference or individual ADC and DAC external references. The external current-sense resistors monitor voltages over the 0 to (V_{DACREF} / 4) range. Two current-sense amplifiers with a preset gain of four monitor the voltage across the sense resistors. The MAX11014/MAX11015 accurately measure their internal die temperature and two external remote diode temperature sensors. The remote pn junctions are typically the base-emitter junction of an npn transistor, either discrete or integrated on a CPU, FPGA, or ASIC.

The MAX11014/MAX11015 also feature an ALARM output that can be triggered during an internal or external overtemperature condition, an excessive current-sense voltage, or an excessive GATE voltage. Figure 4 shows the MAX11014's functional diagram.

The MAX11014 integrates complete dual analog closed-loop drain-current controllers for Class A MESFET amplifier operation. See the *MAX11014 Class A Control Loop* section. The analog control loop sets the drain current through the current-sense resistors. The MESFET gate-drive amplifier can vary the DAC code accordingly if the temperature or other system variables change.

Implement Class A amplifier operation with the following three steps:

1) Characterization

   Characterize the MESFET over temperature to determine the amplifier's set of drain-current values, assuming the part-to-part calibration curve is consistent. There may be an offset shift, but no important change in the shape of the function. Load these values into the MAX11014 LUTs at power-up. In operation, there is a linear interpolation between the values stored in the LUTs.

   Adjust the drain current for other variables such as output power or drain voltage by loading values into the numerical KLUTs.

2) Calibration

   In production of the power amplifier, measure the quiescent drain current at a fixed calibration temperature (probably room) and adjust the $V_{SET(CODE)}$ value until the drain current is within the specified limits for that temperature. The $V_{SET(CODE)}$ value is stored for loading after power-up. Prior to operation, command a PGA calibration after powering up by writing to the PGA calibration control register, setting the TRACK bit to 0 and the DOCAL bit to 1 (see Table 18).

3) Operation

   Upon request, the MAX11014 measures the temperature of the MESFET and compares it with the previous reading. If the temperature reading has changed, the MAX11014 reads the LUTs with the characterization data and updates the DAC to correct the drain current. Setting the TRACK, DOCAL, and SELFTIME bits to 1 in the PGA calibration control register starts automatic monitoring and adjustment of drain current for variations in temperature.

Also, if the KLUTs are used, their values are monitored for changes. A DAC correction is then made if necessary.

For Class AB operation with the MAX11015, measure the MESFET temperature and set the GATE_ voltage through the LUTs and DAC to control the drain current. See the *MAX11015 Class AB Control* section. Implement Class AB amplifier operation with the same three steps as Class A operation, with the exception that the LUTs set the GATE_ voltage for constant drain current with varying temperature.

Power-On Reset

On power-up, the MAX11014/MAX11015 are in full power-down mode (see the *SHUT (Write)* section). To change to normal power mode, write two commands to the shutdown register. Set the FULLPD bit to 0 (other bits in the shutdown register are ignored) on the first command. A second command to this register then activates the internal blocks.

MAX11014 Class A Control Loop

The MAX11014 is designed to set and continuously control the drain current for MESFET power amplifiers configured to operate in Class A. Set the DAC code to control the voltage across the RCS_+ and RCS_- current-sense resistor connections. The MAX11014 internal control loop automatically keeps the voltage across the current-sense resistor to the value set by the DAC. See the *12-Bit DAC* section.

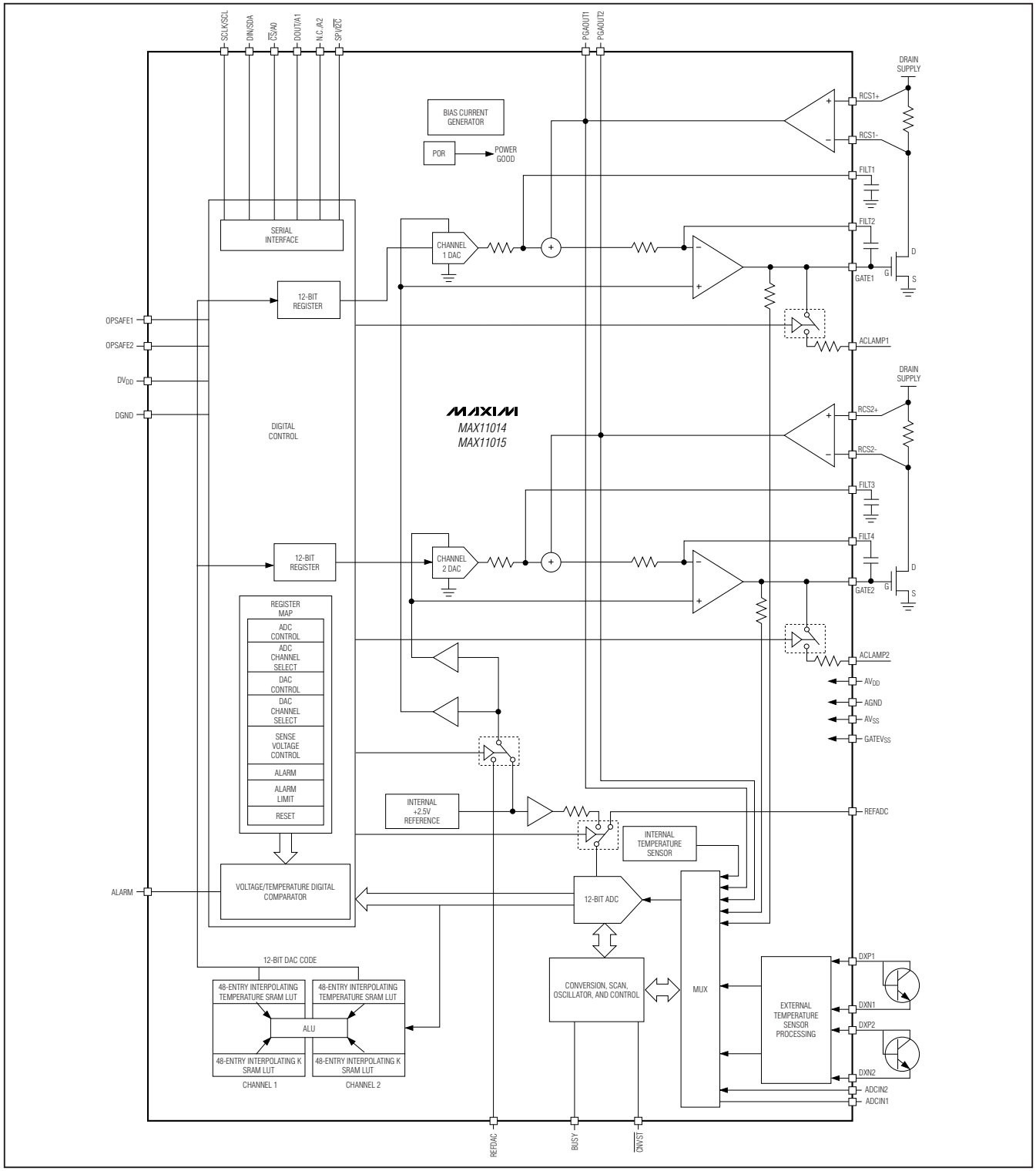


Figure 4. Functional Diagram

Automatic RF MESFET Amplifier Drain-Current Controllers

Once the control loop has been set, the MAX11014 automatically maintains the drain-current value. Figure 5 details the amplifiers that bias the channel 1 and channel 2 control loops.

The dual current-sense amplifiers amplify the voltage between RCS_+ and RCS_- by four and add an offset voltage (+12mV nominally). These current-sense amplifiers amplify sense voltages between 0 and 625mV when V_{REFDAC} = +2.5V. See the *Current-Sense Amplifiers* section.

The current-sense amplifier output injects a scaled-down replica of the MESFET drain current at the summing node to complete the internal analog feedback loop. The summing node drives the gate-drive amplifier through a 100kΩ series resistor. The gate-drive amplifier is configured as an integrator by the external capacitor connected between GATE1/GATE2 and FILT2/FILT4. The gate-drive amplifier includes automatic offset cancellation between 0 and 24mV to null the 12mV offset from the current-sense amplifier. See the *Register Descriptions* and *PGACAL (Write)* sections.

The MAX11014's analog control loop setpoint is described by the following equation:

$$V_{RCS\_+} - V_{RCS\_-} = \frac{V_{FILT}(CODE = 000h) - V_{FILT}}{4}$$

where:

$V_{FILT}(CODE = 000h)$ = V_{FILT1} (channel 1) and V_{FILT3} (channel 2) when the THRUDAC1/THRUDAC2 register code is set to 000h.

V_{FILT} = V_{FILT1} (channel 1) and V_{FILT3} (channel 2).

V_{RCS_+} - V_{RCS_-} = the voltage drop across the current-sense resistor.

Connect a capacitor from FILT2 to GATE1 to form an integrator (setting the control-loop dominant pole) with the channel 1 internal 100kΩ resistor. Connect a capacitor from FILT4 to GATE2 to form an integrator (setting the control-loop dominant pole) with the channel 2 internal 100kΩ resistor. The gate-drive amplifier's output drives the MESFET gates. See the *Gate-Drive Amplifiers* section.

The channel 1 DAC voltage is output to FILT1 through a series 580kΩ resistor. The channel 2 DAC voltage is output to FILT3 through a series 580kΩ resistor. Connect a capacitor from FILT1 to AGND and FILT3 to AGND to set the filter's time constant for the respective channel.

MAX11015 Class AB Control

The MAX11015 is designed to be used with a Class AB amplifier configuration to independently measure the drain current and set the GATE_ output voltages through the serial interface. After sensing the drain current with no RF signal applied, set the DAC code to obtain the desired GATE_ voltage. Figure 6 details the amplifiers that bias the channel 1 and channel 2 control.

The MAX11015 internal 12-bit DAC voltage is applied to the gate-drive amplifier, which has a preset gain of -2. See the *Gate-Drive Amplifiers* section. Setting the DAC code between FFFh and 000h typically produces a GATE_ voltage between 0 and (-2 x V_{REFDAC}). See the *HCFG (Read/Write)* section for details on adjusting the GATE_ maximum voltage.

The channel 1 DAC voltage is output to FILT1 through a series 580kΩ resistor. The channel 2 DAC voltage is output to FILT3 through a series 580kΩ resistor. Connect a capacitor from FILT1 to AGND and FILT3 to AGND to set the filter's time constant for the respective channel. Connect FILT2 and FILT4 to AGND (MAX11015 only).

The dual current-sense amplifiers amplify the voltage between RCS_+ and RCS_- by four and add an offset voltage (+12mV nominally). The current-sense amplifiers amplify sense voltages between 0 and 625mV when V_{REFDAC} = +2.5V. See the *Current-Sense Amplifiers* section.

Current-Sense Amplifiers

The dual current-sense amplifiers amplify the voltage between RCS_+ and RCS_- and add an offset voltage. Connect a resistor between RCS_+ and RCS_- to sense the MESFET drain current. The current-sense amplifiers scale the sense voltage by four. These amplifiers also reject the drain supply voltage that appears as a DC common-mode level on the current signal.

The gate-drive amplifier includes automatic offset cancellation between 0 and 24mV to null the 12mV offset from the current-sense amplifier. See the *PGACAL (Write)* section.

Gate-Drive Amplifiers

The gate-drive amplifiers control the MESFET gate bias settings. The MAX11014's channel 1 and channel 2 DAC voltages are routed through a summing node and into the gate-drive amplifiers. The MAX11015's channel 1 and channel 2 DAC voltages are routed directly to the gate-drive amplifiers, which have a preset gain of -2. See the *12-Bit DAC* section for details on setting the DAC codes.

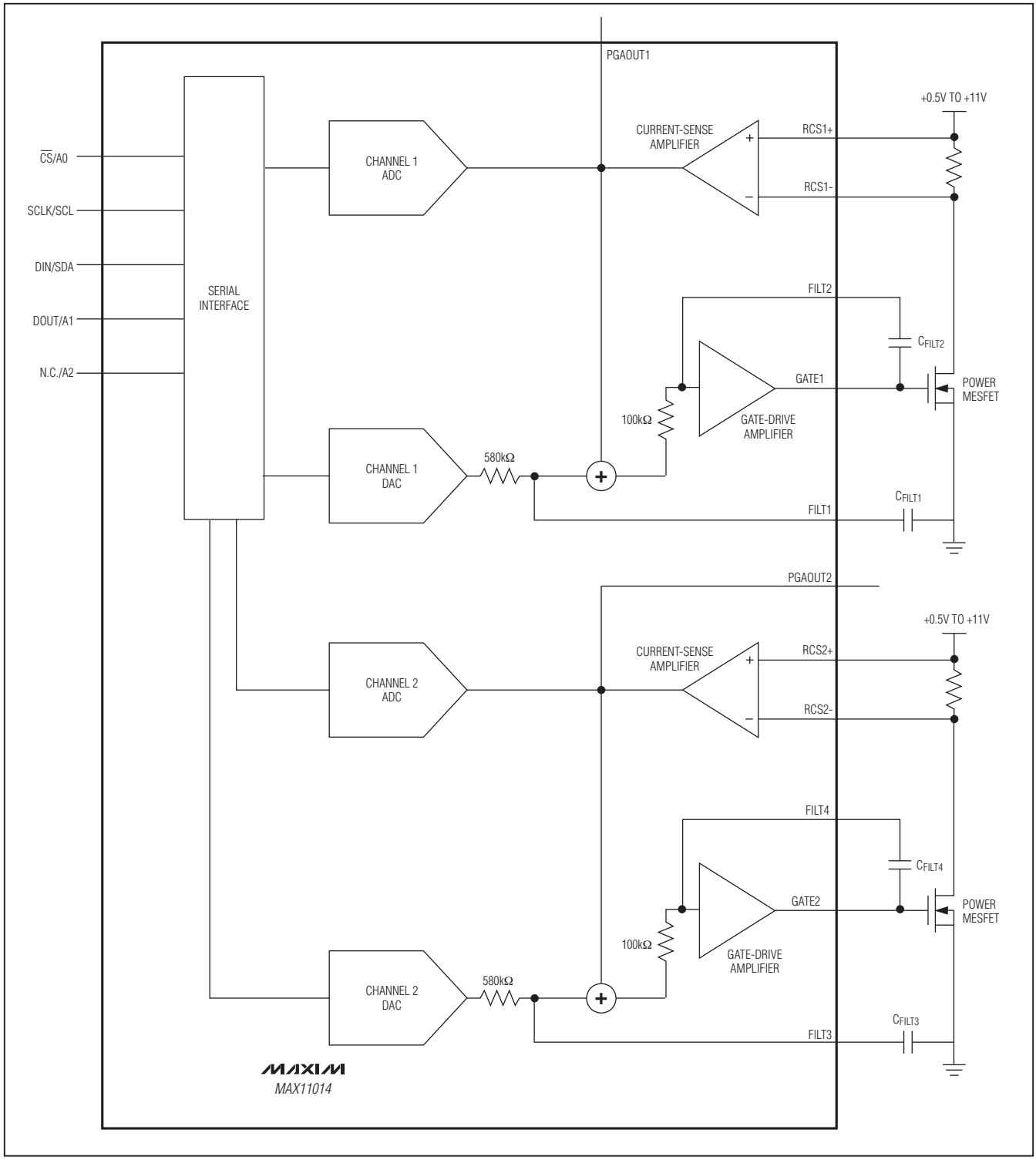


Figure 5. MAX11014 Class A Analog Control Loop

Automatic RF MESFET Amplifier Drain-Current Controllers

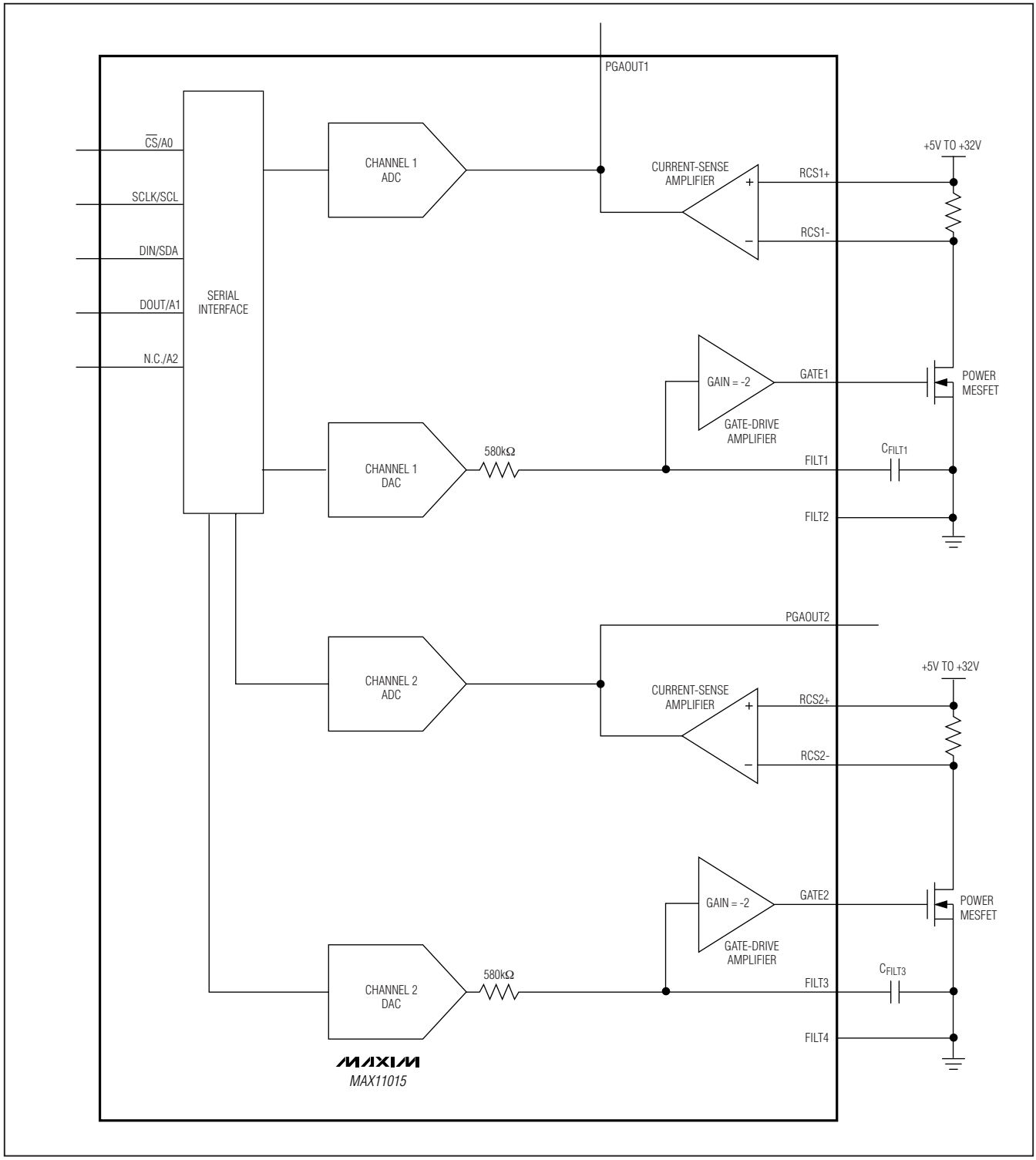


Figure 6. MAX11015 Class AB Analog Control

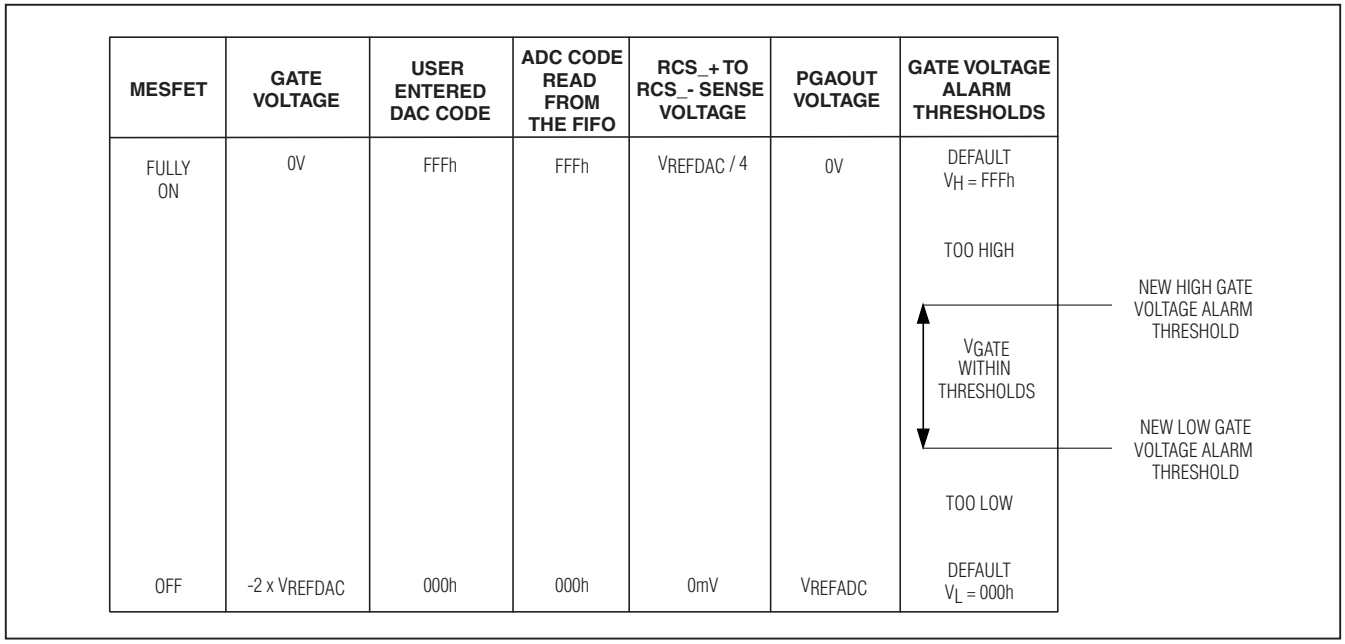


Figure 7. DAC Code Range

Connect the MESFET drain to the RCS_- input. Connect the MESFET's gate to the GATE_ output. Set the GATE_ voltage to -2 x V_{REFDAC} to turn the MESFET fully off. Set the GATE_ voltage to 0V to turn the MESFET fully on. See Figure 7.

The MAX11014/MAX11015 GATE_ output voltage can be clamped to the external voltage applied at ACLAMP_. Setting OPSAFE_ high clamps the GATE_ voltage unconditionally. The GATE_ can also be clamped by different commands issued through the serial interface. These devices can also monitor the alarms through the software to modify the clamping mechanism. See the *Automatic GATE Clamping* and *ALMHCFG (Read/Write)* sections.

12-Bit ADC Description

The MAX11014/MAX11015 ADCs use a fully differential successive-approximation register (SAR) conversion technique and on-chip track-and-hold (T/H) circuitry to convert temperature and voltage signals into 12-bit digital results. The analog inputs accept single-ended input signals. Single-ended signals are converted using a unipolar transfer function. See the *ADC Transfer Function* section for more details.

The internal ADC block converts the results of the internal die temperature, remote diode temperature readings, current-sense voltages, and ADCIN_ voltages. The ADC block also reads back the GATE_ analog output voltage and converts it to a 12-bit digital result. The conversion results are written to the FIFO memory. The FIFO holds up to 15 words (each word of 16 bits) with a leading 4-bit channel tag to indicate which channel the 12-bit data comes from. See Table 25. The FIFO reads back data words either one at a time or continuously. See the *ADCCON (Write)* section. The FIFO always stores the most recent conversion results and allows the oldest data to be overwritten. The FIFO indicates an overflow condition and underflow condition (read of an empty FIFO) through the flag register. See the *FLAG (Read)* section.

Analog Input Track and Hold

The equivalent circuit of Figure 8 details the MAX11014/MAX11015's ADCIN_ input architecture. In track mode, a positive input capacitor is connected to ADCIN1/ADCIN2. A negative input capacitor is connected to AGND. After the T/H enters hold mode, the difference between the sampled input voltages and AGND is converted. The input-capacitance charging rate determines the time required for the T/H to acquire an input signal. The required acquisition time lengthens with the increase of the input signal's source impedance. Any source impedance below 300Ω does not significantly affect the ADC's AC performance. A high-impedance source can be accommodated either by placing a 1µF capacitor between ADCIN_ and AGND. The combination of the analog-input source impedance and the capacitance at the analog input creates an RC

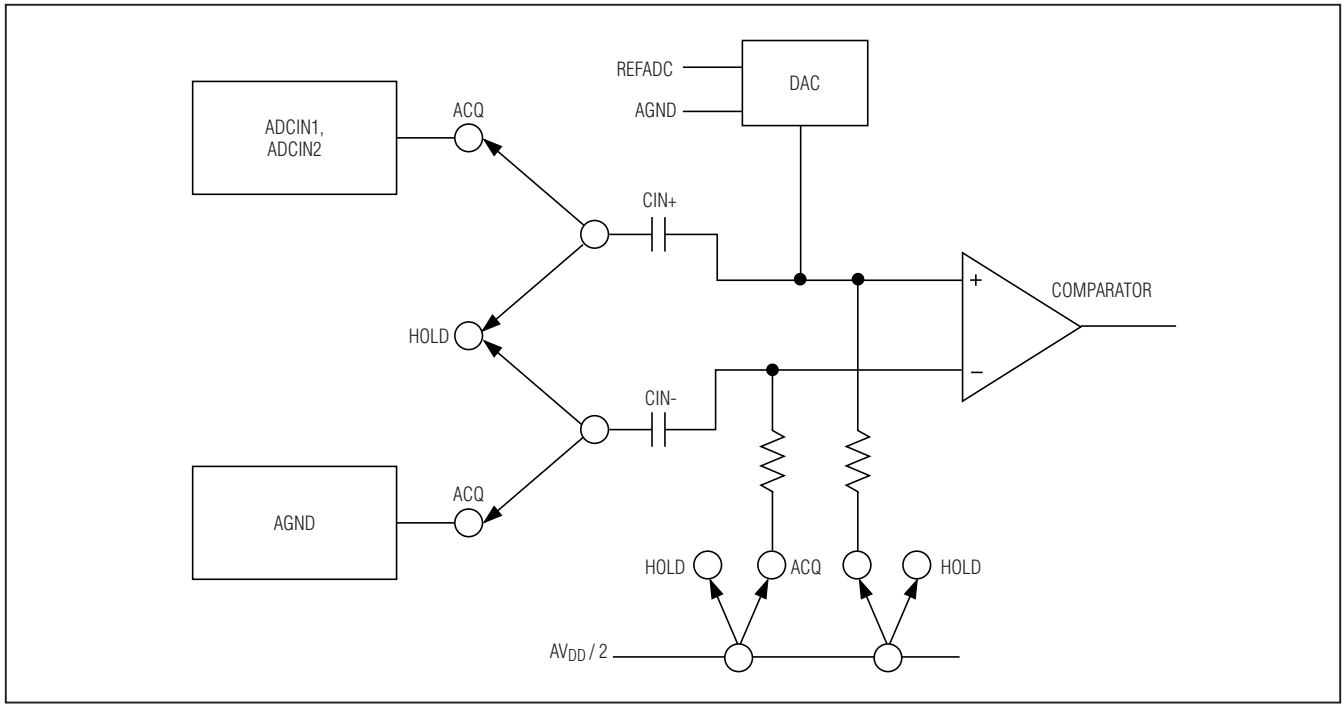


Figure 8. ADC Equivalent Input Circuit

filter that limits the analog-input bandwidth.

Analog Input Protection

Internal ESD protection diodes clamp ADCIN1/ADCIN2 to AV_{DD} and AGND, allowing them to swing from (AGND - 0.3V) to (AV_{DD} + 0.3V) without damage. However, for accurate conversions near full scale, the inputs must not exceed AV_{DD} by more than 50mV or be lower than AGND by 50mV. If an analog input voltage exceeds the supplies, limit the input current to 2mA.

Temperature Measurements

The MAX11014/MAX11015 measure their internal die temperature and two external remote-diode temperatures. Write to the ADC conversion register to command a temperature conversion. See Table 19. Set the CH6 bit to 1 to calculate the remote-diode DXP2/DXN2 temperature sensor reading and load the data into the FIFO. Set the CH1 bit to 1 to calculate the remote-diode DXP1/DXN1 temperature-sensor reading and load the data into the FIFO. Set the CH0 bit to 1 to calculate the internal die temperature-sensor reading and load the data into the FIFO. Temperature data is output in signed two's-complement format at DOUT in SPI mode and SDA in I^2C mode. See Figure 22 for the temperature transfer function.

The MAX11014/MAX11015 perform internal temperature measurements with a diode-connected transistor. The diode bias current changes from 66µA to 4µA to produce a temperature-dependent bias voltage difference. The second conversion result at 4µA is subtracted from the first at 66µA to calculate a digital value that is proportional to absolute temperature. The stored data result is the above digital code minus an offset to adjust from Kelvin to Celsius. The reference voltage for the temperature measurements is derived from the internal reference source to ensure the temperature calibration of 1 LSB corresponding to +0.125°C.

For external temperature readings, connect an npn transistor between DXP_ and DXN_. Connect the base and collector together as shown in Figure 4 to form a base-emitter pn junction. The MAX11014/MAX11015 feature an ALARM output that trips when the internal or external temperature rises above an upper threshold value or drops below a lower threshold value. Set the high and low temperature thresholds through the channel 1/channel 2 high/low temperature ALARM threshold registers. See Tables 3, 4, and 5.

The temperature-sensing circuits power up for the first temperature measurement in an ADC conversion scan. The temperature-sensing block remains on until the end of the scan to avoid an additional 50µs power-up delay for each individual temperature channel. See the

ADCCON (Write) section, Figure 31, and Figure 32. The temperature-sensor circuits remain powered up when the ADC conversion register's continuous convert bit (CONCONV) is set to 1 and the current ADC conversion includes a temperature channel. The temperature-sensor circuits remain powered up until the CONCONV bit is set low.

The external temperature sensor drive current ratio has been optimized for a 2N3904 npn transistor with an ideality factor of 1.0065. The nonideality offset is removed internally by a preset digital coefficient. Using a transistor with a different ideality factor produces a proportionate difference in the absolute measured temperature. For more details on this topic and others related to using an external temperature sensor, see Application Note 1057: *Compensating for Ideality Factor and Series Resistance Differences between Thermal Sense Diodes* and Application Note 1944: *Temperature Monitoring Using the MAX1253/54 and MAX1153/54* on Maxim's website: **www.maxim-ic.com**.

12-Bit DAC

The MAX11014/MAX11015 include two voltage-output, 12-bit monotonic DACs with ±1 LSB integral nonlinearity error and ±0.4 LSB differential nonlinearity error. The DAC operates from the internal +2.5V reference or an external reference voltage supplied at REFDAC. When using an external voltage reference, bypass REFDAC with a 0.1µF capacitor to AGND. The REFDAC external voltage range is +0.7V to +2.5V.

The MAX11014's channel 1/channel 2 DACs set the sense voltage between RCS_+ and RCS_- by controlling the GATE_ bias. See the *MAX11014 Class A Control Loop* section. The MAX11015's channel 1/channel 2 DACs drive the GATE_ outputs directly, independent of the current-sense voltages, through the gate-drive amplifier with a gain of -2. See the *MAX11015 Class AB Control* section.

Set the channel 1/channel 2 DAC code by writing to the respective channel's DAC input registers, DAC input and output registers, or V_{SET} registers. Write to the DAC input registers (Table 16) and use a subsequent write to the software load DAC register (Table 21) to control the timing of the update. Write to the DAC input and output registers (Table 17) to set the DAC output voltage code directly, independent of the software load DAC register bits. Write to the V_{SET} registers (Table 14) to include LUT data in the DAC code. Writing to the V_{SET} registers triggers a $V_{DAC(CODE)}$ calculation as shown in the following equation:

$$V_{DAC(CODE)} = V_{SET(CODE)} = (1 + LUT_K[K] \times LUT_{TEMP}[TEMP])$$

where

$V_{DAC(CODE)}$ = The modified channel 1/channel 2 12-bit DAC code.

$V_{SET(CODE)}$ = The 12-bit DAC code written to the channel 1 /channel 2 V_{SET} registers.

$LUT_K[K]$ = The interpolated, fractional 12-bit KLUT value. The KLUT data is derived from a variety of sources, including: the V_{SET} register value, the K parameter register value, or various ADC channels. See the *SRAM LUTs* section.

$LUT_{TEMP}[TEMP]$ = The interpolated, fractional 12-bit two's-complement temperature LUT value. The temperature LUT data is derived from either internal or external temperature values. See the *SRAM LUTs* section.

The $V_{DAC(CODE)}$ equation code is then loaded into the DAC input register or DAC output register, depending on the corresponding channel's LDAC bit in the software configuration register. See Table 11.

Self-Calibration

Calibrate channel 1 and channel 2 by writing to the PGA calibration control register. The MAX11014/MAX11015 function after power-up without a calibration. However, for best performance after powering up, command a calibration by setting the TRACK bit to 0 and the DOCAL bit to 1 (see Table 18). Subsequently, set the TRACK, DOCAL, and SELFTIME bits to 1 to minimize loss of performance over temperature and supply voltage.

The self-calibration algorithm cancels offsets at the gate-drive amplifier inputs in approximately 95µV increments to improve accuracy. The self-calibration routine can be commanded when the DACs are powered down, but the results will not be accurate. For best results, run the calibration after the DAC power-up time, t_{DPUEXT}. The ADC's operation is suspended during a self-calibration. The end of the self-calibration routine is indicated by the BUSY output returning low. See the *BUSY Output* section. Wait until the end of the self-calibration routine before requesting an ADC conversion.

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ADC/DAC References

The MAX11014/MAX11015 provide an internal low-noise +2.5V reference for the ADCs, DACs, and temperature sensors. Set bits D3–D0 within the hardware configuration register to control the source of the DAC and ADC references. See Tables 10c and 10d.

Connect a voltage source to REFADC between +1.0V and AV_{DD} in external ADC reference mode. Connect a voltage source to REFDAC between +0.7V to +2.5V in external DAC reference mode. When using an external voltage reference, bypass REFADC and REFDAC with 0.1µF capacitors to AGND.

Power Supplies

The MAX11014/MAX11015 operate from separate analog and digital power supplies. Set the analog supply voltage, AV_{DD}, between +4.75V and +5.25V. Set the digital supply voltage, DV_{DD}, between +2.7V and AV_{DD}. Bypass AV_{DD} with a 0.1µF and 1µF capacitor to AGND and DV_{DD} with a 0.1µF and 1µF capacitor to DGND. The analog circuitry typically consumes 2.8mA of supply current and the digital circuitry 3.7mA.

Set the negative analog supply voltages, AV_{SS} and $GATEV_{SS}$, between -4.75V and -5.5V. Connect AV_{SS} and $GATEV_{SS}$ together externally. Bypass each of these negative supplies with a 0.1µF and 1µF capacitor to AGND.

The RCS_+ inputs supply the power to the input section of the current-sense amplifiers. Set RCS_+ between +0.5V and +11V on the MAX11014 and +5V to +32V on the MAX11015. Bypass RCS_+ with a 0.1µF and 1µF capacitor to AGND.

Serial Interface

The MAX11014/MAX11015 feature a pin-selectable I^2C/SPI serial interface. Connect SPI/$\overline{I2C}$ to DGND to select I^2C mode, or connect SPI/$\overline{I2C}$ to DV_{DD} to select SPI mode. SDA and SCL (I^2C mode) and DIN, SCLK, and $\overline{CS}$ (SPI mode) facilitate communication between the MAX11014/MAX11015 and the master.

SPI Compatibility (SPI/$\overline{I2C}$ = DV_{DD})

The MAX11014/MAX11015 communicate through a serial interface, compatible with SPI and MICROWIRE devices. For SPI, ensure that the SPI bus master (typically a µC) runs in master mode so it generates the serial clock signal. Set the SCLK frequency to 20MHz or less, and set the clock polarity (CPOL) and phase (CPHA) in the µC control registers to the same value. The MAX11014/MAX11015 operate with SCLK idling high or low, and thus operate with CPOL = CPHA = 0 or CPOL = CPHA = 1. Set $\overline{CS}$ low to latch input data at DIN on the rising edge of SCLK. Output data at DOUT is updated on the falling edge of SCLK. See Figure 1. Temperature values are available in signed two's-complement format, while all others are in straight binary.

A high-to-low transition on $\overline{CS}$ initiates the 24-bit data input cycle. Once $\overline{CS}$ is low, write an 8-bit command byte (MSB first) at DIN to indicate which internal register is being accessed. The command byte also identifies whether the data to follow is to be written into the serial interface or read out. See the *Register Descriptions* section. After writing the command byte, write two data bytes at DIN or read two data bytes at DOUT. Keep $\overline{CS}$ low throughout the entire 24-bit word write. The serial-interface circuitry is common to the ADC and DAC sections.

When writing data, write an 8-bit command word and 16 data bits at DIN. See Figure 9. Data is input to the serial interface on the rising edge of SCLK. When reading data, write an 8-bit command byte at DIN and read the following 16 data bits at DOUT. See Figure 10. Data transitions at DOUT on the falling edge of SCLK. DIN can be set high or low while data is being transferred out at DOUT.

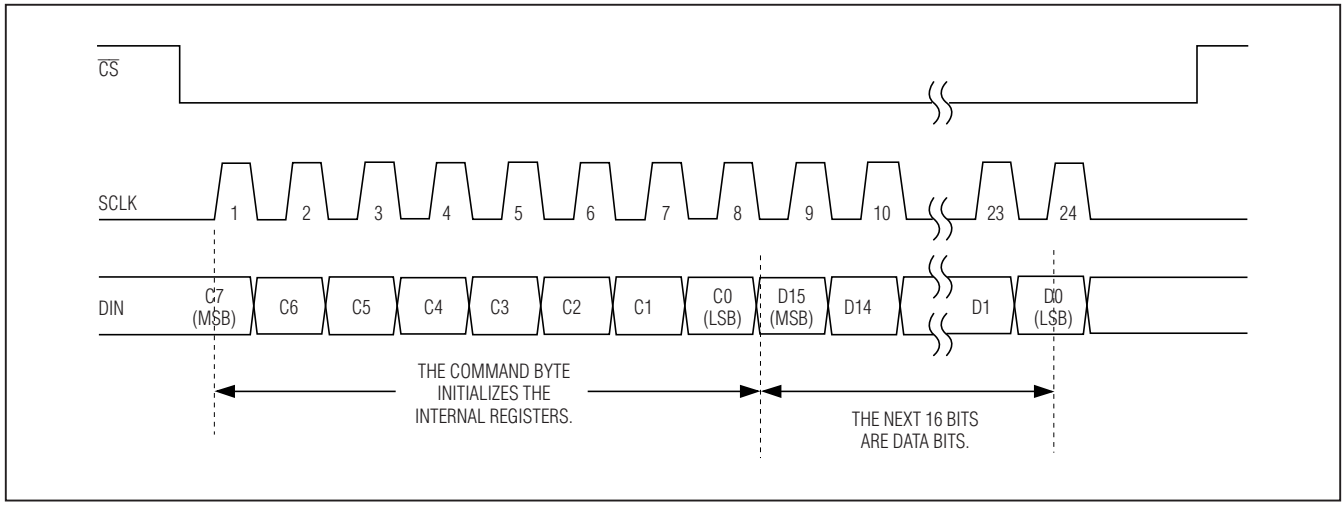

Figure 9. MAX11014/MAX11015 Write Timing

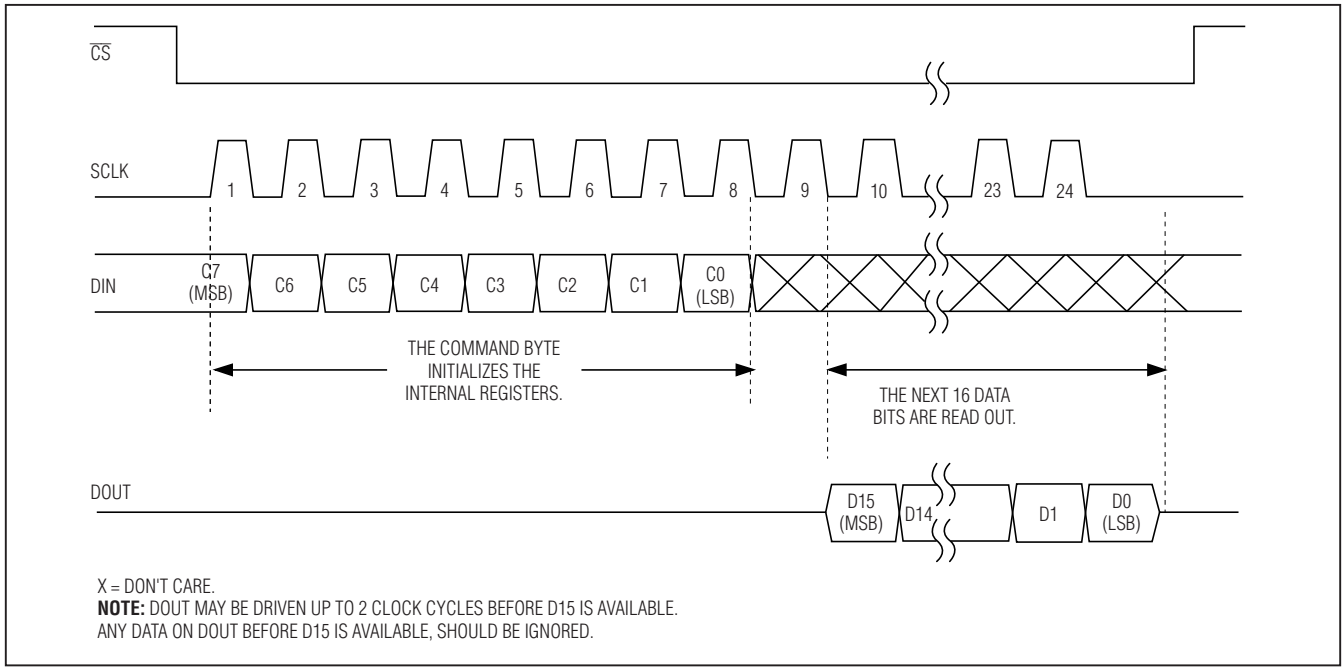

Figure 10. MAX11014/MAX11015 Read Timing

Automatic RF MESFET Amplifier Drain-Current Controllers

I²C Compatibility (SPI/$\overline{I2C}$ = DGND)

The MAX11014/MAX11015 communicate through an I²C-compatible 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX11014/MAX11015 and the master at data rates up to 3.4MHz. The master (typically a µC) initiates data transfer on the bus and generates the SCL signal to permit data transfer. The MAX11014/MAX11015 behave as I²C slave devices that transfer and receive data.

SCL and SDA must be pulled high for proper I²C operation. This is typically done with pullup resistors (1kΩ or greater). Series resistors are optional. The series resistors protect the input architecture from high-voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signals.

One data bit transfers during each SCL clock cycle. A minimum of 9 bytes is required to transfer a byte in or out of the MAX11014/MAX11015 (8 bits and an acknowledge (ACK)/not-acknowledge (NACK) bit). Data is latched in on SCL's rising edge and read out on SCL's falling edge. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is stable and high are considered control signals (see the *START and STOP Conditions* section). Both SDA and SCL remain high when the bus is not busy.

START and STOP Conditions

The master initiates a transmission with a START condition (S), a high-to-low transition on SDA while SCL is high. The master terminates a transmission with a STOP condition (P), a low-to-high transition on SDA while SCL is high (Figure 11). A repeated START condition (Sr) can be used in place of a STOP condition to leave the bus active and the interface mode unchanged (see the *High-Speed Mode* section).

The address byte, command byte, and data bytes are transmitted between the START and STOP conditions. Nine clock cycles are required to transfer the data in or out of the MAX11014/MAX11015. See Figures 15 and 16. If the receiver returns a not-acknowledge bit, the MAX11014/MAX11015 releases the bus. If the not acknowledge occurs in the middle of a 16-bit word, the remaining bits are lost.

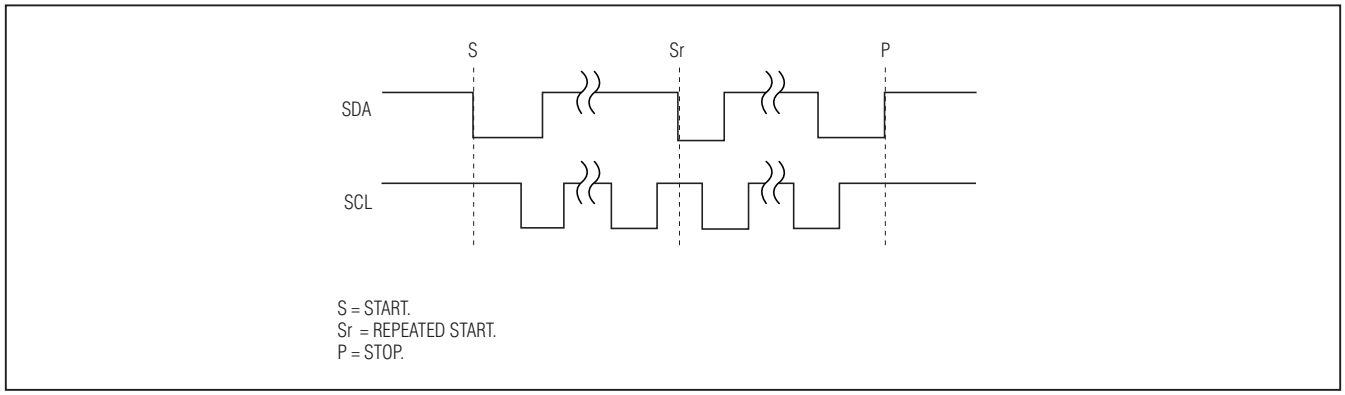

Figure 11. START and STOP Conditions

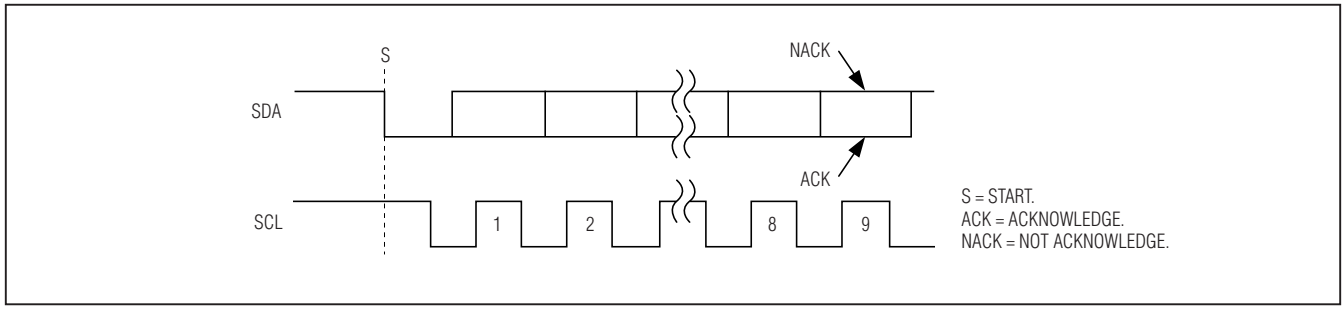

Figure 12. Acknowledge Bits

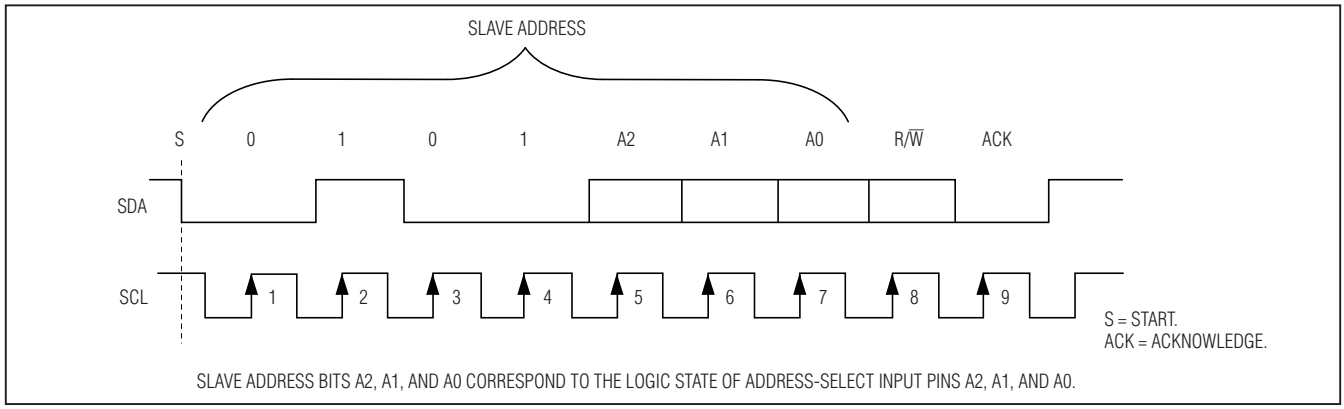

Figure 13. Slave Address Byte

Acknowledge and Not-Acknowledge Conditions

Data transfers are acknowledged with an acknowledge bit or a not-acknowledge bit. Both the master and the MAX11014/MAX11015 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device pulls SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keeps it low during the high period of the clock pulse (Figure 12).

To generate a not-acknowledge condition, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves SDA high during the high period of the clock pulse. Monitor the acknowledge bits to detect an unsuccessful data transfer. An unsuccessful data transfer happens if a receiving device is busy or if a system fault occurs. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

The MAX11014/MAX11015 have a 7-bit I²C slave address. The MSBs of the slave address are factory programmed to 0101. The logic state of address inputs A2, A1, and A0 determine the 3 LSBs of the device address (Figure 13). Connect A2, A1, and A0 to DV_{DD} for a high logic state or DGND for a low logic state. Therefore, a maximum of eight MAX11014/MAX11015 devices can be connected on the same bus at one time.

The MAX11014/MAX11015 continuously wait for a START condition followed by its slave address. When the device recognizes its slave address, it is ready to accept or send data depending on bit 8, the R/$\overline{W}$ bit.

High-Speed Mode

At power-up, the bus timing is set for fast mode (F/S mode, up to 400kHz I²C clock), which limits interface speed. Switch to high-speed mode (HS mode, up to 3.4MHz I²C clock) to increase interface speed. The interface is capable of supporting slow (up to 100kHz), fast (up to 400kHz), and high-speed (up to 3.4MHz) protocols. See Figure 14.

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Transfer from F/S mode to HS mode by addressing all devices on the bus with the HS-mode master code 0000 1XXX (X = don't care). After successfully receiving the HS-mode master code, the MAX11014/MAX11015 issue a NACK, allowing SDA to be pulled high for one cycle.

After the NACK, the MAX11014/MAX11015 operate in HS mode. Send a repeated START followed by a slave address to initiate HS-mode communication. If the master generates a STOP condition, the MAX11014/MAX11015 return to F/S mode. Use a repeated START condition in place of a STOP condition to leave the bus active and the mode unchanged.

Command Byte/Data Bytes (Write Cycle)

Begin a write cycle by issuing a START condition (through the master), followed by 7 slave address bits (Figure 13) and a write bit (R/$\overline{W}$ = 0). After writing the 8th bit, the MAX11014/MAX11015 (the slave) issue an acknowledge signal by pulling SDA low for one clock.

Write the command byte to the slave after writing the slave address (C7–C0, MSB first). See Figures 15 and 17, Table 1, and the *Command Byte* section. Following the command byte, the slave issues another acknowledge signal, pulling SDA low for one clock cycle. After the command byte, write 2 data bytes, allowing for two additional acknowledge signals after each byte. The master ends the write cycle by issuing a STOP condition. When operating in HS mode, a STOP condition returns the bus to F/S mode. See the *High-Speed Mode* section.

The MAX11014/MAX11015's internal conversion clock frequency is 4.8MHz (typ), resulting in a typical conversion time of 4.6µs. Figure 15 shows a complete write cycle.

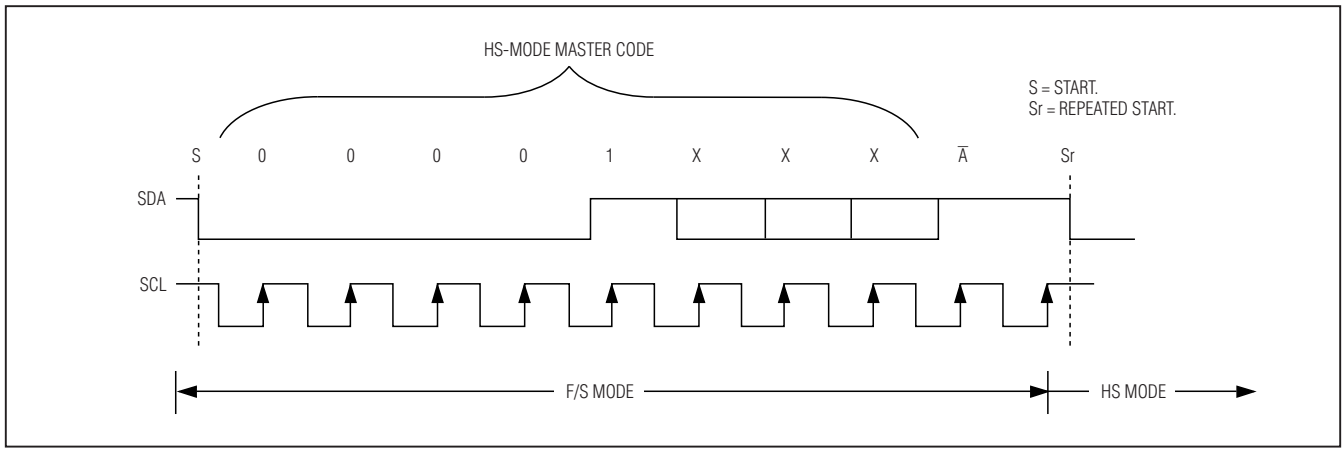

Figure 14. F/S-Mode to HS-Mode Transfer

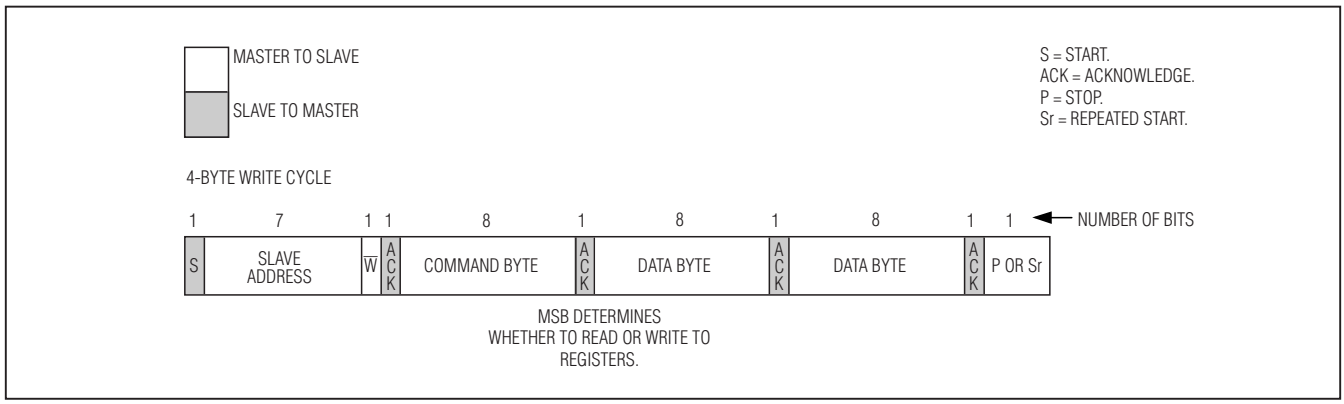

Figure 15. Write Cycle

Command Byte/Data Bytes (Read Cycle)

Begin a read cycle by issuing a START condition followed by writing a 7-bit address (Figure 18) and a read bit (R/$\overline{W}$ = 1). After writing the 8th bit, the MAX11014/MAX11015 (the slave) issue an acknowledge signal by pulling SDA low for one clock cycle.

Write the command byte to the slave after writing the slave address (C7–C0, MSB first). See Figures 16, 18, 19, Table 1, and the *Command Byte* section. Following the command byte, the slave issues another acknowledge signal, pulling SDA low for one clock cycle. After writing the command byte, issue a repeated START condition, write the slave address byte again, and write a 9th bit for an acknowledge signal. After a third acknowledge signal, read out the 2 bytes at SDA. After reading the first byte, the master should send an acknowledge bit. After reading the second byte, the master should send a not-acknowledge bit followed by a STOP signal.

Default Reads

A standard I²C read command involves writing the slave address, command byte, slave address byte again, and then reading the data at SDA. This is detailed in the 5-byte read cycle sequence in Figure 16. Read from the MAX11014/MAX11015 through the default read command to avoid writing a command byte and second slave address byte. See the default read sequence in Figure 16.

Begin a default read cycle by writing the slave address byte followed by an acknowledge bit. Read out the next 2 data bytes, with acknowledge bits from the master to the slave following each byte. Continue to acknowledge the data by sending acknowledge signals. After reading the final byte, the master should send a not-acknowledge bit followed by a STOP signal. The default read cycle reads out the data from the register (located in Table 2) of the previously assigned command byte. See Figure 18. This default read feature is useful for 2-wire reads to maximize the data throughput without having the overhead of setting the slave address and command byte each time.

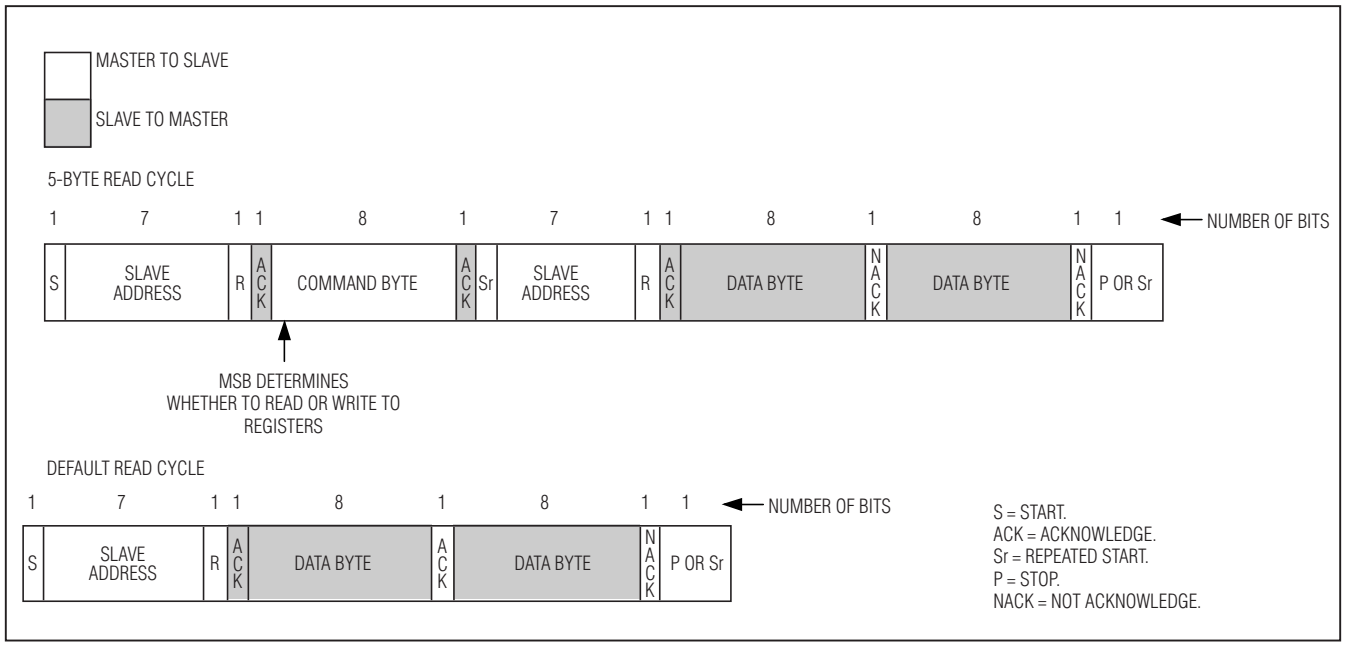

Figure 16. Read Cycle

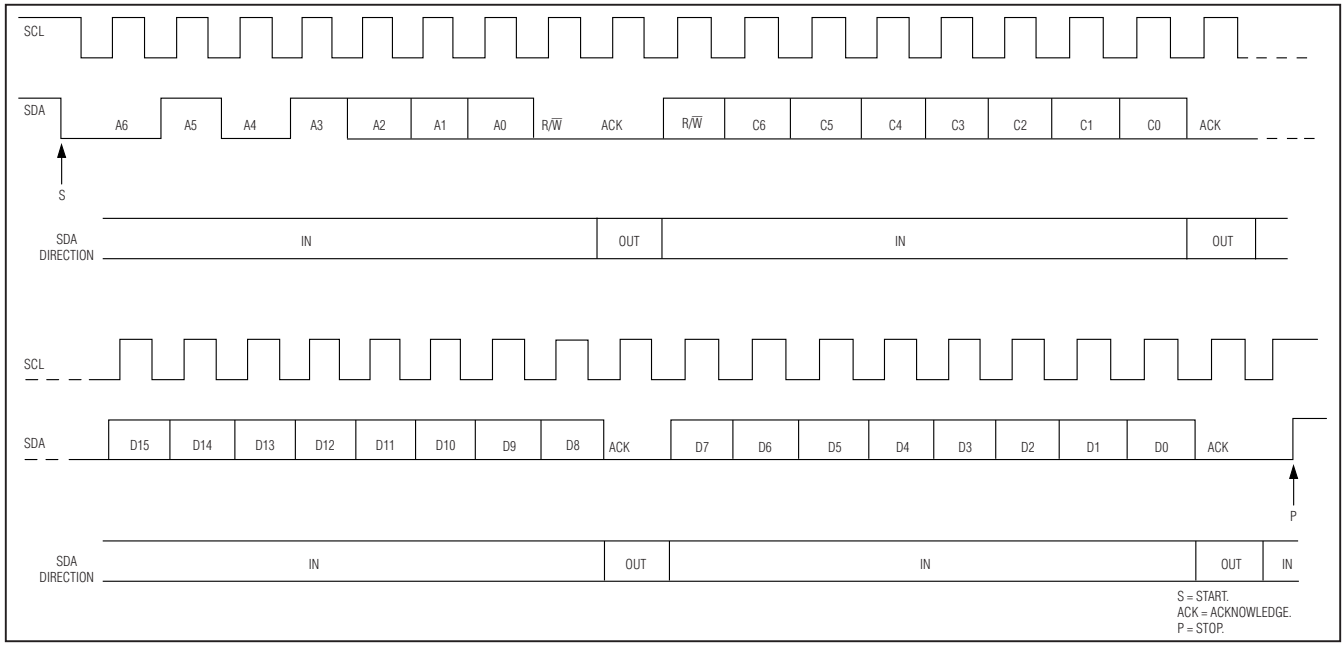

Figure 17. MAX11014/MAX11015 I²C Write Timing

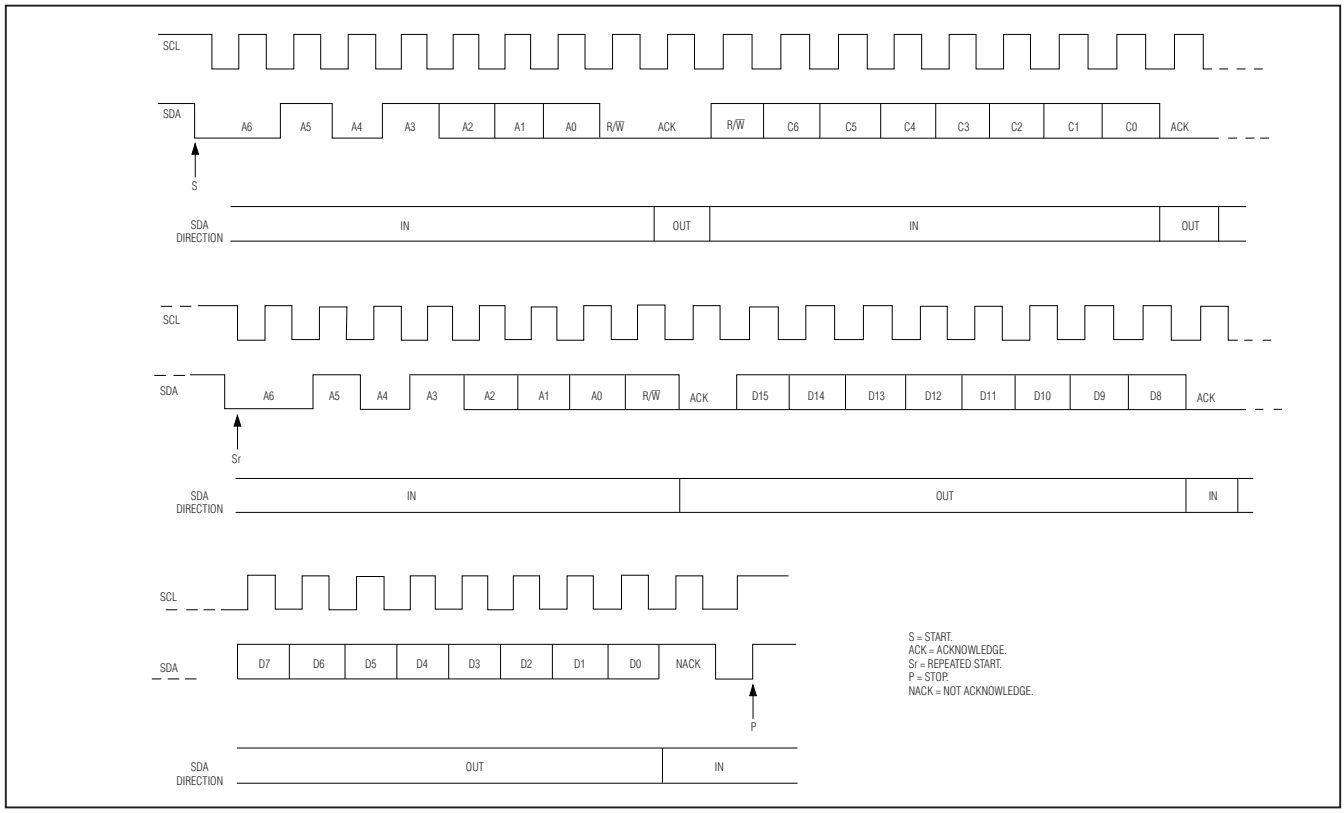

Figure 18. MAX11014/MAX11015 I²C Read Timing

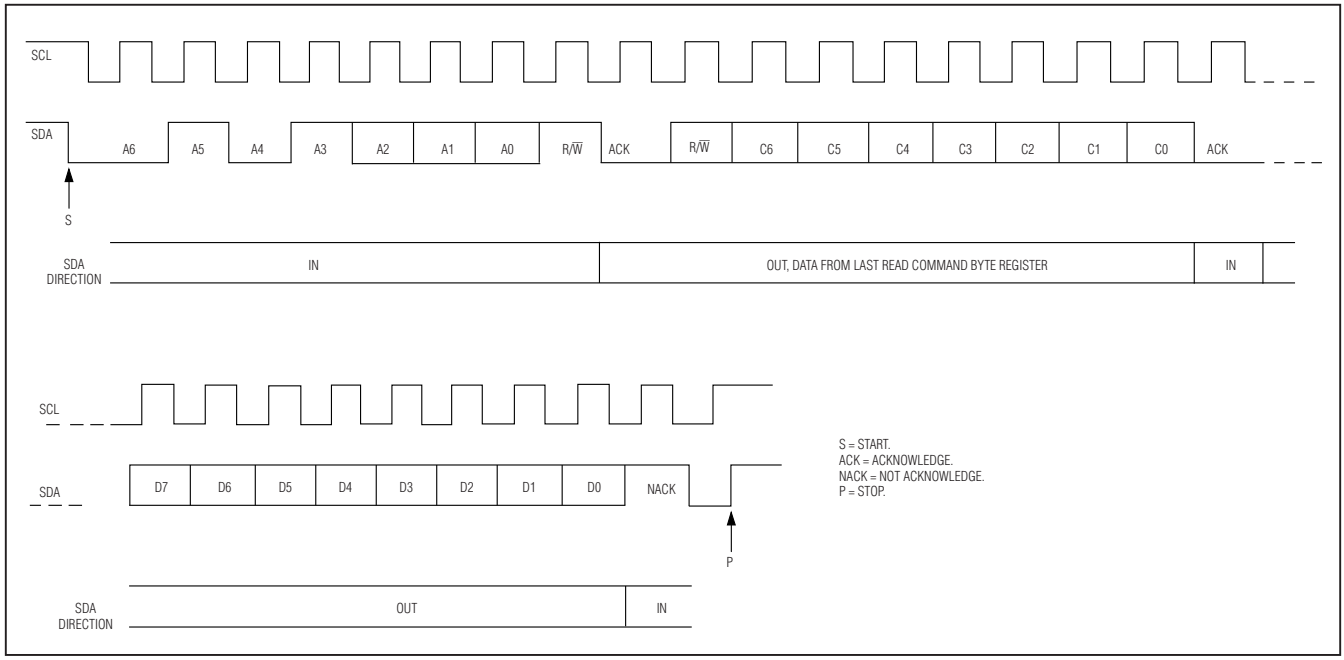

Figure 19. MAX11014/MAX11015 I²C Default Read Timing

Command Byte

Begin a write or read to the MAX11014/MAX11015 by writing a command byte at DIN/SDA. Set bit C7 to 1 for a read operation. Set bit C7 to 0 for a write operation. See Table 1. The remaining bits, C6–C0, determine the register accessed by the command byte. Table 2 indicates the register's read/write access. C7 is the MSB of the command byte and C0 is the LSB. Following the command byte, write or read 2 data bytes to/from bits D15–D0. D15 is the MSB of the 2 data bytes and D0 is the LSB. See Figures 9, 10, 17, 18, and 19 and the *Register Descriptions* section.

Table 1. Input Command Bits

24-BIT SERIAL INPUT WORD																								
COMMAND BYTE								DATA BITS																
MSB																								LSB
C7 R/$\overline{W}$	C6	C5	C4	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

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Table 2. Register Listing (see *Appendix: Startup Code Example* for sample startup sequence)

REGISTER DESCRIPTION	MNEMONIC	HEX CODE	
		WRITE	READ
ADC Conversion	ADCCON	62	—
ALARM Flag Register	ALMFLAG	—	F8
Channel 1 DAC Input	IPDAC1	48	—
Channel 1 DAC Input and Output	THRUDAC1	4A	—
Channel 1 High GATE Voltage ALARM Threshold	VH1	28	A8
Channel 1 High Sense Voltage ALARM Threshold	IH1	24	A4
Channel 1 High Temperature ALARM Threshold	TH1	20	A0
Channel 1 K Parameter	USRK1	44	—
Channel 1 Low GATE Voltage ALARM Threshold	VL1	2A	AA
Channel 1 Low Sense Voltage ALARM Threshold	IL1	26	A6
Channel 1 Low Temperature ALARM Threshold	TL1	22	A2
Channel 1 V_{SET}	VSET1	40	—
Channel 2 DAC Input	IPDAC2	4C	—
Channel 2 DAC Input and Output	THRUDAC2	4E	—
Channel 2 High GATE Voltage ALARM Threshold	VH2	34	B4
Channel 2 High Sense Voltage ALARM Threshold	IH2	30	B0
Channel 2 High Temperature ALARM Threshold	TH2	2C	AC
Channel 2 K Parameter	USRK2	46	—
Channel 2 Low GATE Voltage ALARM Threshold	VL2	36	B6
Channel 2 Low Sense Voltage ALARM Threshold	IL2	32	B2
Channel 2 Low Temperature ALARM Threshold	TL2	2E	AE
Channel 2 V_{SET}	VSET2	42	—
First-In First-Out Memory	FIFO	—	80
Flag Register	FLAG	—	F6
Hardware ALARM Configuration	ALMHCFG	3C	BC
Hardware Configuration	HCFG	38	B8
LUT Address	LUTADD	7A	—
LUT Data	LUTDAT	7C	FC
PGA Calibration Control	PGACAL	5E	—
Shutdown	SHUT	64	—
Software ALARM Configuration	ALMSCFG	3E	BE
Software Clear	SCLR	74	—
Software Configuration	SCFG	3A	BA
Software Load DAC	LDAC	66	—

Register Descriptions

The MAX11014/MAX11015 communicate between the internal registers and external bus lines through the serial interface. Table 1 details the command bits (C7–C0) and the data bits (D15–D0) of the serial input word. Table 2 details the command byte and the subsequent register accessed. Tables 3–27 detail the various read and write internal registers and their power-on reset states.

On power-up, the MAX11014/MAX11015 are in full power-down mode (see the *SHUT (Write)* section). To

Table 3. TH1 and TH2 (Read/Write)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RESET STATE	X	X	X	X	0	1	1	1	1	1	1	1	1	1	1	1
BIT VALUE (°C)	X	X	X	X	MSB (sign)	128	64	32	16	8	4	2	1	0.5	0.25	LSB 0.125

X = Don't care.

Table 4. High/Low Temperature ALARM Threshold Examples

TEMPERATURE SETTING	DATA BITS D11–D0 (TWO'S COMPLEMENT)
-40°C	1110 1100 0000
-1.625°C	1111 1111 0011
0°C	0000 0000 0000
+27.125°C	0000 1101 1001
+105°C	0011 0100 1000

Table 5. TL1 and TL2 (Read/Write)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RESET STATE	X	X	X	X	1	0	0	0	0	0	0	0	0	0	0	0
BIT VALUE (°C)	X	X	X	X	MSB (sign)	128	64	32	16	8	4	2	1	0.5	0.25	LSB 0.125

X = Don't care.

change to normal power mode, write two commands to the shutdown register. Set the FULLPD bit to 0 (other bits in the shutdown register are ignored) on the first command. A second command to this register activates the internal blocks.

TH1 and TH2 (Read/Write)

Set the external channel 1 and channel 2 high temperature ALARM thresholds by writing command bytes 20h and 2Ch, respectively. Following the command byte, write 12 bits of data to bits D11–D0. Read the high temperature channel 1 and channel 2 ALARM thresholds by writing command bytes A0h and ACh, respectively. Following the command byte, read 12 bits of data from bits D11–D0. Bits D15–D12 are don't care. Temperature data must be written and read in two's-complement format, with the LSB corresponding to +0.125°C. See Table 3. The POR value of the high temperature ALARM threshold registers is 0111 1111 1111, which corresponds to +255.875°C. See Table 4 for examples of channel 1/channel 2 high and low temperature threshold settings. See Figures 25 and 27 for ALARM examples.

TL1 and TL2 (Read/Write)

Set the external channel 1 and channel 2 low temperature ALARM thresholds by writing command bytes 22h and 2Eh, respectively. Following the command byte, write 12 bits of data to bits D11–D0. Read the low temperature channel 1 and channel 2 ALARM thresholds by writing command bytes A2h and AEh, respectively. Following the command byte, read 12 bits of data from bits D11–D0. Bits D15–D12 are don't care. Temperature data must be written and read in two's-complement format, with the LSB corresponding to +0.125°C. See Table 5. The POR value of the low temperature ALARM threshold registers is 1000 0000 0000, which corresponds to -256.0°C. See Figures 25 and 27 for ALARM examples.

IH1 and IH2 (Read/Write)

Set the channel 1 and channel 2 high sense voltage ALARM thresholds by writing command bytes 24h and 30h, respectively. Following the command byte, write 12 bits of data to bits D11–D0. Read the high sense voltage channel 1 and channel 2 ALARM thresholds by writing command bytes A4h and B0h, respectively.

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Table 6. IH1 and IH2 (Read/Write)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RESET STATE	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1
BIT VALUE	X	X	X	X	MSB	—	—	—	—	—	—	—	—	—	—	LSB

X = Don't care.

Table 7. IL1 and IL2 (Read/Write)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RESET STATE	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0
BIT VALUE	X	X	X	X	MSB	—	—	—	—	—	—	—	—	—	—	LSB

X = Don't care.

Table 8. VH1 and VH2 (Read/Write)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RESET STATE	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1
BIT VALUE	X	X	X	X	MSB	—	—	—	—	—	—	—	—	—	—	LSB

X = Don't care.

Following the command byte, read 12 bits of data from bits D11–D0. Bits D15–D12 are don't care. Sense voltage data must be written and read in straight binary format. See Table 6. The POR value of the high sense voltage ALARM threshold registers is 1111 1111 1111. See Figures 25 and 27 for ALARM examples.

The sense voltage is measured between RCS_+ and RCS_-. A reading of 1111 1111 1111 corresponds to V_{REFDAC} / 4. A reading of 0000 0000 0000 corresponds to 0mV.

IL1 and IL2 (Read/Write)

Set the channel 1 and channel 2 low sense voltage ALARM thresholds by writing command bytes 26h and 32h, respectively. Following the command byte, write 12 bits of data to bits D11–D0. Read the low sense voltage channel 1 and channel 2 ALARM thresholds by writing command bytes A6h and B2h, respectively. Following the command byte, read 12 bits of data from bits D11–D0. Bits D15–D12 are don't care. Sense voltage data must be written and read in straight binary format. See Table 7. The POR value of the low sense voltage ALARM threshold registers is 0000 0000 0000. See Figures 25 and 27 for ALARM examples.

The sense voltage is measured between RCS_+ and RCS_-. A reading of 1111 1111 1111 corresponds to V_{REFDAC} / 4. A reading of 0000 0000 0000 corresponds to 0mV.

VH1 and VH2 (Read/Write)

Set the channel 1 and channel 2 high GATE voltage ALARM thresholds by writing command bytes 28h and 34h, respectively. Following the command byte, write 12 bits of data to bits D11–D0. Read the high GATE voltage channel 1 and channel 2 ALARM thresholds by writing command bytes A8h and B4h, respectively. Following the command byte, read 12 bits of data from bits D11–D0. Bits D15–D12 are don't care. Voltage data must be written and read in straight binary format. See Table 8. The POR value of the high GATE voltage ALARM threshold registers is 1111 1111 1111. See Figure 7 for a GATE voltage example. See Figures 25 and 27 for ALARM examples.

VL1 and VL2 (Read/Write)

Set the channel 1 and channel 2 low GATE voltage ALARM thresholds by writing command bytes 2Ah and 36h, respectively. Following the command byte, write 12 bits of data to bits D11–D0. Read the low GATE voltage channel 1 and channel 2 ALARM thresholds by writing command bytes AAh and B6h, respectively. Following the command byte, read 12 bits of data from bits D11–D0. Bits D15–D12 are don't care. Voltage data must be written and read in straight binary format. See Table 9. The POR value of the low GATE voltage ALARM threshold registers is 0000 0000 0000. See Figure 7 for a GATE voltage example. See Figures 25 and 27 for ALARM examples.

Table 9. VL1 and VL2 (Read/Write)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RESET STATE	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0
BIT VALUE	X	X	X	X	MSB	—	—	—	—	—	—	—	—	—	—	LSB

X = Don't care.

Table 10. HCFG (Read/Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
X	D15–D12	X	Don't care.
CH2OCM1	D11	0	Maximum GATE2 voltage control bits.
CH2OCM0	D10	0	
CH1OCM1	D9	0	Maximum GATE1 voltage control bits.
CH1OCM0	D8	0	
X	D7	X	Don't care.
ADCMON	D6	0	ADC monitor bit. Set to 1 to load ADC results into the FIFO. Set to 0 to not load any ADC results into the FIFO. The value of ADCMON does NOT affect whether the results from any particular ADC conversion are checked against ALARM limits or examined for changes to the $V_{DAC(CODE)}$ equations.
CKSEL1	D5	0	Clock mode and $\overline{CNVST}$ configuration bits.
CKSEL0	D4	0	
ADCREF1	D3	0	ADC reference select bits.
ADCREF0	D2	0	
DACREF1	D1	0	DAC reference select bits.
DACREF0	D0	0	

HCFG (Read/Write)

Select each channel's maximum GATE voltage, clock mode, ADC monitoring, DAC and ADC reference modes by setting bits D11–D0 in the hardware configuration register. Set the command byte to 38h to write to the hardware configuration register. Set the command byte to B8h to read from the hardware configuration register. Bits D15–D12 are don't care. Set the CH2OCM1/0 bits, D11 and D10, to determine the maximum positive GATE2 output voltage. Set the CH1OCM1/0 bits, D9 and D8, to determine the maximum positive GATE1 output voltage. See Table 10.

Set the ADCMON bit, D6, to 1 to load the ADC results into the FIFO. Set ADCMON to 0 to not load ADC results into the FIFO. Set the CKSEL1/0 bits, D5 and D4, to determine the conversion and acquisition timing clock modes. See Table 10b. Also, see the *Internally Timed Acquisitions and Conversions* and *the Externally Timed Acquisitions and Conversions* sections. Set the ADCREF1/0 bits, D3 and D2, to determine the ADC reference source. See Table 10c. Set the DACREF1/0 bits, D1 and D0, to determine the DAC reference source. See Table 10d.

SCFG (Read/Write)

Write to the software configuration register to determine whether a $V_{DAC(CODE)}$ calculation value is loaded to the DAC input register or DAC input and output register. This register also sets the control modes for the K parameter and temperature lookup values in the $V_{DAC(CODE)}$ calculation. Set the command byte to 3Ah to write to the software configuration register. Set the command byte to BAh to read from the software configuration register.

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Table 10a. Maximum GATE_ Voltage Modes

CH_OCM1	CH_OCM0	FUNCTION
0	0	Maximum positive voltage at GATE_ = AGND.
0	1	Maximum positive voltage at GATE_ = AGND + 250mV.
1	0	Maximum positive voltage at GATE_ = AGND + 500mV.
1	1	Maximum positive voltage at GATE_ = AGND + 750mV.

Table 10b. Clock Modes

CKSEL1	CKSEL0	CONVERSION CLOCK	ACQUISITION/SAMPLING
0	0	Internal	Internally timed acquisitions and conversions. Default state. Begin a conversion by writing to the ADC conversion register to convert all channels specified in this register.
0	1	Internal	Internally timed acquisitions and conversions. Begin a conversion by pulling $\overline{CNVST}$ low only once for at least 20ns to convert all of the channels selected in the ADC conversion register.
1	0	Reserved	Do not use.
1	1	Internal	Externally timed single acquisitions. Conversions internally timed. Begin each individual conversion by pulling $\overline{CNVST}$ low for each channel converted. See the *Electrical Characteristics* table for $\overline{CNVST}$ timing. The MAX11014/MAX11015 acquire while $\overline{CNVST}$ is low and sample when $\overline{CNVST}$ returns high.

Table 10c. ADC Reference Modes

ADCREF1	ADCREF0	ADC VOLTAGE REFERENCE
0	X	External. Bypass REFADC with a 0.1µF capacitor to AGND.
1	0	Internal. Leave REFADC unconnected.
1	1	Internal. Bypass REFADC with a 0.1µF capacitor to AGND for better noise performance.

X = Don't care.

Table 10d. DAC Reference Modes

DACREF1	DACREF0	DAC VOLTAGE REFERENCE
0	X	External. Bypass REFDAC with a 0.1µF capacitor to AGND.
1	0	Internal. Leave REFDAC unconnected.
1	1	Internal. Bypass REFDAC with a 0.1µF capacitor to AGND for better noise performance.

X = Don't care.

Bits D15–D12 of the software configuration register are don't care. Set the LDAC2 bit, D11, to 1 to load the new value of V_{DAC2}, upon completion of a $V_{DAC2(CODE)}$ calculation, into both the channel 2 DAC input and output registers. See Figure 20. Set to 0 to load the new value of V_{DAC2}, upon completion of a $V_{DAC2(CODE)}$ calculation, to only the channel 2 DAC input register. Set the T2COMP1/0 bits, D10 and D9, to control the channel 2 temperature LUT. See Table 11a. Set the KSRC2-2/1/0 bits, D8, D7, and D6, to control the channel 2 K parameter LUT. See Table 11b and the *SRAM LUTs* section.

Set the LDAC1 bit, D5, to 1 to load the new value of V_{DAC1}, upon completion of a $V_{DAC1(CODE)}$ calculation, into both the channel 1 DAC input and output registers. Set to 0 to load the new value of V_{DAC1}, upon completion of a $V_{DAC1(CODE)}$ calculation, to only the channel 1 DAC input register. Set the T1COMP1/0 bits, D4 and D3, to control the channel 1 temperature LUT. See Table 11a. Set the KSRC1-2/1/0 bits, D2, D1, and D0 to control the channel 1 K parameter LUT. See Table 11b and the *SRAM LUTs* section.

Set the channel 1/channel 2 DAC code by writing to the respective channel's DAC input registers, DAC input and output registers, or V_{SET} registers. Write to the DAC input registers (Table 16) and use a subsequent write to the software load DAC register (Table 21) to control the timing of the update. Write to the DAC input and output registers (Table 17) to set the DAC output voltage code directly, independent of the software load DAC register bits. Write to the V_{SET} registers (Table 14) to include LUT data in the DAC code. Writing to the V_{SET} registers triggers a $V_{DAC(CODE)}$ calculation by the following equation:

$$V_{DAC(CODE)} = V_{SET(CODE)}(1 + LUT_K[K] \times LUT_{TEMP}[TEMP])$$

where

$V_{DAC(CODE)}$ = The modified channel1/channel 2 12-bit DAC code.

$V_{SET(CODE)}$ = The 12-bit DAC code written to the channel 1/channel 2 V_{SET} registers.

$LUT_K[K]$ = The interpolated, fractional 12-bit KLUT value. The KLUT data is derived from a variety of sources, including the V_{SET} register value, the K parameter register value, or various ADC channels. See the *SRAM LUTs* section.

$LUT_{TEMP}[TEMP]$ = The interpolated, fractional 12-bit two's-complement temperature LUT value. The temperature LUT data is derived from either internal or external temperature values. See the *SRAM LUTs* section.

When the KSRC_-2/KSRC_-1/KSRC_-0 bits are set to 000 and T_COMP1/T_COMP0 bits are set to 00 or 01, the $V_{DAC(CODE)}$ equation simplifies to:

$$V_{DAC(CODE)} = V_{SET(CODE)}$$

Note: This is a special case and will not trigger a V_{GATE} calculation unless a sample already exists. This functionality should be accessed by the THRUDAC registers.

For temperature samples or sampled KLUT sources to automatically trigger $V_{DAC(CODE)}$ calculations, the ADC must be configured to provide these samples. Therefore, the ADC conversion register (Table 19) must have the relevant channel bits set and the ADC must be in a suitable clocking mode, regardless of the ADCMON bit setting.

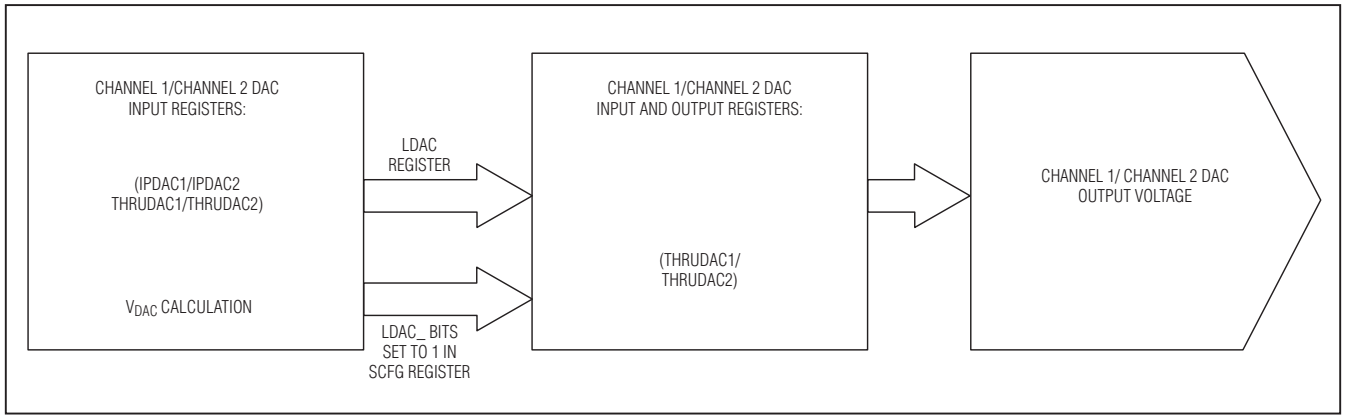

Figure 20. DAC Register Format

Table 11. SCFG (Read/Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
X	D15–D12	X	Don't care.
LDAC2	D11	0	Channel 2 load DAC. Set to 1 to load the new value of $V_{DAC2(CODE)}$, upon completion of a $V_{DAC2(CODE)}$ calculation, into both the channel 2 DAC input and output registers. When set to 1, BUSY pulses high after a new V_{DAC2} output is calculated. Set to 0 to load the new value of $V_{DAC2(CODE)}$, upon completion of a $V_{DAC2(CODE)}$ calculation, to only the channel 2 DAC input register. When set to 0, set the DACCH2 bit high in the software load DAC register to transfer the $V_{DAC(CODE)}$ calculation value from the DAC input register to the DAC output.
T2COMP1	D10	0	Channel 2 temperature LUT control bits.
T2COMP0	D9	0	
KSRC2-2	D8	0	Channel 2 KLUT control bits.
KSRC2-1	D7	0	
KSRC2-0	D6	0	
LDAC1	D5	0	Channel 1 load DAC. Set to 1 to load the new value of V_{DAC1}, upon completion of a $V_{DAC1(CODE)}$ calculation, into both the channel 1 DAC input and output registers. When set to 1, BUSY pulses high after a new V_{DAC1} output is calculated. Set to 0 to load the new value of V_{DAC1}, upon completion of a $V_{DAC1(CODE)}$ calculation, to only the channel 1 DAC input register. When set to 0, set the DACCH1 bit high in the software load DAC register to transfer the $V_{DAC(CODE)}$ calculation value from the DAC input register to the DAC output.
T1COMP1	D4	0	Channel 1 temperature LUT control bits.
T1COMP0	D3	0	
KSRC1-2	D2	0	Channel 1 KLUT control bits.
KSRC1-1	D1	0	
KSRC1-0	D0	0	

Table 11a. Channel 1/Channel 2 Temperature LUT Control Modes

T_COMP1	T_COMP0	FUNCTION
0	0	A change in temperature does not trigger a $V_{DAC(CODE)}$ calculation. Any $V_{DAC(CODE)}$ calculation triggered in another way does not include the temperature lookup. This bit setting simplifies the $V_{DAC(CODE)}$ calculation to $V_{DAC(CODE)} = V_{SET(CODE)} (1 + LUT_K[K])$.
0	1	A change in temperature does not trigger a $V_{DAC(CODE)}$ calculation. Any $V_{DAC(CODE)}$ calculation triggered in another way does not include the temperature lookup. This bit setting simplifies the $V_{DAC(CODE)}$ calculation to $V_{DAC(CODE)} = V_{SET(CODE)} (1 - LUT_K[K])$.
1	0	A change in the channel 1/channel 2 external temperature sensor reading triggers a $V_{DAC(CODE)}$ calculation for the corresponding DAC channel. When a $V_{DAC(CODE)}$ calculation is triggered, the calculation includes the temperature lookup function.
1	1	A change in the internal temperature sensor reading triggers a $V_{DAC(CODE)}$ calculation for the corresponding channel. When a $V_{DAC(CODE)}$ calculation is triggered, the calculation includes the temperature lookup function.

Table 11b. Channel 1/Channel 2 KLUT Control Modes

KSRC_-2	KSRC_-1	KSRC_-0	FUNCTION
0	0	0	No KLUT operations performed. This bit setting simplifies the $V_{DAC(CODE)}$ calculation to: $V_{DAC(CODE)} = V_{SET(CODE)} (1 + LUT_{TEMP}[TEMP])$
0	0	1	The $V_{DAC(CODE)}$ calculation simplifies to: $V_{DAC(CODE)} = V_{SET(CODE)} (1 + LUT_K[VSET] \times LUT_{TEMP}[TEMP])$
0	1	0	The $V_{DAC(CODE)}$ calculation simplifies to: $V_{DAC(CODE)} = V_{SET(CODE)} (1 - LUT_K[USRK] \times LUT_{TEMP}[TEMP])$
0	1	1	The $V_{DAC(CODE)}$ calculation simplifies to: $V_{DAC(CODE)} = V_{SET(CODE)} (1 + LUT_K[\text{sense voltage}] \times LUT_{TEMP}[TEMP])$
1	0	0	The $V_{DAC(CODE)}$ calculation simplifies to: $V_{DAC(CODE)} = V_{SET(CODE)} (1 + LUT_K[ADCIN\_] \times LUT_{TEMP}[TEMP])$
1	0	1	The $V_{DAC(CODE)}$ calculation simplifies to: $V_{DAC(CODE)} = V_{SET(CODE)} + USRK \times LUT_K[VSET] \times LUT_{TEMP}[TEMP]$
1	1	0	The $V_{DAC(CODE)}$ calculation simplifies to: $V_{DAC(CODE)} = V_{SET(CODE)} + USRK \times LUT_K[\text{sense voltage}] \times LUT_{TEMP}[TEMP]$
1	1	1	The $V_{DAC(CODE)}$ calculation simplifies to: $V_{DAC(CODE)} = V_{SET(CODE)} + USRK \times LUT_K[ADCIN\_] \times LUT_{TEMP}[TEMP]$

Table 12. ALMHCFG (Read/Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
X	D15–D12	X	Don't care.
INTEMP	D11	0	Internal temperature conversion bit. Set to 1 to cause ALARM comparisons for channel 2 to use the internal temperature conversion result. Set to 0 to cause ALARM comparisons for channel 2 to use the external temperature conversion result.
ALMCMP	D10	0	ALARM comparator bit. Set to 1 to configure the ALARM output in comparator mode. Set to 0 to configure the ALARM output in interrupt mode.
VGHYST1	D9	0	GATE voltage hysteresis bits. The VGHYST_ bits control the built-in hysteresis level when using the ALARM function in windowing mode for GATE voltage measurements. The same value is used for the GATE voltage ALARM measurements in both channels.
VGHYST0	D8	0	
ITHYST1	D7	0	Sense voltage/temperature hysteresis bits. The ITHYST_ bits control the built-in hysteresis level when using the ALARM function in windowing mode for sense voltage and temperature measurements. The same value is used for the sense voltage and temperature ALARM measurements in both channels.
ITHYST0	D6	0	
ALM2CLMP1	D5	0	Channel 2 ALARM clamp bits.
ALM2CLMP0	D4	0	
ALM1CLMP1	D3	0	Channel 1 ALARM clamp bits.
ALM1CLMP0	D2	0	
ALMPOL	D1	0	ALARM polarity bit. Set to 1 to force the ALARM output to be active-low. Set to 0 to force the ALARM output to be active-high.
ALMOPN	D0	0	ALARM open-drain/push-pull output bit. Set to 1 to configure the ALARM output as open-drain. An external pullup or pulldown resistor is required. Multiple ALARM outputs can be wired together onto a single line in open-drain mode. Set to 0 to configure the ALARM output as a push-pull output (no external resistor required).

ALMHCFG (Read/Write)

The hardware ALARM configuration register controls the active states of the ALARM output. Set the command byte to 3Ch to write to the hardware ALARM configuration register. Set the command byte to BCh to read the hardware ALARM configuration register. Bits D15–D12 are don't care. Set the INTEMP bit, D11, to 1 to cause ALARM comparisons for channel 2 to use the internal temperature conversion result. Set the ALMCMP bit, D10, to 1 to set the ALARM output in comparator mode. Set ALMCMP to 0 to set the ALARM output in interrupt mode. See Figure 25.

When operating in windowing mode, set the VGHYST1/0 bits, D9 and D8, to control the GATE_ voltage ALARM hysteresis level. This hysteresis level applies to both channel 1 and channel 2. See Table 12a and Figure 25. When operating in windowing mode, set the ITHYST1/0 bits, D7 and D6, to control the sense voltage and temperature ALARM hysteresis level. This hysteresis level applies to both channel 1 and channel 2. See Table 12b.

Set the ALM2CLMP1/0 bits, D5 and D4, to control whether or not the GATE2 output is clamped to the external voltage at ACLAMP2. See Table 12c. Set the ALM1CLMP1/0 bits, D3 and D2, to control whether or not the GATE1 output is clamped to the external voltage at ACLAMP1. See Table 12c and the *Automatic GATE Clamping* section. Set the ALMPOL bit, D1, to 1 make the ALARM output active-low. Set ALMPOL to 0 to make the ALARM output active-high. Set the ALMOPN bit, D0, to 1 to make the ALARM output an open-drain output. Set ALMOPN to 0 to force the ALARM output to be push-pull.

Table 12a. GATE Voltage Hysteresis Levels

VGHYST1	VGHYST0	FUNCTION
0	0	8 LSBs of hysteresis.
0	1	16 LSBs of hysteresis.
1	0	32 LSBs of hysteresis.
1	1	64 LSBs of hysteresis.

Table 12b. Sense Voltage/Temperature Hysteresis Levels

ITHYST1	ITHYST0	FUNCTION
0	0	8 LSBs of hysteresis.
0	1	16 LSBs of hysteresis.
1	0	32 LSBs of hysteresis.
1	1	64 LSBs of hysteresis.

Table 12c. ALARM Clamp Modes

ALM_CLMP1	ALM_CLMP0	FUNCTION
0	0	Default state. The GATE_ outputs are clamped to the respective external voltage applied at ACLAMP_ independent of alarms. GATE_ remains clamped until this register value is changed or a software clear command is issued.
0	1	The corresponding ALARM bit in the ALARM flag register goes high if an ALARM condition is triggered by a conversion of sense voltage, temperature, or GATE_ voltage. However, the GATE_ outputs are not clamped.
1	0	Fully automatic clamping. The GATE_ outputs are clamped to the respective external voltage applied at ACLAMP_ when an ALARM condition is triggered. The clamp is removed if a subsequent temperature or sense voltage conversion removes the ALARM condition. GATE_ remains clamped when a GATE_ voltage ALARM is triggered. For a GATE_ voltage ALARM, ALM_CLMP 10 mode functions the same as 11 mode. This exception breaks the feedback loop created by sampling GATE_ voltage and then clamping the same signal.
1	1	Semi-automatic clamping. The GATE_ outputs are clamped to the respective external voltage applied at ACLAMP_ when an ALARM condition is triggered. If an ALARM condition is triggered, the ALM_CLMP bits are overwritten to 00, causing a permanent clamp condition. Clear this permanent clamp condition with a subsequent write to reset the ALM_CLMP bits.

ALMSCFG (Read/Write)

The software ALARM configuration register controls which voltage and temperature channels trigger the ALARM output and whether the ALARM comparators operate in windowing or hysteresis mode. Set the command byte to 3Eh to write to the software ALARM configuration register. Set the command byte to BEh to read the software ALARM configuration register. Bits D15–D12 are don't care. Set the VALARM2 bit, D11, to 1 to enable ALARM functionality for GATE2 voltage measurements. Set the VWIN2 bit, D10, to 1 to monitor the GATE2 voltage with the ALARM comparator in windowing mode. Set VWIN2 to 0 to monitor the GATE2 voltage with the ALARM comparator in hysteresis mode.

Set the TALARM2 bit, D9, to 1 to enable ALARM functionality for channel 2 temperature measurements. Set the TWIN2 bit, D8, to 1 to monitor the channel 2 temperature with the ALARM comparator in windowing mode. Set TWIN2 to 0 to monitor the channel 2 temperature with the ALARM comparator in hysteresis mode. Set the IALARM2 bit, D7, to 1 to enable ALARM functionality for channel 2 sense voltage (RCS2+ to RCS2-) measurements. Set the IWIN2 bit, D6, to 1 to monitor the channel 2 sense voltage with the ALARM comparator in windowing mode. Set IWIN2 to 0 to monitor the channel 2 sense voltage with the ALARM comparator in hysteresis mode.

Table 13. ALMSCFG (Read/Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
X	D15–D12	X	Don't care.
VALARM2	D11	0	Channel 2 GATE voltage ALARM bit. Set to 1 to enable the ALARM functionality for GATE2 voltage measurements. Set to 0 to disable the ALARM functionality for GATE2 voltage measurements.
VWIN2	D10	0	Channel 2 GATE voltage windowing bit. Set to 1 to monitor the GATE2 voltage with the ALARM comparator in windowing mode. Set to 0 to monitor the GATE2 voltage with the ALARM comparator in hysteresis mode.
TALARM2	D9	0	Channel 2 temperature ALARM bit. Set to 1 to enable the ALARM functionality for channel 2 temperature measurements. Set to 0 to disable the ALARM functionality for channel 2 temperature measurements.
TWIN2	D8	0	Channel 2 temperature windowing bit. Set to 1 to monitor the channel 2 temperature with the ALARM comparator in windowing mode. Set to 0 to monitor the channel 2 temperature with the ALARM comparator in hysteresis mode.
IALARM2	D7	0	Channel 2 sense voltage ALARM bit. Set to 1 to enable the ALARM functionality for channel 2 sense voltage measurements. Set to 0 to disable the ALARM functionality for channel 2 sense voltage measurements.
IWIN2	D6	0	Channel 2 sense voltage windowing bit. Set to 1 to monitor the channel 2 sense voltage with the ALARM comparator in windowing mode. Set to 0 to monitor the channel 2 sense voltage with the ALARM comparator in hysteresis mode.
VALARM1	D5	0	Channel 1 GATE voltage ALARM bit. Set to 1 to enable the ALARM functionality for GATE1 voltage measurements. Set to 0 to disable the ALARM functionality for GATE1 voltage measurements.
VWIN1	D4	0	Channel 1 GATE voltage windowing bit. Set to 1 to monitor the GATE1 voltage with the ALARM comparator in windowing mode. Set to 0 to monitor the GATE1 voltage with the ALARM comparator in hysteresis mode.
TALARM1	D3	0	Channel 1 temperature ALARM bit. Set to 1 to enable the ALARM functionality for channel 1 temperature measurements. Set to 0 to disable the ALARM functionality for channel 1 temperature measurements.
TWIN1	D2	0	Channel 1 temperature windowing bit. Set to 1 to monitor the channel 1 temperature with the ALARM comparator in windowing mode. Set to 0 to monitor the channel 1 temperature with the ALARM comparator in hysteresis mode.
IALARM1	D1	0	Channel 1 sense voltage ALARM bit. Set to 1 to enable the ALARM functionality for channel 1 sense voltage measurements. Set to 0 to disable the ALARM functionality for channel 1 sense voltage measurements.
IWIN1	D0	0	Channel 1 sense voltage windowing bit. Set to 1 to monitor the channel 1 sense voltage with the ALARM comparator in windowing mode. Set to 0 to monitor the channel 1 sense voltage with the ALARM comparator in hysteresis mode.

Table 14. VSET1 and VSET2 (Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
X	D15–D12	X	Don't care.
VSET11–VSET0	D11–D0	0000 0000 0000	VSET11 is the MSB and VSET0 is the LSB. Data format is straight binary.

Table 15. USRK1 and USRK2 (Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
X	D15–D12	X	Don't care.
K11–K0	D11–D0	N/A	K11 is the MSB and K0 is the LSB. Data format is straight binary.

Set the VALARM1 bit, D5, to 1 to enable ALARM functionality for GATE1 voltage measurements. Set the VWIN1 bit, D4, to 1 to monitor the GATE1 voltage with the ALARM comparator in windowing mode. Set VWIN1 to 0 to monitor the GATE1 voltage with the ALARM comparator in hysteresis mode. Set the TALARM1 bit, D3, to 1 to enable ALARM functionality for channel 1 temperature measurements. Set the TWIN1 bit, D2, to 1 to monitor the channel 1 temperature with the ALARM comparator in windowing mode. Set TWIN1 to 0 to monitor the channel 1 temperature with the ALARM comparator in hysteresis mode. Set the IALARM1 bit, D1, to 1 to enable ALARM functionality for channel 1 sense voltage (RCS1+ to RCS1-) measurements. Set the IWIN1 bit, D0, to 1 to monitor the channel 1 sense voltage with the ALARM comparator in windowing mode. Set IWIN1 to 0 to monitor the channel 1 sense voltage with the ALARM comparator in hysteresis mode.

VSET1 and VSET2 (Write)

Write to the channel 1/channel 2 V_{SET} registers to set the $V_{SET(CODE)}$ code in the $V_{DAC(CODE)}$ equations. Writing to these registers triggers a $V_{DAC(CODE)}$ calculation. That code is then loaded into either the channel 1/channel 2 DAC input register or channel 1/channel 2 DAC input and output register, depending on the state of the LDAC1/LDAC2 bits in the software configuration register. Set the command byte to 40h to write to the channel 1 V_{SET} register. Set the command byte to 42h to write to the channel 2 V_{SET} register. See Table 14. Bits D15–D12 are don't care. Bits D11–D0 contain the straight binary data.

USRK1 and USRK2 (Write)

Write to the channel 1/channel 2 K parameter registers to set the $LUT_K[K]$ code in the $V_{DAC(CODE)}$ equation. The K parameter register value is loaded into the $V_{DAC(CODE)}$ equation when the KSRC_-2/KSRC_-1/KSRC_-0 bits in the software configuration register are set to 010, 101, 110, or 111. See Table 11b. Use the K parameter as an index to the KLUT or as a multiplier for the $V_{DAC(CODE)}$ equation in place of $V_{SET(CODE)}$ by writing to the software configuration register. See Table 11. Set the command byte to 44h to write to the channel 1 K parameter register. Set the command byte to 46h to write to the channel 2 K parameter register. See Table 15. Bits D15–D12 are don't care. Bits D11–D0 contain the straight binary data.

IPDAC1 and IPDAC2 (Write)

Write to the channel 1/channel 2 DAC input registers to load the DAC code and bypass a $V_{DAC(CODE)}$ calculation. Transfer the code written to the DAC input registers to the channel 1/channel 2 DAC output registers by setting the corresponding DACCH_ bit high in the software load DAC register. Set the command byte to 48h and 4Ch, respectively, to write to the channel 1/channel 2 DAC input registers. See Table 16. Bits D15–D12 are don't care. Bits D11–D0 contain the straight binary data.

Writing to these registers overwrites any previous values loaded from the $V_{DAC(CODE)}$ calculation.

Table 16. IPDAC1 and IPDAC2 (Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
X	D15–D12	X	Don't care.
DAC11–DAC0	D11–D0	0000 0000 0000	DAC11 is the MSB and DAC0 is the LSB. Data format is straight binary.

Table 17. THRUDAC1 and THRUDAC2 (Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
X	D15–D12	X	Don't care.
DAC11–DAC0	D11–D0	N/A	DAC11 is the MSB and DAC0 is the LSB. Data format is straight binary.

Table 18. PGACAL (Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
X	D15–D5	X	Don't care.
HVCAL2	D4	0	Channel 2 high-side calibration bit. Set to 1 to short circuit the current-sense amplifier inputs so that only the offset is apparent at the PGAOUT2 output and the channel 2 current-sense conversion.
HVCAL1	D3	0	Channel 1 high-side calibration bit. Set to 1 to short circuit the current-sense amplifier inputs so that only the offset is apparent at the PGAOUT1 output and the channel 1 current-sense conversion.
TRACK	D2	0	Acquisition/tracking bit. Set to 0 to force the next current-sense calibration to run in acquisition mode. Set to 1 to force the next calibration to run in tracking mode. Set TRACK to 0 the first time through a calibration.
DOCAL	D1	0	Dual calibration bit. Set to 1 to run a current-sense self-calibration routine in both channels 1 and 2. At the end of the calibration routine, DOCAL is set to 0. When DOCAL and SELFTIME are both set to 1, the internal timer is reset at the end of the routine and waits another 13ms before performing the next self-timed calibration.
SELFTIME	D0	0	Self-time bit. Set to 1 to perform a calibration of the current-sense amplifier in both channels 1 and 2 on a self-timed periodic basis (approximately every 15ms). When set to the default state of 0, calibration only occurs when DOCAL is set to 1.

THRUDAC1 and THRUDAC2 (Write)

Write to the channel 1/channel 2 DAC input and output registers to load the DAC code directly to the respective DAC output and bypass a $V_{DAC(CODE)}$ calculation. Set the command byte to 4Ah and 4Eh, respectively, to write to the channel 1/channel 2 DAC input and output registers. See Table 17. Bits D15–D12 are don't care. Bits D11–D0 contain the straight binary data.

Writing to these registers overwrites any previous values loaded from the $V_{DAC(CODE)}$ calculation.

PGACAL (Write)

Write to the PGA calibration control register to calibrate the channel 1 and channel 2 current-sense amplifiers. Set the command byte to 5Eh to write to the PGA calibration control register. See Table 18. Bits D15–D5 are don't care. Set the HVCAL2 bit, D4, to 1 to short circuit the channel 2 current-sense amplifier inputs so that only the offset is apparent at the PGAOUT2 output. Set the HVCAL1 bit, D3, to 1 short circuit the channel 1 current-sense amplifier inputs so that only the offset is apparent at the PGAOUT1 output. Determine the input channel offset (+12mV, typ) by setting the HVCAL_bits and commanding a sense-voltage ADC conversion.

The current-sense calibration routine offers two operation modes: acquisition and tracking. In acquisition mode, the calibration routine operates continuously until the error is minimized to 50µV or less. In tracking mode, the routine operates every 15ms to minimize interference and allow the calibration routine more averaging time. A sample-and-hold circuit prevents switching noise on GATE_ during tracking mode. Set the TRACK bit, D2, to 0 to run the calibration routine in acquisition mode. Set TRACK to 1 to run the calibration routine in tracking mode. Set TRACK to 0 for the first calibration.

Set the DOCAL bit, D1, to 1 to run a current-sense self-calibration routine in both channel 1 and channel 2. At the end of the calibration routine, DOCAL is set back to 0. Set the SELFTIME bit, D0, to 1 to perform a current-sense calibration on a periodic basis, typically every 15ms. Use the DOCAL bit in conjunction with the SELFTIME bit. When a calibration routine is commanded by DOCAL, and SELFTIME is set to 1, the internal timer is reset at the end of the routine and waits another 15ms before performing the next self-timed calibration.

The self-calibration routine can be commanded when the DACs are powered down, but the results are not accurate. For best results, run the calibration after the DAC power-up time, t_{DPUEXT}.

ADCCON (Write)

Write to the ADC conversion register to convert the ADCIN_, GATE_, internal DAC and sense voltages. The ADC conversion register also converts the internal and external temperature readings and sets the interface for continuous conversion. See Table 19. Set the command byte to 62h to write to the ADC conversion register. Bits D15–D12 are don't-care bits. The ADCMON bit in the hardware configuration register must be set to 1 to load ADC results into the FIFO. Set the CONCONV bit, D11, to 1 for continuous ADC conversions.

Set the CH10 bit, D10, to 1 to convert the ADCIN2 voltage. Set the CH9 bit, D9, to 1 to convert the GATE2 voltage. Set the CH8 bit, D8, to 1 to convert the channel 2 DAC code. Set the CH7 bit, D7, to 1 to convert the channel 2 sense voltage. Set the CH6 bit, D6, to 1 to convert the channel 2 external temperature sensor measurement. Set the CH5 bit, D5, to 1 to convert the ADCIN1 voltage. Set the CH4 bit, D4, to 1 to convert the GATE1 voltage. Set the CH3 bit, D3, to 1 to convert the channel 1 DAC code. Set the CH2 bit, D2, to 1 to convert the channel 1 sense voltage. Set the CH1 bit, D1, to 1 to convert the channel 1 external temperature sensor measurement. Set the CH0 bit, D0, to 1 to convert the internal temperature sensor measurement.

Convert any combination of ADC channels through the ADC conversion register. When requesting a conversion of more than one channel, the channels are converted in numerical order from CH0 to CH10.

Setting the CONCONV bit to 1 may cause the FIFO to overflow if data is not read out quickly enough. Continuous-conversion mode is only available in clock modes 00 and 01. See the *Clock Mode 00* and *Clock Mode 01* sections. The ADC does not trigger a busy signal when the CONCONV bit is set. If a temperature channel is included in the scan when CONCONV is set, the internal reference and temperature sensor remain powered up until CONCONV is set to 0. Similarly, if an ADC measurement using the internal reference is included in the scan, the internal reference is turned on prior to the first conversion and remains on until CONCONV is set to 0.

In clock modes 00 and 01, when the CONCONV bit is set to 0 and the current scan (not just the current conversion) is completed, the ADC goes to an idle state awaiting the next command. The BUSY output is set high when the CONCONV bit is set to 0 and remains high until the current scan is completed. See the *BUSY Output* section.

SHUT (Write)

Shut down all internal blocks, as well as the DACs, ADCs, and gate-drive amplifiers individually, through the shutdown register. See Table 20. Set the command byte to 64h to write to the shutdown register. Bits D15–D12 are don't care. Set the FULLPD bit, D11, to 1 to shut down all internal blocks and reduce AV_{DD} supply current to 0.8µA. The FULLPD bit is set to 1 at power-up. Set the FULLPD bit to 0 before writing any other commands to activate all internal blocks and functionality.

Set the FBGON bit, D10, to 1 to keep the internal bandgap reference powered up. Set the WDGPD bit, D9, to 1 to turn off the watchdog oscillator and prevent self-monitoring of the watchdog timer. Set the OSCPD bit, D8, to 1 to power down the internal oscillator. Set the PD2-3 bit, D7, to 1 to power down the channel 2 current-sense amplifier. Set the PD2-2 bit, D6, to 1 to power down the channel 2 gate-drive amplifier. Set the PD2-1 bit, D5, to 1 to power down the channel 2 DAC summing node. Set the PD2-0 bit, D4, to 1 to power down the channel 2 DAC. Set the PD1-3 bit, D3, to 1 to power down the channel 1 current-sense amplifier. Set the PD1-2 bit, D2, to 1 to power down the channel 1 gate-drive amplifier. Set the PD1-1 bit, D1, to 1 to power down the channel 1 DAC summing node. Set the PD1-0 bit, D0, to 1 to power down the channel 1 DAC.

Table 19. ADCCON (Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
X	D15–D12	X	Don't care.
CONCONV	D11	0	Set to 1 to command continuous ADC conversions. The ADCMON bit in the hardware configuration register must be to set to 1 to load ADC results into the FIFO. Continuous conversions are only applicable in clock modes 00 and 01. When CONCONV is set to 1, the ADC continuously converts the channels selected by the ADC conversion register using the conversion mode selected by the CKSEL1/CKSEL0 bits. Results are accumulated in the FIFO. Empty the FIFO quickly enough to prevent overflow conditions.
CH10	D10	0	Set to 1 to convert the ADCIN2 voltage in the next ADC conversion cycle.
CH9	D9	0	Set to 1 to convert the GATE2 voltage in the next ADC conversion cycle. Also, the PD2-3 bit in the shutdown register must be set to 0.
CH8	D8	0	Set to 1 to convert the channel 2 DAC code in the next ADC conversion cycle.
CH7	D7	0	Set to 1 to convert the channel 2 sense voltage in the next ADC conversion cycle.
CH6	D6	0	Set to 1 to convert the channel 2 external temperature-sensor measurement in the next ADC conversion cycle.
CH5	D5	0	Set to 1 to convert the ADCIN1 voltage in the next ADC conversion cycle.
CH4	D4	0	Set to 1 to convert the GATE1 voltage in the next ADC conversion cycle. Also, the PD1-3 bit in the shutdown register must be set to 0.
CH3	D3	0	Set to 1 to convert the channel 1 DAC code in the next ADC conversion cycle.
CH2	D2	0	Set to 1 to convert the channel 1 sense voltage in the next ADC conversion cycle.
CH1	D1	0	Set to 1 to convert the channel 1 external temperature sensor measurement in the next ADC conversion cycle.
CH0	D0	0	Set to 1 to convert the internal temperature sensor measurement in the next ADC conversion cycle.

For maximum accuracy, power up all internal blocks prior to a calibration (MAX11014). The MAX11015 does not require the current-sense amplifier to be powered up for a calibration.

LDAC (Write)

Write to the software load DAC register to load the values stored in the DAC input registers to their respective DAC output registers. Set the command byte to 66h to write to the software load DAC register. See Table 21. Bits D15–D2 are don't care.

Set the DACCH2 bit, D1, to 1 to load the channel 2 DAC output register with the value stored in the channel 2 DAC input register. Set the DACCH1 bit, D0, to 1 to load the channel 1 DAC output register with the value stored in the channel 1 DAC input register. See Figure 20.

Table 20. SHUT (Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
X	D15–D12	X	Don't care.
FULLPD	D11	1	Set to 1 to power down all internal blocks. FULLPD takes precedence over any of the other power-down control bits. All commands in progress are suspended and the DACs and ADC are disabled. The serial interface remains functional. FULLPD is set to 1 on power-up. Set the FULLPD bit to 0 after power-up and before writing any other commands to activate all internal blocks.
FBGON	D10	0	Set to 1 to force the internal bandgap voltage block to power up, remain powered up between conversions, and avoid the 50µs reference power-up delay time. Forcing the internal reference to remain on increases the power dissipation. Set FBGON to its default state of 0 to power the bandgap voltage as required by the ADC.
WDGPD	D9	0	Set to 1 to turn off the watchdog oscillator. The watchdog oscillator monitors the internal ALU and resets the logic state to the startup condition after 80ms. This reduces power consumption but prevents the self-monitoring function of the watchdog timer.
OSCPD	D8	0	Set to 1 to power down the internal oscillator. OSCPD is automatically reset to 0 after receiving the next interface command.
PD2-3	D7	1	Set to 1 to power down the channel 2 current-sense amplifier.
PD2-2	D6	1	Set to 1 to power down the channel 2 gate-drive amplifier.
PD2-1	D5	1	Set to 1 to power down the channel 2 DAC summing node (MAX11014)/DAC buffer (MAX11015). The summing node acts as a buffer in the MAX11015.
PD2-0	D4	1	Set to 1 to power down the channel 2 DAC.
PD1-3	D3	1	Set to 1 to power down the channel 1 current-sense amplifier.
PD1-2	D2	1	Set to 1 to power down the channel 1 gate-drive amplifier.
PD1-1	D1	1	Set to 1 to power down the channel 1 DAC summing node (MAX11014)/DAC buffer (MAX11015). The summing node acts as a buffer in the MAX11015.
PD1-0	D0	1	Set to 1 to power down the channel 1 DAC.

Table 21. LDAC (Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
X	D15–D2	X	Don't care.
DACCH2	D1	N/A	Set to 1 to load the channel 2 DAC output register with the value stored in the channel 2 DAC input register.
DACCH1	D0	N/A	Set to 1 to load the channel 1 DAC output register with the value stored in the channel 1 DAC input register.

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Table 22. SCLR (Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
X	D15–D7	X	Don't care.
FULLRESET	D6	N/A	Write the following sequence to perform a full reset and return all internal registers to their respective reset state: Write to the software clear register once with FULLRESET = 0 and ARMRESET = 1. Write a second word to the software clear register with FULLRESET = 1 and ARMRESET = 0. The full reset takes effect after completion of the second write to this register. After a full software reset, the internal registers return to their power-on state, but the internal oscillator remains running (unlike at power-up). After a full software reset, it is not necessary to set the FULLPD bit to 0 (as it is on a normal power-on reset) before attempting any other commands. The BUSY output is set high and the ALU initializes internal RAM before setting BUSY low.
ARMRESET	D5	0	
ALMSCLR	D4	N/A	Set to 1 to reset all ALARM threshold registers and the ALARM flag register.
CACHECLR	D3	N/A	Set to 1 to force the ALU to clear the pointers and lookup value cache to their power-up values. This forces an LUT operation and a $V_{DAC(CODE)}$ calculation for the next sample, regardless of whether the sample produces a table pointer that is different.
FIFOCLR	D2	N/A	Set to 1 to reset the FIFO address pointers and clear the FIFO's contents.
DAC2CLR	D1	N/A	Set to 1 to reset the channel 2 DAC input and output registers.
DAC1CLR	D0	N/A	Set to 1 to reset the channel 1 DAC input and output registers.

Table 23. LUTADD (Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
LUTWORD7–LUTWORD0	D15–D8	0000 0000	Set these 8 bits to determine the number of LUT words to be read/written.
LUTADD7–LUTADD0	D7–D0	0000 0000	Set these 8 bits to determine the base address for the read/write operation.

SCLR (Write)

Write to the software clear register to reset all of the internal registers, clear the internal ALU or reset the FIFO pointers and clear the FIFO. This register also resets the ALARM threshold registers, ALARM flag register and the DAC registers. Set the command byte to 74h to write to the software clear register. See Table 22. Bits D15–D7 are don't care. The FULLRESET bit, D6, and ARMRESET bit, D5, provide functionality for a full reset. Write the following sequence to perform a full reset and return all internal register bits to their respective reset state:

- Write to the software clear register once with FULLRESET = 0 and ARMRESET = 1.
- Write a second word to the software clear register with FULLRESET = 1 and ARMRESET = 0. The full reset takes effect after completion of the second write to this register.
- It is recommended a FULLRESET be completed after power-up. See *Appendix: Startup Code Example* for sample startup code.

Set the ALMSCLR bit, D4, to 1 to reset all ALARM threshold register bits and the ALARM flag register bits. Set the CACHECLR bit, D3, to 1 to force the ALU to clear the pointers and lookup value cache to their power-up values. This forces a LUT operation and a $V_{DAC(CODE)}$ calculation for the next sample, regardless of whether the sample produces a table pointer that is different. Set the FIFOCLR bit, D2, to 1, reset the FIFO address pointers, and clear the FIFO's contents. Set the DAC2CLR bit, D1, to 1 to reset the channel 2 DAC input and output register bits. Set the DAC1CLR bit, D0, to 1 to reset the channel 1 DAC input and output register bits.

Table 24. LUTDAT (Read/Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
LUTDAT15–LUTDAT0	D15–D0	N/A	The 16-bit data word written to the LUT data or configuration memory space.

Table 25. FIFO

DATA BITS							CONVERSION-DATA ORIGIN
CHANNEL TAG				D11	D10–D1	D0	
D15	D14	D13	D12				
0	0	0	0	MSB	—	LSB	Internal temperature sensor.
0	0	0	1	MSB	—	LSB	Channel 1 external temperature sensor.
0	0	1	0	MSB	—	LSB	Channel 1 sense voltage.
0	0	1	1	MSB	—	LSB	Channel 1 DAC input register.
0	1	0	0	MSB	—	LSB	Channel 1 GATE voltage.
0	1	0	1	MSB	—	LSB	ADCIN1 voltage.
0	1	1	0	MSB	—	LSB	Channel 2 external temperature sensor.
0	1	1	1	MSB	—	LSB	Channel 2 sense voltage.
1	0	0	0	MSB	—	LSB	Channel 2 DAC input register.
1	0	0	1	MSB	—	LSB	Channel 2 GATE voltage.
1	0	1	0	MSB	—	LSB	ADCIN2 voltage.
1	0	1	1	MSB	—	LSB	Reserved.
1	1	0	D12	D11	—	LSB	LUT data value. See Table 28. Bit D12 is the MSB for the LUT configuration words. Bit D11 is the MSB for all other LUT reads.
1	1	1	0	MSB	—	LSB	Conversion may be corrupted. This occurs only when arriving data causes the FIFO to overflow at the same time data is being read out.
1	1	1	1	MSB	—	LSB	Empty FIFO. The current value of the flag register is read out in place of the FIFO data.

LUTADD (Write)

Write to the LUT address register to determine the number of write/read LUT locations, the base address pointer, and the LUT configuration word. See Table 23. Set the command byte to 7Ah to write to the LUT address register. Set the LUTWORD bits, D15–D8, to the number of LUT words to be read/written. Set the LUTADD bits, D7–D0, to determine the base address for the read/write operation.

If the top of LUT memory is reached before the LUTWORD limit is reached, the LUT data register read/write is discontinued. Write 00h to the LUTWORD bits to abort an LUT read/write. See the *SRAM LUT*s section for details on programming the various LUT addresses. See Table 28 for a map of the LUT address locations.

LUTDAT (Read/Write)

Write or read LUT data through the LUT data register. Set the command byte to 7Ch to write to the LUT data register. Set the command byte to FCh to read from the LUT data register. Write 16 bits of data to the LUT data register to load individual address locations with lookup data. See Table 24. The address in the LUT memory space is automatically incremented after each LUT data register write command.

Differentiate LUT data from ADC data from the unique LUT data channel tag 110_. See Table 25.

Table 26. FLAG (Read)

BIT NAME	DATA BIT	RESET	FUNCTION
X	D15–D7	X	Don't care.
RESTART	D6	0	RESTART is set to 1 after either a watchdog timer reset or by commanding a software reset through the software clear register's FULL RESET function. RESTART returns to 0 after a power-on reset or a flag register read command.
ALUBUSY	D5	0	ALUBUSY is set to 1 when the ALU is performing other tasks not covered by specific status bits elsewhere in this register. This includes, for example, the internal memory initialization after power-up.
PGABUSY	D4	0	PGABUSY is set to 1 when the ALU is performing a PGA calibration (whether commanded or self-timed).
ADCBUSY	D3	0	ADCBUSY is set to 1 when the ADC is busy, an ALARM value is being checked, or the ADC results are being loaded into the FIFO. ADCBUSY returns to 0 after the ADC completes all of the conversions in the current scan.
VGBUSY	D2	1	VGBUSY is set to 1 when the ALU is performing a lookup and interpolation or $V_{DAC(CODE)}$ calculation for either channel.
FIFOEMP	D1	1	FIFOEMP is set to 1 when the FIFO is empty and contains no data. FIFOEMP is reset to 0 if data is written into the FIFO. Writing to the software clear register with FIFOCLR set to 1 causes the FIFO to be cleared, which then sets FIFOEMP to 1.
FIFOOVR	D0	0	FIFOOVR functions in one of two modes: 1) Reading the ADC data: FIFOOVR is set to 1 if the FIFO has a data overflow. FIFOOVR is reset to 0 by reading the flag register or by clearing the FIFO through the software clear register. Emptying the FIFO does not clear the FIFOOVR bit. 2) Reading the LUT data: When commanding an LUT read, the FIFO is no longer allowed to overflow (as it is for normal ADC monitoring). FIFOOVR is set to 1 if the LUT is full and set to 0 if the LUT is not full, for that instant in time only.

FIFO

Read the oldest result in the FIFO by writing command byte 80h and reading the next 16 bits at DOUT in SPI mode and SDA in I²C mode. Bits D15–D12 (channel tag) identify which ADC or LUT channel is being converted. Bits D11–D0 contain the ADC/LUT conversion results for that specific channel. Bit D11 is the MSB and bit D0 is the LSB for all ADC and LUT data, with the exception of the LUT configuration words. When reading the LUT configuration registers, bit D12 is the MSB and bit D0 is the LSB. See Table 25.

FLAG (Read)

Read from the flag register to determine the source of a busy condition. Set the command byte to F6h to read the flag register. Bits D15–D7 are don't care. See Table 26. The RESTART bit, D6, is set to 1 after either a watchdog timer reset or by commanding a software reset through the software clear register's FULL RESET function. RESTART is reset to a 0 after a power-on reset or a flag register read command. The ALUBUSY bit, D5, is set to 1 when the ALU is performing other tasks not covered by specific status bits elsewhere in this register. The PGABUSY bit, D4, is set to 1 when the ALU is performing a PGA calibration.

Table 27. ALMFLAG (Read)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
X	D15–D12	X	Don't care.
HIGH-V2	D11	0	HIGH-V2 is set to 1 when the GATE2 voltage exceeds the high threshold setting. HIGH-V2 is reset to 0 by either a read of the ALARM flag register or a software clear command.
LOW-V2	D10	0	LOW-V2 is set to 1 when the GATE2 voltage decreases below the low threshold setting. LOW-V2 is reset to 0 by either a read of the ALARM flag register or a software clear command.
HIGH-I2	D9	0	HIGH-I2 is set to 1 when the channel 2 sense voltage exceeds the high threshold setting. HIGH-I2 is reset to 0 by either a read of the ALARM flag register or a software clear command.
LOW-I2	D8	0	LOW-I2 is set to 1 when the channel 2 sense voltage decreases below the low threshold setting. LOW-I2 is reset to 0 by either a read of the ALARM flag register or a software clear command.
HIGH-T2	D7	0	HIGH-T2 is set to 1 when the channel 2 external temperature exceeds the high threshold setting. HIGH-T2 is reset to 0 by either a read of the ALARM flag register or a software clear command.
LOW-T2	D6	0	LOW-T2 is set to a 1 when the channel 2 external temperature decreases below the low threshold setting. LOW-T2 is reset to 0 by either a read of the ALARM flag register or a software clear command.
HIGH-V1	D5	0	HIGH-V1 is set to 1 when the GATE1 voltage exceeds the high threshold setting. HIGH-V1 is reset to 0 by either a read of the ALARM flag register or a software clear command.
LOW-V1	D4	0	LOW-V1 is set to 1 when the GATE1 voltage decreases below the low threshold setting. LOW-V1 is reset to 0 by either a read of the ALARM flag register or a software clear command.
HIGH-I1	D3	0	HIGH-I1 is set to 1 when the channel 1 sense voltage exceeds the high threshold setting. HIGH-I1 is reset to 0 by either a read of the ALARM flag register or a software clear command.
LOW-I1	D2	0	LOW-I1 is set to 1 when the channel 1 sense voltage decreases below the low threshold setting. LOW-I1 is reset to 0 by either a read of the ALARM flag register or a software clear command.
HIGH-T1	D1	0	HIGH-T1 is set to 1 when the channel 1 external temperature exceeds the high threshold setting. HIGH-T1 is reset to 0 by either a read of the ALARM flag register or a software clear command.
LOW-T1	D0	0	LOW-T1 is set to a 1 when the channel 1 external temperature decreases below the low threshold setting. LOW-T1 is reset to 0 by either a read of the ALARM flag register or a software clear command.

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The ADCBUSY bit, D3, is set to 1 when the ADC is busy, an ALARM value is being checked, or the ADC results are being loaded into the FIFO. ADCBUSY returns to 0 after the ADC completes all of the conversions in the current scan. The VGBUSY bit, D2, is set to 1 when the ALU is performing a lookup and interpolation or $V_{DAC(CODE)}$ calculation for either channel. The FIFOEMP bit, D1, is set to 1 when the FIFO is empty and contains no data. FIFOEMP is reset to 0 if data is written into the FIFO. Writing to the software clear register with FIFOCLR set to 1 causes the FIFO to be cleared, which then sets FIFOEMP to 1.

The functionality of the FIFOOVR bit, D0, depends on whether the FIFO is loaded with ADC data or LUT data. FIFOOVR functions in one of two modes:

1) Reading the ADC data: FIFOOVR is set to 1 if the FIFO has a data overflow. FIFOOVR is reset to 0 only by reading the flag register or by clearing the FIFO through the software clear register. Emptying the FIFO does not clear the FIFOOVR bit.
2) Reading the LUT data: When commanding a LUT read, the FIFO is no longer allowed to overflow. FIFOOVR is set to 1 if the LUT is full and set to 0 if the LUT is not full, for that instant in time only. See the *FIFO Description* section.

ALMFLAG (Read)

Read the ALARM flag register to determine the source of an ALARM condition. Set the command byte to F8h to read the ALARM flag register. Bits D15–D12 are don't care. See Table 27. Bits D11–D0 are all reset to 0 following a read of the ALARM flag register or a software clear command. The HIGH-V2 bit, D11, is set to 1 when the GATE2 voltage exceeds the high threshold setting. The LOW-V2 bit, D10, is set to 1 when the GATE2 voltage decreases below the low threshold setting. The HIGH-I2 bit, D9, is set to 1 when the channel 2 sense voltage exceeds the high threshold setting. The LOW-I2 bit, D8, is set to 1 when the channel 2 sense voltage decreases below the low threshold setting. The HIGH-T2 bit, D7, is set to 1 when the channel 2 external temperature exceeds the high threshold setting. The LOW-T2 bit, D6, is set to a 1 when the channel 2 external temperature decreases below the low threshold setting.

The HIGH-V1 bit, D5, is set to 1 when the GATE1 voltage exceeds the high threshold setting. The LOW-V1 bit, D4, is set to 1 when the GATE1 voltage decreases below the low threshold setting. The HIGH-I1 bit, D3, is set to 1 when the channel 1 sense voltage exceeds the high threshold setting. The LOW-I1 bit, D2, is set to 1 when the channel 1 sense voltage decreases below the low threshold setting. The HIGH-T1 bit, D1, is set to 1 when the channel 1 external temperature exceeds the high threshold setting. The LOW-T1 bit, D0, is set to a 1 when the channel 1 external temperature decreases below the low threshold setting.

FIFO Description

The MAX11014/MAX11015's FIFO stores 15 ADC samples or 16 SRAM LUT data words. Read the FIFO to load the FIFO data onto DOUT in SPI mode and SDA in I²C mode. See Table 25. The ADC sample data includes a 4-bit channel tag, followed by 12 bits of data. The ADC channel tags indicate the source for the temperature or voltage result. The LUT data includes a 3-bit channel tag for LUT configuration word data and a 4-bit tag for all other LUT data. The LUT tags indicate whether the LUT data is temperature (T) or numerical (K)-based. Do not mix ADC results with LUT results in the FIFO.

The FIFO allows overflows of ADC data and it always contains the 15 most recent ADC conversion results. Read the FIFO quickly enough to prevent an overflow condition. Detect if the FIFO has overflowed (indicating a loss of data) by inspecting the FIFOOVR bit in the flag register.

The FIFO does not overflow while outputting SRAM LUT data. Count how many words are output in order (through the numerical representation of the LUTWORD bits in the LUT address register) to tell which LUT data word is being supplied.

ADC Monitoring Mode

Each time the ADC converts a sample in ADC monitoring mode, the data word and its 4-bit channel tag are moved into the FIFO. Load the data from the FIFO to DOUT in SPI mode and SDA in I²C mode by writing command byte 80h.

The hardware configuration register's ADCMON bit determines whether ADC samples are loaded into the FIFO. See Table 10. Set ADCMON to 1 to store ADC samples in the FIFO. Set to 0 to not load ADC results into the FIFO. The value of ADCMON does not affect whether the results from any particular ADC conversion are checked against the ALARM thresholds or examined for changes to the $V_{DAC(CODE)}$ equations.

After reading out all of the ADC FIFO data, the flag register sets the FIFOEMP bit to 1. If a FIFO read command is issued with the FIFO empty, the FIFO returns a channel tag of 1111 and the 12 flag register bits. See Table 25.

The FIFO allows interface reads to be simultaneous with the arrival of new ADC sample or LUT data words. But when the FIFO is full and overflowing, if an ADC sample arrives at exactly the same time as an interface read, there is a possibility of data corruption. This condition is

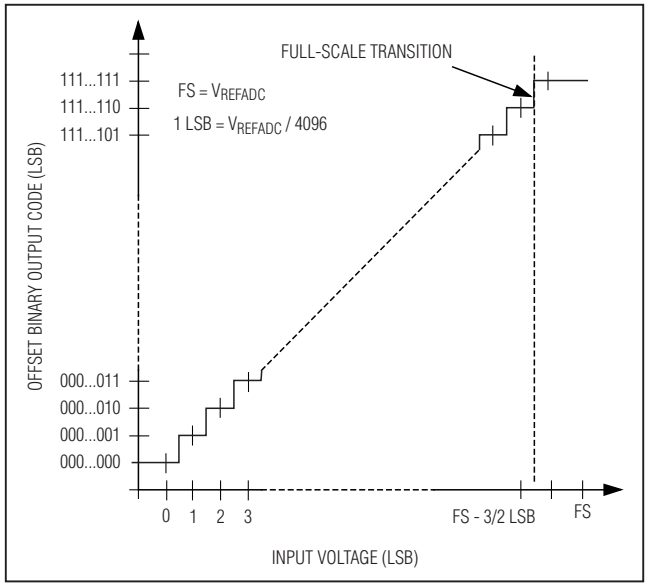

Figure 21. ADC Transfer Function

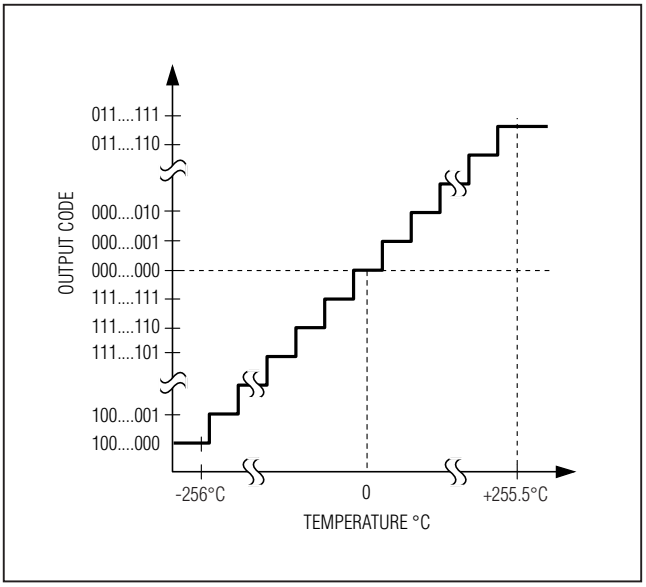

Figure 22. Temperature Transfer Function

indicated by channel tag 1110 (rather than the usual ADC channel tag). In this case, only that particular data item is corrupted and all other FIFO contents remain valid and can be accessed with subsequent reads.

Read the FIFO quickly enough to prevent overflow conditions to entirely avoid the risk of data corruption. At fast serial-interface clock rates, it is possible to read data from the FIFO faster than the ADC loads it. Set a continuous ADC scan in progress and continuously read the FIFO. Assuming the FIFO is being emptied more quickly than it is being filled, the continuous FIFO reads supply a mixture of empty channel tags (1111 and the flag register value), mixed in with the valid ADC results. Separate the valid ADC results from the flag register data based on the 4-bit channel tag.

SRAM LUT Read Mode

After an LUT data register read command, data from the SRAM LUTs is copied into the FIFO. Load the data from the FIFO to DOUT in SPI mode and SDA in I²C mode by reading the FIFO. If SRAM LUT data is written to the FIFO faster than its read out, the FIFO fills up. The copying of data is suspended until the FIFO is read again. If the FIFO is read more quickly than the SRAM LUT loads the values, the data is interspersed with error channel tags (1111 and the flag register value) and valid LUT data.

Output Data Format

All conversion data results are output in 2-byte format, MSB first. Data transitions on DOUT on the falling edges of SCLK in SPI mode. Data transitions on SDA on the rising edge of SCL in I²C mode. Figures 10, 18, and 19 illustrate the MAX11014/MAX11015's read timing. See Figures 21 and 22 for ADC and temperature transfer functions, respectively.

ADC Transfer Function

Data is output in straight binary format, with the exception of temperature results/alarms, which are two's complement. Figure 21 shows the unipolar transfer function for single-ended inputs. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1 LSB = V_{REFADC} / 2.5V for unipolar operation, and 1 LSB = +0.125°C for temperature measurements.

PGAOUT Outputs

The PGAOUT output voltages are derived from a sense voltage conversion. The dual current-sense amplifiers amplify the voltage between RCS_+ and RCS_- by four and add an offset voltage (+12mV nominally). The current-sense amplifiers scale voltages up to +625mV. The MAX11014's Class A control loop detailed in Figure 5. The MAX11015's Class AB analog control is detailed in Figure 6. Calculate the PGAOUT_ voltage with the following equation:

$$V_{PGAOUT\_} = V_{REFADC} - [4 \times (V_{RCS\_+} - V_{RCS\_-}) + 12mV]$$

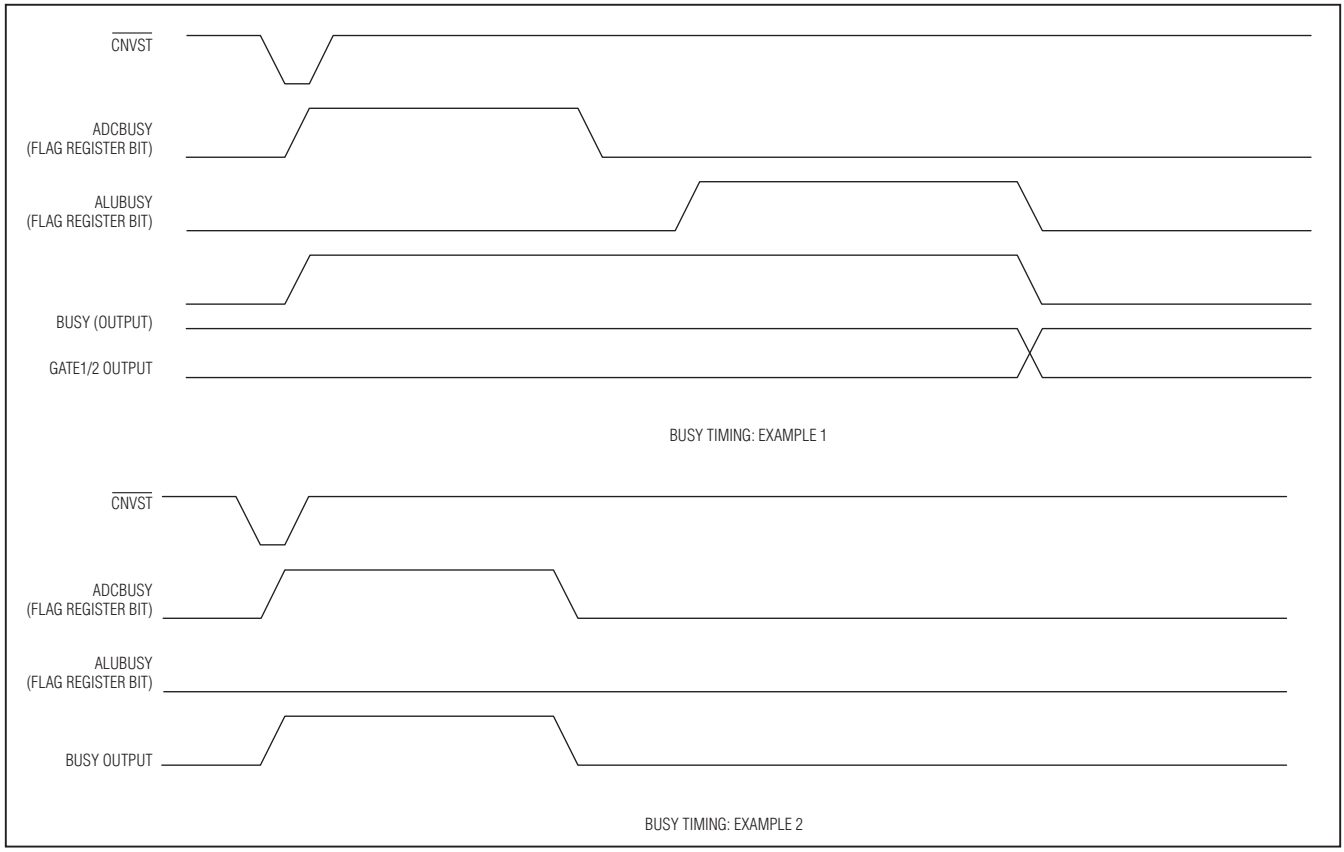

Figure 23. BUSY Timing

Write to the HVCAL_ bits in the PGA calibration control register to short circuit the current-sense amplifier inputs so that only the offset is apparent at the PGAOUT_ output and ADC input.

BUSY Output

The BUSY output goes high for a variety of reasons. The possible causes of BUSY pulsing high include:

- The ADC is converting, but not in continuous conversion mode
- The internal ALU core is performing a power-up initialization
- The internal ALU core is performing a $V_{DAC(CODE)}$ calculation
- The internal ALU core is performing another function
- The self-calibration routine is taking place

When the CONCONV bit is set in the ADC conversion register, the BUSY output does not trigger when the ADC is converting (for all clock modes). This prevents the continuous ADC activity from masking other BUSY events.

The serial interface remains available regardless of the state of BUSY, although certain commands are not appropriate. For example, if BUSY is high for an ADC operation, reading the FIFO does not produce the result for the current conversion. Also, if BUSY triggers due to an ADC conversion, do not enter a second conversion command until BUSY returns low, indicating the previous conversion is complete.

See Figure 23 for a pair of BUSY timing examples. In example 1, an externally timed ADC conversion triggers the ADCBUSY bit in the flag register and forces BUSY high. Next, a $V_{DAC(CODE)}$ calculation triggers the ALUBUSY bit in the flag register and holds BUSY high. In example 2, the $V_{DAC(CODE)}$ calculation is not requested.

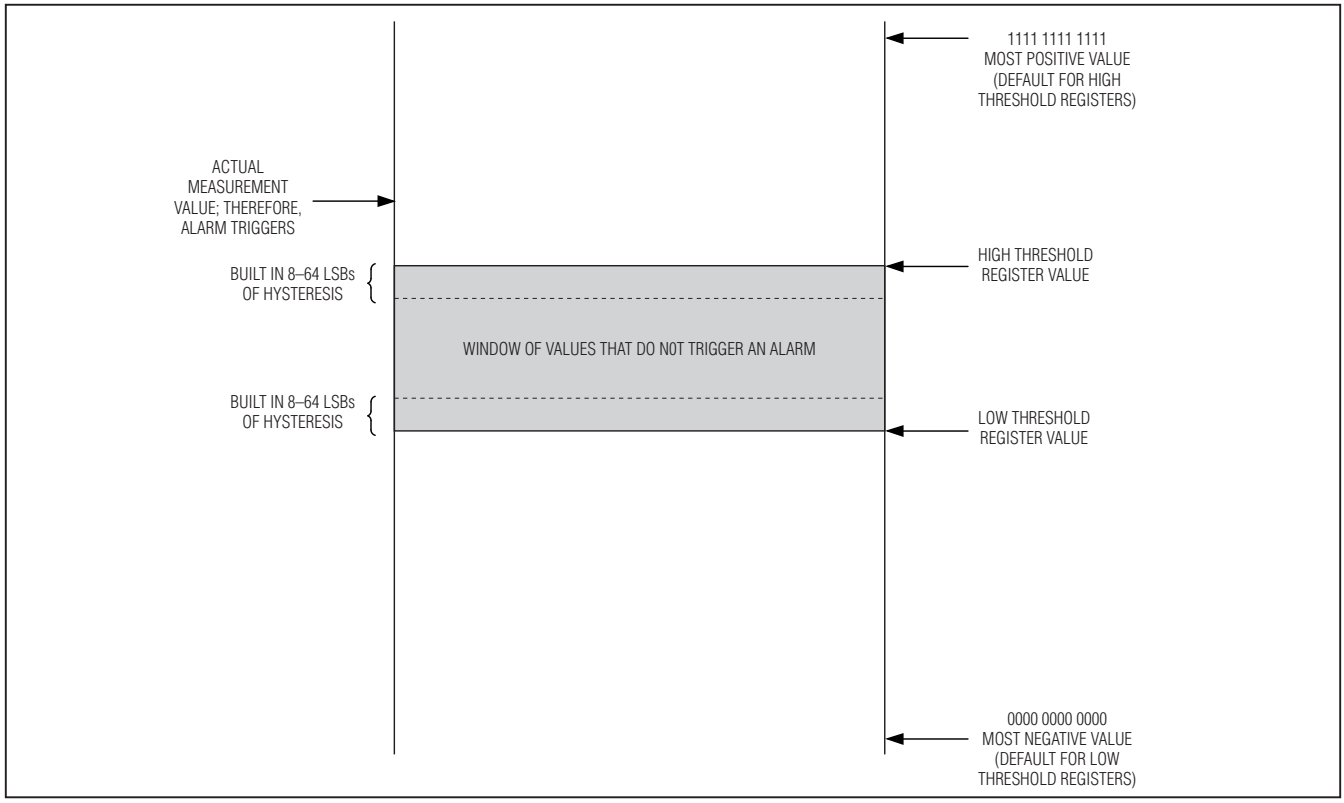

Figure 24. ALARM Window Comparator Example

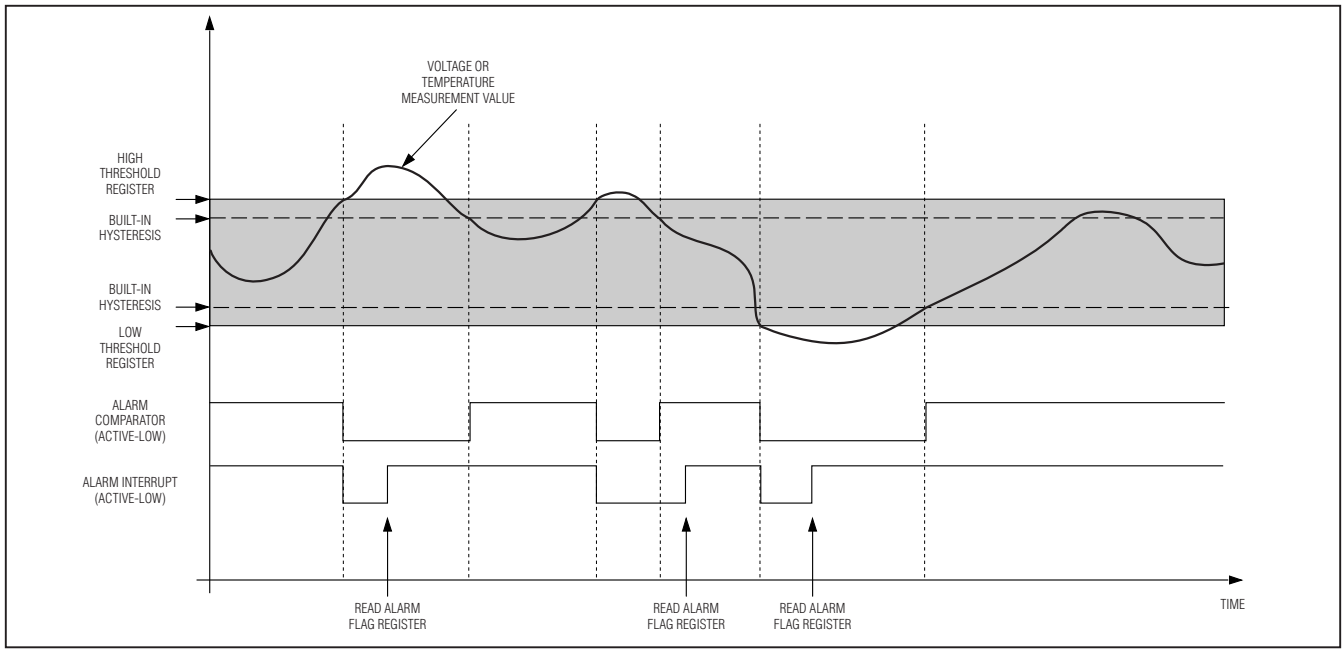

Figure 25. ALARM Window-Mode Timing Example

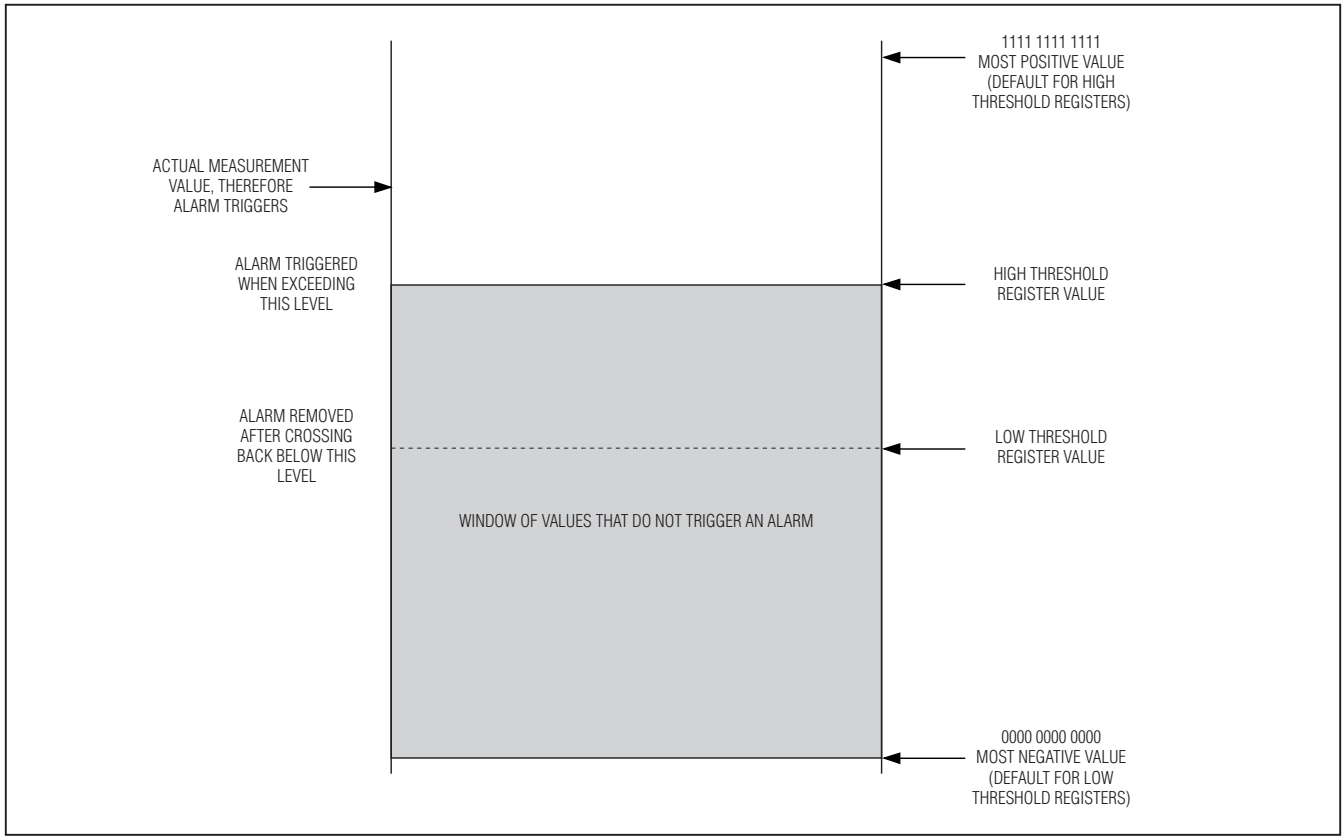

Figure 26. ALARM Hysteresis Comparator Example

ALARM Output

The ALARM output asserts when the corresponding channel's temperature or voltage readings exceed the respective high or low ALARM threshold. Each time the sense voltage, temperature (external for either channel, internal for channel 2), or GATE_ voltage is converted, the measured value is compared to the high and low ALARM threshold values.

The ALARM comparison operates in either window or hysteresis mode. When operating in window comparator mode (TWIN_, IWIN_, or VWIN_ bits in the software ALARM configuration register set to 1), the ADC output values are monitored to ensure that the values are between both the high and low ALARM threshold register values. See Table 13 and Figure 24.

Window comparisons include built-in hysteresis levels, ensuring the ALARM output does not trigger repeatedly when sampling values around the threshold. The ALMHYST bits in the hardware ALARM configuration register vary the built-in hysteresis between 8 and 64 LSBs. The built-in hysteresis acts as a noise filter to prevent unnecessary switching when a sample value is varying slightly around the threshold. The ALARM condition remains in place until the measured value rises above the low threshold value or falls below the high threshold value. Figure 25 details a window-mode timing example.

The ALARM output operates in interrupt or comparator mode. In interrupt mode, the ALARM output asserts until the ALARM flag register is read. In comparator mode, the ALARM output reflects the internal ALARM state and remains asserted for as long as the ALARM conditions are breached. The ALARM output deasserts after the windowing or hysteresis conditions are satisfied.

When operating in hysteresis comparator mode (TWIN_, IWIN_, or VWIN_ bits in the software ALARM configuration register set to 0), the ADC output values are monitored to ensure that the values are below the high set

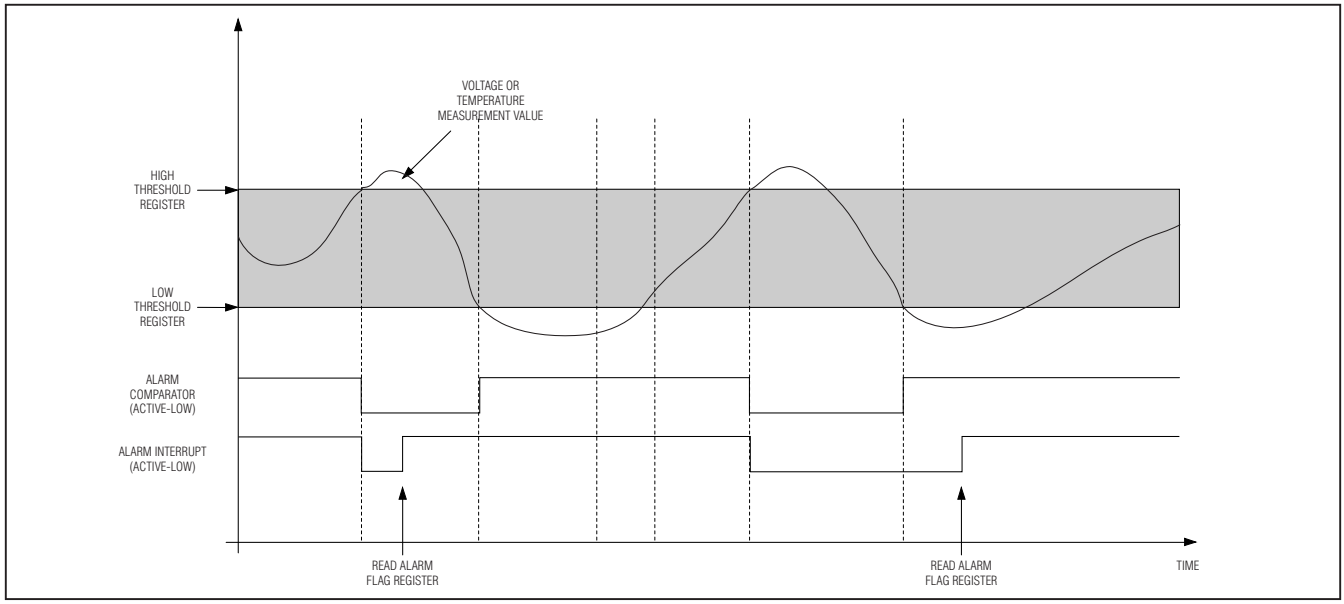

Figure 27. ALARM Hysteresis-Mode Timing Example

ALARM threshold register value. See Figure 26. If an ADC output value exceeds its respective ALARM high threshold register value, the ALARM output triggers. The ALARM condition remains in place until the measured value falls below the low threshold value. Figure 27 details a hysteresis-mode timing example.

When operating in interrupt mode, the ALARM output triggers when the measured ADC output value exceeds either the high or low threshold. However, in interrupt mode, the ALARM output remains active until reading the ALARM flag register. Reading the ALARM flag register resets the flag bits and the ALARM output.

The default values for the high and low threshold registers are the extremes of the measured range (all 1s or all 0s, respectively). The ALARM output can be configured to be open-drain or push-pull and active-high or active-low through the hardware ALARM configuration register. See Table 12. At power-up, the ALARM output is configured as an active-high output that operates in interrupt mode.

Automatic GATE Clamping

Configure the ALARM output to clamp the GATE1 output to ACLAMP1 or GATE2 output to ACLAMP2 in response to an ALARM condition through the hardware ALARM configuration register. See Table 12c. Set the ALM_CLMP_ bits, D5–D2, to clamp the respective channel's GATE output.

Each channel has four possible ALM_CLMP1/ALM_CLMP0 values:

- ALM_CLMP1/ALM_CLMP0 = 00
  Power-on reset state. GATE_ clamps through a series 2.4kΩ resistor to the ACLAMP_, regardless of any ALARM condition. Reset these 2 bits before attempting to change the DAC voltage.
- ALM_CLMP1/ALM_CLMP0 = 01
  The automatic GATE_ clamp is disabled in this mode. The GATE_ outputs are not affected by any ALARM conditions. The ALARM output function operates normally (samples beyond their thresholds still cause ALARM flags to be set and ALARM behaves according to the comparator/interrupt mode).
- ALM_CLMP1/ALM_CLMP0 = 10
  This mode provides fully automatic clamping. Prior to an ALARM condition, the GATE_ voltage is controlled by the sense voltage (MAX11014) or the DAC setting (MAX11015). When an ALARM condition triggers, the GATE_ voltage clamps to ACLAMP_. The clamp is applied as long as the ALARM condition is valid. The GATE_ clamp is released when a subsequent ADC conversion clears the ALARM condition. The GATE_ voltage is then restored to the sense voltage/DAC setting. Configure the ALARM output in comparator mode to assert when the GATE_ clamp is active.

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For a GATE_ voltage ALARM condition, GATE_ remains clamped and ALM_CLMP_ 10 mode functions the same as 11 mode. This exception breaks the feedback loop that would have otherwise been created by sampling the GATE_ voltage and then clamping that same voltage.

- ALM_CLMP1/ALM_CLMP0 = 11
  This mode provides semi-automatic clamping. Prior to an ALARM condition, the GATE_ voltage is controlled by the sense voltage (MAX11014) or the DAC setting (MAX11015). When an ALARM condition is triggered, the GATE_ voltage clamps to ACLAMP_. The clamp holds the GATE_ output in this condition, even if subsequent ADC samples are taken and all ALARM channels are cleared. To release the clamp, rewrite the ALM_CLMP1/ALM_CLMP0 bits to 11 or 01.

OPSAFE Inputs

Set the OPSAFE1 and OPSAFE2 inputs high to clamp the GATE1 and GATE2 outputs to the externally applied voltage at ACLAMP1 and ACLAMP2, respectively. OPSAFE1/OPSAFE2 override any software commands. The ALM_CLMP1/ALM_CLMP0 bits in the hardware ALARM configuration register also provide clamping functionality.

SRAM LUTs

The MAX11014/MAX11015 implement four independent lookup tables (LUTs). The LUTs are temperature based (TLUT) and numeric based (KLUT). Channel 1 and channel 2 each have a separate T and KLUT. Each LUT can store up to 48 separate data words. See Figure 28. In addition to storing data values, the LUT memory also contains configuration registers that specify LUT size, hysteresis bit value, and step size. Table 28 details how the LUTs are configured in memory.

Write data to the LUTs with the following sequence:

1) Write to the LUT address register to set the base address for the first data word (the LUTWORD bits are don't care in LUT writes).
2) Write to the LUT data register to write data values. Each time the LUT data register is written, the address in the LUT memory space is automatically incremented.

Read data from the LUTs with the following sequence:

1) Write to the LUT address register to set the base address for the first data word and the number of LUT words to be read.
2) Issue a single read command of the LUT data register. The MAX11014/MAX11015 then fill the FIFO with the requested LUT data, starting with the data at the LUTADD base address and incrementing until reaching either the top of memory or the number of locations based on the LUTWORD code.
3) Read each of the 16-bit LUT data words (including the 3- or 4-bit channel tag) from the FIFO at DOUT in SPI mode and SDA in I²C mode.

Begin a LUT write or read command by writing to the LUT address register. See Table 23. This register sets the LUT base address and the number of LUT locations to be read in a subsequent read of the LUT data register. Set the command byte to 7Ah to write to the LUT address register. Set the LUTWORD bits, D15–D8, to the number of LUT words (1 to 48) to be output during a LUT read operation. Set the LUTADD bits, D7–D0, to point to the base address of the LUT data. The TLUT1-0 to TLUT1-47 (channel 1) values are stored at addresses 00h to 2Fh. The TLUT2-0 to TLUT2-47 (channel 2) values are stored at addresses 30h to 5Fh. The KLUT1-0 to KLUT1-47 (channel 1) values are stored at addresses 60h to 8Fh. The KLUT2-0 to KLUT2-47 (channel 2) values are stored at addresses 90h to BFh.

The LUTs are defined by setting the following parameters:

1) The table's base value
2) The step size of the table (how far apart the entries are)
3) The hysteresis threshold size
4) The size of the LUT (the number of entries)

LUT Configuration

Write a LUT configuration sequence to initialize the step size, hysteresis threshold size, and size of the LUT. Determine the respective channel's temperature or KLUT configuration with the following sequence:

1) Set the LUTADD bits in the LUT address register to C0h (TLUT1), C1h (TLUT2), C2h (KLUT1) or C3h (KLUT2). See Table 28a.
2) Write to the LUT data register (LUTDAT15–LUTDAT0) to initialize the step size, hysteresis threshold size, and size of the LUT. See Table 28b.

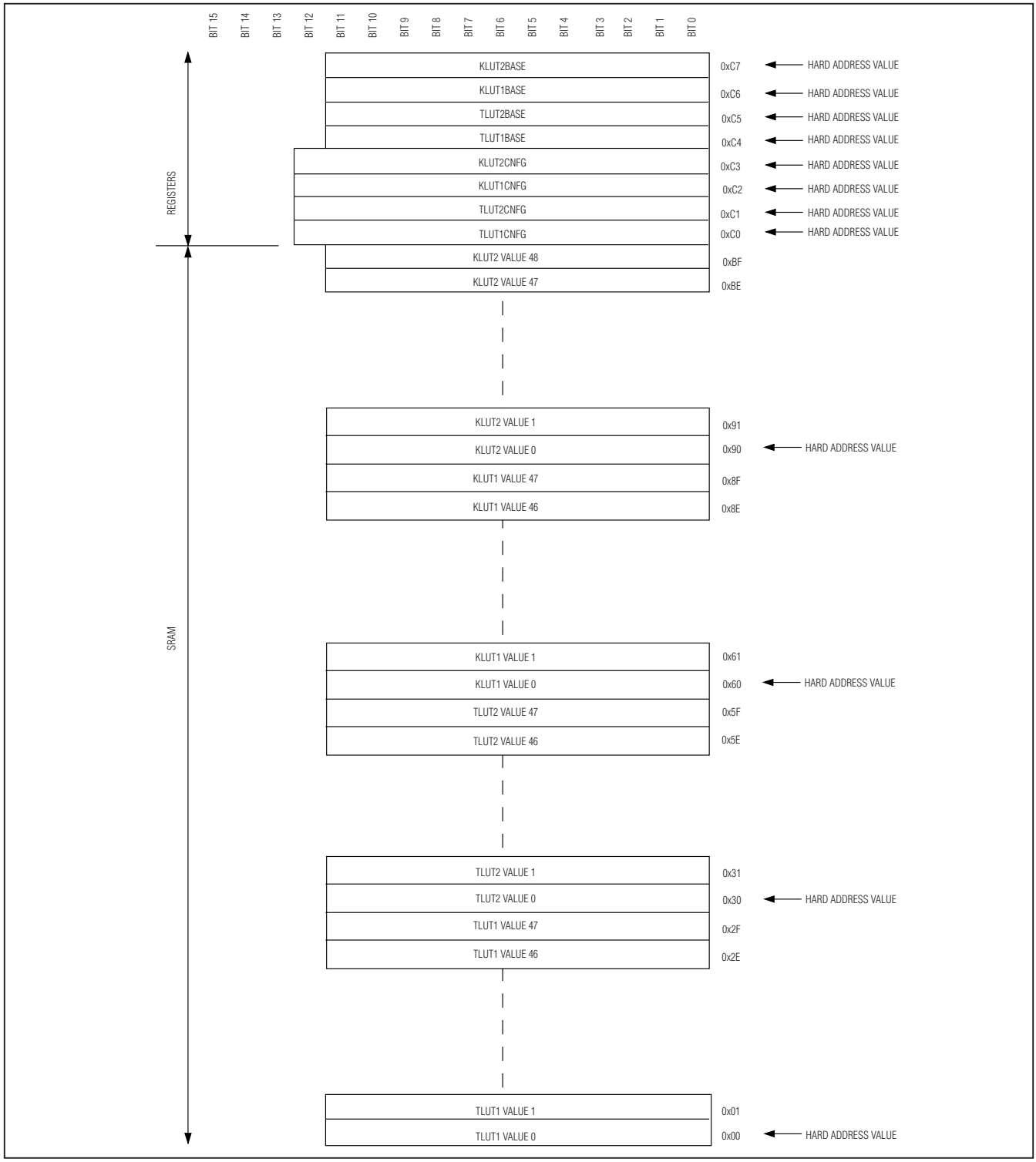

Figure 28. LUT Memory Space

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Table 28. LUT Addresses

LUTADD7–LUTADD0	HEX	FUNCTION
0000 0000 to 0010 1111	00 to 2F	TLUT1-0 to TLUT1-47
0011 0000 to 0101 1111	30 to 5F	TLUT2-0 to TLUT2-47
0110 0000 to 1000 1111	60 to 8F	KLUT1-0 to KLUT1-47
1001 0000 to 1011 1111	90 to BF	KLUT2-0 to KLUT2-47
1100 0000	C0	TLUT1 configuration
1100 0001	C1	TLUT2 configuration
1100 0010	C2	KLUT1 configuration
1100 0011	C3	KLUT2 configuration
1100 0100	C4	TLUT1 base
1100 0101	C5	TLUT2 base
1100 0110	C6	KLUT1 base
1100 0111	C7	KLUT2 base

When performing a write operation, the first 3 LUTDAT bits, D15, D14, and D13 are don't care. When performing a read operation, these bits are set to the LUT data channel tag 110. Bits D12–D7 set the size of the LUT in binary format. Set the LUT size between 8 (001000) and 48 (110000). Bits D6, D5, and D4 set the hysteresis bit threshold. Using the temperature LUT as an example, if the HYS value is 101 (16 bits) and the latest temperature measurement differs from the last one by more than 2°C, a new TLUT operation is performed and a new TLUT value is calculated. Bits D3–D0 set the LUT step size. See Table 28c. The step size is based on the value of 2^N, with N equaling the digital value of the STEP bits. Set the step size between 1 (2^0) and 512 (2^9). Locations 1010 (2^{10}) to 1111 (2^{15}) are reserved. Do not write to these locations.

LUT Base

The following two-step sequence determines the respective channel's temperature or KLUT base value:

1) Set the LUTADD bits in the LUT address register to C4h (TLUT1), C5h (TLUT2), C6h (KLUT1) and C7h (KLUT2). See Table 28d.
2) Write to the LUT data register (LUTDAT15–LUTDAT0) to initialize the base word. The KLUT base value is stored in binary format, with the LSB equaling 1. The TLUT base value is stored in two's-complement format, with the LSB equaling +0.125°C.

Table 28a. LUT Data Register Memory Map

ADDRESS NAME	LUTADD7–LUTADD0 (HEX)	LUTDAT15															LUTDAT0
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TLUT1	00 to 2F	1	1	0	X	MSB	—	—	—	—	—	—	—	—	—	—	LSB
TLUT2	30 to 5F	1	1	0	X	MSB	—	—	—	—	—	—	—	—	—	—	LSB
KLUT1	60 to 8F	1	1	0	X	MSB	—	—	—	—	—	—	—	—	—	—	LSB
KLUT2	90 to BF	1	1	0	X	MSB	—	—	—	—	—	—	—	—	—	—	LSB
TLUT1 Configuration	C0	1	1	0	See Table 28b for bit details.												
TLUT2 Configuration	C1	1	1	0	See Table 28b for bit details.												
KLUT1 Configuration	C2	1	1	0	See Table 28b for bit details.												
KLUT2 Configuration	C3	1	1	0	See Table 28b for bit details.												
TLUT1 Base	C4	1	1	0	X	MSB	—	—	—	—	—	—	—	—	—	—	LSB
TLUT2 Base	C5	1	1	0	X	MSB	—	—	—	—	—	—	—	—	—	—	LSB
KLUT1 Base	C6	1	1	0	X	MSB	—	—	—	—	—	—	—	—	—	—	LSB
KLUT2 Base	C7	1	1	0	X	MSB	—	—	—	—	—	—	—	—	—	—	LSB

X = Don't care.

Table 28b. LUT Configuration

BIT NAME	DATA BIT	RESET	FUNCTION
SIZE5	D12	0	The SIZE field is a straight binary representation of the size of the respective LUT. SIZE5 is the MSB of the 6 SIZE bits. SIZE0 is the LSB. Set the size of the LUT between eight entries (001000) and 48 entries (110000).
SIZE4	D11	0	
SIZE3	D10	0	
SIZE2	D9	0	
SIZE1	D8	0	
SIZE0	D7	0	
HYS2	D6	0	The HYS2, HYS1, and HYS0 bits set the hysteresis bit threshold for each LUT. When the difference between the last index value and the next index value is less than the value set by HYS2, HYS1, and HYS0 bits, the LUT operation for that parameter is omitted and the last value calculated for the respective LUT is used. Set the HYS2 (MSB), HYS1, and HYS0 (LSB) bits to the following hysteresis bit values: 000: 0 bits (a new LUT operation is always performed) 001: 1 bit (if the value differs by 1 bit, a new LUT operation is performed) 010: 2 bits 011: 4 bits 100: 8 bits 101: 16 bits 110: 32 bits 111: 64 bits
HYS1	D5	0	
HYS0	D4	0	
STEP3	D3	0	The STEP3–STEP0 bits determine the LUT 12-bit step size. The step size is a 2^N value. The N value is determined by the STEP bits, with STEP3 being the MSB and STEP0 the LSB. See Table 28c for the TLUT and KLUT step-size equivalents.
STEP2	D2	0	
STEP1	D1	0	
STEP0	D0	0	

Table 28c. LUT Configuration Step Sizes

STEP3	STEP2	STEP1	STEP0	LUT STEP SIZE	TLUT STEP-SIZE EQUIVALENT	KLUT STEP-SIZE EQUIVALENT
0	0	0	0	1	+0.125°C	1
0	0	0	1	2	+0.25°C	2
0	0	1	0	4	+0.5°C	4
0	0	1	1	8	+1°C	8
0	1	0	0	16	+2°C	16
0	1	0	1	32	+4°C	32
0	1	1	0	64	+8°C	64
0	1	1	1	128	+16°C	128
1	0	0	0	256	+32°C	256
1	0	0	1	512	+64°C	512
1	0	1	0	Reserved. Do not use.		
1	0	1	1	Reserved. Do not use.		
1	1	0	0	Reserved. Do not use.		
1	1	0	1	Reserved. Do not use.		
1	1	1	0	Reserved. Do not use.		
1	1	1	1	Reserved. Do not use.		

Table 28d. LUT Base

BIT NAME	DATA BIT	RESET STATE	FUNCTION
BASE11–BASE0	D11–D0	N/A	The base value signifies the starting point for the LUT. The KLUT base value is stored in binary format, with the LSB equaling 1. The TLUT base value is stored in two's-complement format, with the LSB equaling +0.125°C.

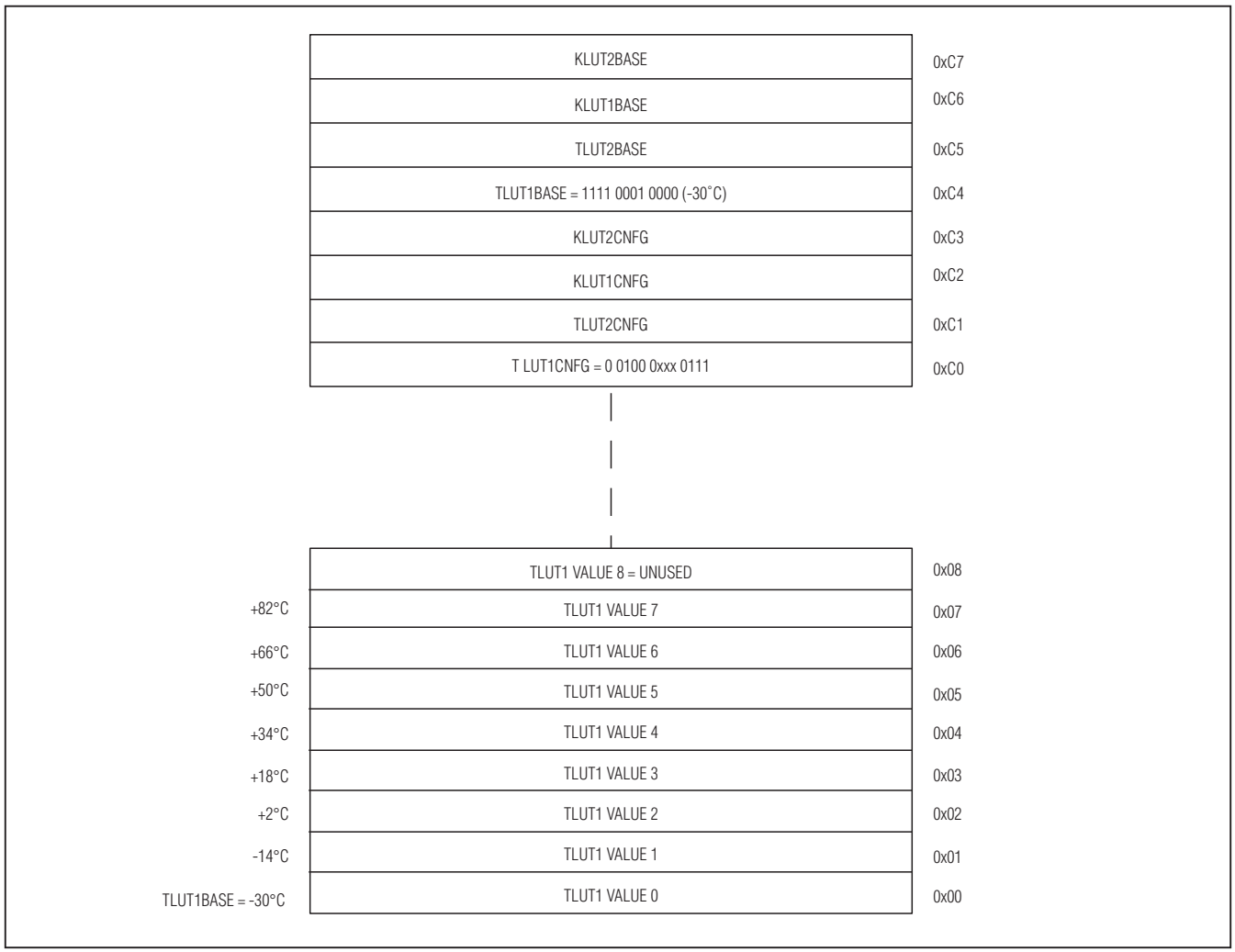

Figure 29. TLUT Example

Both the T and KLUTs contain 12-bit data. The TLUT data is stored in two's-complement format with decimal values ranging from -2048/2048 (-1) to +2047/2048 (+0.9995) in steps of approximately 0.0005.

The KLUT data is stored in binary format with decimal values ranging from 0 to +4095/4096 (0.9998) in steps of approximately 0.0002.

The temperature LUT data is stored in two's-complement format. Figure 29 details a channel 1 TLUT example with eight entries where the base temperature is -30°C and the step size is 128 (+16°C between each entry).

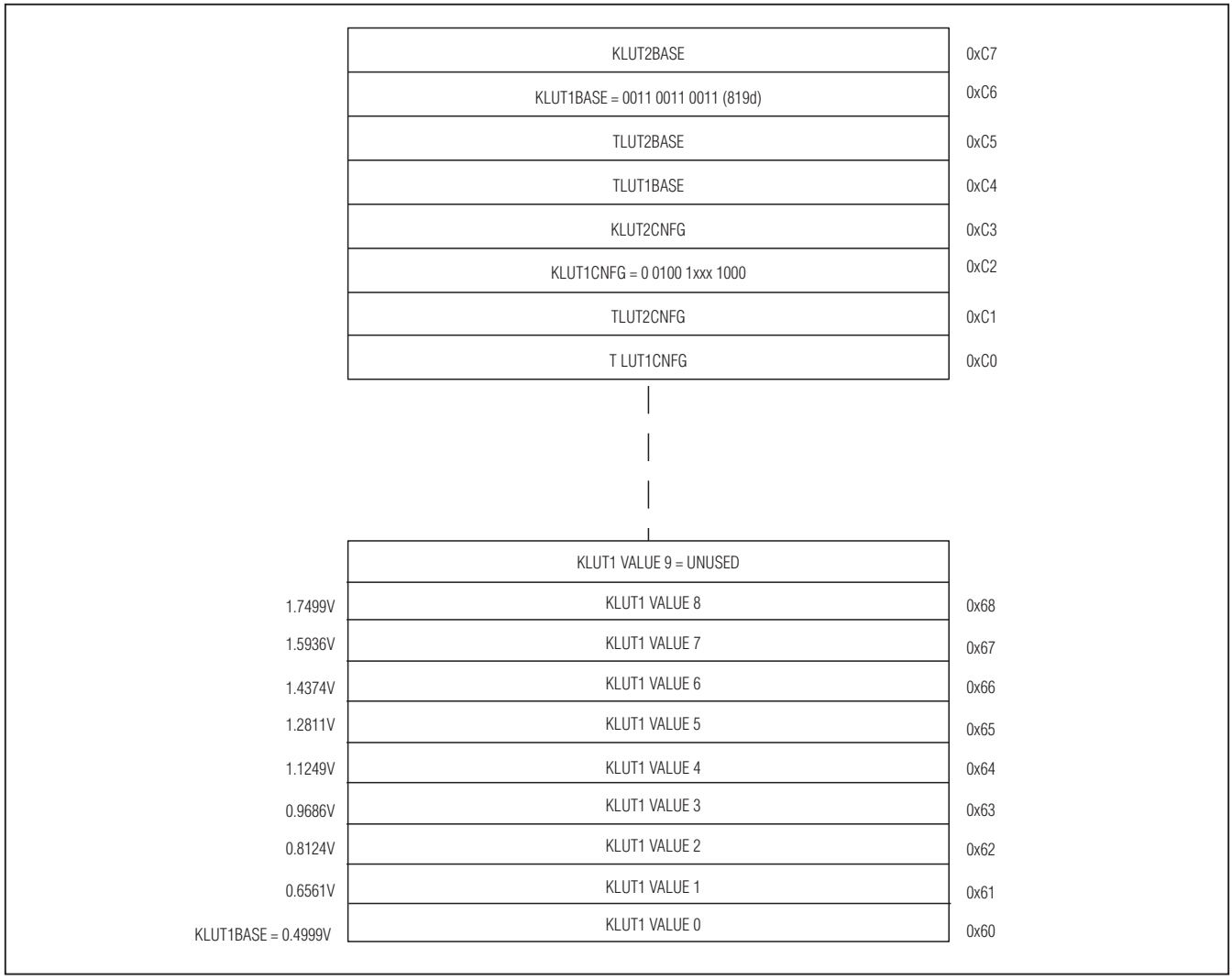

Figure 30. KLUT Example

The KLUT data is stored in straight binary format. Figure 30 details a channel 1 KLUT example with nine entries, a range of 0.5V to 1.7V, and a step size of 256.

Assuming V_{REFDAC} = +2.5V, the base value (819d) is determined by the following equation:

$$\frac{0.5V}{2.5V} \times 4096 = 819d$$

Internally Timed Acquisitions and Conversions

Clock Mode 00

In clock mode 00, power-up, acquisition, conversion, and power-down are all initiated by writing to the ADC conversion register and performed automatically using the internal oscillator. This is the default clock mode. With ADCMON set to 1, the ADC sets the BUSY output high, powers up, scans all requested channels, stores the results in the FIFO, and then powers down. After the scan is complete, the BUSY output is pulled low and the results are available in the FIFO.

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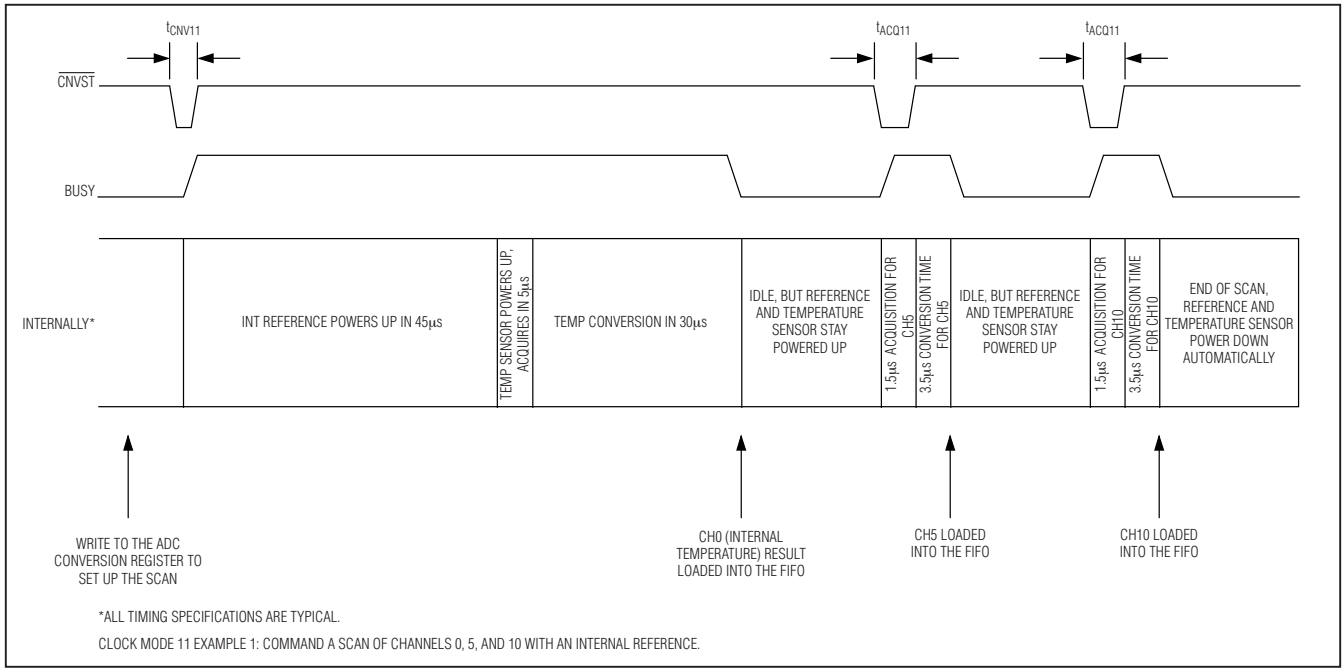

Figure 31. Clock Mode 11 Timing Example 1

Clock Mode 01

In clock mode 01, power-up, acquisition, conversion, and power-down are all initiated by a single $\overline{CNVST}$ low pulse and performed automatically using the internal oscillator. Initiate a scan by writing to the ADC conversion register to indicate which channels to convert. Then set $\overline{CNVST}$ low for at least 20ns only once to convert all of the channels selected in the ADC conversion register. With ADCMON set to 1, the ADC sets the BUSY output high, powers up, scans all requested channels, stores the results in the FIFO, and powers down. After the scan is complete, the BUSY output is pulled low and the results are available in the FIFO.

Externally Timed Acquisitions and Conversions

Clock Mode 10

Clock mode 10 is reserved. Do not use this clock mode.

Clock Mode 11

In clock mode 11, conversions are initiated by $\overline{CNVST}$ one at a time and performed using the internal oscillator. See Figures 31 and 32 for a pair of clock mode 11 timing examples. Initiate a conversion by writing to the ADC conversion register and pulling $\overline{CNVST}$ low for at least 1.5µs for each channel converted. Different timing parameters apply to whether the conversion is a temperature, a voltage using the external reference, or a voltage using the internal reference conversion.

Internal and external temperature conversions are internally timed. Set $\overline{CNVST}$ low for at least 20ns to acquire a temperature conversion. The BUSY output goes high while sampling and the internal reference typically requires 45µs to power up. The temperature sensor circuit requires 5µs to power up. Temperature conversion results are available after an additional 30µs. The typical conversion time of the initial temperature sensor scan is 80µs. Subsequent temperature scans only take 30µs typically as the internal reference and temperature sensor circuits are already powered. See the *Electrical Characteristics* table for more details.

Set $\overline{CNVST}$ low for at least 1.5µs to acquire a voltage conversion using the external reference. The BUSY output goes high while sampling and the conversion results are available after an additional 3.5µs (typ).

Set $\overline{CNVST}$ low for at least 50µs to trigger an initial voltage conversion using the internal reference. The BUSY output goes high and the conversion results are available after an additional 3.5µs typically. Additional voltage conversions do not require the acquisition time of powering up the internal reference. Set $\overline{CNVST}$ low for at least 1.5µs to power up the ADC and place it in track mode. The BUSY output goes high while sampling and the conversion results are available after 5.6µs.

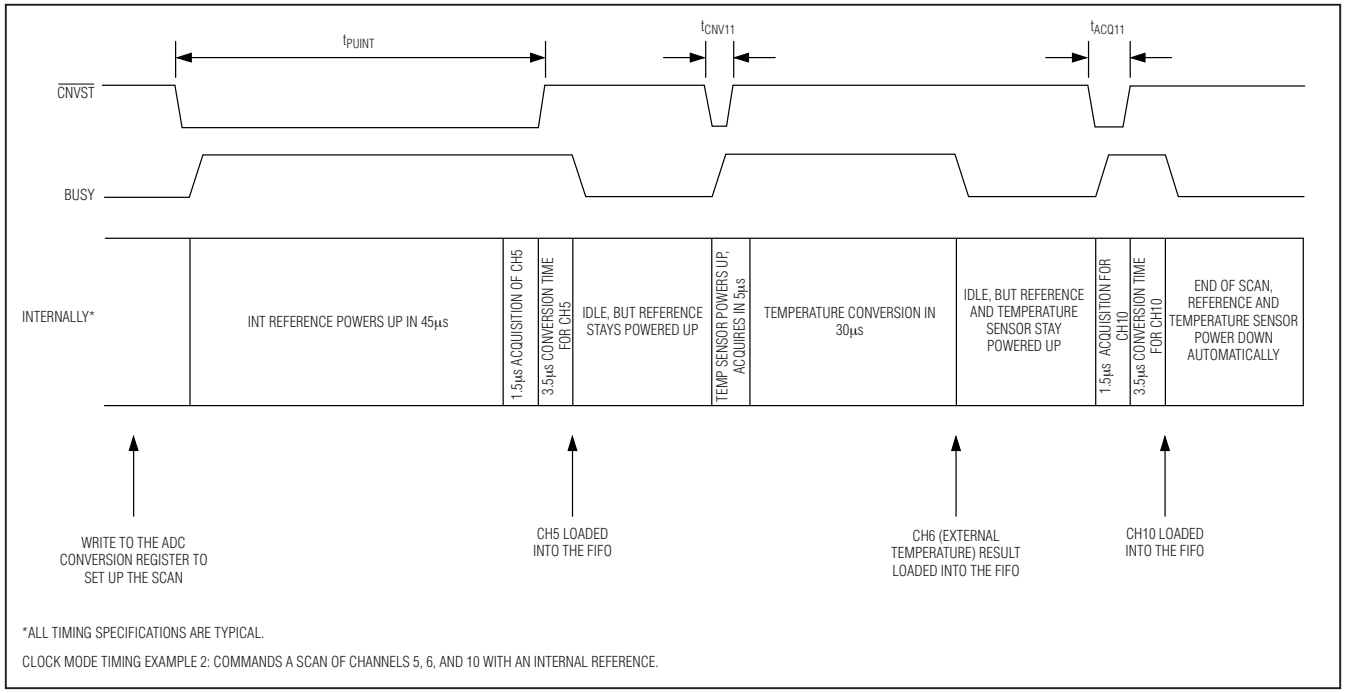

Figure 32. Clock Mode 11 Timing Example 2

Changing Clock Modes During ADC Conversions

If the hardware configuration register's CKSEL1 or CKSEL0 bits are changed while the ADC is performing a conversion (or series of conversions), the MAX11014/MAX11015 reacts in one of three ways:

- CKSEL1/CKSEL0 = 00 and is then changed to another value:
  The ADC completes the already triggered series of conversions and then goes idle. The BUSY output remains high until the conversions are completed. The MAX11014/MAX11015 then responds according to commands with the new clock mode.
- CKSEL1/CKSEL0 = 01 and is then changed to another value:
  If waiting for the initial external trigger, the MAX11014/MAX11015 immediately exit clock mode 01, power down the ADC, and go idle. If a conversion sequence is in progress, that conversion is completed and then the ADC goes idle. The BUSY output remains high until the conversions are completed. The MAX11014/MAX11015 then respond according to commands with the new clock mode.
- CKSEL1/CKSEL0 = 11 and is then changed to another value:
  If waiting for an external trigger, the MAX11014/MAX11015 immediately exit clock mode 11, power down the ADC, and go idle. The BUSY output stays low and waits for the external trigger. If a conversion sequence is in progress, that conversion is completed and then the ADC goes idle.

Turning the Continuous Convert Bit On and Off

When switching between continuous and single convert modes, the clock mode requires resetting to avoid hanging the ADC sequencing routine. To turn off continuous convert, complete the following sequence:

1) Turn off the selected channels but leave the continuous convert bit asserted.
2) Turn off the continuous convert bit.
3) Change from the current clock mode to any other mode.
4) Change the clock mode back.
5) Clear the FIFO.
6) Perform the single conversion.
7) Read the FIFO results.
8) Turn continuous convert back on.

Turning on continuous convert can be done by setting the CONCONV bit in the ADCCON register.

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Applications Information

Layout Considerations

For the external temperature sensor to perform to specifications, care must be taken to place the MAX11014/MAX11015 as close as is practical to the remote diode. Traces of DXP_ and DXN_ should not be routed across noisy lines and buses. DXP_ and DXN_ routes should be guarded by ground traces on either sides and should be routed over a quiet ground plane. Traces should be wide enough (> 10mm) to lower inductance, which tends to pick up radiated noise.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. INL for the MAX11014/MAX11015 is measured using the endpoint method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

ADC Offset Error

For an ideal converter, the first transition occurs at 0.5 LSB, above zero. Offset error is the amount of deviation between the measured first transition point and the ideal first transition point.

ADC Gain Error

When a positive full-scale voltage is applied to the converter inputs, the digital output is all ones (FFFh). The transition from FFEh to FFFh occurs at 1.5 LSB below full scale. Gain error is the amount of deviation between the measured full-scale transition point and the ideal full-scale transition point with the offset error removed.

DAC Offset Error

DAC offset error is determined by loading a code of all zeros into the DAC and measuring the analog output voltage.

DAC Gain Error

DAC gain error is defined as the amount of deviation between the ideal transfer function and the measured transfer function, with the offset error removed, when loading a code of all 1s into the DAC.

Aperture Jitter

Aperture jitter, t_{AJ}, is the statistical distribution of the variation in the sampling instant.

Aperture Delay

Aperture delay (t_{AD}) is the time between the rising edge of the sampling clock and the instant when an actual sample is taken.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise, including thermal noise, reference noise, clock jitter, etc. Therefore, SNR is calculated by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS noise plus distortion. RMS noise plus distortion includes all spectral components to the Nyquist frequency excluding the fundamental and the DC offset:

$$SINAD\ (dB) = 20 \times \log (SIGNAL_{RMS} / NOISE_{RMS})$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the effective number of bits as follows:

$$ENOB = (SINAD - 1.76) / 6.02$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the fundamental amplitude, and V_2 through V_6 are the amplitudes of the first five harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spectral component.

ADC Channel-to-Channel Crosstalk

Bias the ON channel to midscale. Apply a full-scale sine-wave test tone to all OFF channels. Perform an FFT on the ON channel. ADC channel-to-channel crosstalk is expressed in dB as the amplitude of the FFT spur at the frequency associated with the OFF channel test tone.

Intermodulation Distortion (IMD)

IMD is the total power of the intermodulation products relative to the total input power when two tones, f_1 and f_2, are present at the inputs. The intermodulation products are ($f_1 \pm f_2$), ($2 \times f_1$), ($2 \times f_2$), ($2 \times f_1 \pm f_2$), ($2 \times f_2 \pm f_1$). The individual input tone levels are at -7dBFS.

Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC in such a way that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB. Note that the track/hold (T/H) performance is usually the limiting factor for the small-signal input bandwidth.

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB. This point is defined as full-power input bandwidth frequency.

DAC Digital Feedthrough

DAC digital feedthrough is the amount of noise that appears on the DAC output when the DAC digital control lines are toggled.

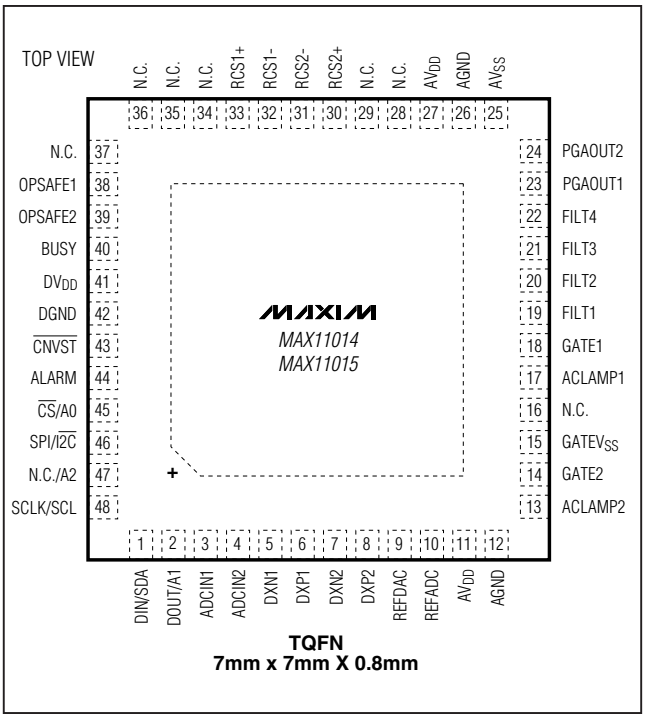
ADC Power-Supply Rejection

Power-supply rejection is defined as the shift in offset error when the power supply is moved from the minimum operating voltage to the maximum operating voltage.

DAC Power-Supply Rejection

DAC PSR is the amount of change in the converter's value at full scale as the power-supply voltage changes from its nominal value. PSR assumes the converter's linearity is unaffected by changes in the power-supply voltage.

Pin Configuration



Chip Information

PROCESS: BiCMOS

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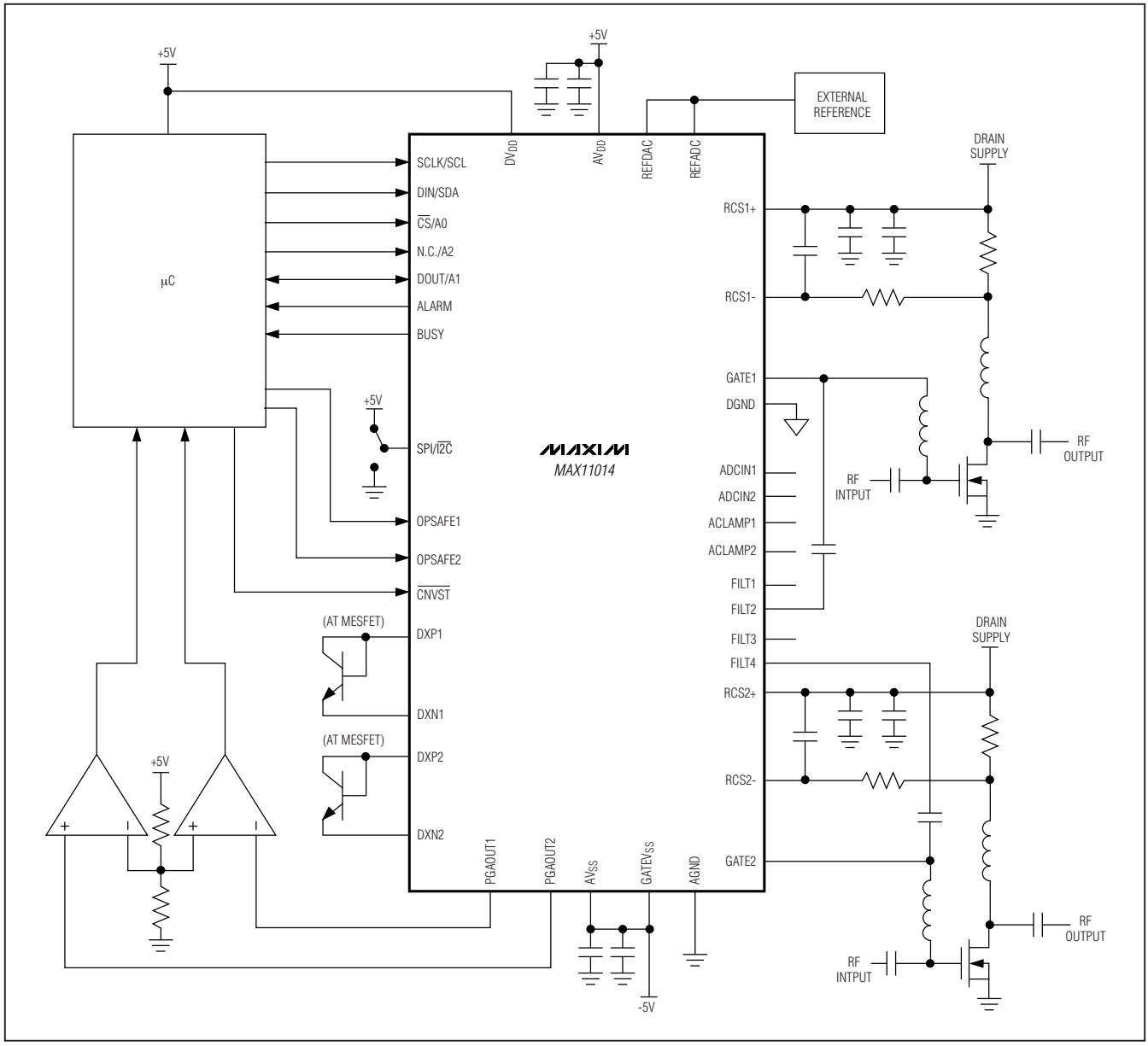
Typical Operating Circuit



Appendix: Startup Code Example

Below is a sample startup code for the MAX11014. This code ensures clean startup of the part irrespective of power supply ramp speed and starts the device regulating to 312.5mV on both channels. Change the THRUDAC_ writes to change the voltage across the sense resistor. Note it should be ran after the power supplies have stabilized. A PGA calibration can be run, but is not required for the part to function.

REGISTER MNEMONIC	REGISTER ADDRESS (hex)	CODE WRITTEN	NOTES
SHUT	0x64	0x0000	Removes the global power-down.
SHUT	0x64	0x0000	Powers up all parts of the MAX11014.
SCLR	0x74	0x0020	Arms the full reset.
SCLR	0x74	0x0040	Completes the full reset.
SCLR	0x74	0x0020	Arms the full reset.*
SCLR	0x74	0x0040	Completes the full reset.*
FLAG	0xF6		Read of FLAG register to verify reset good. Code should read 0xX042 if reset good.
SHUT	0x64	0x0000	Removes the global power-down.
SHUT	0x64	0x0000	Powers up all parts of the MAX11014.
HCFG	0x38	0x004F	Sets internal references for both DAC and ADC.
THRUDAC1	0x4A	0x7FF	Midscale on DAC1, sets sense voltage to 312.5mV.
THRUDAC2	0x4E	0x7FF	Midscale on DAC2, sets sense voltage to 312.5mV.
PGACAL	0x5E	0x0002	Completes tracking CAL (wait for BUSY to fall).
ALMHCFG	0x3C	0x0014	Releases GATE clamps and regulation begins.

**Note double reset. This ensures that the internal ROM is reset correctly after power-up and that the ROM data is latched correctly irrespective of the power-supply ramp speed.*

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 TQFN-EP	T4877-6	**21-0144**

Automatic RF MESFET Amplifier Drain-Current Controllers

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	9/08	Added appendix for generic power-up sequence, added note to EC table, and changed DNL spec	3, 4, 32, 48, 69
3	11/08	Changed EC table and updated *Appendix: Startup Code Example* section	3, 69