**EVALUATION KIT AVAILABLE**

**_MAXIM_**

# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

_MAX1117/MAX1118/MAX1119_

## General Description

The MAX1117/MAX1118/MAX1119 low-power, 8-bit, dual-channel, analog-to-digital converters (ADCs) feature an internal track/hold (T/H) voltage reference (MAX1117/MAX1119), clock, and serial interface. The MAX1118 is specified from +2.7V to +5.5V and consumes only 135µA at 100ksps. The MAX1117 is specified from +2.7V to +3.6V, and the MAX1119 is specified from +4.5V to +5.5V, each consumes only 175µA at 100ksps.

The full-scale analog input range is determined by the internal reference of +2.048V (MAX1117) or +4.096V (MAX1119), or by an externally applied reference ranging from +1V to $V_{DD}$ (MAX1118). All devices feature an automatic shutdown mode that reduces supply current to <1µA when the device is not in use. The 3-wire serial interface directly connects to SPI™, QSPI™, and MICROWIRE™ devices without external logic. Conversions up to 100ksps are performed using an internal clock.

The MAX1117/MAX1118/MAX1119 are available in an 8-pin SOT23 package with a footprint that is only 11% of an 8-pin plastic DIP.

## Applications

Low-Power, Handheld Portable Devices

System Diagnostics

Battery-Powered Test Equipment

Solar-Powered Remote Systems

Receive Signal Strength Indicators

4mA to 20mA Powered Remote Data Acquisition Systems

_SPI/QSPI are trademarks of Motorola, Inc._

_MICROWIRE is a trademark of National Semiconductor, Corp._
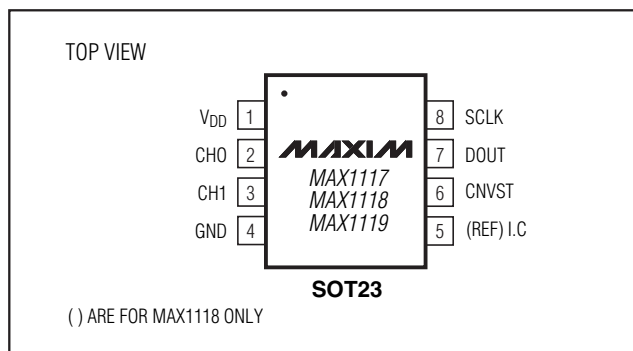
**_Functional Diagram appears at end of data sheet._**

## Features

♦ **Single Supply**
  **+2.7V to +3.6V (MAX1117)**
  **+2.7V to +5.5V (MAX1118)**
  **+4.5V to +5.5V (MAX1119)**

♦ **Internal Track/Hold: 100kHz Sampling Rate**

♦ **Internal Reference**
  **+2.048V (MAX1117)**
  **+4.096V (MAX1119)**

♦ **Reference Input Range: 0 to $V_{DD}$ (MAX1118)**

♦ **SPI/QSPI/MICROWIRE-Compatible Serial Interface**

♦ **Small 8-Pin SOT23 Package**

♦ **Automatic Power-Down**

♦ **Analog Input Range: 0 to $V_{REF}$**

♦ **Low Power**
  **175µA at 100ksps (typ) (MAX1117/MAX1119)**
  **135µA at 100ksps (typ) (MAX1118)**
  **18µA at 10ksps (typ)**
  **1µA (typ) in Power-Down Mode**

## Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE | TOP MARK |
|---|---|---|---|
| **MAX1117**EKA | -40°C to +85°C | 8 SOT23 | AADW |
| **MAX1118**EKA | -40°C to +85°C | 8 SOT23 | AADX |
| **MAX1119**EKA | -40°C to +85°C | 8 SOT23 | AADY |

## Pin Configuration

TOP VIEW

| | | | |
|---|---|---|---|
| $V_{DD}$ | 1 | 8 | SCLK |
| CH0 | 2 | 7 | DOUT |
| CH1 | 3 | 6 | CNVST |
| GND | 4 | 5 | (REF) I.C |

_MAXIM_
MAX1117
MAX1118
MAX1119

**SOT23**

( ) ARE FOR MAX1118 ONLY

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# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND.............................................................-0.3V to +6.0V
CH0,CH1, REF to GND...............................-0.3V to ($V_{DD}$ + 0.3V)
Digital Output to GND ................................-0.3V to ($V_{DD}$ + 0.3V)
Digital Input to GND .............................................-0.3V to +6.0V
Maximum Current into Any Pin .........................................±50mA
Continuous Power Dissipation ($T_A$ = +70°C)
  8-Pin SOT23 (derate 8.9mW/°C above +70°C)............714mW

Operating Temperature Range
  MAX1117EKA ..................................................-40°C to + 85°C
  MAX1118EKA ..................................................-40°C to + 85°C
  MAX1119EKA ..................................................-40°C to + 85°C
Storage Temperature Range .............................-60°C to +150°C
Lead Temperature (soldering, 10s) .................................+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = +2.7V to +3.6V (MAX1117), $V_{DD}$ = +4.5V to +5.5V (MAX1119), $V_{DD}$ = REF = +2.7V to +5.5V (MAX1118),$T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC ACCURACY** | | | | | | |
| Resolution | | | 8 | | | Bits |
| Relative Accuracy (Note 1) | INL | | | | ±1 | LSB |
| Differential Nonlinearity | DNL | | | | ±1 | LSB |
| Offset Error | | | | | ±0.5 | LSB |
| Gain Error | | MAX1118, REF = $V_{DD}$ | | | ±1 | LSB |
| | | MAX1117/MAX1119 | | | ±5 | %FSR |
| Gain Temperature Coefficient | | MAX1118 | | ±5 | | ppm/°C |
| | | MAX1117/MAX1119 | | ±90 | | |
| Total Unadjusted Error | TUE | MAX1118 | | ±0.5 | ±1 | LSB |
| Channel-to-Channnel Offset Matching | | | | ±0.1 | | LSB |
| **DYNAMIC PERFORMANCE** (25kHz sinewave input, $V_{IN}$ = $V_{REF(pp)}$, $f_{SCLK}$ = 5MHz, $f_{sample}$ = 100ksps, $R_{IN}$ = 100Ω) | | | | | | |
| Signal-to-Noise Plus Distortion | SINAD | | | 48 | | dB |
| Total Harmonic Distortion (Up to the 5th Harmonic) | THD | | | -69 | | dB |
| Spurious-Free Dynamic Range | SFDR | | | 66 | | dB |
| Small Signal Bandwidth | $f_{-3dB}$ | | | 4 | | MHz |
| **ANALOG INPUT** | | | | | | |
| Input Voltage Range | | | 0 | | $V_{REF}$ | V |
| Input Leakage Current | | $V_{CH\_}$ = 0 or $V_{DD}$ | | ±0.7 | ±10 | µA |
| Input Capacitance | $C_{IN}$ | | | 18 | | pF |
| **INTERNAL REFERENCE** | | | | | | |
| Voltage | $V_{REF}$ | MAX1117 | | 2.048 | | V |
| | | MAX1119 | | 4.096 | | |

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## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +2.7V to +3.6V (MAX1117), $V_{DD}$ = +4.5V to +5.5V (MAX1119), $V_{DD}$ = REF = +2.7V to +5.5V (MAX1118),$T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)
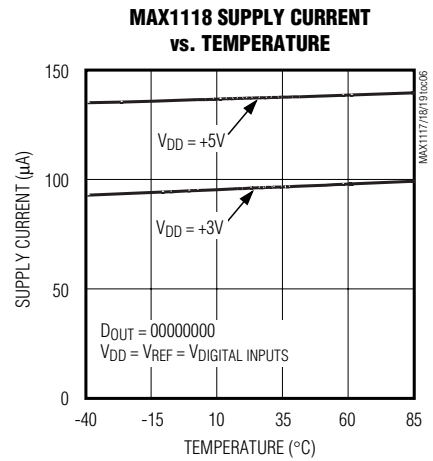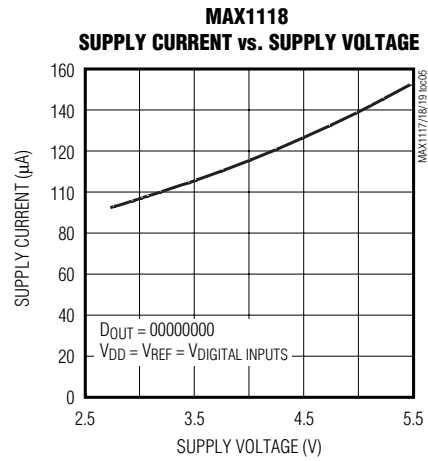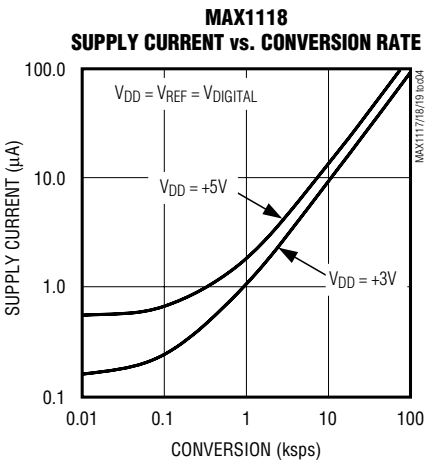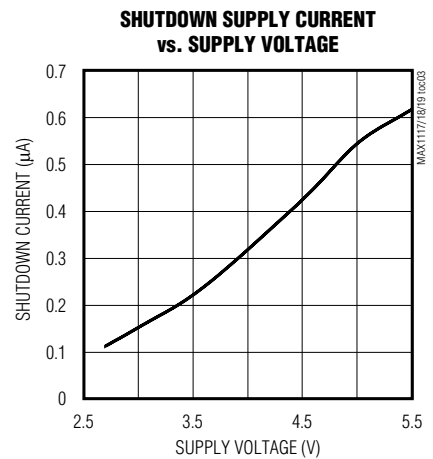
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **EXTERNAL REFERENCE** (MAX1118 ONLY) | | | | | | |
| Input Voltage Range | | | 1.0 | | $V_{DD}$ | V |
| Input Current | | Ave, $V_{DD}$ = REF = +5.5V at 100ksps | | 10 | 20 | µA |
| **POWER REQUIREMENTS** | | | | | | |
| Supply Voltage | $V_{DD}$ | MAX1118 | 2.7 | | 5.5 | V |
| | | MAX1117 | 2.7 | | 5.5 | |
| | | MAX1119 | 4.5 | | 5.5 | |
| Supply Current (Note 2) | $I_{DD}$ | MAX1119, $f_{SAMPLE}$ = 100ksps, zero-scale input | | 182 | 230 | µA |
| | | MAX1117/MAX1118, $f_{SAMPLE}$ = 100ksps, zero-scale input | | 135 | 190 | |
| | | MAX1119, $f_{SAMPLE}$ = 10ksps, zero-scale input | | 19 | 25 | |
| | | MAX1117/MAX1118, $f_{SAMPLE}$ = 10ksps, zero-scale input | | 14 | 21 | |
| | | Shutdown | | 0.8 | 10 | |
| Supply Rejection Ratio | PSRR | Full-scale or 0 input | | ±0.5 | ±1 | LSB/V |
| **DIGITAL INPUTS (CNVST AND SCLK)** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 2 | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.8 | V |
| Input Hystersis | $V_{HYST}$ | | | 0.2 | | V |
| Input Current High | $I_{IH}$ | | | | ±10 | µA |
| Input Current Low | $I_{IL}$ | | | | ±10 | µA |
| Input Capacitance | $C_{IN}$ | | | 2 | | pF |
| **DIGITAL OUTPUT (DOUT)** | | | | | | |
| Output High Voltage | $V_{OH}$ | $I_{SOURCE}$ = 2mA | $V_{DD}$ - 0.5 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 2mA | | | 0.4 | V |
| | | $I_{SINK}$ = 4mA | | | 0.8 | V |
| Three-State Leakage Current | $I_L$ | | | ±0.01 | ±10 | µA |
| Three-State Output Capacitance | $C_{OUT}$ | | | 4 | | pF |
| **TIMING CHARACTERISTICS** (Figures 6a–6d) | | | | | | |
| CNVST High Time | $t_{csh}$ | | 100 | | | ns |
| CNVST Low Time | $t_{csi}$ | | 100 | | | ns |
| Conversion Time | $t_{conv}$ | | | | 7.5 | µs |
| Serial Clock High Time | $t_{ch}$ | | 75 | | | ns |
| Serial Clock Low Time | $t_{cl}$ | | 75 | | | ns |
| Serial Clock Period | $t_{cp}$ | | 200 | | | ns |
| Falling of CNVST to DOUT Active | $t_{csd}$ | $C_{LOAD}$ = 100pF, Figure 1 | | | 100 | ns |

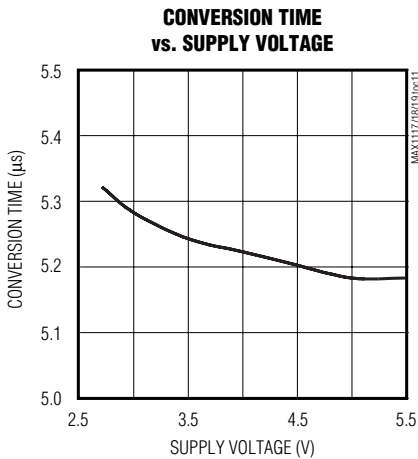**MAX1117/MAX1118/MAX1119**

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# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +2.7V to +3.6V (MAX1117), $V_{DD}$ = +4.5V to +5.5V (MAX1119), $V_{DD}$ = REF = +2.7V to +5.5V (MAX1118),$T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Serial Clock Falling Edge to DOUT | $t_{cd}$ | $C_{LOAD}$ = 100pF | 10 | | 100 | ns |
| Serial Clock Rising Edge to DOUT High-Z | $t_{chz}$ | $C_{LOAD}$ = 100pF, Figure 2 | 100 | | 500 | ns |
| Last Serial Clock to Next CNVST (Successive Conversions on CH0) | $t_{ccs}$ | | 50 | | | ns |

**Note 1:** Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range and offset have been calibrated.

**Note 2:** Input = 0, with logic input levels of 0 and $V_{DD}$.

## Typical Operating Characteristics

($V_{DD}$ = +3V (MAX1117), $V_{DD}$ = +5V (MAX1119), $V_{DD}$ = $V_{REF}$ = +3V (MAX1118), $f_{SCLK}$ = 5MHz, $f_{SAMPLE}$ = 100ksps, $C_{LOAD}$ = 100pF, $T_A$ = +25°C, unless otherwise noted.)
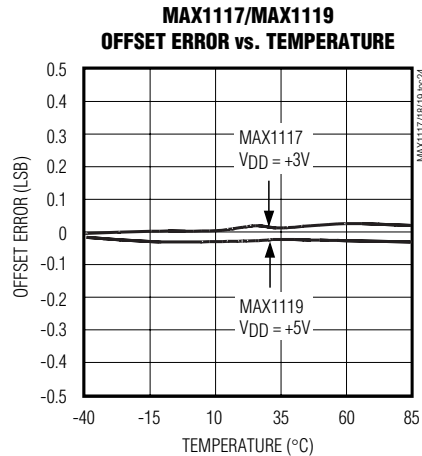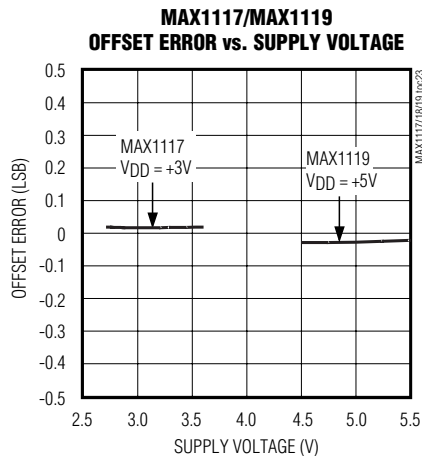
INTEGRAL NONLINEARITY vs.OUTPUT CODE

DIFFERENTIAL NONLINEARITY vs.OUTPUT CODE

SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE

MAX1118 SUPPLY CURRENT vs. CONVERSION RATE

MAX1118 SUPPLY CURRENT vs. SUPPLY VOLTAGE

MAX1118 SUPPLY CURRENT vs. TEMPERATURE

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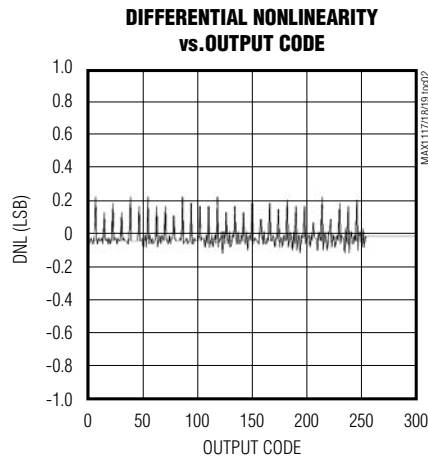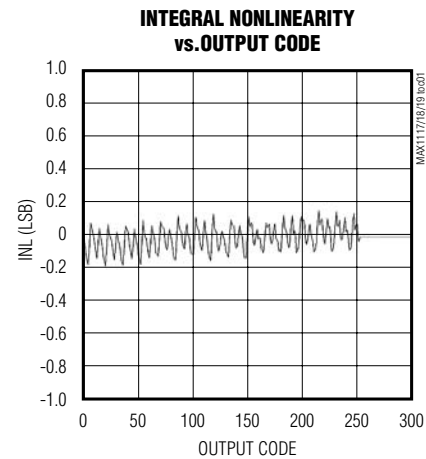
## Typical Operating Characteristics (continued)

($V_{DD}$ = +3V (MAX1117), $V_{DD}$ = +5V (MAX1119), $V_{DD}$ = $V_{REF}$ = +3V (MAX1118), $f_{SCLK}$ = 5MHz, $f_{SAMPLE}$ = 100ksps, $C_{LOAD}$ = 100pF, $T_A$ = +25°C, unless otherwise noted.)
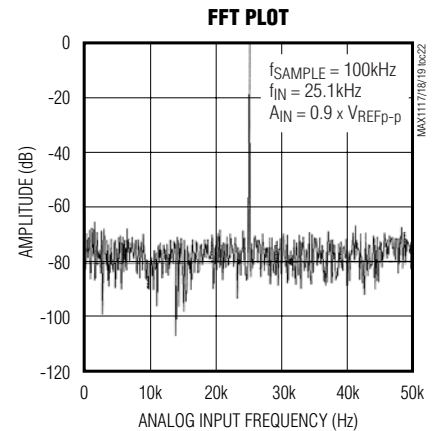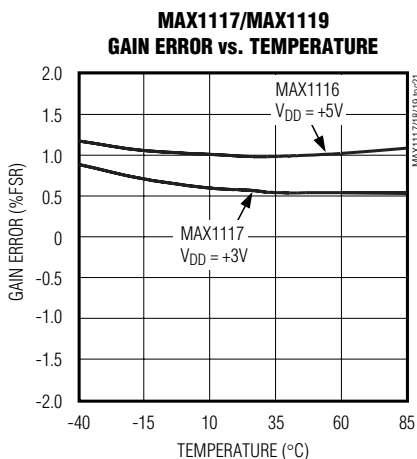
**MAX1117/MAX1119 SUPPLY CURRENT vs. CONVERSION RATE**

**MAX1117/MAX1119 SUPPLY CURRENT vs. SUPPLY VOLTAGE**

**MAX1117/MAX1119 SUPPLY CURRENT vs. TEMPERATURE**

**CONVERSION TIME vs. SUPPLY VOLTAGE**

**CONVERSION TIME vs. TEMPERATURE**

**FFT PLOT**

**MAX1118 GAIN ERROR vs. SUPPLY VOLTAGE**

**MAX1118 GAIN ERROR vs. TEMPERATURE**

**MAX1118 GAIN ERROR vs. REFERENCE VOLTAGE**

MAX1117/MAX1118/MAX1119

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MAX1117/MAX1118/MAX1119
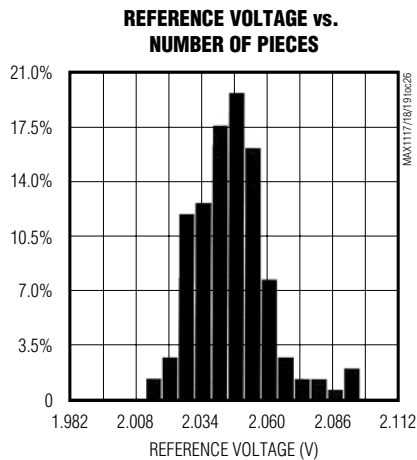
## Typical Operating Characteristics (continued)

($V_{DD}$ = +3V (MAX1117), $V_{DD}$ = +5V (MAX1119), $V_{DD}$ = $V_{REF}$ = +3V (MAX1118), $f_{SCLK}$ = 5MHz, $f_{SAMPLE}$ = 100ksps, $C_{LOAD}$ = 100pF, $T_A$ = +25°C, unless otherwise noted.)

**MAX1118**
**OFFSET ERROR vs. SUPPLY VOLTAGE**

**MAX1118**
**OFFSET ERROR vs. TEMPERATURE**

**MAX1118**
**OFFSET ERROR vs. REFERENCE VOLTAGE**

**MAX1117/MAX1119**
**GAIN ERROR vs. SUPPLY VOLTAGE**

**MAX1117/MAX1119**
**GAIN ERROR vs. TEMPERATURE**

**FFT PLOT**

**MAX1117/MAX1119**
**OFFSET ERROR vs. SUPPLY VOLTAGE**

**MAX1117/MAX1119**
**OFFSET ERROR vs. TEMPERATURE**

**MAXIM**

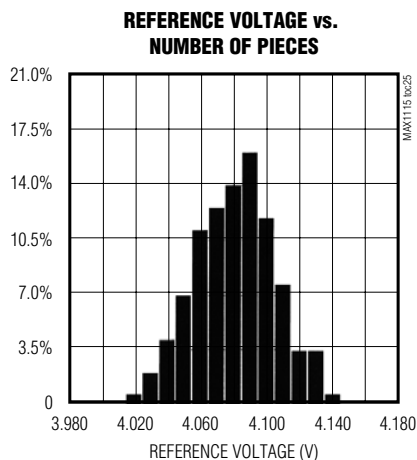### Typical Operating Characteristics (continued)

($V_{DD}$ = +3V (MAX1117), $V_{DD}$ = +5V (MAX1119), $V_{DD}$ = $V_{REF}$ = +3V (MAX1118), $f_{SCLK}$ = 5MHz, $f_{SAMPLE}$ = 100ksps, $C_{LOAD}$ = 100pF, $T_A$ = +25°C, unless otherwise noted.)

REFERENCE VOLTAGE vs.
NUMBER OF PIECES

REFERENCE VOLTAGE vs.
NUMBER OF PIECES
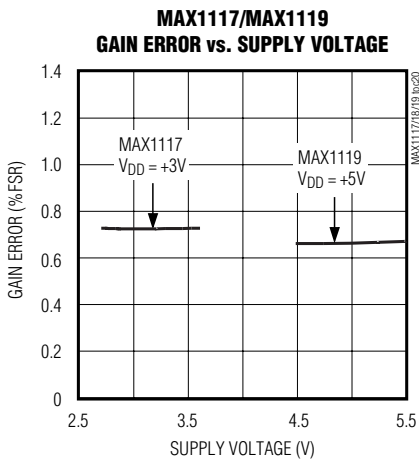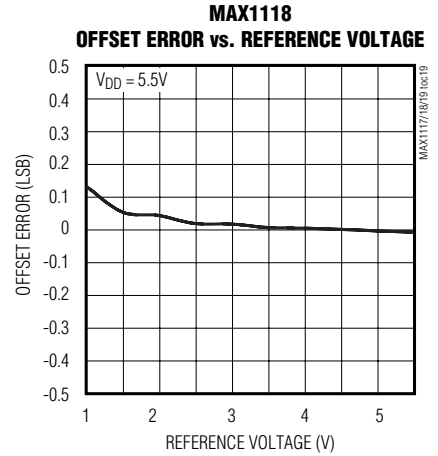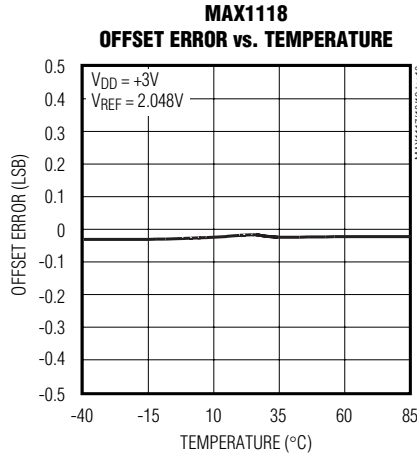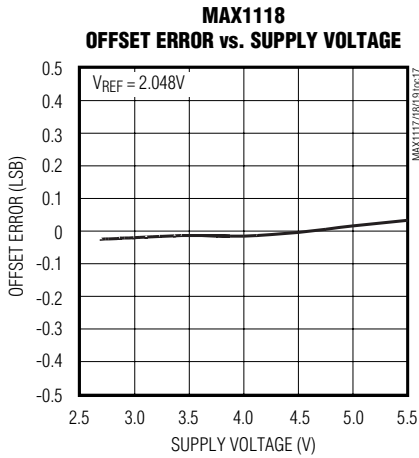
### Pin Description

| PIN | NAME | FUNCTION |
|-----|------|----------|
| 1 | VDD | Positive Supply Voltage |
| 2 | CH0 | CH0 Analog Voltage Input |
| 3 | CH1 | CH1 Analog Voltage Input |
| 4 | GND | Ground |
| 5 | I.C.(REF) | Internally Connected. Connect to ground. (Reference Input, MAX1118 only.) |
| 6 | CNVST | Convert/Start Input. CNVST initiates a power-up and starts a conversion on its falling edge. |
| 7 | DOUT | Serial Data Output. Data is clocked out on the falling edge of SCLK. DOUT goes low at the start of a conversion and presents the MSB at the completion of a conversion. DOUT goes high impedance once data has been fully clocked out. |
| 8 | SCLK | Serial Clock. Used for clocking out data on DOUT. |

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MAX1117/MAX1118/MAX1119
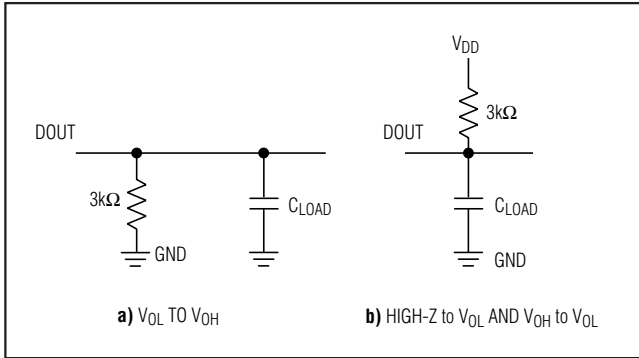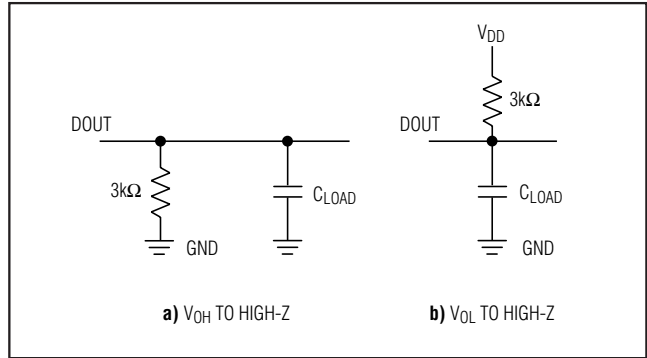


Figure 1. Load Circuits for Enable Time



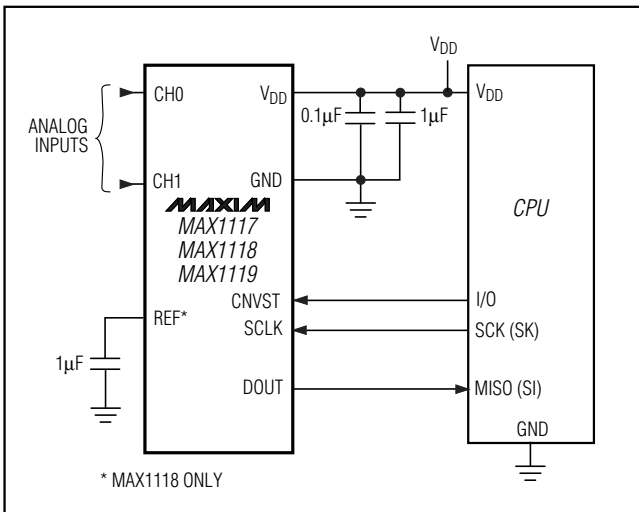Figure 2. Load Circuits for Disable Time
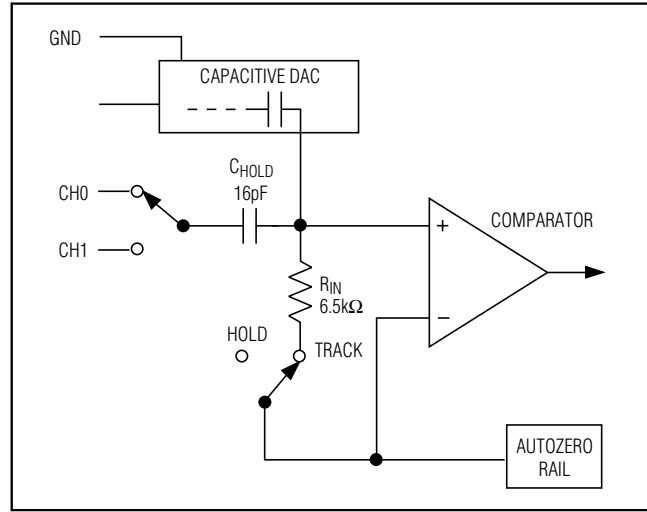


Figure 3. Typical Operating Circuit



Figure 4. Equivalent Input Circuit

## Detailed Description

The MAX1117/MAX1118/MAX1119 ADCs use a successive-approximation conversion technique and input T/H circuitry to convert an analog signal to an 8-bit digital output. The SPI/QSPI/MICROWIRE compatible interface directly connects to microprocessors (µPs) without additional circuity (Figure 3).

### Track/Hold

The input architecture of the ADC is illustrated in Figure 4's equivalent-input circuit and is composed of the T/H, the input multiplexer, the input comparator, the switched capacitor DAC, and the auto-zero rail.

The acquisition interval begins with the falling edge of CNVST. During the acquisition interval, the analog inputs (CH0, CH1) are connected to the holding capacitor ($C_{HOLD}$). Once the acquisition has completed, the T/H switch opens and $C_{HOLD}$ is connected to GND, retaining the charge on $C_{HOLD}$ as a sample of the signal at the analog input.

Sufficiently low source impedance is required to ensure an accurate sample. A source impedance <1.5kΩ is recommended for accurate sample settling. A 100pF capacitor at the ADC inputs will also improve the accuracy of an input sample.

### Conversion Process

The MAX1117/MAX1118/MAX1119 conversion process is internally timed. The total acquisition and conversion process takes <7.5µs. Once an input sample has been acquired, the comparator's negative input is then con-

nected to an autozero supply. Since the device requires only a single supply, the negative input of the comparator is set to equal $V_{DD}/2$. The capacitive DAC restores the positive input to $V_{DD}/2$ within the limits of 8-bit resolution. This action is equivalent to transferring a charge $Q_{IN} = 16pF \times V_{IN}$ from $C_{HOLD}$ to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog-input signal.

### Input Voltage Range

Internal protection diodes that clamp the analog input to $V_{DD}$ and GND allow the input pins (CH0, CH1) to swing from (GND - 0.3V) to ($V_{DD}$ + 0.3V) without damage. However, for accurate conversions, the inputs must not exceed ($V_{DD}$ + 50mV) or be less than (GND - 50mV).

### Input Bandwidth

The ADC's input tracking circuitry has a 4MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

### Serial Interface

The MAX1117/MAX1118/MAX1119 have a 3-wire serial interface. The CNVST and SCLK inputs are used to control the device, while the three-state DOUT pin is used to access the conversion results.

The serial interface provides connection to microcontrollers (µCs) with SPI, QSPI, and MICROWIRE serial interfaces at clock rates up to 5MHz. The interface supports either an idle high or low SCLK format. For SPI and QSPI, set CPOL = CPHA = 0 or CPOL = CPHA = 1 in the SPI control registers of the µC. Figure 5 shows the MAX1117/MAX1118/MAX1119 common serial-interface connections. See Figures 6a–6d for details on the serial interface timing and protocol.

### Digital Inputs and Outputs

The MAX1117/MAX1118/MAX1119 perform conversions using an internal clock. This frees the µP from the burden of running the SAR conversion clock and allows the conversion results to be read back at the µP's convenience at any clock rate up to 5MHz.

The acquisition interval begins with the falling edge of CNVST. CNVST can idle between conversions in either a high or low state. If idled in a low state, CNVST must

be brought high for at least 50ns, then brought low to initiate a conversion. To select CH1 for conversion, the CNVST pin must be brought high and low for a second time (Figures 6c and 6d).

After CNVST is brought low, allow 7.5µs for the conversion to be completed. While the internal conversion is in progress, DOUT is low. The MSB is present at the DOUT pin immediately after conversion is completed. The conversion result is clocked out at the DOUT pin and is coded in straight binary (Figure 7). Data is clocked out at SCLK's falling edge in MSB-first format at rates up to 5MHz. Once all data bits are clocked out, DOUT goes high impedance (100ns to 500ns after the rising edge) of the eighth SCLK pulse.
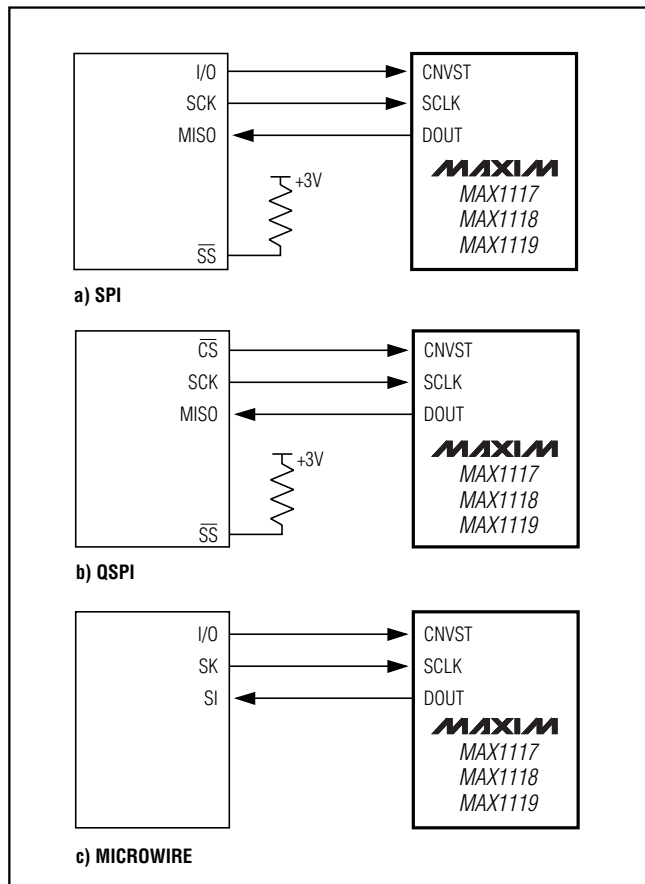


Figure 5. Common Serial-Interface Connections

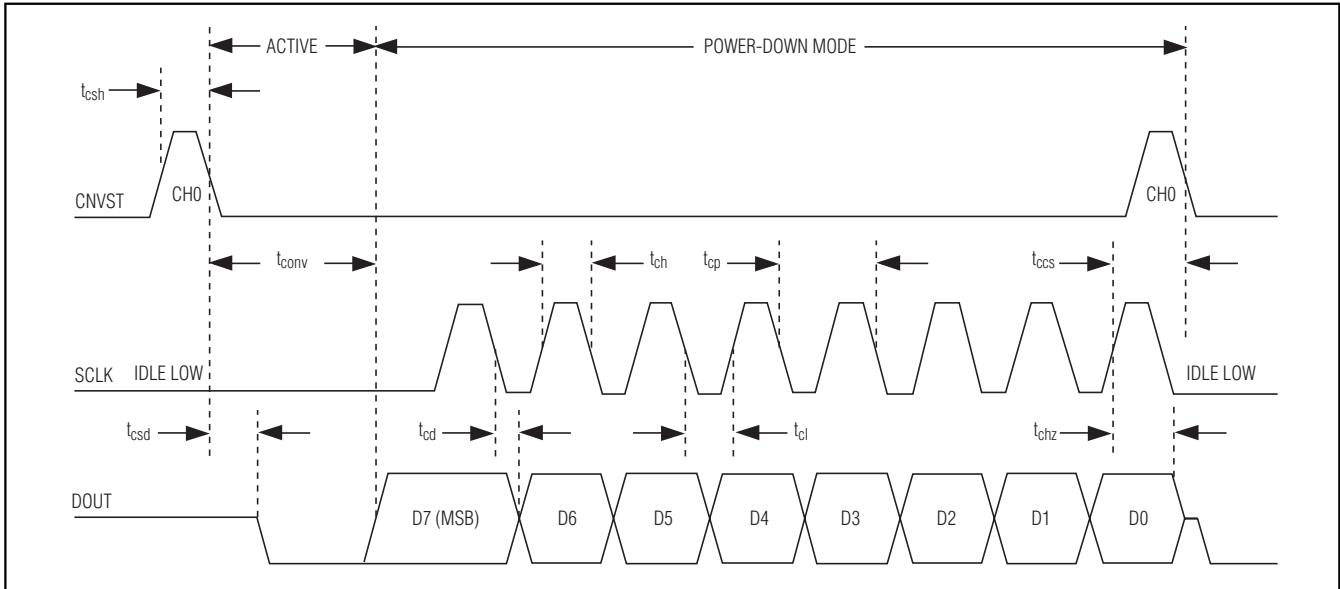# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs



*Figure 6a. Conversion and Interface Timing, Conversion on CH0 with SCLK Idle Low*
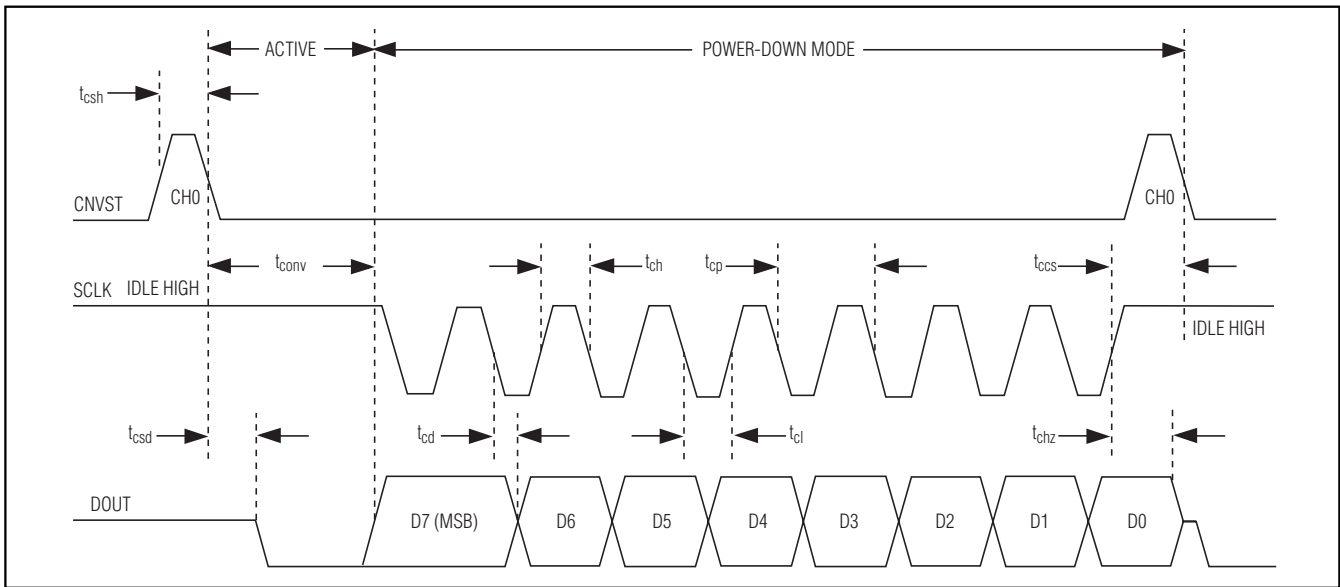


*Figure 6b. Conversion and Interface Timing, Conversion on CH0 with SCLK Idle High*

During the conversion process, SCLK is ignored. Only after a conversion is complete will SCLK cause serial data to be output. Falling edges on CNVST, during an active conversion process, interrupt the current conversion and cause the input multiplexer to switch to CH1. To reinitiate a conversion on CH0, it is necessary to allow for a conversion to be complete and all of the data to be read out. Once a conversion has been completed, the MAX1117/MAX1118/MAX1119 will go into AutoShutdown™ mode (<1µA typ) until the next conversion is initiated.

*AutoShutdown is a trademark of Maxim Integrated Products.*

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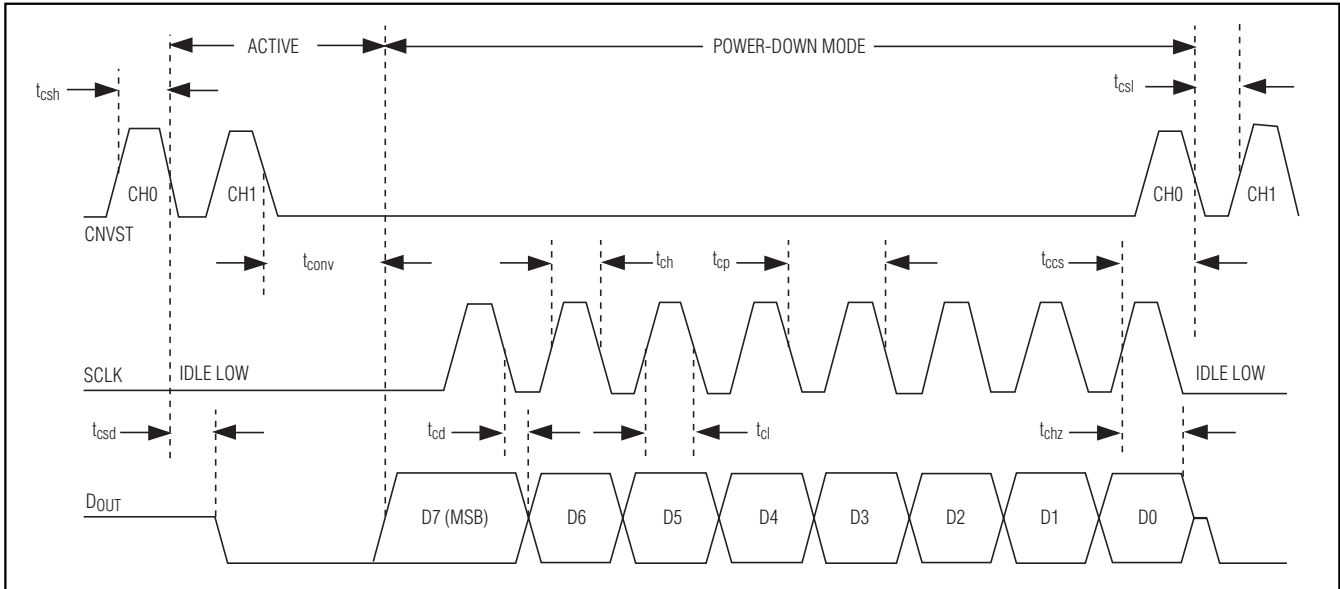
MAX1117/MAX1118/MAX1119



Figure 6c. Conversion and Interface Timing, Conversion on CH1 with SCLK Idle Low
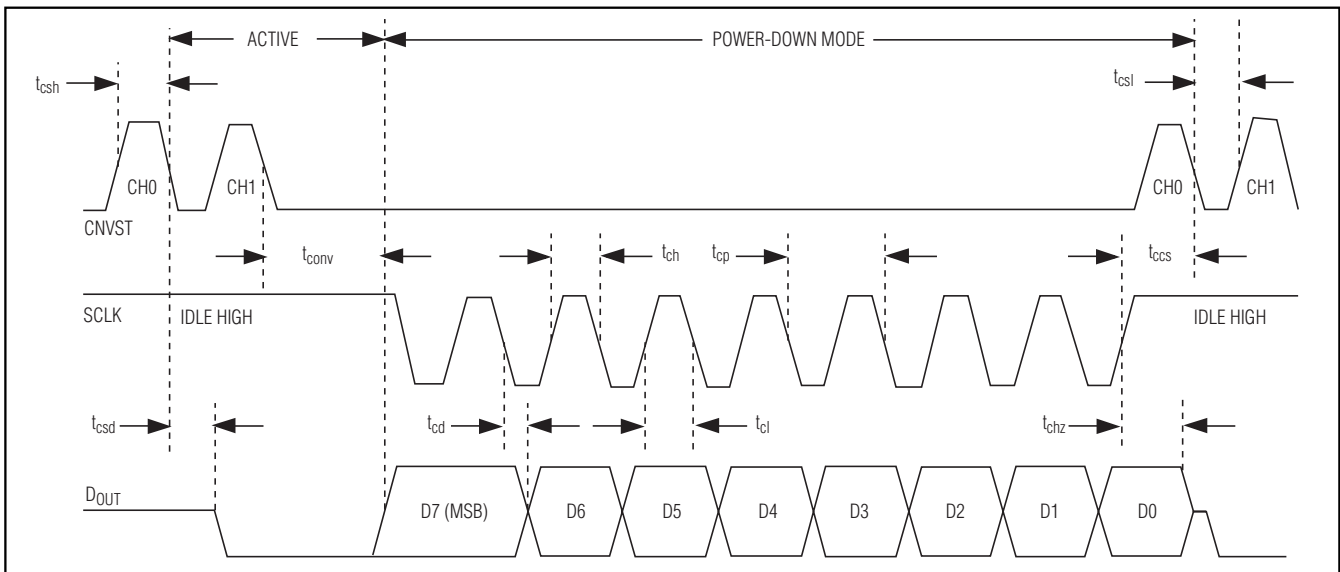


Figure 6d. Conversion and Interface Timing, Conversion on CH1 with SCLK Idle High

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# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs
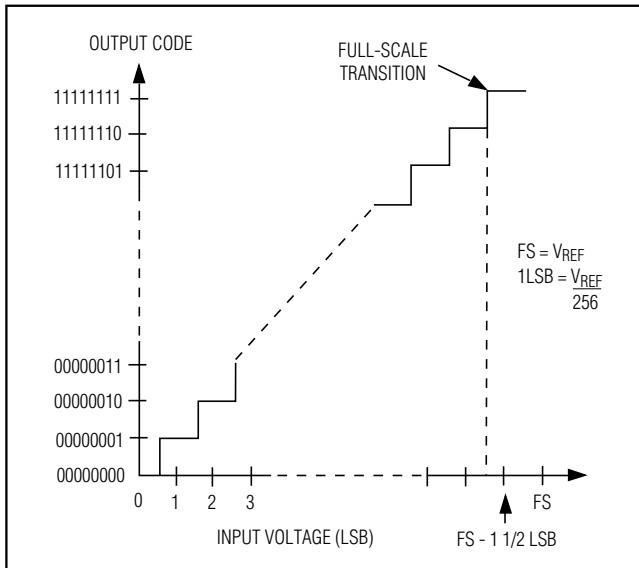


Figure 7. Input/Output Transfer Function



Figure 8. Power-Supply Connections

## _____ Applications Information

### Power-On Reset

When power is first applied, the MAX1117/MAX1118/ MAX1119 are in AutoShutdown state (<1μA typ). A conversion can be started by toggling CNVST high to low. Powering up the MAX1117/MAX1118/MAX1119 with CNVST low will not start a conversion. Conversions initiated prior to the external reference settling (MAX1118) will result in errors. Thus, it is necessary to allow the external reference to stabilize prior to initiating a conversion.

### AutoShutDown and Supply Current Requirements

The MAX1117/MAX1118/MAX1119 are designed to automatically shutdown once a conversion is complete without any external control. An input sample and conversion process will typically take 5μs to complete, during which time the supply current to the analog sections of the device is fully on. All analog circuitry is shutdown after a conversion completes, which results in a supply current of <1μA (see Shutdown Current vs. Supply Voltage Plot in the *Typical Operating Characteristics*). The digital conversion result is maintained in a static register and is available for access through the serial interface at any time.

The power consumption consequence of this architecture is dramatic when relatively slow conversion rates are needed. For example, at a conversion rate of 10ksps, the average supply current for the MAX1117 is
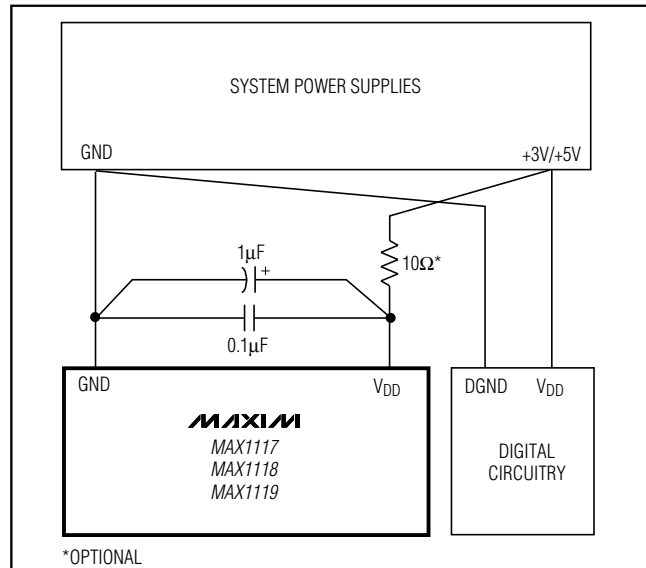
15μA, while at 1ksps it drops to 1.5μA and at 0.1ksps it is just 0.3μA, or a miniscule 1μW of power consumption (see Average Supply Current vs. Conversion Rate Plot in the *Typical Operating Characteristics*).

### External Voltage Reference (MAX1118)

Connect an external reference between +1V and $V_{DD}$ at the REF pin. The DC input impedance at REF is extremely high, consisting of leakage current only (10nA typ). During a conversion, the reference must be able to deliver up to 20μA average load current and have an output impedance of 100Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 10nF or larger capacitor.

### Transfer Function

Figure 7 depicts the input/output transfer function. Output coding is binary with a +2.048V reference 1LSB = 8mV ($V_{REF}$/256).

### Layout, Grounding, Bypassing

For best performance, the board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another or run digital lines underneath the ADC package.

Figure 8 shows the recommended system-ground connections. A single-point analog ground (star-ground point) should be established at the ADC ground. Connect all analog grounds to the star ground. The ground return to the power supply for the star ground

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**MAX1117/MAX1118/MAX1119**

## Functional Diagrams



MAXIM
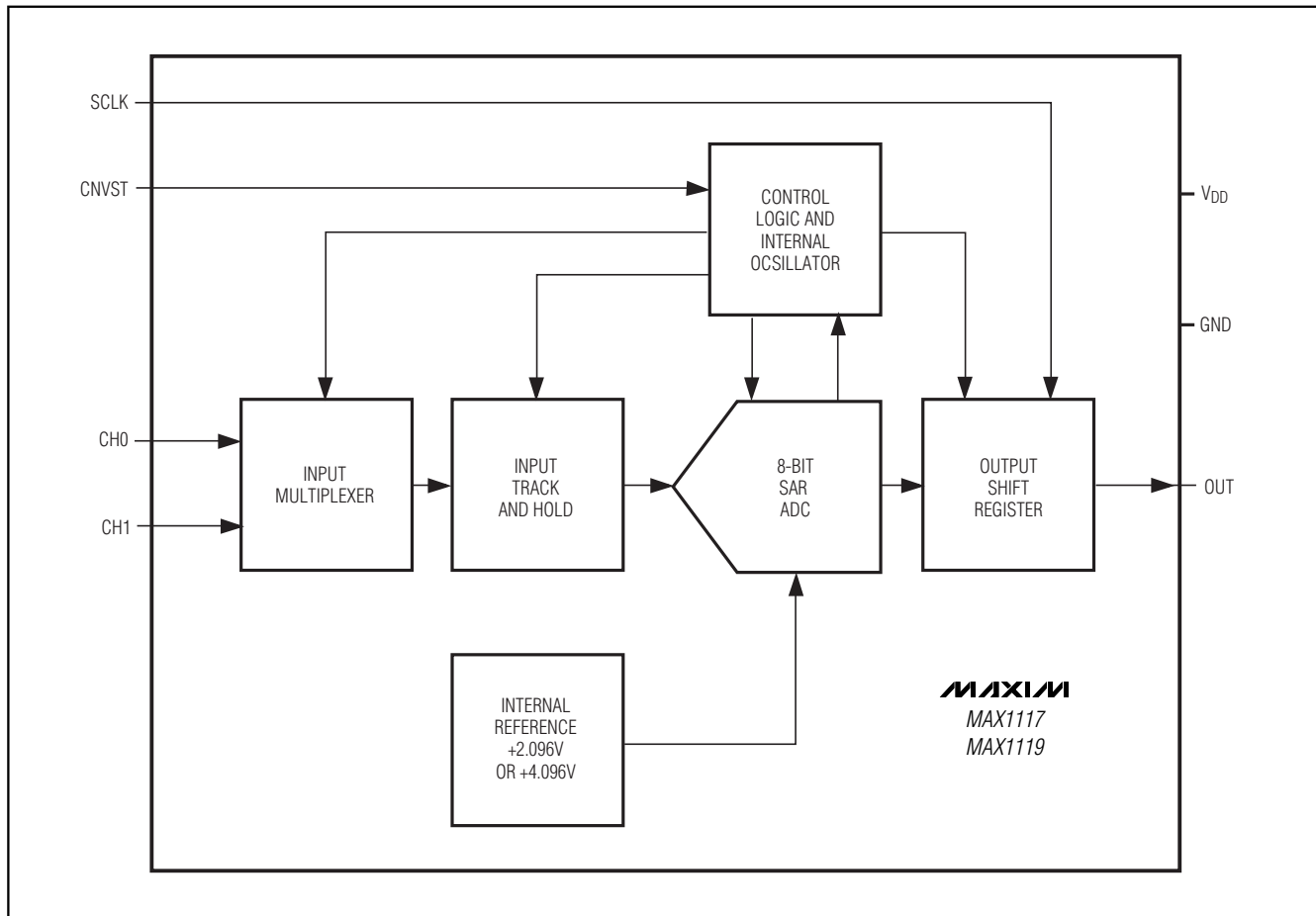
MAX1117
MAX1119

should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the $V_{DD}$ power supply may affect the comparator in the ADC. Bypass the supply to the star ground with a 0.1µF capacitor close to the $V_{DD}$ pin of the MAX1117/MAX1118/MAX1119. Minimize capacitor lead lengths for best supply-noise rejection. If the power supply is noisy, a 1µF capacitor in conjunction with a 10Ω series resistor can be connected to form a lowpass filter.
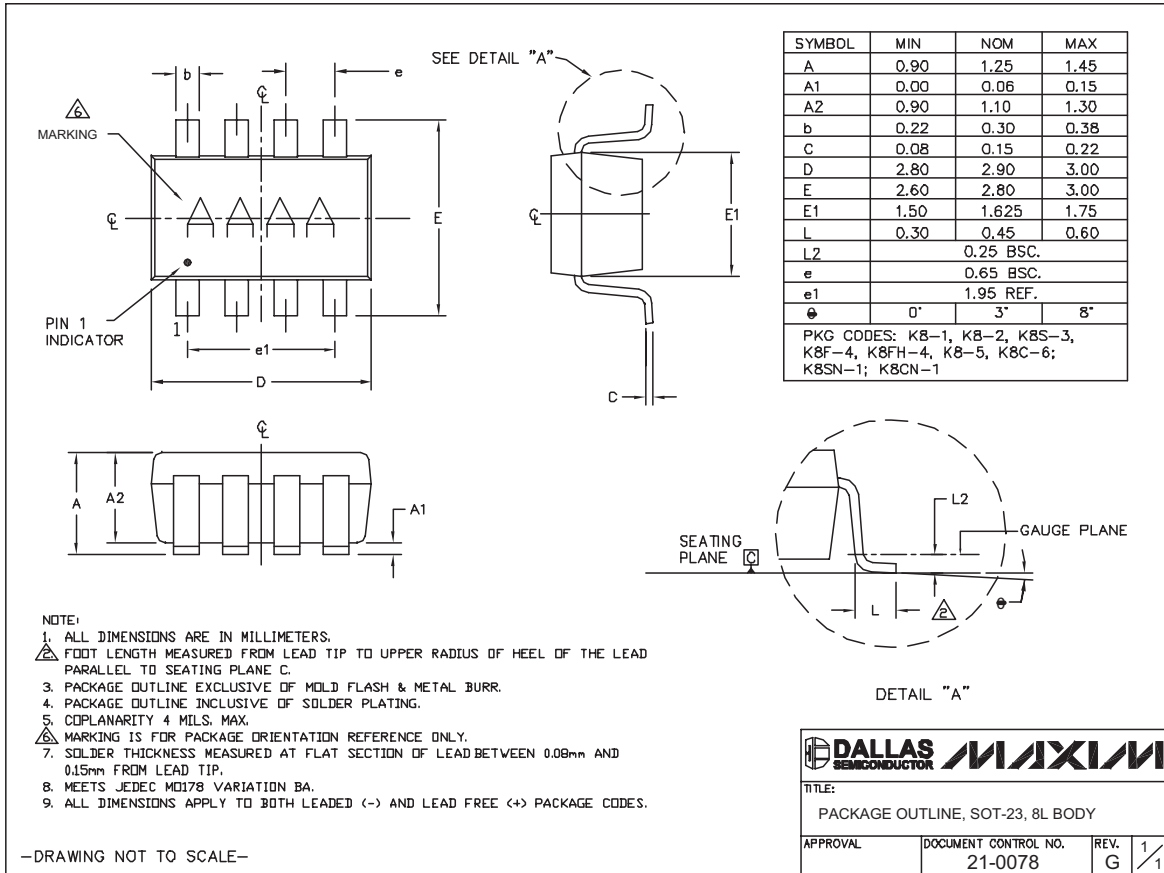
## Chip Information

TRANSISTOR COUNT: 2000
PROCESS: BiCMOS

# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



SOT23, 8L.EPS

| SYMBOL | MIN | NOM | MAX |
|--------|------|-------|------|
| A | 0.90 | 1.25 | 1.45 |
| A1 | 0.00 | 0.06 | 0.15 |
| A2 | 0.90 | 1.10 | 1.30 |
| b | 0.22 | 0.30 | 0.38 |
| C | 0.08 | 0.15 | 0.22 |
| D | 2.80 | 2.90 | 3.00 |
| E | 2.60 | 2.80 | 3.00 |
| E1 | 1.50 | 1.625 | 1.75 |
| L | 0.30 | 0.45 | 0.60 |
| L2 | | 0.25 BSC. | |
| e | | 0.65 BSC. | |
| e1 | | 1.95 REF. | |
| θ | 0° | 3° | 8° |

PKG CODES: K8-1, K8-2, K8S-3, K8F-4, K8FH-4, K8-5, K8C-6; K8SN-1; K8CN-1

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS, MAX.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178 VARIATION BA.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

—DRAWING NOT TO SCALE—

**DALLAS SEMICONDUCTOR** / **MAXIM**

TITLE:
PACKAGE OUTLINE, SOT-23, 8L BODY

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|----------|----------------------|------|---|
| | 21-0078 | G | 1/1 |

**14** _____**Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA  94086 408-737-7600**