MAX11410

24-Bit Multi-Channel Low-Power 1.9ksps Delta-Sigma ADC with PGA

General Description

The MAX11410 is a low-power, multi-channel, 24-bit delta-sigma ADC with features and specifications that are optimized for precision sensor measurement.

The input section includes a low-noise programmable gain amplifier (PGA) with very high input impedance and available gains from 1x to 128x to optimize the overall dynamic range. Input buffers provide isolation of the signal inputs from the switched-capacitor sampling network when the PGA is not in use, making the ADC easy to drive even with high-impedance sources.

Several integrated features simplify precision sensor applications. The programmable matched current sources provide excitation for resistive sensors. An additional current sink and current source aid in detecting broken sensor wires. The 10-channel input multiplexer provides the flexibility needed for complex, multi-sensor measurements. GPIOs reduce isolation components and ease control of switches or other circuitry.

When used in single-cycle mode, the digital filter settles within a single conversion cycle. The available FIR digital filter allows single-cycle settling in 16ms while providing more than 90dB simultaneous rejection of 50Hz and 60Hz line noise.

The integrated on-chip oscillator requires no external components. If needed, an external clock source may be used instead. Control registers and conversion data are accessed through the SPI-compatible serial interface.

Applications

- Sensor Measurement
- Portable Instruments
- Resistive Bridge Measurement

Benefits and Features

- High Resolution And Low Noise For Signal Sources With Wide Dynamic Range
  - 24-Bit Resolution
  - Programmable Gain Amplifier With 1, 2, 4, 8, 16, 32, 64, and 128 Gain Options
  - 90dB Simultaneous 60Hz and 50Hz Power Line Rejection
  - 3ppm Typical INL with No Missing Codes
- Optimized Features For More Efficient System Design
  - 10 Analog Inputs May be Used for Single-Ended/ Fully Differential in Any Combination
  - Two Dedicated/One Shared Differential Voltage Reference Inputs
  - On-Demand Offset and Gain Self-Calibration
- Low Power for Efficient Systems
  - 2.7V to 3.6V Analog Supply Range
  - 1.7V to 3.6V I/O Supply Range
  - <1µA Sleep Mode
- Standard SPI-Compatible Control Interface
- Selectable Internal/External Oscillator
- Operating Temperature Range from -40°C to +125°C
- Small 28-Pin 4mm x 4mm TQFN Package: Lead-Free and RoHS Compliant

***Ordering Information** appears at end of data sheet.*

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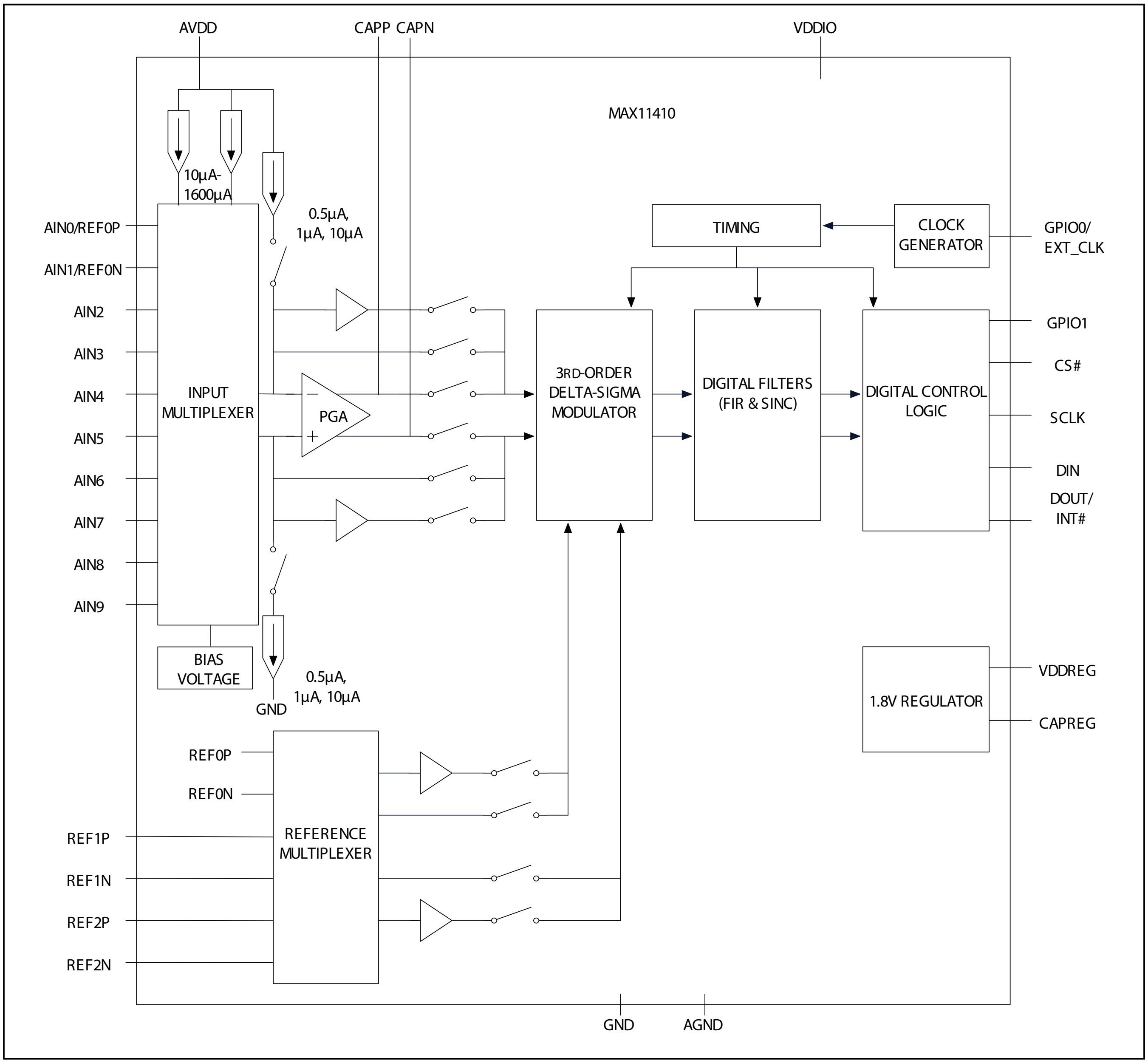
Simplified Block Diagram



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Absolute Maximum Ratings

AV_{DD} to GND (GND = AGND = DGND) ....-0.3V to +3.6V
V_{DDIO} to GND (GND = AGND = DGND) ....-0.3V to 3.6V
AV_{DD} to V_{DDIO} ....-0.3V to 1.8V
Analog Inputs (AIN__, REF__) to AGND
(GND = AGND = DGND) ....-0.3V to AV_{DD} + 0.3V
CAPP, CAPN, V_{DDREG}, CAPREG to GND
(GND = AGND = DGND)......................-0.3V to AV_{DD} + 0.3V
Digital Inputs and Outputs to GND
(GND = AGND = DGND).................... -0.3V to V_{DDIO} + 0.3V
GPIO Inputs to GND (GND = AGND = DGND)
....-0.3V to AV_{DD} + 0.3V
Maximum Current Into Any Pin 50mA
ESD Rating—ll Pins 2kV
Continuous Power Dissipation
(Single-Layer Board, T_A = +70°C, derate 20.8) 1667mW
Continuous Power Dissipation
(Multilayer Board, T_A = +70°C,
derate 28.6mW/°C above +70°C)............................ 2286mW
Operating Temperature Range........................ -40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range .... -40°C to +150°C
Lead Temperature (soldering, 10 sec) ....+300°C
Soldering Temperature (reflow)......................................+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Thermal Resistance, Single-Layer Board (TQFN)
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....48°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).................3°C/W

Thermal Resistance, Four-Layer Board (TQFN)
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....35°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).................3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(AV_{DD} = +3.3V, V_{DDIO} = +1.8V, V_{REFP} - V_{REFN} = AV_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted., T_A=+25°C for typical specifications, unless otherwise noted, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
Full-Scale Input Voltage				$\pm V_{REF}$/ Gain		
Absolute Input Voltage		Buffers disabled	A_{GND} - 30mV		AV_{DD} + 30mV	V
Input Voltage Range		Unipolar	0		V_{REF}	V
		Bipolar	$-V_{REF}$		V_{REF}	
Common Mode Voltage Range	V_{CM}	AIN buffers/PGA disabled	A_{GND}		AV_{DD}	V
		Buffers enabled	A_{GND} + 0.1		AV_{DD} - 0.1	
		PGA gain = 1 to 16	A_{GND} + 0.1 + (V_{IN}) (Gain)/2		AV_{DD} - 0.1 - (V_{IN}) (Gain)/2	
		PGA gain = 32 to 128	A_{GND} + 0.2 + (V_{IN}) (Gain)/2		AV_{DD} - 0.2 - (V_{IN}) (Gain)/2	

Electrical Characteristics (continued)

(AV_{DD} = +3.3V, V_{DDIO} = +1.8V, V_{REFP} - V_{REFN} = AV_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted., T_A=+25°C for typical specifications, unless otherwise noted, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Current		Buffer disabled		±1		µA/V
		Buffer enabled	-13		+13	nA
		PGA enabled, Note 2	-1		+1	
Absolute Input Current		Buffer disabled		±1		µA/V
		Buffer enabled	-65		+65	nA
		PGA enabled, -40°C to +85°C, Note 2	-1		+1	
		PGA enabled, -40°C to +125°C, Note 2	-5		+5	
Input Capacitance		Bypass mode		10		pF
Input Sampling Rate	f_S			246		kHz
SYSTEM PERFORMANCE						
Resolution				24		bits
Data Rate		50/60Hz FIR filter, single-cycle conversions		1, 2, 4, 8, 16		
		50Hz FIR filter, single-cycle conversions		1.3, 2.5, 5, 10, 20, 35.6		sps
		60Hz FIR filter, single-cycle conversions		1.3, 2.5. 5, 10, 20, 36.5		
		SINC4 filter, single-cycle conversions		1, 2.5, 5, 10, 15, 30, 60, 120, 240, 480		
		SINC4 filter, continuous conversions		4, 10, 20, 40, 60, 120, 240, 480, 960, 1920		
		SINC4 filter, duty cycle conversions		0.25, 0.63, 1.25, 2.5, 5, 10, 15, 30, 60, 120		

Electrical Characteristics (continued)

(AV_{DD} = +3.3V, V_{DDIO} = +1.8V, V_{REFP} - V_{REFN} = AV_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted., T_A=+25°C for typical specifications, unless otherwise noted, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Rate Tolerance		Determined by internal clock accuracy	-6		6	%
Integral Nonlinearity	INL	Differential input, reference buffer enabled, PGA = 1, tested @ 16sps, Note 4	-12	+3	+12	ppm FSR
		Differential input, PGA = 2 - 16, Note 4		6		ppmFS
		Differential input, PGA = 32 - 64, Note 4		11		ppmFS
		Differential input, PGA = 128, Note 4		15		
Offset Error		Referred to modulator input. After self and system calibration; V_{REFP} - V_{REFN} = 2.5V. Tested at 16sps. Note 5.	-25	±0.5	+25	µV
Offset Error Drift				50		nV/°C
PGA Gain Settings				1, 2, 4, 8, 16, 32, 64,128		
Digital Gain Settings				2, 4		
PGA Gain Error		No calibration, Note 3		±0.1		%
		Gain = 1, after system calibration, Note 3	-0.002		+0.002	%
PGA Gain Drift				20		ppm/°C
Input Noise	V_n	FIR50/60Hz, 16.8sps, PGA = 128. See Tables 1 and 4 for other conditions.		188		nV_{RMS}
Noise-Free Resolution	NFR	FIR50/60Hz, 16.8sps, PGA = 1. See Table 3 for other conditions.		17.2		Bits
Normal Mode Rejection (Internal Clock)	NMR	50Hz/60Hz FIR filter, 50Hz ±1%, 16sps conversion, Note 2	81.8			dB
		50Hz/60Hz FIR filter, 60Hz ±1%, 16sps single-cycle conversion, Note 2	94.4			dB
		50Hz FIR filter, 50Hz ±1%, 35.6sps single-cycle conversion, Note 2	39.2			dB
		60Hz FIR filter, 60Hz ±1%, 35.6sps single-cycle conversion, Note 2	42.3			dB
		SINC4 filter, 50Hz ±1%, 10sps single-cycle conversion, Note 2	55.1			dB
		SINC4 filter 60Hz ±1%, 10sps single-cycle conversion, Note 2	90.4			dB

Electrical Characteristics (continued)

(AV_{DD} = +3.3V, V_{DDIO} = +1.8V, V_{REFP} - V_{REFN} = AV_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted., T_A=+25°C for typical specifications, unless otherwise noted, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Normal Mode Rejection (External Clock)	NMR	50 Hz/60Hz FIR filter, 50Hz or 60Hz ±1%, 16sps single-cycle conversion		96		dB
		50Hz FIR filter, 50Hz ±1%, 35.6sps single-cycle conversion		45		
		60Hz FIR filter, 60Hz ±1%, 35.6sps single-cycle conversion		49		
		SINC4 filter, 50Hz ±1%, 10sps single-cycle conversion		80		
		SINC4 filter, 60Hz ±1%, 10 SPS single-cycle conversion		95		
Common-Mode Rejection	CMR	DC rejection, any PGA gain	90			dB
	CMR60	50/60Hz rejection, PGA enabled	100			
Power Supply Rejection	PSRRA		70	80		dB
REFERENCE INPUTS						
Reference Voltage Range		Reference buffer(s) disabled	A_{GND} - 30m		AV_{DD} + 30m	V
		Reference buffer(s) enabled	A_{GND} + 0.1		AV_{DD} - 0.1	
Reference Voltage Input		V_{REF} = V_{REFP} - V_{REFN}	0.75	2.5	AV_{DD}	V
Reference Input Current		Reference buffer disabled		2.1		µA/V
		Reference buffer enabled	-200	61	+200	nA
Reference Input Capacitance		Reference buffers disabled		15		pF
BURNOUT CURRENT SOURCES						
Current				0.5,1,10		µA
Initial Tolerance				±10		%
Drift				0.1		%/°C

Electrical Characteristics (continued)

(AV_{DD} = +3.3V, V_{DDIO} = +1.8V, V_{REFP} - V_{REFN} = AV_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted., T_A=+25°C for typical specifications, unless otherwise noted, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MATCHED CURRENT SOURCES						
Matched Current Source Outputs				10, 50, 75, 100, 125, 150, 175, 200, 225, 250, 300, 400, 600, 800, 1200, 1600		µA
Current Source Output Voltage Compliance		IDAC ≤ 250µA	0		AV_{DD} - 0.7	V
		IDAC = 1.6mA	0		AV_{DD} - 1.2	
Initial Tolerance		T_A = 25°C, Note 2	-5	±1	+5	%
Temperature Drift		Each IDAC		50		ppm/°C
Current Matching		Between IDACs		±0.1		%
Temperature Drift Matching		Between IDACs		10		ppm/C
Current Source Output Noise	I_N	Output current = 250µA. SINC4 filter, 60sps continuous. Noise is referred to input.		0.47		pA rms
V_{BIAS} OUTPUTS						
V_{BIAS} Voltage				AV_{DD}/2		V
V_{BIAS} Voltage Output Impedance				125K (active), 20K (passive), 125K (passive)		Ω

Electrical Characteristics (continued)

(AV_{DD} = +3.3V, V_{DDIO} = +1.8V, V_{REFP} - V_{REFN} = AV_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted., T_A=+25°C for typical specifications, unless otherwise noted, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDO						
LDO Output Capacitance			100			nF
LDO Output Voltage			1.62	1.8	1.98	V
System Timing						
Power-On Wake-Up Time		From AV_{DD} > V_{POR}		240		µs
Sleep Wake-Up Time				1.25		ms
PGA Power-Up Time		C_{FILTER} = 0		0.25		ms
		C_{FILTER} = 20nF		2		
		C_{FILTER} = 100nF		10		
PGA Settling Time		After changing gain settings to Gain = 1. C_{FILTER} = 0.		0.25		ms
		After changing gain settings to Gain = 1. C_{FILTER} = 100nF.		10		
		After changing gain settings to Gain = 128. C_{FILTER} = 0.		2		
Input Multiplexer Power-Up Time		Settled to 21 bits with 10pF load		2		µs
Input Multiplexer Channel-to-Channel Settling Time		Settled to 21 bits with 2K external source resistor		2		µs
V_{BIAS} Power-Up Time		Active generator; settled within 1% of final value; C_{LOAD} = 1µF		10		ms
		125K passive generator; settled within 1% of final value; C_{LOAD} = 1µF		575		
		20K passive generator; settled within 1% of final value; C_{LOAD} = 1µF		90		
V_{BIAS} Settling Time		Active generator; settled within 1% of final value; C_{LOAD} = 1µF		10		ms
		125K passive generator; settled within 1% of final value; C_{LOAD} = 1µF		605		
		20K passive generator; settled within 1% of final value; C_{LOAD} = 1µF		100		
Matched Current Source Startup Time				110		µs
Matched Current Source Settling Time				12.5		µs

Electrical Characteristics (continued)

(AV_{DD} = +3.3V, V_{DDIO} = +1.8V, V_{REFP} - V_{REFN} = AV_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted., T_A=+25°C for typical specifications, unless otherwise noted, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SPECIFICATIONS						
Analog Supply	AV_{DD}		2.7		3.6	V
Interface Supply	V_{DDIO}		1.7		3.6	V
AV_{DD} Currents		Sleep mode		0.5	3	µA
		Standby mode		115	150	
		Bypass mode, IDAC, V_{BIAS} sources off, AV_{DD} = V_{REF} = V_{IN} = 3.6V, SINC4 filter, continuous conversions at 60sps.		390	550	
		Buffered mode, IDAC, V_{BIAS} sources off, AV_{DD} = V_{REF} = V_{IN} = 3.6V, SINC4 filter, continuous conversions at 60sps.		425	600	
		PGA enabled, IDAC, V_{BIAS} sources off, AV_{DD} = V_{REF} = V_{IN} = 3.6V, SINC4 filter, continuous conversions at 60SPS. T_A = -40°C to 105°C			700	
		PGA enabled, IDAC, V_{BIAS} sources off, AV_{DD} = V_{REF} = V_{IN} = 3.6V, SINC4 filter, continuous conversions at 60sps. T_A = -40°C to 125°C.		520	750	
V_{DDIO} Operating Current		All modes of operation		0.3	2	µA
V_{DDREG} Current				48		µA
AVDD Duty Cycle Power Mode		Bypass mode, IDAC, V_{BIAS} sources off, AV_{DD} = V_{REF} = V_{IN} = 3.6V, SINC4 filter, continuous conversions at 15sps.		280	380	µA
		Buffered mode, IDAC, V_{BIAS} sources off, AV_{DD} = V_{REF} = V_{IN} = 3.6V, SINC4 filter, continuous conversions at 15sps.		300	400	
		PGA enabled, IDAC, V_{BIAS} sources off, AV_{DD} = V_{REF} = V_{IN} = 3.6V, SINC4 filter, continuous conversions at 15sps.		400	580	
SPI TIMING SPECIFICATIONS						
SCLK Frequency	f_{SCLK}		0		8	MHz
SCLK Period	t_{SCLK}		125			ns
SCLK Pulse-Width High	t_{CH}		50			ns
SCLK Pulse-Width Low	t_{CL}		50			ns

Electrical Characteristics (continued)

(AV_{DD} = +3.3V, V_{DDIO} = +1.8V, V_{REFP} - V_{REFN} = AV_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted., T_A=+25°C for typical specifications, unless otherwise noted, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CSB Fall to SCLK Fall Setup Time	t_{CSS0}	CSB falling edge to the 1st SCLK falling edge	40			ns
CSB Rise to SCLK Fall Hold Time	t_{CSH1}	Applies to the last active SCLK falling edge	3			ns
CSB Rise to SCLK Fall	t_{CSA}	Applies to last active SCLK falling edge, aborted sequence	12			ns
CSB Pulse-Width High	t_{CSPW}		40			ns
SCLK Fall to $\overline{CS}$ Fall	t_{CSF}	Applies to the last active SCLK falling edge	100			ns
DIN to SCLK Rise Setup Time	t_{DS}		40			ns
DIN to SCLK Rise Hold Time	t_{DH}		2			ns
DOUT Propagation Delay	t_{DOT}	Delay from the falling clock edge to the transition on DOUT			40	ns
DOUT Enable Time	t_{DOE}		0		40	ns
DOUT Disable Time	t_{DOZ}				25	ns
Bus Capacitance	C_B				20	pF
LOGIC INPUTS AND OUTPUTS (NON-GPIO)						
Input Current		Leakage current			±1	uA
Input Low Voltage	V_{IL}				0.3 x V_{DDIO}	V
Input High Voltage	V_{IH}		0.7 x V_{DDIO}			V
Input Hysteresis	V_{HYS}			200		mV
Input Capacitance				5		pF
Output Low Level	V_{OL}	I_{OL} = 1mA, V_{DDIO} = 1.8V and 3.6V			0.1 x V_{DDIO}	V
Output High Level	V_{OH}	I_{OL} = 1mA, V_{DDIO} = 1.8V and 3.6V	0.9 x V_{DDIO}			V
High-Z Leakage Current		Note 2	-100		+100	nA
High-Z Output Capacitance				9		pF

Electrical Characteristics (continued)

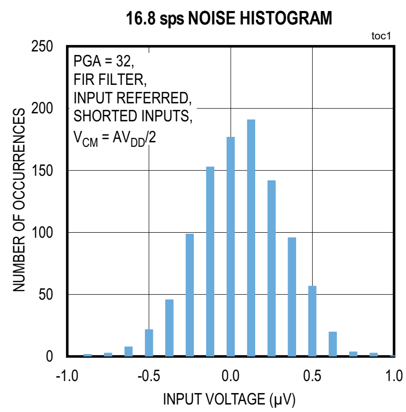
(AV_{DD} = +3.3V, V_{DDIO} = +1.8V, V_{REFP} - V_{REFN} = AV_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted., T_A=+25°C for typical specifications, unless otherwise noted, Note 1)

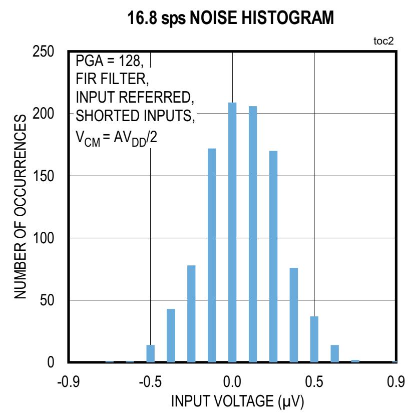
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL PURPOSE INPUT AND OUTPUT (GPIO)						
Input Current		Leakage current			±1	µA
Input Low Voltage	V_{IL}				0.3 x V_{DDIO}	V
Input High Voltage	V_{IH}		0.7 x V_{DDIO}			V
Input Hysteresis	V_{HYS}			200		mV
Output Low Level	V_{OL}	I_{OL} = 1mA, A_{VDD} = 2.7V and 3.6V			0.1 x AV_{DD}	V
Output High Level	V_{OH}	I_{OL} = 1mA, AV_{DD} = 2.7V and 3.6V	0.9 x AV_{DD}			V
Low-Side Power Switch Current		GPIO output voltage = 1V	25			mA
Low-Side Power Switch Impedance		GPIO output voltage = 1V			35	Ω
Internal Clock Output Frequency			2.3347	2.4576	2.5805	MHz
Internal Clock Output Duty Cycle			40		60	%
External Clock Input Frequency				2.4576		MHz
External Clock Input Duty Cycle			30		70	%

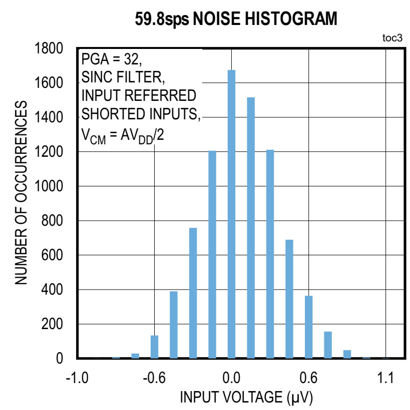
Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.
Note 2: These specifications are not fully tested and are guaranteed by design and/or characterization.
Note 3: Gain error does not include zero-scale errors. It is calculated as (full-scale error – offset error). After calibration, gain error is on the order of the noise.
Note 4: ppmFS is parts per million of full scale.
Note 5: After calibration, the offset voltage is on the order of the noise.

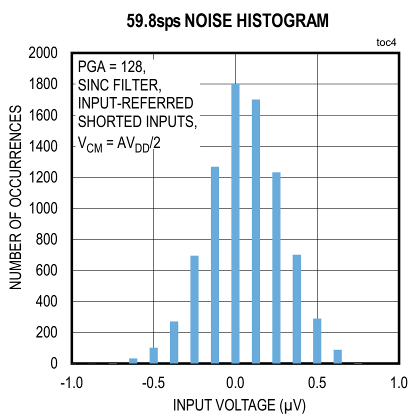
Typical Operating Characteristics

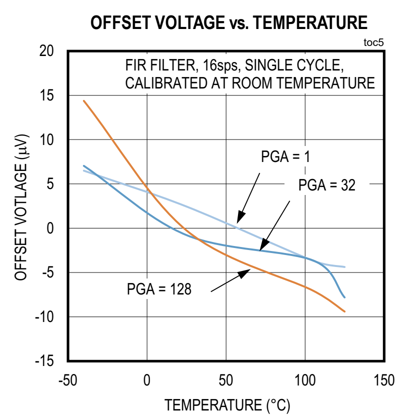
(V_{AVDD} = 3.3V, V_{REF} = 2.5V, Internal clock, T_A = 25°C unless otherwise noted.)

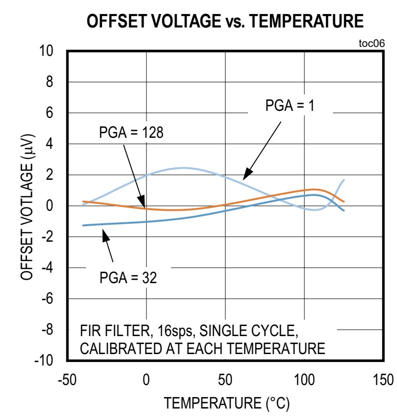


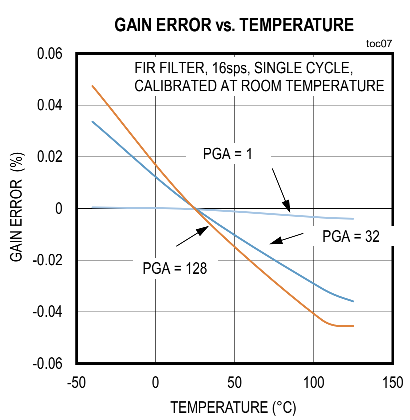


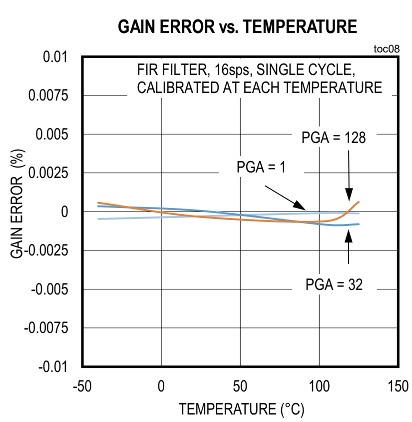


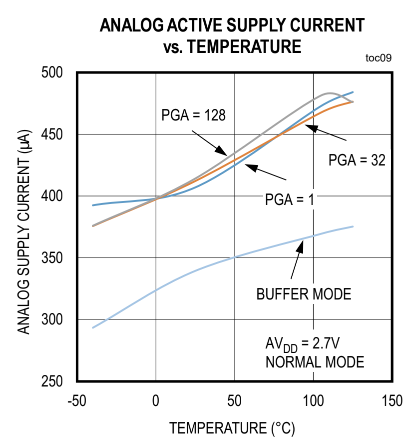






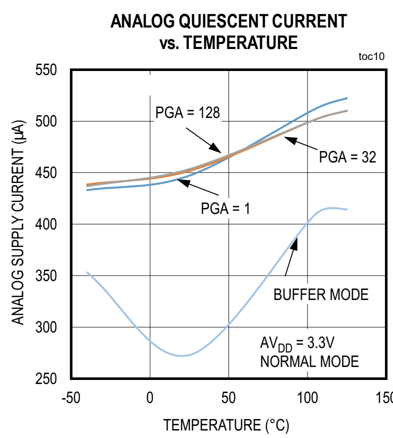


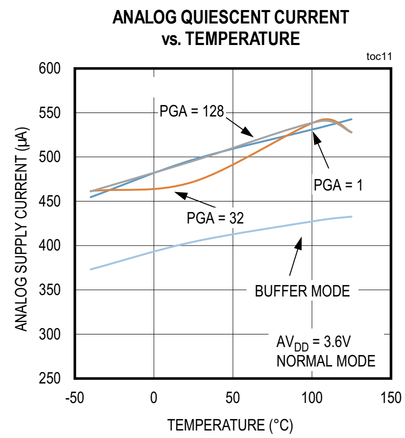


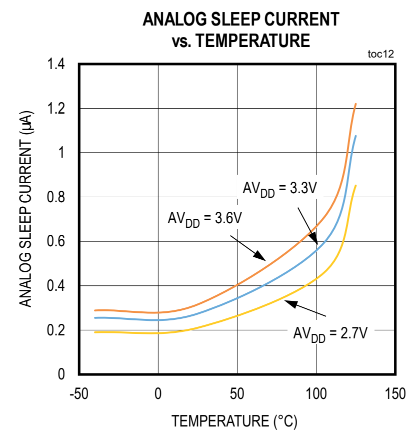


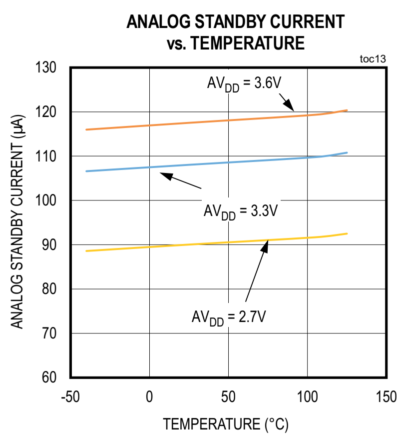
Typical Operating Characteristics (continued)

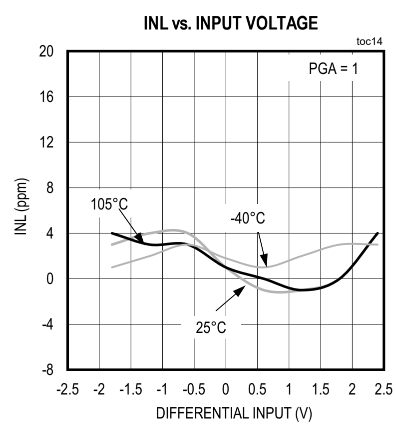
(V_{AVDD} = 3.3V, V_{REF} = 2.5V, Internal clock, T_A = 25°C unless otherwise noted.)

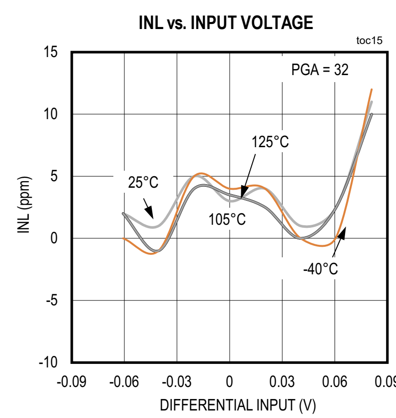


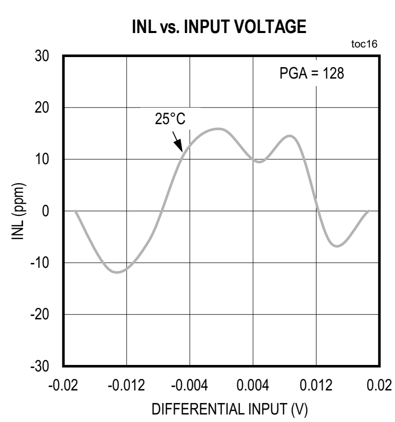


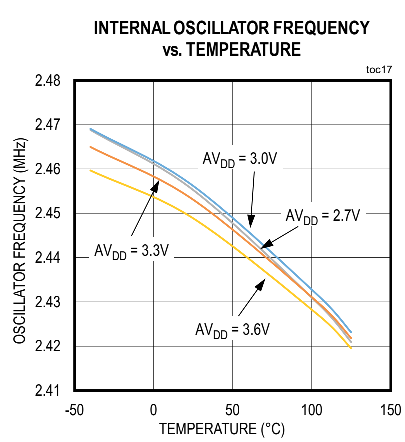


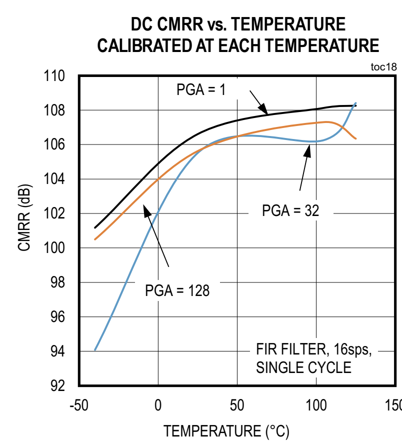








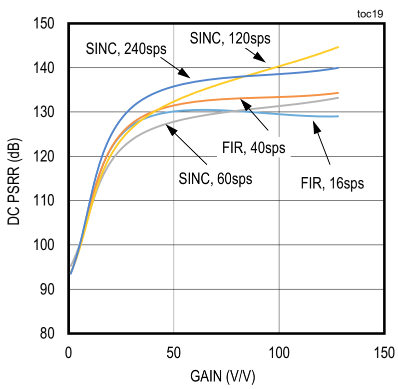




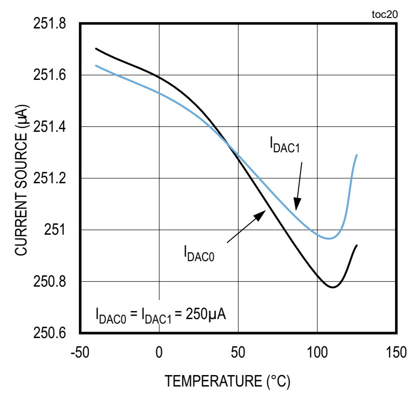
Typical Operating Characteristics (continued)

(V_{AVDD} = 3.3V, V_{REF} = 2.5V, Internal clock, T_A = 25°C unless otherwise noted.)

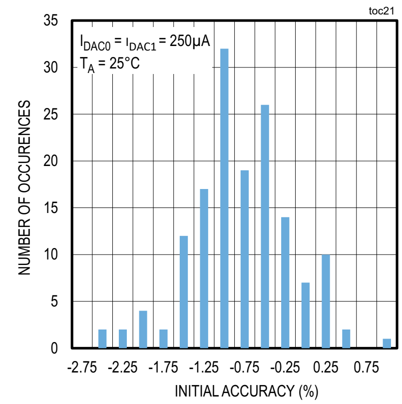
DC PSRR vs. GAIN



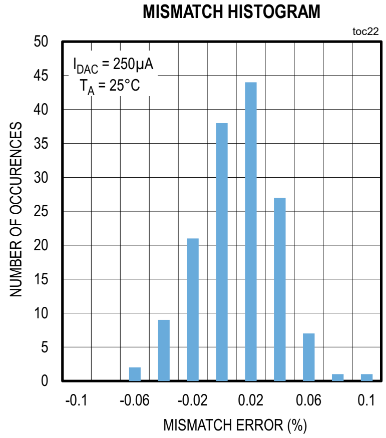
MATCHED CURRENT SOURCE DRIFT



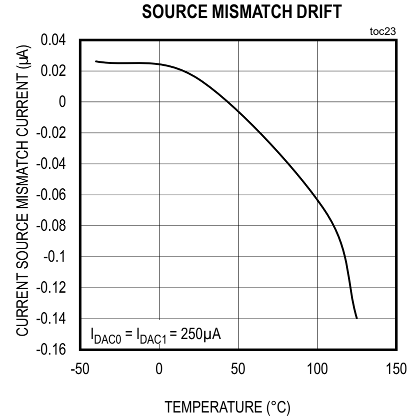
MATCHED CURRENT SOURCE ACCURACY HISTOGRAM



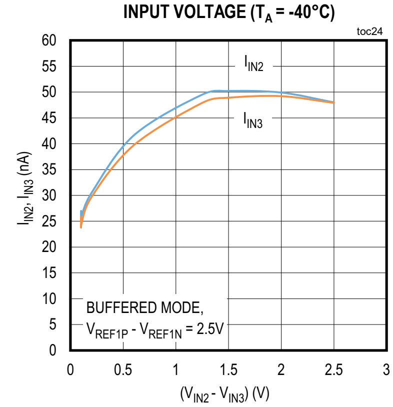
MATCHED CURRENT SOURCE MISMATCH HISTOGRAM



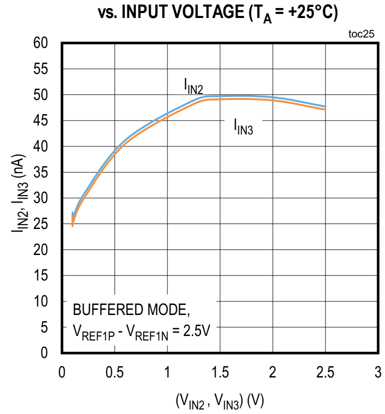
MATCHED CURRENT SOURCE MISMATCH DRIFT



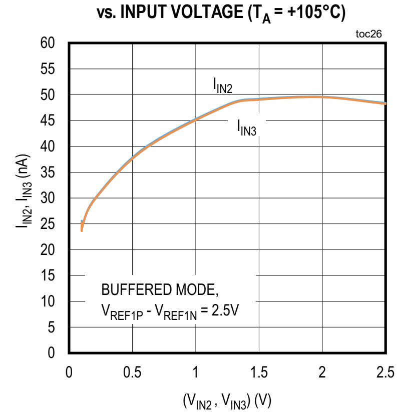
ABSOLUTE INPUT CURRENT vs. INPUT VOLTAGE (T_A = -40°C)



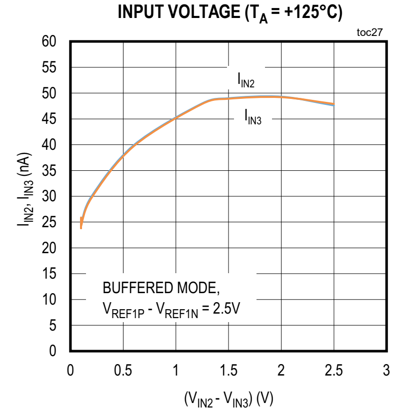
ABSOLUTE INPUT CURRENT vs. INPUT VOLTAGE (T_A = +25°C)



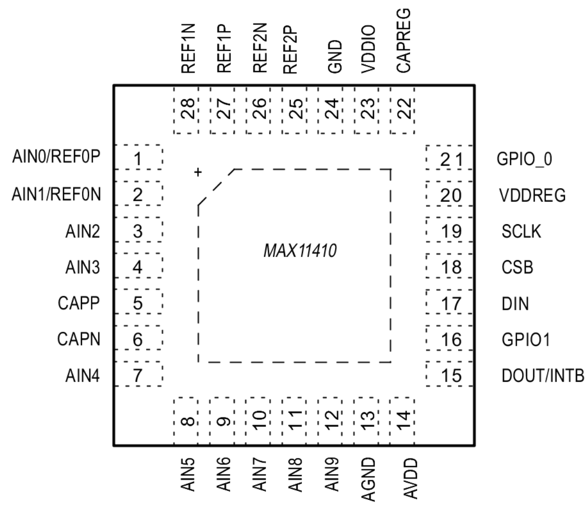
ABSOLUTE INPUT CURRENT vs. INPUT VOLTAGE (T_A = +105°C)



ABSOLUTE INPUT CURRENT vs. INPUT VOLTAGE (T_A = +125°C)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION	REFSUPPLY	TYPE
MAX11410				
1	AIN0/REF0P	Channel 0 Analog Input/Positive Differential Reference 0 Input. When used as an analog input, may serve as either the positive or negative differential input. May also serve as current source output. When used as a reference input, REF0P must be more positive than REF0N.	AV_{DD}	Analog Input
2	AIN1/REF0N	Channel 1 Input/Negative Differential Reference 0 Input. When used as an analog input, may serve as either the positive or negative differential input. May also serve as current source output. When used as a reference input, REF0P must be more positive than REF0N.	AV_{DD}	Analog Input
3	AIN2	Channel 2 Input. May serve as either the positive or negative differential input. May also serve as current source output.	AV_{DD}	Analog Input
4	AIN3	Channel 3 Input. May serve as either the positive or negative differential input. May also serve as current source output.	AV_{DD}	Analog Input
5	CAPP	PGA Output. Connect 1nF capacitor across CAPP and CAPN.	AV_{DD}	Output
6	CAPN	PGA output. Connect 1nF capacitor across CAPP and CAPN	AV_{DD}	Output
7	AIN4	Channel 4 Input. May serve as either the positive or negative differential input. May also serve as current source output.	AV_{DD}	Analog Input
8	AIN5	Channel 5 Input. May serve as either the positive or negative differential input. May also serve as current source output.	AV_{DD}	Analog Input
9	AIN6	Channel 6 Input. May serve as either the positive or negative differential input. May also serve as current source output.	AV_{DD}	Analog Input

Pin Description (continued)

PIN	NAME	FUNCTION	REFSUPPLY	TYPE
MAX11410				
10	AIN7	Channel 7 Input. May serve as either the positive or negative differential input. May also serve as current source output.	AV_{DD}	Analog Input
11	AIN8	Channel 8 Input. May serve as either the positive or negative differential input. May also serve as current source output.	AV_{DD}	Analog Input
12	AIN9	Channel 9 Input. May serve as either the positive or negative differential input. May also serve as current source output.	AV_{DD}	Analog Input
13	AGND	Analog Ground Voltage for AV_{DD} Supply. Connect AGND and GND together.	N/A	Ground
14	AVDD	Analog Supply Voltage, +2.7V to +3.6V with respect to AGND.	AV_{DD}	Power
15	DOUT/INTB	This pin serves a dual function. Serial Data Output: the device will drive this pin in response to a serial clock at SCLK, when data is read from the internal registers. In addition to the serial data output function, the DOUT/INTB pin also indicates an enabled interrupt condition has occurred when the pin is asserted low. To view the interrupt state on DOUT/INTB, enable CSB.	V_{DDIO}	Digital Output
16	GPIO1	Register-Controlled, General-Purpose Input/Output.	AV_{DD}	Digital I/O
17	DIN	Serial Data Input. Data present at DIN is shifted in to the part's internal registers in response to a serial clock at SCLK, either when the part is accessed for an internal register write or for a command operation.	V_{DDIO}	Digital Input
18	CSB	Chip Select Bar. Active-Low Logic Input. Use CSB to select the IC for access through the serial interface. CSB is used for frame synchronization for communications when SCLK is continuous. CSB transitioning from low to high is used to reset the SPI interface.	V_{DDIO}	Digital Input
19	SCLK	Serial Clock. Logic Input. Apply an external serial clock to this input to issue commands to or access data.	V_{DDIO}	Digital Input
20	VDDREG	Digital Regulator Supply, Connect to AVDD.	AV_{DD}	Power
21	GPIO0	Register Controlled General Purpose Input/Output and External Clock Signal Input. When external clock mode is selected (EXTCLK = 1), provide a 2.4576MHz clock signal at CLK. Other frequencies can be used, but the data rate and digital filter notch frequencies scale accordingly.	AV_{DD}	Digital I/O
22	CAPREG	Digital Regulator Output. Connect a 100nF capacitor from CAPREG to AGND.	AV_{DD}	Power
23	VDDIO	Digital Interface Supply (+1.8V to +3.6V).	V_{DDIO}	Power
24	GND	Ground Reference for V_{DDIO}. Connect to AGND.	N/A	Ground
25	REF2P	Positive Differential Reference 2 Input. REF2P must be more positive than REF2N.	AV_{DD}	Analog Input
26	REF2N	Negative Differential Reference 2 Input. REF2P must be more positive than REF2N.	AV_{DD}	Analog Input
27	REF1P	Positive Differential Reference 1 input. REF1P must be more positive than REF1N.	AV_{DD}	Analog Input
28	REF1N	Negative Differential Reference 1 input. REF1P must be more positive than REF1N.	AV_{DD}	Analog Input

Detailed Description

This low-power, multi-channel, 24-bit delta-sigma ADC has features and specifications that are optimized for precision measurement of sensors and other analog signal sources.

The input section includes a low-noise programmable gain amplifier (PGA) with very high input impedance and available gains from 1x to 128x to optimize the overall dynamic range. Low-power input buffers may be enabled to provide isolation of the signal source from the modulator's switched-capacitor sampling network when the PGA is not in use, reducing the supply current requirements compared to the PGA.

Several integrated features simplify precision sensor applications. The programmable matched current sources provide excitation for resistive sensors; sixteen different current levels are available, allowing sensor full-scale range to be tuned for optimum signal-to-noise ratio. An additional current sink and current source supply small current levels to aid in detecting broken sensor wires. The 5-channel differential/10-channel single-ended multiplexer provides the flexibility needed for complex multi-sensor measurements. GPIOs reduce isolation components and ease control of switches or other circuitry.

The ADC can operate in continuous conversion mode at data rates up to 1920sps, and in single-cycle conversion mode at rates up to 480sps. When used in single-cycle mode, the digital filter settles within a single conversion cycle. The available FIR digital filter allows single-cycle settling in 16ms while providing more than 90dB simultaneous rejection of 50Hz and 60Hz line noise.

The integrated on-chip oscillator requires no external components. If needed, an external clock source may be used instead. Control registers and conversion data are accessed through the SPI-compatible serial interface.

Analog Inputs

The ten analog inputs (AIN0–AIN9) are configurable for differential/single-ended operation. For each conversion, the input multiplexer can be configured such that any of the ten analog inputs or AVDD can be used as the positive input. Additionally, any of the ten analog inputs or AGND can be used as the negative input for the differential measurement. The multiplexer outputs may either drive the ADC inputs directly or drive low-power buffers. They then drive the ADC or the PGA inputs.

AIN0 and AIN1 are internally connected to the reference multiplexer. When used as reference inputs, they serve as REF0P and REF0N.

Each of the two current sources (IDAC0 and IDAC1) can be routed to any of the ten analog inputs. The bias voltage source (V_{BIAS}) can be routed to any of analog inputs AIN0–AIN7.

Signal Path Considerations

Three signal-path options are available to trade power-supply current against input impedance, gain, and input voltage range by enabling the PGA or the input buffers, or bypassing both and driving the modulator directly. The PGA control register selects among these options, which are summarized below.

Bypass (Direct Signal Path) Mode

In bypass mode, the multiplexer outputs are directly connected to the ADC modulator inputs. In this mode, the input buffer and the PGA are disabled for minimum power-supply current. This mode allows input voltages from V_{AGND} - 30mV to V_{AVDD} + 30mV, and adds no amplifier noise to the signal. Input bias current is typically 1µA/V, which is appropriate when driving with a low source resistance.

For smaller signal amplitudes, “digital gains” of 2 and 4 are available when using the direct signal path. See the *Digital Gain* section for more information.

Buffered Mode

In buffered mode, the multiplexer outputs drive the inputs to the low-power signal buffers, which then drive the ADC modulator inputs. Selecting buffered mode disables the PGA. Input voltages from V_{AGND} + 100mV to V_{AVDD} - 100mV are accepted in this mode, and no amplifier noise is added to the signal. The input bias current, typically 61nA, is significantly less than that in the direct mode, so higher source resistances may be accommodated without causing appreciable errors. Enabling the input buffers increases the power supply current by 35µA (typical) compared to the bypassed (direct signal path) mode.

As with the bypassed mode, digital gains of 2 and 4 are available when using the buffered mode. See the *Digital Gain* section for more information.

PGA Mode

The programmable gain amplifier (PGA) provides gains of 1, 2, 4, 8, 16, 32, 64, or 128. Selecting PGA mode enables the PGA, connects the PGA inputs to the multiplexer outputs, connects the PGA outputs to the ADC modulator inputs, and disables the low-power input buffers. The PGA accepts input voltages from V_{AGND} + 100mV to V_{AVDD} - 100mV for gains up to 16, and V_{AGND} + 200mV to V_{AVDD} - 200mV for gains from 32 to 128. When enabled, the PGA supply current is typically 130µA.

Input current in PGA mode is much lower than in the Buffered or Direct modes, so the PGA mode is a good choice for maintaining precision when source resistances are high. Note that the input current in PGA mode is dominated by multiplexer leakage current, and is highest when the input voltage, including that of unused inputs, is nearest AVDD or GND. For applications that are most sensitive to the effects of input current, connect any unused inputs to a voltage near $AV_{DD}/2$.

Note that the maximum usable gain will be limited by the reference voltage and input voltage. Ensure that the differential input voltage multiplied by the PGA gain is less than or equal to the reference voltage:

$$V_{IN} \times GAIN \leq V_{REF}$$

Where

V_{IN} = differential input voltage

GAIN = PGA gain

V_{REF} = reference voltage

Also ensure that the input common-mode voltage (V_{CM}) falls within the acceptable common-mode voltage range of the PGA:

$$200mV + (V_{IN} \times GAIN)/2 \leq V_{CM} \leq A_{VDD} – 200mV - (V_{IN} \times GAIN)/2 \text{ for gains of 32 to 128 or}$$

$$100mV + (V_{IN} \times GAIN)/2 \leq V_{CM} \leq A_{VDD} - 100mV - (V_{IN} \times GAIN)/2 \text{ for gains of 1 to 16}$$

Where

V_{CM} = (AIN_P- AIN_N)/2

Digital Gain

Programmable digital gain settings of 2 and 4 are available in the Direct and Buffered modes. Select the desired gain using the Gain bits of the PGA register. Digital gain selections greater than or equal to 4 will result in digital gain equal to 4. The input range is 0V to V_{REF}/GAIN for unipolar conversions or $\pm V_{REF}$/GAIN for bipolar conversions.

The modulator produces 32 bits of data, and for unity gain, the 8 LSBs are truncated before the data is stored in the 24-bit conversion data registers. Selecting a digital gain of 2 causes the MSB and the 7 LSBs to be discarded, thus producing 24 bits of data with an effective "gain" of 2. Note that, for any data rate, the noise floor remains constant, independent of the digital gain setting. Digital gain is useful for systems whose input noise is dominated by the source, or systems that can take advantage of averaging multiple readings to improve effective resolution. For cases when the output noise is below an LSB, using digital gain can decrease the input-referred noise at the expense of reduced dynamic range.

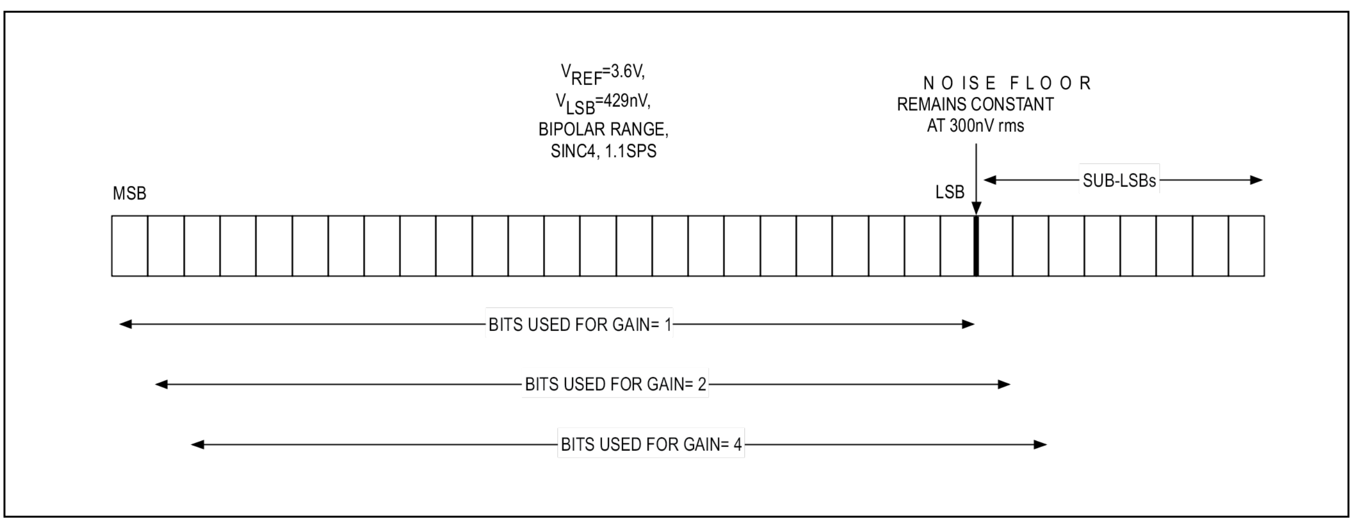


Figure 1. Digital Programmable Gain Example.

Noise Performance

The input-referred noise depends on the selected data rate, filter, input signal path (bypass, buffer, or PGA), and the PGA gain (when selected). This is illustrated in the tables below. Table 1 shows input-referred noise voltage (in μV_{RMS}). Table 2 shows effective resolution, which is defined as:

Effective Resolution = Log_2(FSR/rms noise), where

FSR is the full-scale input range (5V in bipolar mode with a 2.5V reference), and

rms noise is the input-referred rms noise.

The third table shows noise-free resolution (NFR), which is defined as

NFR = Log_2(FSR/p-p noise), where

FSR is the full-scale input range, (5V in bipolar mode with a 2.5V reference), and

p-p noise is 6.6 times the input-referred rms noise.

Values shown are for continuous conversions. Single-cycle data rates are similar for the FIR filters, and are one-fourth the continuous data rate for the SINC4 filter. Note that higher PGA gain reduces the input-referred noise, but because the input voltage range is reduced, the effective resolution decreases.

Table 1. Input-Referred Noise(μV_{RMS}) with V_{REF} = 2.5V, AV_{DD} = 3.3V, and inputs shorted.

FILTER	RATE (SPS)	BY-PASS	BUF-FER	PGA 1X	PGA 2X	PGA 4X	PGA 8X	PGA 16X	PGA 32X	PGA 64X	PGA 128X
FIR50/60	1	0.648	0.681	0.372	0.248	0.095	0.058	0.069	0.067	0.057	0.051
FIR50/60	2.1	3.241	3.128	3.489	1.747	0.807	0.430	0.187	0.109	0.078	0.057
FIR50/60	4.2	4.398	4.256	4.758	2.350	1.223	0.599	0.303	0.175	0.108	0.113
FIR50/60	8.4	4.511	4.428	5.259	2.529	1.326	0.684	0.373	0.218	0.152	0.139
FIR50/60	16.8	4.743	4.621	5.179	2.575	1.367	0.633	0.399	0.247	0.211	0.188
FIR50	1.3	1.716	1.741	1.589	0.833	0.388	0.169	0.082	0.065	0.068	0.055
FIR50	2.7	3.656	3.640	4.009	2.053	0.983	0.505	0.245	0.119	0.087	0.091
FIR50	5.3	4.374	4.315	4.912	2.480	1.252	0.631	0.312	0.185	0.127	0.121
FIR50	10.6	4.469	4.412	5.306	2.606	1.312	0.647	0.347	0.203	0.151	0.141
FIR50	21.3	4.604	4.511	5.363	2.655	1.351	0.680	0.386	0.230	0.232	0.199
FIR50	39.9	4.710	4.571	5.317	2.633	1.349	0.709	0.449	0.323	0.265	0.291
FIR60	1.3	1.721	1.765	1.470	0.794	0.370	0.160	0.072	0.072	0.056	0.068
FIR60	2.7	3.677	3.719	3.987	1.988	1.030	0.504	0.230	0.147	0.093	0.061
FIR60	5.3	4.303	4.417	4.951	2.473	1.220	0.636	0.309	0.168	0.141	0.121
FIR60	10.6	4.663	4.522	5.174	2.636	1.344	0.632	0.330	0.235	0.190	0.182
FIR60	21.3	4.781	4.672	5.449	2.780	1.336	0.760	0.369	0.268	0.219	0.225
FIR60	39.9	4.499	4.726	5.116	2.711	1.293	0.719	0.456	0.373	0.222	0.290
Sinc4	1.1	0.399	0.436	0.156	0.106	0.074	0.062	0.074	0.057	0.040	0.039
Sinc4	2.5	3.565	3.573	3.899	1.954	0.982	0.479	0.222	0.111	0.070	0.062
Sinc4	5	4.432	4.339	4.854	2.435	1.239	0.611	0.305	0.171	0.104	0.079
Sinc4	10	4.542	4.591	5.192	2.602	1.274	0.664	0.339	0.190	0.135	0.134
Sinc4	59.8	4.920	4.508	5.066	2.658	1.284	0.655	0.297	0.281	0.214	0.234
Sinc4	119.7	2.736	2.459	3.045	1.553	0.959	0.620	0.367	0.355	0.293	0.276
Sinc4	239.4	2.762	3.000	3.366	1.683	0.948	0.596	0.540	0.473	0.383	0.365
Sinc4	478.7	3.414	2.766	2.758	1.623	1.023	0.685	0.458	0.562	0.478	0.536
Sinc4	957.4	4.434	3.840	4.503	2.462	1.603	1.104	0.774	1.082	0.692	0.725
Sinc4	1914.8	24.496	24.785	25.092	14.761	5.831	3.855	2.152	1.332	1.115	1.038

Table 2. Effective Resolution with V_{REF} = 2.5V, AV_{DD} = 3.3V, and Inputs Shorted.

FILTER	RATE (SPS)	BY-PASS	BUF-FER	PGA 1X	PGA 2X	PGA 4X	PGA 8X	PGA 16X	PGA 32X	PGA 64X	PGA 128X
FIR50/60	1	22.880	22.808	23.682	23.267	23.652	23.354	22.112	21.150	20.392	19.554
FIR50/60	2.1	20.557	20.608	20.451	20.449	20.563	20.470	20.672	20.455	19.934	19.395
FIR50/60	4.2	20.117	20.164	20.003	20.021	19.963	19.992	19.975	19.767	19.462	18.401
FIR50/60	8.4	20.080	20.107	19.859	19.915	19.847	19.800	19.677	19.448	18.971	18.097
FIR50/60	16.8	20.008	20.045	19.881	19.889	19.802	19.912	19.578	19.274	18.500	17.668
FIR50	1.3	21.475	21.454	21.585	21.518	21.620	21.820	21.863	21.205	20.131	19.432
FIR50	2.7	20.383	20.390	20.250	20.216	20.279	20.239	20.283	20.328	19.776	18.713
FIR50	5.3	20.125	20.144	19.957	19.943	19.929	19.917	19.934	19.690	19.230	18.302
FIR50	10.6	20.094	20.112	19.846	19.872	19.861	19.881	19.781	19.557	18.979	18.084
FIR50	21.3	20.051	20.080	19.831	19.845	19.819	19.809	19.627	19.371	18.358	17.585
FIR50	39.9	20.018	20.061	19.843	19.857	19.822	19.750	19.410	18.883	18.169	17.036
FIR60	1.3	21.470	21.433	21.698	21.587	21.688	21.902	22.059	21.053	20.422	19.137
FIR60	2.7	20.375	20.359	20.258	20.262	20.211	20.241	20.374	20.020	19.681	19.300
FIR60	5.3	20.148	20.110	19.946	19.947	19.967	19.906	19.946	19.824	19.078	18.300
FIR60	10.6	20.032	20.077	19.882	19.855	19.827	19.916	19.851	19.344	18.652	17.710
FIR60	21.3	19.996	20.030	19.808	19.778	19.835	19.649	19.693	19.153	18.447	17.405
FIR60	39.9	20.084	20.013	19.899	19.815	19.883	19.729	19.388	18.677	18.426	17.040
Sinc4	1.1	23.580	23.453	24.933	24.498	24.002	23.266	22.015	21.385	20.892	19.923
Sinc4	2.5	20.420	20.416	20.290	20.287	20.280	20.315	20.427	20.425	20.088	19.258
Sinc4	5	20.106	20.136	19.974	19.970	19.944	19.965	19.967	19.799	19.518	18.921
Sinc4	10	20.070	20.055	19.877	19.874	19.904	19.843	19.814	19.646	19.145	18.156
Sinc4	59.8	19.955	20.081	19.913	19.843	19.893	19.863	20.006	19.084	18.476	17.352
Sinc4	119.7	20.801	20.955	20.647	20.619	20.314	19.944	19.701	18.747	18.026	17.111
Sinc4	239.4	20.788	20.668	20.503	20.503	20.331	19.999	19.143	18.335	17.639	16.706
Sinc4	478.7	20.482	20.786	20.790	20.555	20.220	19.800	19.380	18.084	17.320	16.154
Sinc4	957.4	20.105	20.312	20.083	19.954	19.573	19.111	18.623	17.140	16.784	15.718
Sinc4	1914.8	17.639	17.622	17.604	17.370	17.710	17.307	17.148	16.840	16.096	15.200

Table 3. Noise-Free Resolution with V_{REF} = 2.5V, AV_{DD} = 3.3V, and Inputs Shorted.

FILTER	RATE (SPS)	BY-PASS	BUF-FER	PGA 1X	PGA 2X	PGA 4X	PGA 8X	PGA 16X	PGA 32X	PGA 64X	PGA 128X
FIR50/60	1	20.158	20.085	20.959	20.545	20.929	20.631	19.389	18.427	17.670	16.831
FIR50/60	2.1	17.835	17.886	17.728	17.726	17.841	17.748	17.950	17.732	17.211	16.672
FIR50/60	4.2	17.394	17.442	17.281	17.299	17.241	17.270	17.252	17.045	16.740	15.679
FIR50/60	8.4	17.358	17.384	17.136	17.192	17.124	17.078	16.955	16.726	16.248	15.375
FIR50/60	16.8	17.285	17.323	17.158	17.166	17.080	17.190	16.856	16.551	15.777	14.946
FIR50	1.3	18.752	18.731	18.863	18.795	18.898	19.098	19.140	18.483	17.409	16.709
FIR50	2.7	17.661	17.667	17.528	17.493	17.556	17.517	17.561	17.605	17.053	15.991
FIR50	5.3	17.402	17.422	17.235	17.221	17.207	17.195	17.211	16.967	16.508	15.579
FIR50	10.6	17.371	17.390	17.123	17.149	17.139	17.158	17.059	16.835	16.257	15.362
FIR50	21.3	17.328	17.358	17.108	17.122	17.096	17.087	16.904	16.649	15.636	14.863
FIR50	39.9	17.295	17.338	17.120	17.134	17.099	17.028	16.687	16.160	15.446	14.313
FIR60	1.3	18.747	18.711	18.976	18.864	18.966	19.179	19.337	18.331	17.699	16.414
FIR60	2.7	17.652	17.636	17.536	17.540	17.489	17.519	17.652	17.297	16.959	16.578
FIR60	5.3	17.426	17.388	17.223	17.225	17.244	17.184	17.224	17.101	16.355	15.577
FIR60	10.6	17.310	17.354	17.160	17.133	17.104	17.194	17.129	16.621	15.929	14.987
FIR60	21.3	17.274	17.307	17.085	17.056	17.113	16.926	16.970	16.431	15.724	14.683
FIR60	39.9	17.361	17.290	17.176	17.092	17.160	17.006	16.665	15.955	15.703	14.318
Sinc4	1.1	20.857	20.730	22.211	21.775	21.279	20.543	19.293	18.662	18.169	17.201
Sinc4	2.5	17.697	17.694	17.568	17.565	17.557	17.593	17.704	17.703	17.366	16.536
Sinc4	5	17.383	17.414	17.252	17.247	17.222	17.242	17.244	17.076	16.796	16.199
Sinc4	10	17.348	17.332	17.155	17.152	17.182	17.121	17.092	16.924	16.423	15.433
Sinc4	59.8	17.232	17.358	17.190	17.121	17.170	17.141	17.284	16.362	15.753	14.629
Sinc4	119.7	18.079	18.233	17.924	17.896	17.592	17.221	16.979	16.025	15.303	14.388
Sinc4	239.4	18.065	17.946	17.780	17.780	17.608	17.277	16.421	15.612	14.916	13.983
Sinc4	478.7	17.760	18.063	18.067	17.833	17.498	17.077	16.657	15.362	14.597	13.431
Sinc4	957.4	17.383	17.590	17.360	17.231	16.851	16.389	15.900	14.417	14.061	12.995
Sinc4	1914.8	14.917	14.900	14.882	14.647	14.987	14.584	14.426	14.118	13.374	12.478

Reference Inputs

There are three selectable differential reference voltage inputs. Select the reference input using bits REF_SEL<2:0> in the CTRL register. Either VREFP, VREFN, or both may be buffered, as determined by the REFBUFP_EN and REFBUFN_EN bits. With the reference buffer disabled, the input current is a few microamps (2.1μA/V, typical). Enabling a reference buffer reduces the reference input current to 65nA, typical. With the buffer enabled, the common-mode voltage range for V_{REFP} and V_{REFN} is between 100mV and V_{AVDD} - 100mV. With the buffer disabled, the common-mode range is between GND and V_{AVDD}.

Selectable buffers allow flexibility in using resistive voltage references. For example, if a voltage reference is generated by driving a current through a grounded reference resistor, V_{REFN} may be unbuffered, allowing it to be connected directly to GND, while V_{REFP} is buffered, helping reduce the effect of input bias current on the reference voltage.

Low-Power Considerations

Several operating modes help to optimize power and performance. As discussed in the *Signal Path Considerations* section, applications that do not require the gain or low input bias current available in PGA mode can reduce supply current by 130μA by disabling the PGA. For low-impedance sources, the input buffers may be disabled for further power savings. Similarly, the reference buffers may be disabled when the source resistance is low. The modulator has a selectable "duty cycle" mode for low power at lower sampling rates. The IC may be placed into sleep mode between conversions to reduce the average power-supply current.

Modulator Duty Cycle Mode

In addition to its normal operating mode, the modulator can be operated in a 1/4 duty cycle mode to reduce power consumption for a given data rate at the expense of noise. The noise performance of a ΔΣ ADC generally improves when increasing the OSR (lowering the output data rate) because more samples of the internal modulator can be averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be required. For these applications, the internal duty cycling mode can yield significant power savings by periodically entering a low-power state between conversions. In principle, the modulator runs in normal mode with a duty cycle of 25%, performing one "normal" conversion and then automatically entering a low-power state for three consecutive conversion cycles. The noise performance in duty-cycle mode is therefore comparable to the noise performance in normal mode at four times the data rate. The duty-cycle mode can be selected using Direct, Buffered, or PGA signal paths. Neither the input buffers nor PGA are duty cycled while in duty cycle mode.

Select duty-cycle mode using the CONV_TYPE bits in the CONV_START register. To minimize current consumption in duty-cycle mode, set the signal path for an appropriate low-power mode (see the *Signal Path Considerations* section).

Sleep Mode

Sleep mode (controlled by the PD register) powers down all analog circuitry including the internal oscillator, resulting in 0.5μA typical current consumption. Exit sleep mode either by writing to the PD register or (when enabled) by using a GPIO trigger.

Table 4. Analog Supply Current Comparison for Various Operating Modes (Typical Values Shown)

FUNCTION	SUPPLY CURRENT	INPUT RANGE	INPUT CURRENT
Normal Conversion, 60sps, Buffers and PGA Off (Bypass Mode)	390μA	AGND - 30mV to AV_{DD} + 30mV	1μA/V
Duty-Cycle Conversion, 15sps, Buffers and PGA Off (Bypass Mode)	280μA	AGND - 30mV to AV_{DD} + 30mV	1μA/V
Sleep Mode	0.5μA	N/A	—
Input Buffers	35μA	AGND + 100mV to AV_{DD} - 100mV	65nA
PGA	130μA	AGND + 100mV to AV_{DD} - 100mV	1nA
Reference Buffers Disabled	—	AGND - 30mV to AV_{DD} + 30mV	2.1μA/V
Reference Buffers Enabled (Each)	17.5μA	AGND + 100mV to AV_{DD} - 100mV	61nA

Circuit Settling Time

The input to the ADC will require some time to settle after changing the state of the multiplexer, PGA, current sources, and other analog components. When using the sequencer, insert appropriate wait times when changing the state of any of these components.

Input Multiplexer

Settling time for changes to the state of the input multiplexer depends on several factors. These include the delay time of the nonoverlap circuits and the on-resistance of the multiplexer switches, but are dominated by the output impedance of the external source, the impedance (cables, protection components, etc.) between the external source and the multiplexer, any input filter capacitance, the 10pF capacitance on the input to the PGA and modulator blocks, and whether or not the I_{DAC} current sources or the V_{BIAS} source are being used. To obtain an accurate conversion, wait until the multiplexer is fully settled before starting a new conversion. With no added capacitance at the inputs, the settling time after a multiplexer channel change with a 2kΩ source is typically 2μs.

PGA

PGA settling time is primarily limited by the external PGA filter. A 100nF external capacitor across CAPP and CAPN reduces noise by limiting the bandwidth of the PGA. This results in a 2kHz single-pole lowpass filter at the PGA's output. Settling to 22-bit accuracy (0.25ppm) requires 15.25 time constants or 7.6mS for a 2kHz bandwidth. Therefore, the PGA typically dominates the settling time of the input when changing multiplexer settings or changing the PGA's gain.

Reference Multiplexer

Settling time for the reference input multiplexer is similar to that of the input multiplexer but with less complexity, as the reference multiplexer has fewer channels and does not have the I_{DAC} current sources or the V_{BIAS} source as possible inputs. The delay is still dependent on the on-resistance of the reference multiplexer switches, the impedance between the reference source and the reference multiplexer, the output impedance of the reference source, and the input capacitance of the modulator. For accurate conversions, it is important to wait until the reference multiplexer is fully settled before starting a new conversion.

Normally the reference should be located close to the reference inputs, so the resistance between the source and the input should be negligible. If the reference source is an active voltage reference, the source impedance should be low enough to ignore. In some cases, the reference source may be a resistor with a value of a few kilohms. So long as the source resistance is less than around 10kΩ, the settling time contribution from the reference source resistance will be less than 1μs and can generally be ignored.

Excitation Current Source

Enabling/disabling the current source(s) will require time for any input capacitance to charge or discharge. This can be especially important when external capacitors have been added at the inputs for noise filtering.

V_{BIAS} Source

The V_{BIAS} source generates a bias voltage equal to $V_{DD}/2$. There are three V_{BIAS} modes, controlled by the V_{BIAS} register field.

The first mode is an active bias generator featuring a class AB output stage with a series 125kΩ resistor to create a nominal output impedance of 125kΩ. The active bias generator mode reduces current and channel to channel crosstalk. In active mode, if the output is not settled to $V_{DD}/2$, the series resistor is bypassed by a separate low-impedance class AB output stage to decrease settling time. When the output settles to $V_{DD}/2$, the resistor is reasserted for improved noise filtering.

The second and third modes create the V_{BIAS} with resistive voltage-dividers to offer fixed output impedance (either 125kΩ or 20kΩ) at the expense of increased current consumption. The 125kΩ mode offers increased supply noise filtering at the expense of increased settling time. The 20kΩ mode offers reduced settling time, but is higher in current consumption and offers less supply noise filtering.

The bias voltage can be switched into the input channels via the V_{BIAS_SEL} register field.

Sensor Excitation Current Sources

The Matched Current Sources can be programmed to provide 16 different levels of matched currents from 10μA to 1600μA with ±10% accuracy, 0.1% matching, and 50ppm/°C temperature drift from -40°C to +85°C. Either current source or both may be enabled, and each current source may be connected to any one of the ten analog inputs. Note that only one current source may be connected to any input, and a current source may not be connected to an input that has V_{BIAS} connected to it.

Burnout Currents

The internal, selectable 1μA, 5μA, and 10μA burnout current source and sink may be used to detect a sensor fault or wire break.

When enabled, the current source is connected to the selected positive analog input (AINP) and the current sink is connected to the selected negative analog input (AINN).

In case of an open circuit in the sensor input path, these burn-out currents pull the positive input towards AV_{DD} and the negative input towards AGND, resulting in a full-scale reading. (Note that a full-scale reading may also indicate that the sensor is overdriven or that the reference voltage is absent.)

Calibration

The ADC can, on demand, automatically calibrate its internal offset and gain errors as well as system offset and gain errors, and store the calibration values in dedicated registers. The calibration register value defaults are zero (offset) and one (gain). Calibration values may be calculated and stored automatically via a CAL_START command or written directly to the registers through the serial interface. The CAL_START command selects the type of calibration to be performed (self-calibration, PGA gain calibration, system calibration) and initiates the calibration cycle. There is a separate gain calibration register for each PGA gain.

Calibration values are applied to the conversion results stored in the DATA registers according to the following equation:

DATA[0:7] = SYS_GAIN_[A,B] x (((Conversion - SELF_OFF) x SELF_GAIN[1:128]) - SYS_OFF_[A,B])

where

DATA[0:7] is the ADC Data Result destination register, selected by the DEST[3:0] register field,

Conversion is the ADC's conversion result before calibration results are applied,

SELF_GAIN[1:128] is the internal gain correction value for the selected gain.

SELF_OFF is the internal offset correction value,

SYS_GAIN_[A,B] is the selected system gain correction value, and

SYS_OFF_[A,B] is the selected system offset correction value.

All calibration operations are performed at the filter settings programmed into the LINEF[1:0] and RATE[3:0] registers.

There are two sets of system calibration registers, A and B. Either A, B, or neither set can be applied to the ADC conversion result, selectable by the SYSC_SEL register.

Note that calibration routines are performed using the conversion rate, PGA gain, and filter settings in the control registers. In general, slower conversion rates will exhibit lower noise and will therefore produce more accurate calibration.

Self-Calibration

In self-calibration, the required connections to zero and full scale are made internally using the PGA gain setting set in the GAIN register. Self-calibration is typically sufficient to achieve offset and gain accuracy on the order of the noise. When gain is 1, self calibration provides 20ppm of typical full-scale accuracy. The self-calibration routine does not include external effects such as source resistance of the signal driving the input pins, which can change the offset and gain of the system. The range of digital gain correction is from 0.5x to 2.0x. The range of offset correction is $\pm V_{REF}/4$. The tables below show example values for gain and offset calibration codes.

Table 5. Gain Calibration Codes

CODE DESCRIPTION	GAIN	CODE
Maximum Gain Correction	1.999999881	0xFFFFFF
1 LSB Greater Than Unity Gain	$1 + 1/2^{23}$	0x800001
Unity Gain	1.000000	0x800000
1 LSB Less Than Unity Gain	$1 - 1/2^{23}$	0x7FFFFF
Minimum Recommended Gain Correction	0.5	0x400000
Zero Gain	0	0x000000

Table 6. Offset Calibration Codes

CODE DESCRIPTION	OFFSET	CODE
Maximum Offset Correction	$0.25V_{REF}$	0x7FFFFF
Positive 0.25LSB (Bipolar) or 0.5LSB (Unipolar)	$0.25V_{REF}/(2^{23} - 1)$	0x000001
Zero Offset Correction	0V	0x000000
Negative 0.25LSB (Bipolar) or 0.5LSB (Unipolar)	$- 0.25V_{REF}/(2^{23} - 1)$	0xFFFFFF
Minimum Offset Correction	$- 0.25V_{REF}(1+1/(2^{23} - 1))$	0x800000

PGA Self-Calibration

To ensure the lowest possible gain error, eight separate Self-Gain Calibration registers store the calibration factors for each PGA gain from 1x to 128x. When performing gain calibration, the register corresponding to the currently selected PGA gain will be updated. Perform a PGA gain calibration for each PGA gain setting that will be used. Not doing so will yield errors for conversions performed using the gains that have not been calibrated. Self calibration will update the 1x self gain register.

System Offset and Gain Calibration

A system calibration enables calibration of system zero scale and system full scale by presenting a zero-scale signal or a full-scale signal to the selected input pins and initiating a system zero-scale or system gain calibration command. As an alternative to automatic generation of the system calibration values, values may be directly written to the internal calibration registers to achieve any digital offset or scaling required. The range of digital offset correction is $\pm V_{REF}/4$. The range of digital gain correction is from 0.5x to 2.0x. The resolution of offset correction is 0.5 LSB.

Automatic system calibration requires applying the appropriate external signals to the selected AIN inputs. Therefore, the input multiplexer must be properly configured prior to system calibration. Two sets of system calibration coefficients may be created and stored (SYS_OFF_A and SYS_GAIN_A, and SYS_OFF_B and SYS_GAIN_B). Conversions may be performed using either or neither of these sets of coefficients.

Request a system offset calibration by presenting a system zero-scale signal level to the input pins and programming the CAL_START register with the appropriate value. The SYS_OFF_A or SYS_OFF_B register then updates with the value that corrects the chip zero scale.

Request a system gain calibration by presenting a system full-scale signal level to the input pins and programming the CAL_START register with the appropriate value. The SYS_GAIN_A or SYS_GAIN_B register then updates with the value that corrects the chip full scale. A system offset calibration is required prior to system gain calibration to ensure accurate gain calculation.

Sensitivity of Calibration Coefficients

Calibration needs to be repeated if external factors change.

- Both offset and gain calibration (PGA GAIN = 1) should be performed if AV_{DD} supply voltage changes.
- Temperature change affects the calibration accuracy to a much lesser extent (10°C change results in 0.2ppm offset error drift and 0.5ppm gain error drift).
- For gain settings >1, the PGA has reduced sensitivity to supply changes compared to the modulator (28ppm over supply range) but it is still comparable to the *Electrical Characteristics* table specification.

Therefore, it is a good idea to recalibrate in the unlikely case that the supply voltage changes from the minimum AV_{DD} to the maximum AV_{DD} and vice versa. Note that calibration is done at the currently selected data rate, so for best results, set the data rate to a value equal to or lower than the lowest rate that will be used for conversions.

Table 7a. Example of Self-Calibration

STEP	DESCRIPTION	REGISTER	COMMENTS
1	Select Filter and Rate	FILTER (0x08)	For best results, select a rate no faster than the rate that will be used for conversions. A slower rate will result in more accurate calibration. This will determine the time required to execute a calibration.
2	Select Clock Source and Format.	CTRL (0x11)	For best results, select the clock source (internal or external) that will be used for conversions. If external clock is selected, ensure that the external clock is operating before beginning calibration. Format selection doesn't affect results.
3	Start Calibration	CAL_START	Write XXXXX000 to CAL_START. Two conversions will execute at the rate controlled by the FILTER register. The SELF_OFFSET and SELF_GAIN_1 registers will be updated.

Table 7b. Example of PGA Gain Calibration

STEP	DESCRIPTION	REGISTER	COMMENTS
1	Select Filter and Rate	FILTER (0x08)	For best results, select a rate no faster than the rate that will be used for conversions. A slower rate will result in more accurate calibration. Filter selection doesn't affect results.
3	Select Gain and Signal Path	PGA (0x0E)	For best results, select signal path that will be used for conversions. Gain selection causes calibration value to be saved in the associated SELF_GAIN_ register and applied whenever the associated gain is selected.
4	Select Clock Source and Format	CTRL (0x11)	For best results, select the clock source (internal or external) that will be used for conversions. If external clock is selected, ensure that the external clock is operating before beginning calibration. Format selection doesn't affect results.
5	Select PGA Gain and Start Calibration	CAL_START	Write XXXXX001 to CAL_START. One conversion will execute at the rate controlled by the FILTER register. The SELF_GAIN__ register for the selected gain will be updated.

Table 7c. Example of System Offset Calibration

STEP	DESCRIPTION	REGISTER	COMMENTS
1	Apply "System Zero"	N/A	Apply the input voltage that should result in a conversion result of 0 to appropriate analog input(s).
2	Select Filter and Rate	CTRL (0x11)	For best results, select a rate no faster than the rate that will be used for conversions. A slower rate will result in more accurate calibration.
3	Select Reference Input	REF (0x09)	For best results, select a reference voltage equal to or near value that will be used for conversions.
4	Set Input Multiplexer	MUX_CNTRL0 (0x0B)	Select the inputs to which "system zero" is applied.
5	Select Gain and Signal Path	PGA (0x0E)	For best results, select the signal path that will be used for conversions. Gain selection doesn't affect results.
6	Select Clock Source and Format	CTRL (0x11)	For best results, select the clock source (internal or external) that will be used for conversions. If external clock is selected, ensure that the external clock is operating before beginning calibration. Format selection doesn't affect results.
7	Select System Offset and Start calibration	CAL_START	Write XXXXX100 to store in SYS_OFF_A register or XXXXX110 to store in SYS_OFF_B register.

Table 7d. Example of System Gain Calibration

STEP	DESCRIPTION	REGISTER	COMMENTS
1	Apply "System Full-Scale"	N/A	Apply an input voltage that should result in a full-scale conversion result to the appropriate analog input(s).
2	Select Filter and Rate	FILTER (0x08)	For best results, select a rate no faster than the rate that will be used for conversions. A slower rate will result in more accurate calibration.
3	Select Reference Input	CTRL (0x09)	For best results, select a reference voltage equal to or near value that will be used for conversions.
4	Set Input Multi-plexer	MUX_CNTRL0 (0x0B)	Select inputs to which "system full-scale" is applied.
5	Select Gain and Signal Path	PGA (0x0E)	For best results, select the signal path that will be used for conversions. Select the gain that, when combined with the applied input voltage, yields a full-scale conversion result .
6	Select Clock Source and Format	CTRL (0x11)	For best results, select the clock source (internal or external) that will be used for conversions. If external clock is selected, ensure that the external clock is operating before beginning calibration. Format selection doesn't affect results.
7	Select System Offset and Start Calibration	CAL_START	Write XXXXX101 to store in SYS_GAIN_A register or XXXXX111 to store in SYS_GAIN_B register.

GPIOs

Two general-purpose digital IOs increase the ADC's flexibility. When used as an output, a GPIO can be used as a microcontroller interrupt, a control signal for a multiplexer or multichannel switch, or a modulator clock output. GPIO pins configured as outputs operate on the AVDD rail. Care should be taken when using the GPIO pins in input mode to avoid bringing the signal above V_{AVDD} + 0.3V.

When configured as an input, a GPIO can be used as an external clock input, an ADC start control, or a sequence start control. When using GPIO0 as external clock input (EXTCLK = 1), apply a 2.4576MHz clock signal to the pin. Other frequencies can be used, but the data rate and digital filter notch frequencies scale accordingly. GPIO pins configured as inputs accept inputs at V_{DDIO} levels (not to exceed AV_{DD}).

The GPIO ports are configurable with the GP0_CTRL and GP1_CTRL registers. The registers select whether a GPIO will be used as an input or as an output, and if used as an output, the output configuration (CMOS/open-drain).

Low-Side Power Switch

The GPIO pins can be configured to function as a low-side power switch with less than 35Ω on-resistance (25mA switch current) to reduce system power consumption in bridge sensor applications by powering down a bridge circuit between conversions.

Select automatic low-side switch operation by setting the GP_OSEL and GP_DIR register bits:

GP0_CTRL = 1000_0101 (switch normally open, closed during ADC conversions)

"Manually" control the low-side power switch by configuring a GPIO as an open-drain output, and switch between state Logic 0 and Logic 1:

GP0_CTRL = 1000_0100 (Logic 0, switch closed)

GP0_CTRL = 1000_0100 (Logic 1, switch open)

GP0_CTRL = 1000_0100 (Logic 0, switch closed)

Conversion Data Formats

The conversion data format is selected by the FORMAT and U_BN bits in the CTRL register, as shown in Table 7a. The Unipolar/Bipolar Select (U_BN) bit selects whether the input range is bipolar or unipolar. A '1' in this bit location selects unipolar input range and a '0' selects bipolar input range. The Format Select (FORMAT) bit controls the data format when in bipolar mode (U_BN =0). Unipolar data is always in straight binary format. The FORMAT bit has no effect in Unipolar mode (U_BN = 1). In bipolar mode, if the FORMAT bit = 1, then the data format is offset binary. If the FORMAT bit = 0, then the data format is two's complement.

Digital Filter

The configurable digital filter has selectable notch frequencies (50 and 60, 50, 60, or SINC4) and selectable data rates. The filter rejection and frequency response is determined by the LINEF and RATE field settings in the FILTER register.

The simultaneous 50Hz/60Hz rejection FIR filter provides well over 90dB rejection of 50Hz and 60Hz at 16sps and significant rejection of their harmonics. The 50Hz and 60Hz FIR filter settings provide a lower level of attenuation for those frequencies, but at a faster conversion time than available with the simultaneous 50Hz/ 60Hz FIR filter. The SINC4 setting enables a 4th-order SINC filter that can operate at continuous data rates up to 1920sps, with the first notch at the continuous data rate. The available conversion rates are determined by the LINEF setting.

Note that data rate for a given RATE setting is determined by the type of conversion selected in the CONV_START or GP_CONV register, based on a nominal clock period of 2.456MHz. In continuous conversion mode with LINEF = 11, the digital filter has a settling time of 4x the sample rate. The first sample will not be available until the expiration of that settling time. Subsequent samples will be available at the listed sample rate. The filter sample rate is determined by the combination of LINEF and RATE settings, as well as the type of conversion launched by the CONV_START command. Data rates and rejection specifications for all settings are summarized below.

Table 8. Conversion Data Formats

MODE	BIPOLAR MODE			UNIPOLAR MODE	
FORMAT		1	0		X
U_BN		0	0		1
Code Description	Input Voltage (V_{AINP}-V_{AINN})	Offset Binary	2's Complement	Input Voltage (V_{AINP}-V_{AINN})	Straight Binary (Unipolar Mode)
Positive Full Scale	≥VREF	0xFFFFFF	0x7FFFFF	≥V_{REF}	0xFFFFFF
Positive FS – 1LSB	$V_{REF}(1-1/(2^{23}-1))$	0xFFFFFE	0x7FFFFE	$V_{REF}(1-1/(2^{24}-1))$	0xFFFFFE
Positive Mid-Scale	$V_{REF}(1+1/(2^{23}-1))/2$	0xC00000	0x400000	$V_{REF}(1+1/(2^{24}-1))/2$	0x800000
Positive 1 LSB	$V_{REF}/(2^{23}-1)$	0x800001	0x000001	$VREF/(2^{24}-1)$	0x000001
	0V	0x800000	0x000000	0V	0x000000
Negative 1 LSB	$- V_{REF}/(2^{23}-1)$	0x7FFFFF	0xFFFFFF	<0V	0x000000
Negative FS + 1LSB	$-V_{REF}$	0x000001	0x800001	<0V	0x000000
Negative FS	$- V_{REF}(1+1/(2^{23}-1))$	0x000000	0x800000	<0V	0x000000

Table 9a. LINEF = 00 Data Rate and Filter Rejection Settings

RATE VALUE	FILTER TYPE	REJECTION (HZ)	DATA RATE (SPS)		
			Single Cycle	Continuous	Duty Cycle
0000	FIR50/60	50/60Hz	1.0	1.1	0.3
0001	FIR50/60	50/60Hz	2.0	2.1	0.5
0010	FIR50/60	50/60Hz	4.0	4.2	1.1
0011	FIR50/60	50/60Hz	8.0	8.4	2.1
0100-1111	FIR50/60	50/60Hz	16.0	16.8	4.2

Table 9b. LINEF = 01 Data Rate and Filter Rejection Settings

RATE VALUE	FILTER TYPE	REJECTION (HZ)	DATA RATE (SPS)		
			Single Cycle	Continuous	Duty Cycle
0000	FIR50	50Hz	1.3	1.3	0.3
0001	FIR50	50Hz	2.5	2.7	0.7
0010	FIR50	50Hz	5.0	5.3	1.3
0011	FIR50	50Hz	10.0	10.7	2.7
0100	FIR50	50Hz	20.0	21.3	5.3
0101-1111	FIR50	50Hz	35.6	40	10.0

Table 9c. LINEF = 10 Data Rate and Filter Rejection Settings

RATE VALUE	FILTER TYPE	REJECTION (HZ)	DATA RATE (SPS)		
			Single Cycle	Continuous	Duty Cycle
0000	FIR60	60Hz	1.3	1.3	0.3
0001	FIR60	60Hz	2.5	2.7	0.7
0010	FIR60	60Hz	5.0	5.3	1.3
0011	FIR60	60Hz	10.0	10.7	2.7
0100	FIR60	60Hz	20	21.3	5.3
0101-1111	FIR60	60Hz	35.6	40	10.0

Table 9d. LINEF = 11 Data Rate and Filter Rejection Settings

RATE VALUE	FILTER TYPE	REJECTION (HZ)	DATA RATE (SPS)		
			Single Cycle	Continuous	Duty Cycle
0000	SINC4	4	1	4	1
0001	SINC4	10	2.5	10	2.5
0010	SINC4	20	5	20	5
0011	SINC4	40	10	40	10
0100	SINC4	60	15	60	15
0101	SINC4	120	30	120	30
0110	SINC4	240	60	240	60
0111	SINC4	480	120	480	120
1000	SINC4	960	240	960	240
1001-1111	SINC4	1920	480	1920	480

Sequencer

The sequencer is a powerful feature that allows a sequence of commands to be programmed into the sequence buffer (μC0-μC52 registers). When a sequence is initiated by a write to the SEQ_START register or (when configured) a rising edge on a GPIO pin, the sequencer will serially execute commands as if it were the SPI master writing those commands to the control registers. The initiated sequence will begin executing at the address in the SEQ_ADDR or GP_SEQ_ADDR, depending on which is selected. Sequences will execute until a PD command is encountered or until the sequencer is interrupted by a write from the SPI master. If no PD command is encountered, the sequence will execute in a loop and wrap around from μc52->μC0.

All μC registers are '0000' by default, which corresponds to a 'PD:Normal' commmand. PD commands function as a sequence stop. The completion of a sequence can be configured to generate an interrupt via the SEQ_RDY_IE bit. A wraparound, a PD execution, or a SEQ_START inside of a sequence will cause the assertion of SEQ_RDY. As with a continuous conversion with CONV_RDY, executing the sequencer in a loop will auto-clear SEQ_RDY prior to re-asserting it.

Using a SEQ_START command within the sequencer microcode will function as a GOTO statement, enabling multiple continuous sequences to be programmed into the sequencer's μC register space. A CONV_START, CAL_START, or WAIT_START command will prevent the sequencer from advancing until the command is completed. Sequence timing can be controlled with a WAIT_START command. Wait durations should be programmed according to the settling time of the associated internal and external circuitry.

The currently executing microcode address and data can be read back via the read-only μCADDR register. The μCADDR[6:0] can be read back at any time to determine the currently executing microcode address. A read of 0x00 indicates that the sequencer is inactive. Values of 0x3A-0x6E indicate an active sequence.

Active sequences are exited by a write to any register, resetting the μCADDR register to 0x00. Launching a sequence does not reset the control registers. All register states will be retained, either as a result of a prior write or a prior sequence execution.

Sequencer Notes

1. Registers with 24-Bit data operands (UTHRESH, LTHRESH, SELF_OFF, STATUS_IE, etc) are not supported in sequencer mode. Programming a register that has a 24-bit operand into a μC register will result in a '0000' or 'PD' being written to the μC register.
2. Writing a μC address to a μC register will result in a '0000' or 'PD' being written to the register.

Sequencer Example

Below is shown a populated sequence buffer. Three SEQ_START examples are discussed below:

1) The interface executes SEQ_START <μC0>

The sequencer will execute the commands shown (configure the input multiplexer, select buffered signal path, wait, convert and store in data location 1, configure the input multiplexer, wait, convert and store in data location 2, initiate a power down, issue a SEQ_RDY status, and halt the sequence at register μC7.

2) The interface executes SEQ_START <μC8>

The sequencer will execute the commands starting at μC8 and continuing through μC48 in a loop until the the sequencer is interrupted with a write to the interface. This sequence configures the input multiplexer for various combinations of AIN0 through AIN0, performing a conversion with a variety of PGA settings, storing the results in DATA0->DATA7. A SEQ_RDY will be asserted at the end of the sequence (μC48) and deasserted when the sequence starts again (μC8).

3) The interface executes SEQ_START <μC49>

The Sequencer will execute the commands shown from address μC49 (program the input multiplexer and filter, wait, perform a self-calibration) and wraparound continuing execution at μC0. Ultimately, the sequencer will initiate a power down, issue a SEQ_RDY status, and halt the sequence at register μC7.

Table 10. Populated Sequence Register Example.

SEQUENCER REGISTER	SEQUENCER ADDRESS	COMMAND ADDRESS BITS 15:8	COMMAND NAME	COMMAND DATA BITS 7:0	COMMENTS
µC0	0x3A	0x0B	MUX_CTRL0	0x01	Select AINP = AIN0, AINN = AIN1.
µC1	0x3B	0x0E	PGA	0x00	Select buffered input, gain = 1.
µC2	0x3C	0x10	WAIT	0xD0	Insert wait time of (WAIT_EXT * 16) * (WAIT*16) * 407ns. Assuming WAIT_EXT = 0, wait time = 1.3ms.
µC3	0x3D	0x01	CONV_ START	0x10	Initiate a single conversion and send data to DATA1 register.
µC4	0x3E	0x0B	MUX_CTRL0	0x23	Select AINP = AIN2, AINN = AIN3.
µC5	0x3F	0x10	WAIT	0xD0	Insert wait time of 1.3ms (assuming WAIT_EXT = 0).
µC6	0x40	0x01	CONV_ START	0x20	Initiate a single conversion and send data to DATA2 register.
µC7	0x41	0x00	PD	0x10	Enter Sleep Mode, issue SEQ_RDY status, halt sequence.
µC8	0x42	0x0E	PGA	0x21	Select PGA, Gain = 2.
µC9	0x43	0x0B	MUX_CTRL0	0x01	Select AINP = AIN0, AINN = AIN1.
µC10	0x44	0x10	WAIT	0xD0	Insert wait time of 1.3ms (assuming WAIT_EXT = 0).
µC11	0x45	0x08	FILTER	0x04	Select 50/60Hz rejection, 16sps.
µC12	0x46	0x01	CONV_ START	0x00	Initiate a single conversion and send data to DATA0 register.
µC13	0x47	0x0E	PGA	0x22	Select PGA, Gain = 4.
µC14	0x48	0x0B	MUX_CTRL0	0x23	Select AINP = AIN2, AINN = AIN3.
µC15	0x49	0x10	WAIT	0xD0	Insert wait time of 1.3ms (assuming WAIT_EXT=0).
µC16	0x4A	0x08	FILTER	0x04	Select 50/60Hz rejection, 16sps.
µC17	0x4B	0x01	CONV_ START	0x10	Initiate a single conversion and send data to DATA1 register.
µC18	0x4C	0x0E	PGA	0x20	Select PGA, Gain = 1.
µC19	0x4D	0x0B	MUX_CTRL0	0x45	Select AINP = AIN4, AINN = AIN5.
µC20	0x4E	0x10	WAIT	0xD0	Insert wait time of 1.3ms (assuming WAIT_EXT = 0).
µC21	0x4F	0x08	FILTER	0x04	Select 50/60Hz rejection, 16sps.
µC22	0x50	0x01	CONV_ START	0x20	Initiate a single conversion and send data to DATA2 register.
µC23	0x51	0x0E	PGA	0x02	Select buffered input, digital gain = 4.
µC24	0x52	0x0B	MUX_CTRL0	0x03	Select AINP = AIN0, AINN = AIN3.
µC25	0x53	0x10	WAIT	0xD0	Insert wait time of 1.3ms (assuming WAIT_EXT = 0).
µC26	0x54	0x08	FILTER	0x04	Select 50/60Hz rejection, 16sps.

Table 10. Populated Sequence Register Example. (continued)

SEQUENCER REGISTER	SEQUENCER ADDRESS	COMMAND ADDRESS BITS 15:8	COMMAND NAME	COMMAND DATA BITS 7:0	COMMENTS
µC27	0x55	0x01	CONV_ START	0x30	Initiate a single conversion and send data to DATA3 register.
µC28	0x56	0x0E	PGA	0x24	Select PGA, Gain = 16.
µC29	0x57	0x0B	MUX_CTRL0	0x78	Select AINP = AIN7, AINN = AIN8.
µC30	0x58	0x10	WAIT	0xD0	Insert wait time of 1.3ms (assuming WAIT_EXT = 0).
µC31	0x59	0x08	FILTER	0x04	Select 50/60Hz rejection, 16sps.
µC32	0x5A	0x01	CONV_ START	0x40	Initiate a single conversion and send data to DATA4 register.
µC33	0x5B	0x0E	PGA	0x22	Select PGA, Gain = 4.
µC34	0x5C	0x0B	MUX_CTRL0	0x69	Select AINP = AIN6, AINN = AIN9.
µC35	0x5D	0x10	WAIT	0xD0	Insert wait time of 1.3ms (assuming WAIT_EXT = 0).
µC36	0x5E	0x08	FILTER	0x04	Select 50/60Hz rejection, 16sps.
µC37	0x5F	0x01	CONV_ START	0x50	Initiate a single conversion and send data to DATA5 register.
µC38	0x60	0x0E	PGA	0x22	Select PGA, Gain = 4.
µC39	0x61	0x0B	MUX_CTRL0	0x20	Select AINP = AIN2, AINN = AIN0.
µC40	0x62	0x10	WAIT	0xD0	Insert wait time of 1.3ms (assuming WAIT_EXT = 0).
µC41	0x63	0x08	FILTER	0x04	Select 50/60Hz rejection, 16sps.
µC42	0x64	0x01	CONV_ START	0x60	Initiate a single conversion and send data to DATA6 register.
µC43	0x65	0x0E	PGA	0x27	Select PGA, Gain = 128.
µC44	0x66	0x0B	MUX_CTRL0	0x19	Select AINP = AIN1, AINN = AIN9.
µC45	0x67	0x10	WAIT	0xD0	Insert wait time of 1.3ms (assuming WAIT_EXT = 0).
µC46	0x68	0x08	FILTER	0x04	Select 50/60Hz rejection, 16sps.
µC47	0x69	0x01	CONV_ START	0x70	Initiate a single conversion and send data to DATA7 register.
µC48	0x6A	0x02	SEQ_START	0x42	Loop back to sequencer address 0x42 and restart sequence.
µC49	0x6B	0x0B	MUX_CTRL0	0x26	Select AINP = AIN2, AINN = AIN6.
µC50	0x6C	0x08	FILTER	0x04	Select 50/60Hz rejection, 16sps.
µC51	0x6D	0x10	WAIT	0xD0	Insert wait time of 1.3ms (assuming WAIT_EXT = 0).
µC52	0x6E	0x03	CAL_START	0x00	Perform a self-calibration. Wrap around to µC0 (0x3A) and continue.

SPI Interface

The interface is Mode 0 SPI/QSPI™/MICROWIRE®/DSP compatible. Data is strobed in on SCLK rising edges. The content of the SPI operation consists of a one-byte register address and read/write command followed by a one, two, or three-byte control or data word. Programming is by a variable cycle (dictated by the register byte width) SPI instruction framed by a CSB low interval. To abort a command sequence, the rise of CSB must precede the updating rising edge of SCLK.

Data out (DOUT) is updated on the falling edge of SCLK.

Until power-on or other wakeup times have elapsed, reads and writes will have no effect.

DOUT/INTB

This output serves a dual function. In addition to the serial-data output function, DOUT/INTB also indicates the interrupt condition when CSB is low. To find the interrupt state, assert CSB low and sample the INTB/DOUT output. When performing a device readback, the DOUT/INTB pin will reflect the interrupt states until the 9th SCLK falling edge, at which point it will transition to the DOUT data.

SPI Transactions

All transactions consist of a read/write bit, register address, and register data (returned or written). All registers are either 8, 16, or 24 bits in length. Program word execution happens on either the 16th, 24th, or 32nd edge, depending on the programmed register word length. Paired SPI register reads and writes are not supported. Writing to any register while a calibration or conversion is in progress will result in the calibration or conversion being aborted. Readback of any register will not affect either calibration or conversion. Registers are read and written MSB first.

There are three sets of registers for control, status, and data. The 8-bit registers control conversion and power modes, multiplexer connections, and other functions. The 24-bit registers contain conversion data, calibration coefficients, status information, and control over which status bits are reflected in interrupt outputs. the 16-bit registers contain the command addresses and data values for the sequencer.

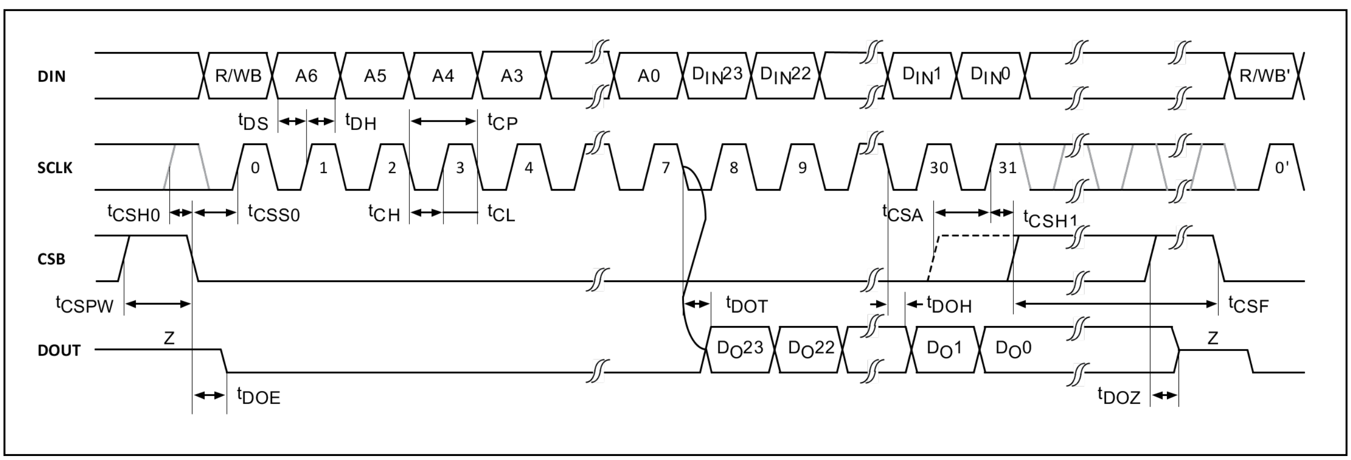


Figure 2. SPI Timing Diagram

Register Address Byte

Write to this register (shown in clock cycles 0 through 7 in the SPI Timing Diagram) to begin any read or write transaction. The R/WB bit selects whether the transaction is a read or write. The REG_ADDR bits select the address of the register to be written or read. There are three register maps, with register widths of 8, 16, and 24 bits. Because register sizes are variable, the REG_ADDR bits also determine the length of the transaction.

<table>
<tr><th>REGISTER</th><th>ADDRESS</th><th>R/W</th><th>SIZE (BITS)</th><th>DEFAULT VALUE</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>ADDR</td><td>XX</td><td>W</td><td>8</td><td>—</td><td>R/WB</td><td colspan="7">REG_ADDR[6:0]</td></tr>
</table>

<table>
<tr><th>FIELD NAME</th><th>BIT(S)</th><th>DEFAULT</th><th colspan="2">FUNCTION</th></tr>
<tr><td>—</td><td>7:2</td><td>—</td><td colspan="2">—</td></tr>
<tr><td rowspan="3">R/WB</td><td rowspan="3">7</td><td rowspan="3">—</td><td>R/WB</td><td>DESCRIPTION</td></tr>
<tr><td>0</td><td>Write to the register at address REG_ADDR[6:0].</td></tr>
<tr><td>1</td><td>Read the register at address REG_ADDR[6:0].</td></tr>
<tr><td rowspan="2">REG_ADDR[6:0]</td><td rowspan="2">6:0</td><td rowspan="2">—</td><td>REG_ADDR[6:0]</td><td>DESCRIPTION</td></tr>
<tr><td></td><td>Read or write (based the value of R/WB) the register at this address.</td></tr>
</table>

Register Map

8-Bit Control RegistersPD (0x00)

<table>
<tr><th>ADDRESS</th><th>NAME</th><th>MSB</th><th></th><th></th><th></th><th></th><th></th><th></th><th>LSB</th></tr>
<tr><td colspan="10">CONTROL</td></tr>
<tr><td>0x00</td><td>PD[7:0]</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td colspan="2">PD[1:0]</td></tr>
<tr><td>0x01</td><td>CONV_START[7:0]</td><td>—</td><td colspan="3">DEST[2:0]</td><td>—</td><td>—</td><td colspan="2">CONV_TYPE [1:0]</td></tr>
<tr><td>0x02</td><td>SEQ_START[7:0]</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td></tr>
<tr><td>0x03</td><td>CAL_START[7:0]</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td colspan="3">CAL_TYPE[2:0]</td></tr>
<tr><td>0x04</td><td>GP0_CTRL[7:0]</td><td colspan="2">GP0_DIR[1:0]</td><td colspan="2">GP0_ISEL[1:0]</td><td>—</td><td colspan="3">GP0_OSEL[2:0]</td></tr>
<tr><td>0x05</td><td>GP1_CTRL[7:0]</td><td colspan="2">GP1_DIR[1:0]</td><td colspan="2">GP1_ISEL[1:0]</td><td>—</td><td colspan="3">GP1_OSEL[2:0]</td></tr>
<tr><td>0x06</td><td>GP_CONV[7:0]</td><td>—</td><td colspan="3">GP_DEST [2:0]</td><td>—</td><td>—</td><td colspan="2">GP_CONV_TYPE [1:0]</td></tr>
<tr><td>0x07</td><td>GP_SEQ_ ADDR[7:0]</td><td>—</td><td colspan="7">GP_SEQ_ADDR[6:0]</td></tr>
<tr><td>0x08</td><td>FILTER[7:0]</td><td>—</td><td>RE- SERVED (0)</td><td colspan="2">LINEF[1:0]</td><td colspan="4">RATE[3:0]</td></tr>
<tr><td>0x09</td><td>CTRL[7:0]</td><td>EXTCLK</td><td>U_BN</td><td>FORMAT</td><td>REF- BUFP_ EN</td><td>REF- BUFN_ EN</td><td colspan="3">REF_SEL[2:0]</td></tr>
<tr><td>0x0A</td><td>SOURCE[7:0]</td><td colspan="2">VBIAS_MODE[1:0]</td><td colspan="2">BRN_MODE[1:0]</td><td colspan="4">IDAC_MODE[3:0]</td></tr>
<tr><td>0x0B</td><td>MUX_CTRL0[7:0]</td><td colspan="4">AINP_SEL[3:0]</td><td colspan="4">AINN_SEL[3:0]</td></tr>
<tr><td>0x0C</td><td>MUX_CTRL1[7:0]</td><td colspan="4">IDAC1_SEL[3:0]</td><td colspan="4">IDAC0_SEL[3:0]</td></tr>
<tr><td>0x0D</td><td>MUX_CTRL2[7:0]</td><td>VBIAS_ SEL_7</td><td>VBIAS_ SEL_6</td><td>VBIAS_ SEL_5</td><td>VBIAS_ SEL_4</td><td>VBIAS_ SEL_3</td><td>VBIAS_ SEL_2</td><td>VBIAS_ SEL_1</td><td>VBIAS_ SEL_0</td></tr>
<tr><td>0x0E</td><td>PGA[7:0]</td><td>—</td><td>—</td><td colspan="2">SIG_PATH[1:0]</td><td>—</td><td colspan="3">GAIN[2:0]</td></tr>
<tr><td>0x0F</td><td>WAIT_EXT[7:0]</td><td colspan="8">WAIT_EXT[7:0]</td></tr>
<tr><td>0x10</td><td>WAIT_START[7:0]</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td></tr>
</table>

PD (0x00)

This register selects the power-down state to be executed. While in a sequence, executing a power-down command will cause the sequencer to stop and issue a SEQ_RDY status. In standby or sleep mode, writing an asynchonous start command (WAIT_START, CONV_START, SEQ_START, WAIT_START), will initiate wakeup, causing the PD state to change to normal mode. During wakeup, the PD register will read '10' and transition to '00' after the wakeup timer expires. Asynchronous start operations will be delayed until the wakeup timer expires.

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	PD[1:0]	
Reset	—	—	—	—	—	—	0x2	
Access Type	—	—	—	—	—	—	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
PD	1:0		00: Normal mode 01: Standby mode—Powers down all analog circuity, but not the internal voltage regulator 10: Sleep mode—Powers down all analog circuitry including the internal voltage regulator 11: Reset—all registers reset to POR state (Self Clearing to 01 standy mode)

CONV_START (0x01)

The CONV_START register initiates conversions, selects the type of conversion to be performed (CONV_TYPE), and selects the register to which the conversion result will be written (DEST). Eight registers are available for ADC conversion results. The three DEST bits select which of these registers the current conversion will be stored in. The CONV_TYPE bits control what type of conversion is to be executed. If in PD: SLEEP or PD: STANDBY mode, writing to this register changes the mode to PD: Normal mode and then initiates the conversion.

BIT	7	6	5	4	3	2	1	0
Field	—	DEST[2:0]			—	—	CONV_TYPE[1:0]	
Reset	—				—	—		
Access Type	—	Write, Read			—	—	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
DEST	6:4		000: Store result in DATA0 001: Store result in DATA1 010: Store result in DATA2 011: Store result in DATA3 100: Store result in DATA4 101: Store result in DATA5 110: Store result in DATA6 111: Store result in DATA7
CONV_TYPE	1:0		00: Single conversion 01: Continuous conversions 10, 11: 1:4 Duty cycled conversions (modulator low-power mode)

SEQ_START (0x02)

A write to the SEQ_START register will immediately execute a sequence beginning at the sequencer address written to the SEQ_ADDR field. Using a SEQ_START command within a sequence will function as a GOTO statement, enabling multiple continuous sequences to be programmed. Writing an address that is outside of the sequencer's microcode address range (0x3A through 0x6E) will result in that write being ignored (no sequence will start). See the *Sequencer* section for more information. If in PD:SLEEP or PD:STANDBY mode, writing to this register changes the mode to PD:Normal Mode and then executes the sequence

CAL_START (0x03)

Writing to this register will execute a calibration as selected by the CAL_TYPE bits. Successful completion of a calibration will result in an update of the corresponding calibration value registers. All calibrations are performed at the filter settings in the LINEF[1:0] and RATE[3:0] register fields at the time the calibration is initiated. If in PD: SLEEP or PD: STANDBY mode, writing to this register changes the mode to PD: normal mode and then initiates the calibration.

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	CAL_TYPE[2:0]		
Reset	—	—	—	—	—			
Access Type	—	—	—	—	—	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
CAL_TYPE	2:0		000: Performs a self-calibration. Resulting offset calibration value is stored in the SELF_OFF register, and the 1x gain calibration value is stored in the SELF_GAIN_1 register. 001: Performs a PGA gain calibration at the currently programmed PGA gain. A 'No Op' will result if PGA Gain calibration is executed with the PGA disabled via the SIG_PATH register, or with the GAIN register set to 1x.The resulting gain calibration value is stored in the SELF_GAIN_[2-128] register corresponding to the currently programmed PGA GAIN setting. 010: Reserved 011: Reserved 100: Performs a system offset calibration. The resulting calibration value is stored in the SYS_OFF_A register. 101: Performs a system gain calibration. The resulting calibration value is stored in the SYS_GAIN_A register. 110: Performs a system offset calibration. The resulting calibration value is stored in the SYS_OFF_B register. 111: Performs a system gain calibration. The resulting calibration value is stored in the SYS_GAIN_B register.

GP0_CTRL (0x04)

The GP0_CTRL register controls the behavior of GPIO0. Writes of reserved values are ignored. The GPIO_0 Direction Select field (GP0_DIR) selects whether GPIO_0 will behave as an input or an output. Open-drain or CMOS output MAX11410 may be selected. The GPI0_0 Input Select field (GP0_INSEL) selects the operation of the GPIO_0 pin when configured as an input using the GP0_DIR field.

The GPIO Output Select field, GP0_OSEL, controls the output operation of the GPIO_0 pin when configured as an output using the GP0_DIR field. When the GPIO is set for rising-edge-triggered conversion start or rising-edge-triggered sequencer start, if in PD: SLEEP or PD: STANDBY mode, the rising edge changes the mode to PD: normal mode and then initiates the conversion or sequence. The minimum pulse width for a GPIO input is 2 x t_{CLK}.

BIT	7	6	5	4	3	2	1	0
Field	GP0_DIR[1:0]		GP0_ISEL[1:0]		—	GP0_OSEL[2:0]		
Reset					—			
Access Type	Write, Read		Write, Read		—	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
GP0_DIR	7:6		00: Input mode, reference to V_{DDIO} (default) 01: Reserved 10: Output mode, open-drain output 11: Output mode, CMOS output
GP0_ISEL	5:4		00: GPIO_0 input disabled (default) 01: GPIO_0 input configured as rising-edge-triggered conversion start 10: GPIO_0 input configured as rising-edge-triggered conversion start 11: Reserved
GP0_OSEL	2:0		000: GPIO_0 output disabled, high Z (default) 001: GPIO_0 output is configured as INTRB (active low) 010: GPIO_0 output is configured as INTR (active high) 011: GPIO_0 output is configured as state Logic 0 100: GPIO_0 output is configured as state Logic 1 101: GPIO_0 output is configured as automatic low-side switch operation (CMOS output mode overridden) 110: GPIO_0 output is configured as modulator active status 111: GPIO_0 output is configured as system clock (2.456Mhz Nominal)

GP1_CTRL (0x05)

The GP1_CTRL register controls the behavior of GPIO1. Writes of reserved values are ignored. The GPIO_1 Direction Select field (GP0_DIR) selects whether GPIO_1 will behave as an input or an output. Open-drain or CMOS output may be selected. The GPIO_1 Input Select field, GP1_INSEL, selects the operation of the GPIO_1 pin when configured as an input using the GP1_DIR field. The GPIO_1 Output Select Field (GP1_OSEL) controls the output operation of the GPIO_1 pin when configured as an output operation using the GP1_DIR field.

When the GPIO is set for rising-edge-triggered conversion start or rising-edge-triggered sequencer start, if in PD: SLEEP or PD: STANDBY mode, the rising edge changes the mode to PD: normal mode and then initiates the conversion or sequence. The minimum pulse width for a GPIO input is 2 x t_{CLK}.

BIT	7	6	5	4	3	2	1	0
Field	GP1_DIR[1:0]		GP1_ISEL[1:0]		—	GP1_OSEL[2:0]		
Reset					—			
Access Type	Write, Read		Write, Read		—	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
GP1_DIR	7:6		00: Input mode, reference to VDDIO (default) 01: Reserved 10: Output mode, open-drain output 11: Output mode, CMOS output
GP1_ISEL	5:4		00: GPIO_1 input disabled (default) 01: GPIO_1 input configured as rising-edge-triggered conversion start 10: GPIO_1 input configured as rising-edge-triggered conversion start 11: Reserved
GP1_OSEL	2:0		000: GPI1_0 output disabled, high Z (default) 001: GPIO_1 output is configured as INTRB (active low) 010: GPIO_1 output is configured as INTR (active high) 011: GPIO_1 output is configured as state Logic 0 100: GPIO_1 output is configured as state Logic 1 101: GPIO_1 output is configured as system clock (2.456Mhz Nominal) 110: GPIO_1 output is configured as modulator active status 111: GPIO_1 output is configured as automatic low-side switch operation (CMOS output mode overridden)

GP_CONV (0x06)

The GP_CONV register selects the type of conversion to be performed when initiated by a GPIO (when the GPIO is configured as a Conversion Start input), and selects the register to which the conversion result will be written. Writing to this register does not execute a conversion. When a GPIO initiates a conversion, the conversion results will be written to the data register selected by the GPIO Conversion Destination field (GP_DEST). The GPIO Conversion Type field selects the type of conversion that will be initiated by a GPIO.

BIT	7	6	5	4	3	2	1	0
Field	—	GP_DEST[2:0]			—	—	GP_CONV_TYPE[1:0]	
Reset	—				—	—		
Access Type	—	Write, Read			—	—	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GP_DEST	6:4		000: Store result in DATA0 001: Store result in DATA1 010: Store result in DATA2 011: Store result in DATA3 100: Store result in DATA4 101: Store result in DATA5 110: Store result in DATA6 111: Store result in DATA7
GP_CONV_TYPE	1:0		00: Single conversion 01: Continuous conversions 10, 11: 1:4 Duty cycled conversions (modulator low-power mode)

GP_SEQ_ADDR (0x07)

The GP_SEQ_ADDR register selects the target sequencer address when a sequence is initiated by a GPIO (when the GPIO is configured as a Sequencer Start input). Writing to this register does not initiate a sequence. Valid values are 0x3A - 0x6F. Writes of invalid addresses will be ignored.

BIT	7	6	5	4	3	2	1	0
Field	—	GP_SEQ_ADDR[6:0]						
Reset	—	0x3A						
Access Type	—	Write, Read						

BITFIELD	BITS	DESCRIPTION
GP_SEQ_ADDR	6:0	Write the address of the Sequencer (Microcode) register at which a sequence should be initiated by a Sequencer Start GPIO event.

FILTER (0x08)

The Filter register selects both the conversion data rate and the behavior of the digital filter. The LINEF field selects one of four digital filter options. The RATE field select the data rate. The options available for the RATE field are determined by the LINEF selection. See the tables in the *Digital Gain* section for details.

BIT	7	6	5	4	3	2	1	0
Field	—	RESERVED (0)	LINEF[1:0]		RATE[3:0]			
Reset	—							
Access Type	—	Write, Read	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED (0)	6	Reserved; always set to 0.	0: Always set to 0.
LINEF	5:4	Sets filter type.	00: Simultaneous 50/60Hz FIR rejection (default) 01: 50Hz FIR rejection 10: 60Hz FIR rejection 11: SINC4
RATE	3:0	Sets conversion rate based on LINEF value. See Table 9a through Table 9d for details.	

CTRL (0x09)

The CTRL register selects the clock source, the unipolar/bipolar data format, the reference inputs, and the reference buffers.

The External Clock Enable (EXTCLK) bit selects the whether the system clock source will be internal or external. Setting EXTCLK to '1' will override any settings in the GP0_CTRL register. A write to the EXTCLK bit inside of a sequence will be ignored. Changing clock sources inside of a sequence is not supported; a write to the EXTCLK bit inside of a sequence will be ignored.

The Unipolar/Bipolar Select (U_BN) bit selects whether the input range is bipolar or unipolar. A ‘1’ in this bit location selects unipolar input range and a ‘0’ selects bipolar input range. The Format Select (FORMAT) bit controls the data format when in bipolar mode (U_BN = 0). Unipolar data is always in straight binary format. The FORMAT bit has no effect in Unipolar mode (U_BN = 1). In bipolar mode, if the FORMAT bit = 1, then the data format is offset binary. If the FORMAT bit = 0, then the data format is two’s complement. (See Table 6.)

Writing to the FORMAT or U_BN bits does not change the values programmed in any threshold registers. However, it will affect the interpretation of these registers. When updating the FORMAT or U_BN bits, threshold registers should be re-written with values that agree with the new format. Any input exceeding the available input range is limited to the minimum or maximum data value.

The Reference P-Side and N-Side Buffer Enable bits (REFBUFP and REFBUFN) control whether the reference input buffers will be enabled.

The Reference Select field (REF_SEL) selects the reference source for the ADC. Available selections include the three differential reference input pairs, the analog power supply voltage, and the single-ended REFP__ inputs.

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	EXTCLK	U_BN	FORMAT	REFBUFP_EN	REFBUFN_EN	REF_SEL[2:0]		
Reset	0x0	0x0	0x0	0x0	0x0	0x1		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
EXTCLK	7		0: Internal clock enabled (default) 1: External clock enabled via GPIO_0 pin
U_BN	6		0: Bipolar input range (default) 1: Unipolar input range
FORMAT	5		0: Two’s complement format. Applies only when bipolar input range is enabled. (default) 1: Offset binary format
REFBUFP_EN	4		0: Power down the reference P-side buffer and bypass, driving the ADC reference input directly from the reference mux (default) 1: Enable the reference P-side buffer
REFBUFN_EN	3		0: Power down the reference N-side buffer and bypass, driving the ADC reference input directly from the reference mux (default) 1: Enable the reference N-side buffer
REF_SEL	2:0		000: AIN0(REF0P)/AIN1(REF0N) 001: REF1P/REF1N (default) 010: REF2P/REF2N 011: AVDD/AGND 100: AIN0(REF0P)/AGND (single-ended mode) 101: REF1P/AGND (single-ended mode) 110: REF2P/AGND (single-ended mode) 111: AVDD/AGND

SOURCE (0x0A)

The SOURCE register configures the excitation current sources, burnout current sources, and bias voltage source.

The V_{BIAS} Mode Control field (VBIAS_MODE) selects the operating mode for the $AV_{DD}/2$ bias voltage source. The bias voltage may be supplied by an amplifier (Active mode) or by a resistive divider (either 125kΩ or 20kΩ source resistance).

The Burnout Current Source Select field (BRN_MODE) selects the nominal current value for the burnout detection current source and sink. Three current values are available.

The Matched Current Source (IDAC_MODE) field selects the nominal current output for the two matched excitation current sources.

Note that simultaneously enabling the IDAC and VBIAS sources on the same analog input is not supported. Enabling V_{BIAS} on an analog input with an IDAC enabled will clear the corresponding IDAC enable. Enabling an IDAC on an analog input with V_{BIAS} enabled will clear the corresponding V_{BIAS} enable.

BIT	7	6	5	4	3	2	1	0
Field	VBIAS_MODE[1:0]		BRN_MODE[1:0]		IDAC_MODE[3:0]			
Reset								
Access Type	Write, Read		Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
VBIAS_MODE	7:6		00: Active mode (default) 01: High impedance; 125kΩ output impedance 10: Low impedance; 20kΩ output impedance 11: Low impedance; 20kΩ output impedance
BRN_MODE	5:4		00: Powered down, burnout sources disabled (default) 01: 0.5μA burnout current sources enabled 10: 1μA burnout current sources enabled 11: 10μA burnout current sources enabled
IDAC_MODE	3:0		0000: 10μA (default) 0001: 50μA 0010: 75μA 0011: 100μA 0100: 125μA 0101: 150μA 0110: 175μA 0111: 200μA 1000: 225μA 1001: 250μA 1010: 300μA 1011: 400μA 1100: 600μA 1101: 800μA 1110: 1200μA 1111: 1600μA

MUX_CTRL0 (0x0B)

The MUX_CTRL0 register selects which analog inputs are connected to AINP and AINN. AINP_SEL selects the multiplexer connection to the positive analog input, and AINN_SEL selects the multiplexer connection to the negative analog input. AINP may also be connected to V_{DD} and AINN may also be connected GND. The default mode is for both AINP and AINN to be unconnected.

BIT	7	6	5	4	3	2	1	0
Field	AINP_SEL[3:0]				AINN_SEL[3:0]			
Reset	0xF				0xF			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
AINP_SEL	7:4		0000: AINP = AIN0 0001: AINP = AIN1 0010: AINP = AIN2 0011: AINP = AIN3 0100: AINP = AIN4 0101: AINP = AIN5 0110: AINP = AIN6 0111: AINP = AIN7 1000: AINP = AIN8 1001: AINP = AIN9 1010: AINP = AVDD 1011: AINN = Unconnected 1100: AINN = Unconnected 1101: AINN = Unconnected 1110: AINN = Unconnected 1111: AINN = Unconnected (default)
AINN_SEL	3:0		0000: AINN = AIN0 0001: AINN = AIN1 0010: AINN = AIN2 0011: AINN = AIN3 0100: AINN = AIN4 0101: AINN = AIN5 0110: AINN = AIN6 0111: AINN = AIN7 1000: AINN = AIN8 1001: AINN = AIN9 1010: AINN = GND 1011: AINN = Unconnected 1100: AINN = Unconnected 1101: AINN = Unconnected 1110: AINN = Unconnected 1111: AINN = Unconnected (default)

MUX_CTRL1 (0x0C)

The MUX_CTRL1 register enables the matched excitation current sources and selects which input each is connected to. IDAC1 and IDAC0 may be connected to any of the ten analog inputs, or may be powered down and unconnected.

BIT	7	6	5	4	3	2	1	0
Field	IDAC1_SEL[3:0]				IDAC0_SEL[3:0]			
Reset	0xF				0xF			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
IDAC1_SEL	7:4		0000: AIN0 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 1000: AIN8 1001: AIN9 1010: Unconnected; IDAC1 powered down. 1011: Unconnected; IDAC1 powered down. 1100: Unconnected; IDAC1 powered down. 1101: Unconnected; IDAC1 powered down. 1110: Unconnected; IDAC1 powered down. 1111: Unconnected; IDAC1 powered down.(Default)
IDAC0_SEL	3:0		0000: AIN0 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 1000: AIN8 1001: AIN9 1010: Unconnected; IDAC0 powered down. 1011: Unconnected; IDAC0 powered down. 1100: Unconnected; IDAC0 powered down. 1101: Unconnected; IDAC0 powered down. 1110: Unconnected; IDAC0 powered down. 1111: Unconnected; IDAC0 powered down.(Default)

MUX_CTRL2 (0x0D)

This register enables of the connection of V_{BIAS} source to the input mux. AIN0 to AIN7 are available for connection to the VBIAS source. Each bit of the VBIAS_SEL register corresponds to a switch enable for an analog input so the V_{BIAS} source may be connected to more than one analog input.

BIT	7	6	5	4	3	2	1	0
Field	VBIAS_ SEL_7	VBIAS_ SEL_6	VBIAS_ SEL_5	VBIAS_ SEL_4	VBIAS_ SEL_3	VBIAS_ SEL_2	VBIAS_ SEL_1	VBIAS_ SEL_0
Reset								
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VBIAS_ SEL_7	7		0: Unconnected 1: AIN7
VBIAS_ SEL_6	6		0: Unconnected 1: AIN6
VBIAS_ SEL_5	5		0: Unconnected 1: AIN5
VBIAS_ SEL_4	4		0: Unconnected 1: AIN4
VBIAS_ SEL_3	3		0: Unconnected 1: AIN3
VBIAS_ SEL_2	2		0: Unconnected 1: AIN2
VBIAS_ SEL_1	1		0: Unconnected 1: AIN1
VBIAS_ SEL_0	0		0: Unconnected 1: AIN0

PGA (0x0E)

The PGA register controls the signal path by enabling or disabling the input buffers and the PGA, and by setting the gain. The Signal Path Select field (SIG_PATH) selects whether the multiplexer output will be connected to the modulator directly, through the low-power buffer, or through the PGA. The GAIN field selects the analog gain setting for the PGA. When When the input signal buffer or direct signal path is selected, this field selects the digital gain setting. When configured for digital gain (PGA disabled) any gain setting higher than 4x will default to 4x.

BIT	7	6	5	4	3	2	1	0
Field	—	—	SIG_PATH[1:0]		—	GAIN[2:0]		
Reset	—	—			—			
Access Type	—	—	Write, Read		—	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SIG_PATH	5:4		00: Buffered, low-power, unity-gain path (PGA disabled, digital gain) [default] 01: Bypass path (signal buffer disabled,PGA disabled, digital gain) 10: PGA path (signal buffer disabled, analog gain) 11: Reserved
GAIN	2:0		000: 1 (default) 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128

WAIT_EXT (0x0F)

This register extends the count range of the WAIT command.

Wait Clocks = (WAIT_EXT*16) * (WAIT * 16)

For a 2.456MHz clock, the minimum wait period is 6.5μsec. The maximum wait period using the wait extender is 6.77s. A write to the wait extension will not cause a wait command to execute. Reading this register will return the written value.

When WAIT_EXT = 0x00, no wait extension is applied and the wait period is equal to (WAIT * 16). In the absence of a reset, the WAIT_EXT selection applies to all subsequent WAIT_START commands.

BIT	7	6	5	4	3	2	1	0
Field	WAIT_EXT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAIT_EXT	7:0	

WAIT_START (0x10)

A write to this register will execute a 'wait' operation with a clock count equal to

Wait Clocks = (WAIT_EXT x 16) * (WAIT x 16)

For a 2.456MHz input clock, the minimum wait period is 6.5μsec. The maximum wait period utilizing the wait extender is 6.77s.

Reading this register will return the current count value, as decremented since the last WAIT execution. Writing to any register during a wait will abort the count operation, but will not reset the register. Writing "0x00" to this register will result in a 'No Op', and no WAIT_DONE status will be issued. If in PD: SLEEP or PD: STANDBY mode, writing to this register changes the mode to PD: Normal Mode.

24-Bit Control, Data, and Status Registers

ADDRESS	NAME	MSB							LSB
REVISION DATA									
0x11	PART_ID[23:16]	—	—	—	—	—	—	—	—
	PART_ID[15:8]	—	—	—	—	—	—	—	—
	PART_ID[7:0]	—	—	—	—	—	REV_ID[2:0]		
SYSTEM CALIBRATION REGISTERS									
0x12	SYSC_SEL[23:16]	–	–	–	–	–	–	–	–
	SYSC_SEL[15:8]	SYSC_SEL_7[1:0]		SYSC_SEL_6[1:0]		–	–	SYSC_SEL_4[1:0]	
	SYSC_SEL[7:0]	SYSC_SEL_3[1:0]		SYSC_SEL_2[1:0]		SYSC_SEL_1[1:0]		SYSC_SEL_0[1:0]	
0x13	SYS_OFF_A[23:16]	SYS_OFF_A[23:16]							
	SYS_OFF_A[15:8]	SYS_OFF_A[15:8]							
	SYS_OFF_A[7:0]	SYS_OFF_A[7:0]							
0x14	SYS_OFF_B[23:16]	SYS_OFF_B[23:16]							
	SYS_OFF_B[15:8]	SYS_OFF_B[15:8]							
	SYS_OFF_B[7:0]	SYS_OFF_B[7:0]							
0x15	SYS_GAIN_A[23:16]	SYS_GAIN_A[23:16]							
	SYS_GAIN_A[15:8]	SYS_GAIN_A[15:8]							
	SYS_GAIN_A[7:0]	SYS_GAIN_A[7:0]							
0x16	SYS_GAIN_B[23:16]	SYS_GAIN_B[23:16]							
	SYS_GAIN_B[15:8]	SYS_GAIN_B[15:8]							
	SYS_GAIN_B[7:0]	SYS_GAIN_B[7:0]							
SELF-CALIBRATION REGISTERS									
0x17	SELF_OFF[23:16]	SELF_OFF[23:16]							
	SELF_OFF[15:8]	SELF_OFF[15:8]							
	SELF_OFF[7:0]	SELF_OFF[7:0]							
0x18	SELF_GAIN_1[23:16]	SELF_GAIN_1[23:16]							
	SELF_GAIN_1[15:8]	SELF_GAIN_1[15:8]							
	SELF_GAIN_1[7:0]	SELF_GAIN_1[7:0]							
0x19	SELF_GAIN_2[23:16]	SELF_GAIN_2[23:16]							
	SELF_GAIN_2[15:8]	SELF_GAIN_2[15:8]							
	SELF_GAIN_2[7:0]	SELF_GAIN_2[7:0]							
0x1A	SELF_GAIN_4[23:16]	SELF_GAIN_4[23:16]							
	SELF_GAIN_4[15:8]	SELF_GAIN_4[15:8]							
	SELF_GAIN_4[7:0]	SELF_GAIN_4[7:0]							

24-Bit Control, Data, and Status Registers (continued)

ADDRESS	NAME	MSB							LSB
0x1B	SELF_GAIN_8[23:16]	SELF_GAIN_8[23:16]							
	SELF_GAIN_8[15:8]	SELF_GAIN_8[15:8]							
	SELF_GAIN_8[7:0]	SELF_GAIN_8[7:0]							
0x1C	SELF_GAIN_16[23:16]	SELF_GAIN_16[23:16]							
	SELF_GAIN_16[15:8]	SELF_GAIN_16[15:8]							
	SELF_GAIN_16[7:0]	SELF_GAIN_16[7:0]							
0x1D	SELF_GAIN_32[23:16]	SELF_GAIN_32[23:16]							
	SELF_GAIN_32[15:8]	SELF_GAIN_32[15:8]							
	SELF_GAIN_32[7:0]	SELF_GAIN_32[7:0]							
0x1E	SELF_GAIN_64[23:16]	SELF_GAIN_64[23:16]							
	SELF_GAIN_64[15:8]	SELF_GAIN_64[15:8]							
	SELF_GAIN_64[7:0]	SELF_GAIN_64[7:0]							
0x1F	SELF_GAIN_128[23:16]	SELF_GAIN_128[23:16]							
	SELF_GAIN_128[15:8]	SELF_GAIN_128[15:8]							
	SELF_GAIN_128[7:0]	SELF_GAIN_128[7:0]							
LOWER-THRESHOLD REGISTERS									
0x20	LTHRESH0[23:16]	LTHRESH0[23:16]							
	LTHRESH0[15:8]	LTHRESH0[15:8]							
	LTHRESH0[7:0]	LTHRESH0[7:0]							
0x21	LTHRESH1[23:16]	LTHRESH1[23:16]							
	LTHRESH1[15:8]	LTHRESH1[15:8]							
	LTHRESH1[7:0]	LTHRESH1[7:0]							
0x22	LTHRESH2[23:16]	LTHRESH2[23:16]							
	LTHRESH2[15:8]	LTHRESH2[15:8]							
	LTHRESH2[7:0]	LTHRESH2[7:0]							
0x23	LTHRESH3[23:16]	LTHRESH3[23:16]							
	LTHRESH3[15:8]	LTHRESH3[15:8]							
	LTHRESH3[7:0]	LTHRESH3[7:0]							
0x24	LTHRESH4[23:16]	LTHRESH4[23:16]							
	LTHRESH4[15:8]	LTHRESH4[15:8]							
	LTHRESH4[7:0]	LTHRESH4[7:0]							
0x25	LTHRESH5[23:16]	LTHRESH5[23:16]							
	LTHRESH5[15:8]	LTHRESH5[15:8]							
	LTHRESH5[7:0]	LTHRESH5[7:0]							

24-Bit Control, Data, and Status Registers (continued)

<table>
<tr><th>ADDRESS</th><th>NAME</th><th>MSB</th><th></th><th></th><th></th><th></th><th></th><th></th><th>LSB</th></tr>
<tr><td rowspan="3">0x26</td><td>LTHRESH6[23:16]</td><td colspan="8">LTHRESH6[23:16]</td></tr>
<tr><td>LTHRESH6[15:8]</td><td colspan="8">LTHRESH6[15:8]</td></tr>
<tr><td>LTHRESH6[7:0]</td><td colspan="8">LTHRESH6[7:0]</td></tr>
<tr><td rowspan="3">0x27</td><td>LTHRESH7[23:16]</td><td colspan="8">LTHRESH7[23:16]</td></tr>
<tr><td>LTHRESH7[15:8]</td><td colspan="8">LTHRESH7[15:8]</td></tr>
<tr><td>LTHRESH7[7:0]</td><td colspan="8">LTHRESH7[7:0]</td></tr>
<tr><td colspan="10">UPPER-THRESHOLD REGISTERS</td></tr>
<tr><td rowspan="3">0x28</td><td>UTHRESH0[23:16]</td><td colspan="8">UTHRESH0[23:16]</td></tr>
<tr><td>UTHRESH0[15:8]</td><td colspan="8">UTHRESH0[15:8]</td></tr>
<tr><td>UTHRESH0[7:0]</td><td colspan="8">UTHRESH0[7:0]</td></tr>
<tr><td rowspan="3">0x29</td><td>UTHRESH1[23:16]</td><td colspan="8">UTHRESH1[23:16]</td></tr>
<tr><td>UTHRESH1[15:8]</td><td colspan="8">UTHRESH1[15:8]</td></tr>
<tr><td>UTHRESH1[7:0]</td><td colspan="8">UTHRESH1[7:0]</td></tr>
<tr><td rowspan="3">0x2A</td><td>UTHRESH2[23:16]</td><td colspan="8">UTHRESH2[23:16]</td></tr>
<tr><td>UTHRESH2[15:8]</td><td colspan="8">UTHRESH2[15:8]</td></tr>
<tr><td>UTHRESH2[7:0]</td><td colspan="8">UTHRESH2[7:0]</td></tr>
<tr><td rowspan="3">0x2B</td><td>UTHRESH3[23:16]</td><td colspan="8">UTHRESH3[23:16]</td></tr>
<tr><td>UTHRESH3[15:8]</td><td colspan="8">UTHRESH3[15:8]</td></tr>
<tr><td>UTHRESH3[7:0]</td><td colspan="8">UTHRESH3[7:0]</td></tr>
<tr><td rowspan="3">0x2C</td><td>UTHRESH4[23:16]</td><td colspan="8">UTHRESH4[23:16]</td></tr>
<tr><td>UTHRESH4[15:8]</td><td colspan="8">UTHRESH4[15:8]</td></tr>
<tr><td>UTHRESH4[7:0]</td><td colspan="8">UTHRESH4[7:0]</td></tr>
<tr><td rowspan="3">0x2D</td><td>UTHRESH5[23:16]</td><td colspan="8">UTHRESH5[23:16]</td></tr>
<tr><td>UTHRESH5[15:8]</td><td colspan="8">UTHRESH5[15:8]</td></tr>
<tr><td>UTHRESH5[7:0]</td><td colspan="8">UTHRESH5[7:0]</td></tr>
<tr><td rowspan="3">0x2E</td><td>UTHRESH6[23:16]</td><td colspan="8">UTHRESH6[23:16]</td></tr>
<tr><td>UTHRESH6[15:8]</td><td colspan="8">UTHRESH6[15:8]</td></tr>
<tr><td>UTHRESH6[7:0]</td><td colspan="8">UTHRESH6[7:0]</td></tr>
<tr><td rowspan="3">0x2F</td><td>UTHRESH7[23:16]</td><td colspan="8">UTHRESH7[23:16]</td></tr>
<tr><td>UTHRESH7[15:8]</td><td colspan="8">UTHRESH7[15:8]</td></tr>
<tr><td>UTHRESH7[7:0]</td><td colspan="8">UTHRESH7[7:0]</td></tr>
</table>

24-Bit Control, Data, and Status Registers (continued)

CONVERSION DATA REGISTERS									
0x30	DATA0[23:16]	DATA0[23:16]							
	DATA0[15:8]	DATA0[15:8]							
	DATA0[7:0]	DATA0[7:0]							
0x31	DATA1[23:16]	DATA1[23:16]							
	DATA1[15:8]	DATA1[15:8]							
	DATA1[7:0]	DATA1[7:0]							
0x32	DATA2[23:16]	DATA2[23:16]							
	DATA2[15:8]	DATA2[15:8]							
	DATA2[7:0]	DATA2[7:0]							
0x33	DATA3[23:16]	DATA3[23:16]							
	DATA3[15:8]	DATA3[15:8]							
	DATA3[7:0]	DATA3[7:0]							
0x34	DATA4[23:16]	DATA4[23:16]							
	DATA4[15:8]	DATA4[15:8]							
	DATA4[7:0]	DATA4[7:0]							
0x35	DATA5[23:16]	DATA5[23:16]							
	DATA5[15:8]	DATA5[15:8]							
	DATA5[7:0]	DATA5[7:0]							
0x36	DATA6[23:16]	DATA6[23:16]							
	DATA6[15:8]	DATA6[15:8]							
	DATA6[7:0]	DATA6[7:0]							
0x37	DATA7[23:16]	DATA7[23:16]							
	DATA7[15:8]	DATA7[15:8]							
	DATA7[7:0]	DATA7[7:0]							
STATUS AND INTERRUPT REGISTERS									
0x38	Status[23:16]	TOR_7	TOR_6	TOR_5	TOR_4	TOR_3	TOR_2	TOR_1	TOR_0
	Status[15:8]	TUR_7	TUR_6	TUR_5	TUR_4	TUR_3	TUR_2	TUR_1	TUR_0
	Status[7:0]	SYS-GOR	—	—	—	WAIT_DONE	CAL_RDY	SEQ_RDY	CONV_RDY
0x39	Status_IE[23:16]	TOR_IE_7	TOR_IE_6	TOR_IE_5	TOR_IE_4	TOR_IE_3	TOR_IE_2	TOR_IE_1	TOR_IE_0
	Status_IE[15:8]	TUR_IE_7	TUR_IE_6	TUR_IE_5	TUR_IE_4	TUR_IE_3	TUR_IE_2	TUR_IE_1	TUR_IE_0
	Status_IE[7:0]	SYS-GOR_IE	—	—	DATA_RDY_IE	WAIT_DONE_IE	CAL_RDY_IE	SEQ_RDY_IE	CONV_RDY_IE

PART_ID (0x11)

This register contains the silicon revision ID.

BIT	23	22	21	20	19	18	17	16
Field	—	—	—	—	—	—	—	—
Reset	—	—	—	—	—	—	—	—
Access Type	—	—	—	—	—	—	—	—
Bit	15	14	13	12	11	10	9	8
Field	—	—	—	—	—	—	—	—
Reset	—	—	—	—	—	—	—	—
Access Type	—	—	—	—	—	—	—	—
Bit	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	REV_ID[2:0]		
Reset	—	—	—	—	—			
Access Type	—	—	—	—	—	Read Only		

BITFIELD	BITS	DESCRIPTION
REV_ID	2:0	Silicon revision ID.

SYSC_SEL (0x12)

There are two sets of system calibration registers, A (SYS_OFF_A and SYS_GAIN_A) and B (SYS_OFF_B and SYS_GAIN_B). The SYSC_SEL bits select whether calibration set A, B, or neither set will be applied to the ADC conversion result stored in the destination register, as selected by the this register.

BIT	23	22	21	20	19	18	17	16
Field	—	—	—	—	—	—	—	—
Reset	—	—	—	—	—	—	—	—
Access Type	—	—	—	—	—	—	—	—
Bit	15	14	13	12	11	10	9	8
Field	SYSC_SEL_7[1:0]		SYSC_SEL_6[1:0]		—	—	SYSC_SEL_4[1:0]	
Reset					—	—		
Access Type	Write, Read		Write, Read		—	—	Write, Read	
Bit	7	6	5	4	3	2	1	0
Field	SYSC_SEL_3[1:0]		SYSC_SEL_2[1:0]		SYSC_SEL_1[1:0]		SYSC_SEL_0[1:0]	
Reset								
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SYSC_SEL_7	15:14		00: SYS_OFF_A & SYS_GAIN_A calibration values are applied to the conversion result stored in DATA7 SYSC_SEL_7[1:0] register. (Default) 01: SYS_OFF_B & SYS_GAIN_B calibration values are applied to the conversion result stored in DATA7 register. 10, 11: System calibration disabled for DATA7 register. (Only self-calibration will be applied.)
SYSC_SEL_6	13:12		00: SYS_OFF_A & SYS_GAIN_A calibration values are applied to the conversion result stored in DATA6 SYSC_SEL_7[1:0] register. (Default) 01: SYS_OFF_B & SYS_GAIN_B calibration values are applied to the conversion result stored in DATA6 register. 10, 11: System calibration disabled for DATA6 register. (Only self-calibration will be applied.)
SYSC_SEL_4	9:8		00: SYS_OFF_A & SYS_GAIN_A calibration values are applied to the conversion result stored in DATA4 SYSC_SEL_7[1:0] register. (Default) 01: SYS_OFF_B & SYS_GAIN_B calibration values are applied to the conversion result stored in DATA4 register. 10, 11: System calibration disabled for DATA4 register. (Only self-calibration will be applied.)

BITFIELD	BITS	DESCRIPTION	DECODE
SYSC_ SEL_3	7:6		00: SYS_OFF_A & SYS_GAIN_A calibration values are applied to the conversion result stored in DATA3 SYSC_SEL_7[1:0] register. (Default) 01: SYS_OFF_B & SYS_GAIN_B calibration values are applied to the conversion result stored in DATA3 register. 10, 11: System calibration disabled for DATA3 register. (Only self-calibration will be applied.)
SYSC_ SEL_2	5:4		00: SYS_OFF_A & SYS_GAIN_A calibration values are applied to the conversion result stored in DATA2 SYSC_SEL_7[1:0] register. (Default) 01: SYS_OFF_B & SYS_GAIN_B calibration values are applied to the conversion result stored in DATA2 register. 10, 11: System calibration disabled for DATA2 register. (Only self-calibration will be applied.)
SYSC_ SEL_1	3:2		00: SYS_OFF_A & SYS_GAIN_A calibration values are applied to the conversion result stored in DATA1 SYSC_SEL_7[1:0] register. (Default) 01: SYS_OFF_B & SYS_GAIN_B calibration values are applied to the conversion result stored in DATA1 register. 10, 11: System calibration disabled for DATA1 register. (Only self-calibration will be applied.)
SYSC_ SEL_0	1:0		00: SYS_OFF_A & SYS_GAIN_A calibration values are applied to the conversion result stored in DATA0 SYSC_SEL_7[1:0] register. (Default) 01: SYS_OFF_B & SYS_GAIN_B calibration values are applied to the conversion result stored in DATA0 register. 10, 11: System calibration disabled for DATA0 register. (Only self-calibration will be applied.)

SYS_OFF_A (0x13)

The system offset A calibration value is subtracted from each conversion result, if selected by the SYSC_DEST_SEL register.

The data is always in 2's complement binary format, and is unaffected by the U_BN and FORMAT bits. Writes to SYS_OFF_A are allowed. A value written to the register remains valid until either a new value is written or until an on-demand system-calibration operation is performed, which will overwrite the current value.

The system offset calibration value applied to the selected destination register is subtracted from the conversion result after self-calibration, but before system gain correction. It is also applied prior to the 1x or 2x scale factor associated with bipolar and unipolar modes.

BIT	23	22	21	20	19	18	17	16
Field	SYS_OFF_A[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	SYS_OFF_A[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	SYS_OFF_A[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SYS_OFF_A	23:0	Offset calibration value subtracted from selected conversion results.

SYS_OFF_B (0x14)

The system offset B calibration value is subtracted from each conversion result, if selected by the SYSC_DEST_SEL register.

The data is always in 2's complement binary format, and is unaffected by the U_BN and FORMAT bits. Writes to SYS_OFF_B are allowed. A value written to the register remains valid until either a new value is written or until an on-demand system-calibration operation is performed, which will over-write the current value.

The system offset calibration value applied to the selected destination register is subtracted from the conversion result after self-calibration, but before system gain correction. It is also applied prior to the 1x or 2x scale factor associated with bipolar and unipolar modes.

BIT	23	22	21	20	19	18	17	16
Field	SYS_OFF_B[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	SYS_OFF_B[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	SYS_OFF_B[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SYS_OFF_B	23:0	Offset calibration value subtracted from selected conversion results.

SYS_GAIN_A (0x15)

The System Gain Calibration A value is used to scale the offset-corrected conversion result, if selected by the SYSC_DEST_SEL register. The format is fixed point, unsigned binary, and is unaffected by the U_BN and FORMAT bits. The binary point is located after the MSB. The MSB corresponds to 2^0, and the LSB corresponds to 2^{-23}.

Writes to this register are allowed. A value written to the register remains valid until either a new value is written or until an on-demand system-calibration operation is performed, which will overwrite the current value. The system gain calibration value scales the offset corrected result by up to 1.999999881x or can correct a gain error of –50%. The amount of positive gain error that can be corrected is determined by modulator overload characteristics, which may be as much as +25%.

BIT	23	22	21	20	19	18	17	16
Field	SYS_GAIN_A[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	SYS_GAIN_A[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	SYS_GAIN_A[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SYS_GAIN_A	23:0	System Gain A Calibration Value

SYS_GAIN_B (0x16)

The System Gain Calibration B value is used to scale the offset-corrected conversion result, if selected by the SYSC_DEST_SEL register. The format is fixed point, unsigned binary, and is unaffected by the U_BN and FORMAT bits. The binary point is located after the MSB. The MSB corresponds to 2^0, and the LSB corresponds to 2^{-23}.

Writes to this register are allowed. A value written to the register remains valid until either a new value is written or until an on-demand system-calibration operation is performed, which will overwrite the current value. The system gain calibration value scales the offset corrected result by up to 1.999999881x or can correct a gain error of -50%. The amount of positive gain error that can be corrected is determined by modulator overload characteristics, which may be as much as +25%.

BIT	23	22	21	20	19	18	17	16
Field	SYS_GAIN_B[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	SYS_GAIN_B[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	SYS_GAIN_B[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SYS_GAIN_B	23:0	System Gain B Calibration Values

SELF_OFF (0x17)

The self-calibration offset value is subtracted from the conversion result, provided that the NOSELFOC bit is set to 0.

The format is always 2's complement binary format, and is unaffected by the U_BN and FORMAT bits. Writing to the self-calibration register is allowed. The value remains valid until either a new write is completed or an on-demand self-calibration operation is performed, which will overwrite the current value.

The self-calibration offset value is subtracted from the conversion result before the self-calibration gain correction and before the system offset and gain correction. It is also applied prior to the 2x scale factor associated with unipolar mode.

BIT	23	22	21	20	19	18	17	16
Field	SELF_OFF[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	SELF_OFF[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	SELF_OFF[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SELF_OFF	23:0	Self-calibration offset value.

SELF_GAIN_1 (0x18)

The self-calibration gain value scales the self-calibration offset-corrected conversion result before the system offset and gain calibration values have been applied. There is a self-gain calibration register for each of the eight selectable gain settings. The format is fixed point, unsigned binary, and is unaffected by the U_BN and FORMAT bits. The binary point is located after the MSB. The MSB corresponds to 2^0, and the LSB corresponds to 2^{-23}. A write to the system-calibration register is allowed. The written value remains valid until either a new write is completed or until an on-demand system-calibration operation is performed, which overwrites the current value. The self-calibration gain value scales the self-cal offset corrected conversion result by up to 2x or can correct a gain error of approximately –50%. The gain will be corrected to within 2 LSB.

BIT	23	22	21	20	19	18	17	16
Field	SELF_GAIN_1[23:16]							
Reset								
Access Type	Write, Read							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	SELF_GAIN_1[15:8]							
Reset								
Access Type	Write, Read							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	SELF_GAIN_1[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SELF_GAIN_1	23:0	Self-gain correction value for gain = 1.

SELF_GAIN_2 (0x19)

BIT	23	22	21	20	19	18	17	16
Field	SELF_GAIN_2[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	SELF_GAIN_2[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	SELF_GAIN_2[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SELF_GAIN_2	23:0	Self-gain correction value for gain = 2.

SELF_GAIN_4 (0x1A)

BIT	23	22	21	20	19	18	17	16
Field	SELF_GAIN_4[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	SELF_GAIN_4[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	SELF_GAIN_4[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SELF_GAIN_4	23:0	Self-gain correction value for gain = 4.

SELF_GAIN_8 (0x1B)

BIT	23	22	21	20	19	18	17	16
Field	SELF_GAIN_8[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	SELF_GAIN_8[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	SELF_GAIN_8[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SELF_GAIN_8	23:0	Self-gain correction value for gain = 8.

SELF_GAIN_16 (0x1C)

BIT	23	22	21	20	19	18	17	16
Field	SELF_GAIN_16[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	SELF_GAIN_16[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	SELF_GAIN_16[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SELF_GAIN_16	23:0	Self-gain correction value for gain = 16.

SELF_GAIN_32 (0x1D)

BIT	23	22	21	20	19	18	17	16
Field	SELF_GAIN_32[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	SELF_GAIN_32[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	SELF_GAIN_32[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SELF_GAIN_32	23:0	Self-gain correction value for gain = 32.

SELF_GAIN_64 (0x1E)

BIT	23	22	21	20	19	18	17	16
Field	SELF_GAIN_64[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	SELF_GAIN_64[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	SELF_GAIN_64[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SELF_GAIN_64	23:0	Self-gain correction value for gain = 64.

SELF_GAIN_128 (0x1F)

BIT	23	22	21	20	19	18	17	16
Field	SELF_GAIN_128[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	SELF_GAIN_128[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	SELF_GAIN_128[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SELF_GAIN_128	23:0	Self-gain correction value for gain = 128.

LTHRESH0 (0x20)

LTHRESH0 holds the lower comparison threshold for the value in the DATA0 register. The comparison result is indicated by the TUR_0 status bit. The comparison result indicated by TUR_0 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	LTHRESH0[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	LTHRESH0[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	LTHRESH0[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LTHRESH0	23:0	Lower comparison threshold for DATA0 value.

LTHRESH1 (0x21)

LTHRESH1 holds the lower comparison threshold for the value in the DATA1 register. The comparison result is indicated by the TUR_1 status bit. The comparison result indicated by TUR_1 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	LTHRESH1[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	LTHRESH1[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	LTHRESH1[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LTHRESH1	23:0	Lower comparison threshold for DATA1 value.

LTHRESH2 (0x22)

LTHRESH2 holds the lower comparison threshold for the value in the DATA2 register. The comparison result is indicated by the TUR_2 status bit. The comparison result indicated by TUR_2 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	LTHRESH2[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	LTHRESH2[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	LTHRESH2[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LTHRESH2	23:0	Lower comparison threshold for DATA2 value.

LTHRESH3 (0x23)

LTHRESH3 holds the lower comparison threshold for the value in the DATA3 register. The comparison result is indicated by the TUR_3 status bit. The comparison result indicated by TUR_3 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	LTHRESH3[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	LTHRESH3[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	LTHRESH3[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LTHRESH3	23:0	Lower comparison threshold for DATA3 value.

LTHRESH4 (0x24)

LTHRESH4 holds the lower comparison threshold for the value in the DATA4 register. The comparison result is indicated by the TUR_4 status bit. The comparison result indicated by TUR_4 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	LTHRESH4[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	LTHRESH4[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	LTHRESH4[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LTHRESH4	23:0	Lower comparison threshold for DATA4 value.

LTHRESH5 (0x25)

LTHRESH5 holds the lower comparison threshold for the value in the DATA5 register. The comparison result is indicated by the TUR_5 status bit. The comparison result indicated by TUR_5 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	LTHRESH5[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	LTHRESH5[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	LTHRESH5[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LTHRESH5	23:0	Lower comparison threshold for DATA5 value.

LTHRESH6 (0x26)

LTHRESH6 holds the lower comparison threshold for the value in the DATA6 register. The comparison result is indicated by the TUR_6 status bit. The comparison result indicated by TUR_6 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	LTHRESH6[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	LTHRESH6[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	LTHRESH6[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LTHRESH6	23:0	Lower comparison threshold for DATA6 value.

LTHRESH7 (0x27)

LTHRESH7 holds the lower comparison threshold for the value in the DATA7 register. The comparison result is indicated by the TUR_7 status bit. The comparison result indicated by TUR_7 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	LTHRESH7[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	LTHRESH7[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	LTHRESH7[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LTHRESH7	23:0	Lower comparison threshold for DATA7 value.

UTHRESH0 (0x28)

UTHRESH0 holds the upper comparison threshold for the value in the DATA0 register. The comparison result is indicated by the TOR_0 status bit. The comparison result indicated by TOR_0 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	UTHRESH0[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	UTHRESH0[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	UTHRESH0[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
UTHRESH0	23:0	Upper comparison threshold for DATA0 value.

UTHRESH1 (0x29)

UTHRESH1 holds the upper comparison threshold for the value in the DATA1 register. The comparison result is indicated by the TOR_1 status bit. The comparison result indicated by TOR_1 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	UTHRESH1[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	UTHRESH1[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	UTHRESH1[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
UTHRESH1	23:0	Upper comparison threshold for DATA1 value.

UTHRESH2 (0x2A)

UTHRESH2 holds the upper comparison threshold for the value in the DATA2 register. The comparison result is indicated by the TOR_2 status bit. The comparison result indicated by TOR_2 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	UTHRESH2[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	UTHRESH2[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	UTHRESH2[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
UTHRESH2	23:0	Upper comparison threshold for DATA2 value.

UTHRESH3 (0x2B)

UTHRESH3 holds the upper comparison threshold for the value in the DATA3 register. The comparison result is indicated by the TOR_3 status bit. The comparison result indicated by TOR_3 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	UTHRESH3[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	UTHRESH3[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	UTHRESH3[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
UTHRESH3	23:0	Upper comparison threshold for DATA3 value.

UTHRESH4 (0x2C)

UTHRESH4 holds the upper comparison threshold for the value in the DATA4 register. The comparison result is indicated by the TOR_4 status bit. The comparison result indicated by TOR_4 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	UTHRESH4[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	UTHRESH4[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	UTHRESH4[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
UTHRESH4	23:0	Upper comparison threshold for DATA4 value.

UTHRESH5 (0x2D)

UTHRESH5 holds the upper comparison threshold for the value in the DATA5 register. The comparison result is indicated by the TOR_5 status bit. The comparison result indicated by TOR_5 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	UTHRESH5[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	UTHRESH5[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	UTHRESH5[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
UTHRESH5	23:0	Upper comparison threshold for DATA5 value.

UTHRESH6 (0x2E)

UTHRESH6 holds the upper comparison threshold for the value in the DATA6 register. The comparison result is indicated by the TOR_6 status bit. The comparison result indicated by TOR_6 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	UTHRESH6[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	UTHRESH6[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	UTHRESH6[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
UTHRESH6	23:0	Upper comparison threshold for DATA6 value.

UTHRESH7 (0x2F)

UTHRESH7 holds the upper comparison threshold for the value in the DATA7 register. The comparison result is indicated by the TOR_7 status bit. The comparison result indicated by TOR_7 is affected by the U_BN and FORMAT bits. If the U_BN and/or FORMAT bits are changed, the threshold value should be changed accordingly.

BIT	23	22	21	20	19	18	17	16
Field	UTHRESH7[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	UTHRESH7[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	UTHRESH7[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
UTHRESH7	23:0	Upper comparison threshold for DATA7 value.

DATA0 (0x30)

The ADC conversion result is stored in DATA0 if this register is selected by the state of the DEST or GP_DEST register.

BIT	23	22	21	20	19	18	17	16
Field	DATA0[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	DATA0[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	DATA0[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DATA0	23:0	Conversion data.

DATA1 (0x31)

The ADC conversion result is stored in DATA1 if this register is selected by the state of the DEST or GP_DEST register.

BIT	23	22	21	20	19	18	17	16
Field	DATA1[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	DATA1[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	DATA1[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DATA1	23:0	Conversion data.

DATA2 (0x32)

The ADC conversion result is stored in DATA2 if this register is selected by the state of the DEST or GP_DEST register.

BIT	23	22	21	20	19	18	17	16
Field	DATA2[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	DATA2[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	DATA2[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DATA2	23:0	Conversion data.

DATA3 (0x33)

The ADC conversion result is stored in DATA3 if this register is selected by the state of the DEST or GP_DEST register.

BIT	23	22	21	20	19	18	17	16
Field	DATA3[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	DATA3[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	DATA3[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DATA3	23:0	Conversion data.

DATA4 (0x34)

The ADC conversion result is stored in DATA4 if this register is selected by the state of the DEST or GP_DEST register.

BIT	23	22	21	20	19	18	17	16
Field	DATA4[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	DATA4[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	DATA4[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DATA4	23:0	Conversion data.

DATA5 (0x35)

The ADC conversion result is stored in DATA5 if this register is selected by the state of the DEST or GP_DEST register.

BIT	23	22	21	20	19	18	17	16
Field	DATA5[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	DATA5[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	DATA5[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DATA5	23:0	Conversion data.

DATA6 (0x36)

The ADC conversion result is stored in DATA6 if this register is selected by the state of the DEST or GP_DEST register.

BIT	23	22	21	20	19	18	17	16
Field	DATA6[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	DATA6[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	DATA6[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DATA6	23:0	Conversion data.

DATA7 (0x37)

The ADC conversion result is stored in DATA7 if this register is selected by the state of the DEST or GP_DEST register.

BIT	23	22	21	20	19	18	17	16
Field	DATA7[23:16]							
Reset								
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	DATA7[15:8]							
Reset								
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	DATA7[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DATA7	23:0	Conversion data.

Status (0x38)

The STATUS register can be read to determine the state of the device and determine the cause of INTB signal assertion. Most STATUS register bits are cleared by a STATUS Register Read.

The TOR bits are Threshold Register Over-Range Status bits. When one is set, it indicates that the corresponding DATA register value is greater than the value set by the UTHRESH register or the ADC conversion result has created a digital under-range condition. TOR will clear when the STATUS register is read. TOR register bits do not self-clear.

The TUR bits are Threshold Register Under-Range Status bits. When one is set, it indicates that the corresponding DATA register value is less than the value set by the LTHRESH register or the ADC conversion result has created a digital underrange condition. TUR will clear when the STATUS register is read. TUR register bits do not self-clear.

The System Gain Over-Range Status bit (SYSGOR) indicates that a system gain calibration was overrange. The SYS_GAIN calibration coefficient has a maximum value of 1.9999999 (0xFFFFFF). When set to ‘1’, SYSGOR indicates that full-scale value out of the converter is likely not available. SYS_GOR will clear when the STATUS register is read, or if a new System Gain calibration yeilds a valid result.

The DATA_RDY bit indicates that the DATA registers contain unread ADC conversion results. This bit is cleared when all unread DATA registers have been read. Unlike other status bits, DATA_RDY is not cleared by a STATUS register read. The DATA_RDY status bit is a logical OR of 8 internal register status bits that are set when new ADC data is written to a DATA register, and are cleared when the corresponding DATA register is read.

Example 1: A CONV_START is performed with 0x70 as the operand. The ADC completes the single conversion. DATA7 contains new conversion data and DATA_RDY is set. Next, the contents of the DATA7 register are read. This causes the corresponding internal register to clear, and the DATA_RDY status bit is cleared.

Example 2: A CONV_START is performed with 0x61 as the operand. The ADC is in a continuous-conversion mode, writing to the DATA6 register and setting the DATA_RDY status bit. The DATA_RDY bit remains set until the DATA6 register has been read. As the ADC is continuously converting, the DATA_RDY bit will be set again as new data is written to the DATA6 register.

Example 3: The following sequence is written

CONV_START, 0x00 (DATA_RDY is set) CONV_START, 0x20

CONV_START, 0x40

CONV_START, 0x60

DATA_RDY[0], DATA_RDY[2], DATA_RDY[4], and DATA_RDY[6] are set internally, thereby setting the DATA_RDY status bit after the first conversion is complete. The ATA0, DATA2, DATA4, and DATA6 registers are then read. After the last DATA register is read, all corresponding internal registers are cleared, and the DATA_RDY status bit is cleared.

The WAIT_DONE bit indicates that the WAIT operation has completed. This status is cleared by a read of the status register or a write to the WAIT_START register

The CAL_RDY bit indicates that a new calibration result is available in the SYS_CAL or SELF_CAL registers. CAL_RDY is cleared by a read of the status register or a write to the CAL_START register.

The SEQ_RDY bit indicates that an initiated sequence has completed at least one iteration. SEQ_RDY is cleared by a read of the status register, a write to the SEQ_START register (including within a sequence), or a sequence wraparound from μC52->μC0.

The CONV_RDY bit indicates that a new conversion result is available in the DATA registers. CONV_RDY is cleared by a read of the status register, a write to the CONV_START register (including within a sequence), or prior to the availability of a new conversion result in continuous or duty cycle mode.

BIT	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	TOR_7	TOR_6	TOR_5	TOR_4	TOR_3	TOR_2	TOR_1	TOR_0
Reset								
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	TUR_7	TUR_6	TUR_5	TUR_4	TUR_3	TUR_2	TUR_1	TUR_0
Reset								
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	SYSGOR	–	–	–	WAIT_ DONE	CAL_RDY	SEQ_RDY	CONV_RDY
Reset		–	–	–				
Access Type	Write, Read	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TOR_7	23		0: Normal operation 1: Threshold overrange/digital overrange condition on channel 7. Clears when the STATUS register is read.
TOR_6	22		0: Normal operation 1: Threshold overrange/digital overrange condition on channel 6. Clears when the STATUS register is read.

BITFIELD	BITS	DESCRIPTION	DECODE
TOR_5	21		0: Normal operation 1: Threshold overrange/digital overrange condition on channel 5. Clears when the STATUS register is read.
TOR_4	20		0: Normal operation 1: Threshold overrange/digital overrange condition on channel 4. Clears when the STATUS register is read.
TOR_3	19		0: Normal operation 1: Threshold overrange/digital overrange condition on channel 3. Clears when the STATUS register is read.
TOR_2	18		0: Normal operation 1: Threshold overrange/digital overrange condition on channel 2. Clears when the STATUS register is read.
TOR_1	17		0: Normal operation 1: Threshold overrange/digital overrange condition on channel 1. Clears when the STATUS register is read.
TOR_0	16		0: Normal operation 1: Threshold overrange/digital overrange condition on channel 0. Clears when the STATUS register is read.
TUR_7	15		0: Normal operation 1: Threshold underrange/digital underrange condition on channel 7. Clears when the STATUS register is read.
TUR_6	14		0: Normal operation 1: Threshold underrange/digital underrange condition on channel 6. Clears when the STATUS register is read.
TUR_5	13		0: Normal operation 1: Threshold underrange/digital underrange condition on channel 5. Clears when the STATUS register is read.
TUR_4	12		0: Normal operation 1: Threshold underrange/digital underrange condition on channel 4. Clears when the STATUS register is read.
TUR_3	11		0: Normal operation 1: Threshold underrange/digital underrange condition on channel 3. Clears when the STATUS register is read.
TUR_2	10		0: Normal operation 1: Threshold underrange/digital underrange condition on channel 2. Clears when the STATUS register is read.
TUR_1	9		0: Normal operation 1: Threshold underrange/digital underrange condition on channel 1. Clears when the STATUS register is read.

BITFIELD	BITS	DESCRIPTION	DECODE
TUR_0	8		0: Normal operation 1: Threshold underrange/digital underrange condition on channel 0. Clears when the STATUS register is read.
SYSGOR	7		0: No fault detected 1: A system gain calibration was overrange. Clears when the STATUS register is read.
WAIT_DONE	3		0: No change 1: Wait operation has completed. Clears on a read of the STATUS register or a write to the WAIT_START register
CAL_RDY	2		0: No change 1: Calibration complete. New calibration result(s) Available in the SYS or SELF calibration registers. Clears on a read of the STATUS register or a write to the CAL_START register.
SEQ_RDY	1		0: No sequence completed, or status bit has been reset. 1: Sequence has completed at least one iteration. Cleared by a read of the status register, a write to the SEQ_START register (including within a sequence), or a sequence wraparound from µC52->µC0.
CONV_RDY	0		0: Normal operation 1: New conversion result(s) available in the DATA registers. Cleared by a read of the STATUS register, a write to the CONV_START register, or just prior to the availability of a new conversion result in continuous or duty cycle mode.

Status_IE (0x39)

The STATUS_IE Register enables or disables status events from appearing as a logic OR of the INT signal state. For every status register bit, there is a corresponding STATUS_IE bit. This register allows the INT signal to be used as a system interrupt for any or all system status sources. Writing a 1 to a bit causes the corresponding STATUS bit state to assert an interrupt. The specific cause of the interrupt can be discerned by reading the STATUS register. An interrupt can be masked by disabling its corresponding enable bit in this register.

The default value of this register is 0x000001, enabling only CONV_RDY by default.

BIT	23	22	21	20	19	18	17	16
Field	TOR_IE_7	TOR_IE_6	TOR_IE_5	TOR_IE_4	TOR_IE_3	TOR_IE_2	TOR_IE_1	TOR_IE_0
Reset								
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
Bit	15	14	13	12	11	10	9	8
Field	TUR_IE_7	TUR_IE_6	TUR_IE_5	TUR_IE_4	TUR_IE_3	TUR_IE_2	TUR_IE_1	TUR_IE_0
Reset								
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read
Bit	7	6	5	4	3	2	1	0
Field	SYSGOR_IE	—	—	DATA_RDY_IE	WAIT_DONE_IE	CAL_RDY_IE	SEQ_RDY_IE	CONV_RDY_IE
Reset		—	—					
Access Type	Write, Read	—	—	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TOR_IE_7	23		0: TOR_7 does not affect INT state. 1: INT asserts when TOR_7 = 1.
TOR_IE_6	22		0: TOR_6 does not affect INT state. 1: INT asserts when TOR_6 = 1.
TOR_IE_5	21		0: TOR_5 does not affect INT state. 1: INT asserts when TOR_5 = 1.
TOR_IE_4	20		0: TOR_4 does not affect INT state. 1: INT asserts when TOR_4 = 1.
TOR_IE_3	19		0: TOR_3 does not affect INT state. 1: INT asserts when TOR_0 = 1.
TOR_IE_2	18		0: TOR_2 does not affect INT state. 1: INT asserts when TOR_2 = 1.
TOR_IE_1	17		0: TOR_1 does not affect INT state. 1: INT asserts when TOR_1 = 1.
TOR_IE_0	16		0: TOR_0 does not affect INT state. 1: INT asserts when TOR_0 = 1.
TUR_IE_7	15		0: TUR_7 does not affect INT state. 1: INT asserts when TUR_7 = 1.

BITFIELD	BITS	DESCRIPTION	DECODE
TUR_IE_6	14		0: TUR_6 does not affect INT state. 1: INT asserts when TUR_6 = 1.
TUR_IE_5	13		0: TUR_5 does not affect INT state. 1: INT asserts when TUR_5 = 1.
TUR_IE_4	12		0: TUR_4 does not affect INT state. 1: INT asserts when TUR_4 = 1.
TUR_IE_3	11		0: TUR_3 does not affect INT state. 1: INT asserts when TUR_3 = 1.
TUR_IE_2	10		0: TUR_2 does not affect INT state. 1: INT asserts when TUR_2 = 1.
TUR_IE_1	9		0: TUR_1 does not affect INT state. 1: INT asserts when TUR_1 = 1.
TUR_IE_0	8		0: TUR_0 does not affect INT state. 1: INT asserts when TUR_0 = 1.
SYSGOR_IE	7		0: SYSGOR does not affect INT state. 1: INT asserts when SYSGOR = 1.
DATA_ RDY_IE	4		0: DATA_RDY does not affect INT state. 1: INT asserts when DATA_RDY = 1.
WAIT_ DONE_IE	3		0: WAIT_DONE does not affect INT state. 1: INT asserts when WAIT_DONE = 1.
CAL_RDY_IE	2		0: CAL_RDY does not affect INT state. 1: INT asserts when CAL_RDY = 1.
SEQ_ RDY_IE	1		0: SEQ_RDY does not affect INT state. 1: INT asserts when SEQ_RDY = 1.
CONV_ RDY_IE	0		0: CONV_RDY does not affect INT state. 1: INT asserts when CONV_RDY = 1.

16-bit Sequencer Registers

ADDRESS	NAME	MSB							LSB
SEQUENCER REGISTERS									
0x3A	µC 0[15:8]	—	REG_ADDR[6:0]						
	µC 0[7:0]	REG_DATA[7:0]							
0x3B	µC 1[15:8]	—	REG_ADDR[6:0]						
	µC 1[7:0]	REG_DATA[7:0]							
0x3C	µC 2[15:8]	—	REG_ADDR[6:0]						
	µC 2[7:0]	REG_DATA[7:0]							
0x3D	µC 3[15:8]	—	REG_ADDR[6:0]						
	µC 3[7:0]	REG_DATA[7:0]							
0x3E	µC 4[15:8]	—	REG_ADDR[6:0]						
	µC 4[7:0]	REG_DATA[7:0]							
0x3F	µC 5[15:8]	—	REG_ADDR[6:0]						
	µC 5[7:0]	REG_DATA[7:0]							

ADDRESS	NAME	MSB							LSB
0x40	µC 6[15:8]	—	REG_ADDR[6:0]						
	µC 6[7:0]	REG_DATA[7:0]							
0x41	µC 7[15:8]	—	REG_ADDR[6:0]						
	µC 7[7:0]	REG_DATA[7:0]							
0x42	µC 8[15:8]	—	REG_ADDR[6:0]						
	µC 8[7:0]	REG_DATA[7:0]							
0x43	µC 9[15:8]	—	REG_ADDR[6:0]						
	µC 9[7:0]	REG_DATA[7:0]							
0x44	µC 10[15:8]	—	REG_ADDR[6:0]						
	µC 10[7:0]	REG_DATA[7:0]							
0x45	µC 11[15:8]	—	REG_ADDR[6:0]						
	µC 11[7:0]	REG_DATA[7:0]							
0x46	µC 12[15:8]	—	REG_ADDR[6:0]						
	µC 12[7:0]	REG_DATA[7:0]							
0x47	µC 13[15:8]	—	REG_ADDR[6:0]						
	µC 13[7:0]	REG_DATA[7:0]							
0x48	µC 14[15:8]	—	REG_ADDR[6:0]						
	µC 14[7:0]	REG_DATA[7:0]							
0x49	µC 15[15:8]	—	REG_ADDR[6:0]						
	µC 15[7:0]	REG_DATA[7:0]							
0x4A	µC 16[15:8]	—	REG_ADDR[6:0]						
	µC 16[7:0]	REG_DATA[7:0]							
0x4B	µC 17[15:8]	—	REG_ADDR[6:0]						
	µC 17[7:0]	REG_DATA[7:0]							
0x4C	µC 18[15:8]	—	REG_ADDR[6:0]						
	µC 18[7:0]	REG_DATA[7:0]							
0x4D	µC 19[15:8]	—	REG_ADDR[6:0]						
	µC 19[7:0]	REG_DATA[7:0]							
0x4E	µC 20[15:8]	—	REG_ADDR[6:0]						
	µC 20[7:0]	REG_DATA[7:0]							
0x4F	µC 21[15:8]	—	REG_ADDR[6:0]						
	µC 21[7:0]	REG_DATA[7:0]							
0x50	µC 22[15:8]	—	REG_ADDR[6:0]						
	µC 22[7:0]	REG_DATA[7:0]							
0x51	µC 23[15:8]	—	REG_ADDR[6:0]						
	µC 23[7:0]	REG_DATA[7:0]							

ADDRESS	NAME	MSB							LSB
0x52	µC 24[15:8]	—	REG_ADDR[6:0]						
	µC 24[7:0]	REG_DATA[7:0]							
0x53	µC 25[15:8]	—	REG_ADDR[6:0]						
	µC 25[7:0]	REG_DATA[7:0]							
0x54	µC 26[15:8]	—	REG_ADDR[6:0]						
	µC 26[7:0]	REG_DATA[7:0]							
0x55	µC 27[15:8]	—	REG_ADDR[6:0]						
	µC 27[7:0]	REG_DATA[7:0]							
0x56	µC 28[15:8]	—	REG_ADDR[6:0]						
	µC 28[7:0]	REG_DATA[7:0]							
0x57	µC 29[15:8]	—	REG_ADDR[6:0]						
	µC 29[7:0]	REG_DATA[7:0]							
0x58	µC 30[15:8]	—	REG_ADDR[6:0]						
	µC 30[7:0]	REG_DATA[7:0]							
0x59	µC 31[15:8]	—	REG_ADDR[6:0]						
	µC 31[7:0]	REG_DATA[7:0]							
0x5A	µC 32[15:8]	—	REG_ADDR[6:0]						
	µC 32[7:0]	REG_DATA[7:0]							
0x5B	µC 33[15:8]	—	REG_ADDR[6:0]						
	µC 33[7:0]	REG_DATA[7:0]							
0x5C	µC 34[15:8]	—	REG_ADDR[6:0]						
	µC 34[7:0]	REG_DATA[7:0]							
0x5D	µC 35[15:8]	—	REG_ADDR[6:0]						
	µC 35[7:0]	REG_DATA[7:0]							
0x5E	µC 36[15:8]	—	REG_ADDR[6:0]						
	µC 36[7:0]	REG_DATA[7:0]							
0x5F	µC 37[15:8]	—	REG_ADDR[6:0]						
	µC 37[7:0]	REG_DATA[7:0]							
0x60	µC 38[15:8]	—	REG_ADDR[6:0]						
	µC 38[7:0]	REG_DATA[7:0]							
0x61	µC 39[15:8]	—	REG_ADDR[6:0]						
	µC 39[7:0]	REG_DATA[7:0]							
0x62	µC 40[15:8]	—	REG_ADDR[6:0]						
	µC 40[7:0]	REG_DATA[7:0]							
0x63	µC 41[15:8]	—	REG_ADDR[6:0]						
	µC 41[7:0]	REG_DATA[7:0]							

ADDRESS	NAME	MSB							LSB
0x64	µC 42[15:8]	—	REG_ADDR[6:0]						
	µC 42[7:0]	REG_DATA[7:0]							
0x65	µC 43[15:8]	—	REG_ADDR[6:0]						
	µC 43[7:0]	REG_DATA[7:0]							
0x66	µC 44[15:8]	—	REG_ADDR[6:0]						
	µC 44[7:0]	REG_DATA[7:0]							
0x67	µC 45[15:8]	—	REG_ADDR[6:0]						
	µC 45[7:0]	REG_DATA[7:0]							
0x68	µC 46[15:8]	—	REG_ADDR[6:0]						
	µC 46[7:0]	REG_DATA[7:0]							
0x69	µC 47[15:8]	—	REG_ADDR[6:0]						
	µC 47[7:0]	REG_DATA[7:0]							
0x6A	µC 48[15:8]	—	REG_ADDR[6:0]						
	µC 48[7:0]	REG_DATA[7:0]							
0x6B	µC 49[15:8]	—	REG_ADDR[6:0]						
	µC 49[7:0]	REG_DATA[7:0]							
0x6C	µC 50[15:8]	—	REG_ADDR[6:0]						
	µC 50[7:0]	REG_DATA[7:0]							
0x6D	µC 51[15:8]	—	REG_ADDR[6:0]						
	µC 51[7:0]	REG_DATA[7:0]							
0x6E	µC 52[15:8]	—	REG_ADDR[6:0]						
	µC 52[7:0]	REG_DATA[7:0]							
0x6F	µCADDR[15:8]	—	—	—	—	—	—	—	—
	µCADDR[7:0]	—	µCADDR[6:0]						

µC (0x3A, 0x3B, 0x3C, 0x3D, 0x3E, 0x3F, 0x40, 0x41, 0x42, 0x43, 0x44, 0x45, 0x46, 0x47, 0x48, 0x49, 0x4A, 0x4B, 0x4C, 0x4D, 0x4E, 0x4F, 0x50, 0x51, 0x52, 0x53, 0x54, 0x55, 0x56, 0x57, 0x58, 0x59, 0x5A, 0x5B, 0x5C, 0x5D, 0x5E, 0x5F, 0x60, 0x61, 0x62, 0x63, 0x64, 0x65, 0x66, 0x67, 0x68, 0x69, 0x6A, 0x6B, 0x6C, 0x6D, 0x6E)

BIT	15	14	13	12	11	10	9	8
Field	—	REG_ADDR[6:0]						
Reset	—							
Access Type	—	Write, Read						
Bit	7	6	5	4	3	2	1	0
Field	REG_DATA[7:0]							
Reset								
Access Type	Write, Read							

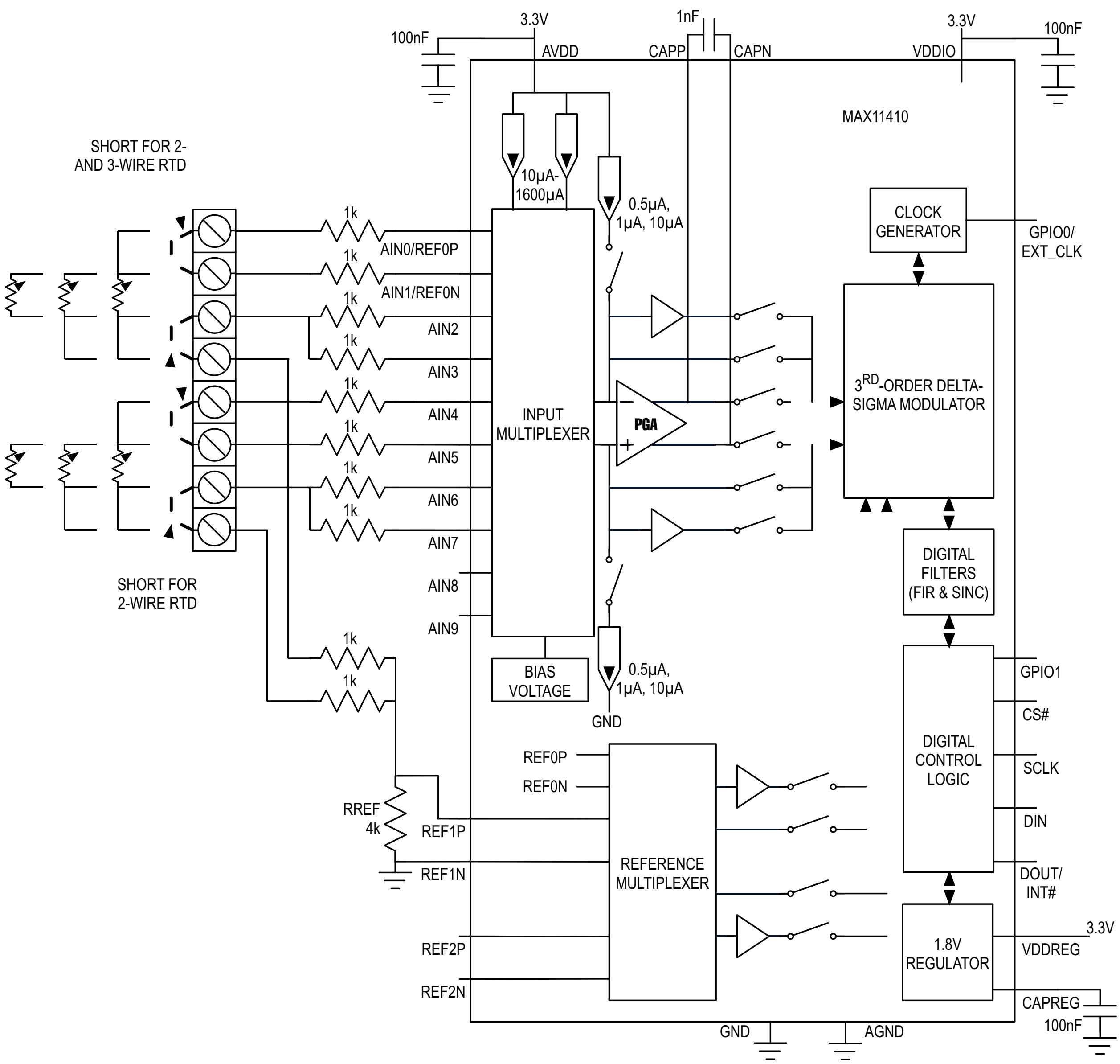
BITFIELD	BITS	DESCRIPTION
REG_ADDR	14:8	Write the address of an 8-bit control register to include it in the sequence.
REG_DATA	7:0	Write the command that corresponds to the register selected by the REG_ADDR field.

µCADDR (0x6F)

BIT	15	14	13	12	11	10	9	8
Field	—	—	—	—	—	—	—	—
Reset	—	—	—	—	—	—	—	—
Access Type	—	—	—	—	—	—	—	—
Bit	7	6	5	4	3	2	1	0
Field	—	µCADDR[6:0]						
Reset	—							
Access Type	—	Read Only						

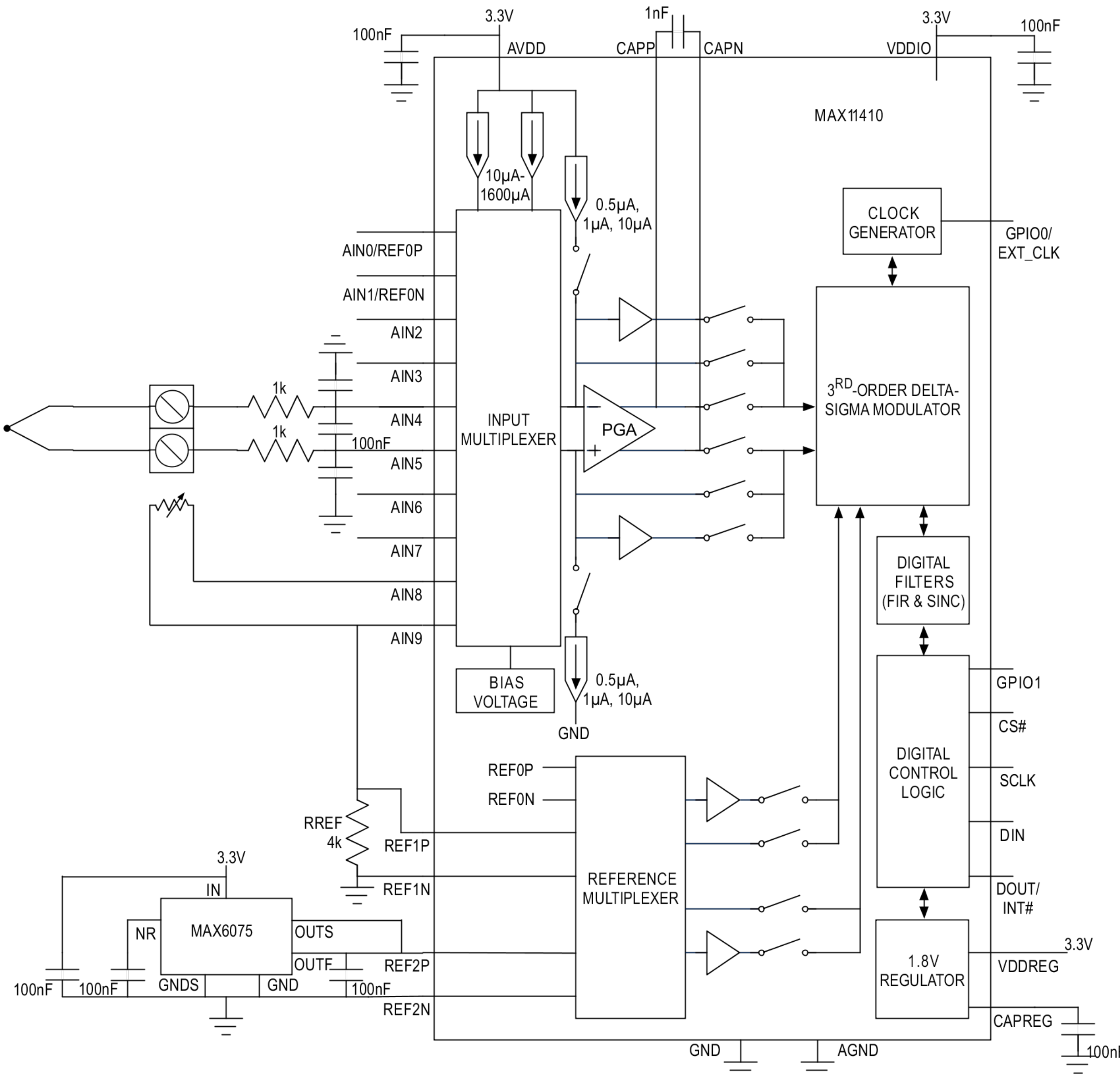
BITFIELD	BITS	DESCRIPTION
µCADDR	6:0	Address of currently executing sequence command.

Typical Application Circuits



A. Two-RTD Temperature Measurement Circuit

Typical Application Circuits (continued)



B. Thermocouple Temperature Measurement Circuit

Two-RTD Temperature Measurement Circuit (2- 3-, and 4-Wire)

In *Typical Application Circuit A*, AIN1 and AIN2 serve as the analog inputs for measuring the voltage across the first RTD, with AIN0 and AIN3 providing the RTD excitation currents. AIN5 and AIN6 are the analog inputs for the second RTD, with AIN4 and AIN7 providing the RTD excitation current. Up to 1000Ω (at 0°C) RTDs, such as Pt1000s can be measured over a full 850°C operating range.

The 1kΩ resistors provide over-voltage protection for the inputs. Although not shown, a 100nF filter capacitor will normally be connected across REF1P and REF1N. A 100nF filter capacitor will be connected across AIN1/AIN2, with a 10nF from AIN1 to GND and from AIN2 to GND. Capacitors will be similarly connected to AIN5 and AIN6.

If the first RTD is a 4-wire or 2-wire unit, set IDAC0 to source 200µA from AIN0. This current will flow through the RTD and through RREF, creating a voltage drop of 800mV across RREF. The voltage across RREF serves as the reference voltage for measurement of the RTD resistance. Because the same current flows through the RTD and RREF, the conversion data will be the ratio of the RTD resistance to RREF. Note that any error in the value of RREF will directly affect the accuracy of the RTD measurement, so use a low-drift, accurate resistor for RREF. If a singletemperature system calibration is performed, RREF may have a relaxed initial tolerance. Note that, while the 4-wire connection can eliminate errors due to cable resistance, any lead resistance will add to the apparent RTD resistance measurement when using a 2-wire connection. Therefore, the 2-wire connection is normally used only when the RTD is close to the circuit.

If a 3-wire RTD is used, IDAC0 will again source current from AIN0, and IDAC1 will source current from AIN3. If the lead resistances are equal, the voltage drops across the two upper leads will be equal, and therefore the voltage measured between AIN1 and AIN2 will be equal to the RTD voltage. Because both excitation currents will flow through RREF, the current values should be reduced to 150µA to maintain voltage headroom. The output code will be half the ratio of the RTD resistance to RREF because 300µA flows through RREF, but only 150µA flows through the RTD.

Thermocouple Measurement Circuit

Measuring temperature with a thermocouple requires two measurements. The thermocouple voltage is measured using a precision voltage reference. In addition, a separate sensor must measure the temperature at the "cold junction" – the point at which the thermocouple wires make contact with copper at the input connector. Cold-junction temperature may be measured in a number of different ways—with a stand-alone temperature sensor, a thermistor, an RTD, or a diode-connected transistor. *Typical Application Circuit B* uses an RTD to measure cold-junction temperature.

1kΩ protection resistors connect the thermocouple output to AIN4 and AIN5. Set the PGA gain to an appropriate value for the thermocouple being used. For example, a K-type thermocouple produces a maximum output voltage of about 54mV. Setting the PGA gain to 32 results in a maximum PGA output voltage of about 1.7V, which is appropriate for use with the 2.5V reference shown. Bias the thermocouple to $V_{DD}/2$ using the internal bias voltage generator. Select AIN5 as the pin to which the internal bias generator is connected. To detect an unconnected thermocouple or a broken thermocouple wire, enable the burnout current generator. An open circuit will result in an overrange input.

To measure the cold-junction temperature using an RTD, set IDAC0 to source 200µA from AIN8. This current will flow through the RTD and through RREF, creating a voltage drop of 800mV across RREF. The voltage across RREF serves as the reference voltage for measurement of the RTD resistance. Because the same current flows through the RTD and RREF, the conversion data will be the ratio of the RTD resistance to RREF. Note that any error in the value of RREF will directly affect the accuracy of the RTD measurement, so use a low-drift, accurate resistor for RREF. If a single-temperature system calibration is performed, RREF may have a relaxed initial tolerance. Because the RTD is close to the ADC, a 2-wire RTD may be used.

Although not shown, a 100nF filter capacitor will normally be connected across REF1P and REF1N. A 100nF filter capacitor will be connected across AIN4/AIN5, with a 10nF from AIN4 to GND and from AIN5 to GND. Capacitors will be similarly connected to AIN8 and AIN9. Additional thermocouples may be connected to the unused inputs.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARKING
MAX11410ATI+	-40°C to +125°C	28 TQFN-EP*	11410A

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
TQFN	T2844+1	21-0139	90-0035

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/16	Initial release	—
1	5/17	Updated PGA Gain specification in *Electrical Characteristics* table	9
2	7/18	Updated PD (0x00) section and Table 4	26, 40

