

MAX12900

Ultra-Low-Power 4-20mA Sensor Transmitter

General Description

The MAX12900 is an ultra-low-power, highly integrated 4-20mA sensor transmitter. The MAX12900 integrates ten building blocks in a small package: a wide input supply voltage LDO, two conditioner circuits for pulse-width-modulated (PWM) inputs, two low-power, low-drift, general-purpose operational amplifiers (op amp) one wide bandwidth, zero-offset drift operational amplifier; two diagnostic comparators, a power-up sequencer with power good output to allow for a smooth power-up, and a low-drift voltage reference.

The MAX12900 converts PWM data from a microcontroller into current over a 4-20mA loop with two, three, or four-wire configurations.

The equivalent to an ultra-low-power, high-resolution, digital-to-analog converter is realized with the combination of two-PWM signals received from a microcontroller, the two conditioner circuits, and an active filter built with the integrated low-power op amp. The outputs of the two conditioner circuits provide a stable PWM amplitude over voltage supply and temperature variation. The wide bandwidth amplifier, in combination with a discrete transistor, converts a voltage input into a current output and allows HART and Foundation Fieldbus H1 signal modulation. The zero-offset operational amplifier and the low-drift voltage reference provide negligible error over wide temperature. The low-power operational amplifier and comparators provide building blocks for enhanced diagnostic features. Supply rail monitoring, output current readback, open circuit and failure detection are a few examples of diagnostic features. All these features, as well as ultra-low-power and high accuracy make the MAX12900 ideal for loop-powered smart sensor transmitters for industrial application.

The MAX12900 is available in 5mm x 5mm 32-pin TQFN package and operates over a wide industrial temperature range of -40°C to +125°C.

Benefits and Features

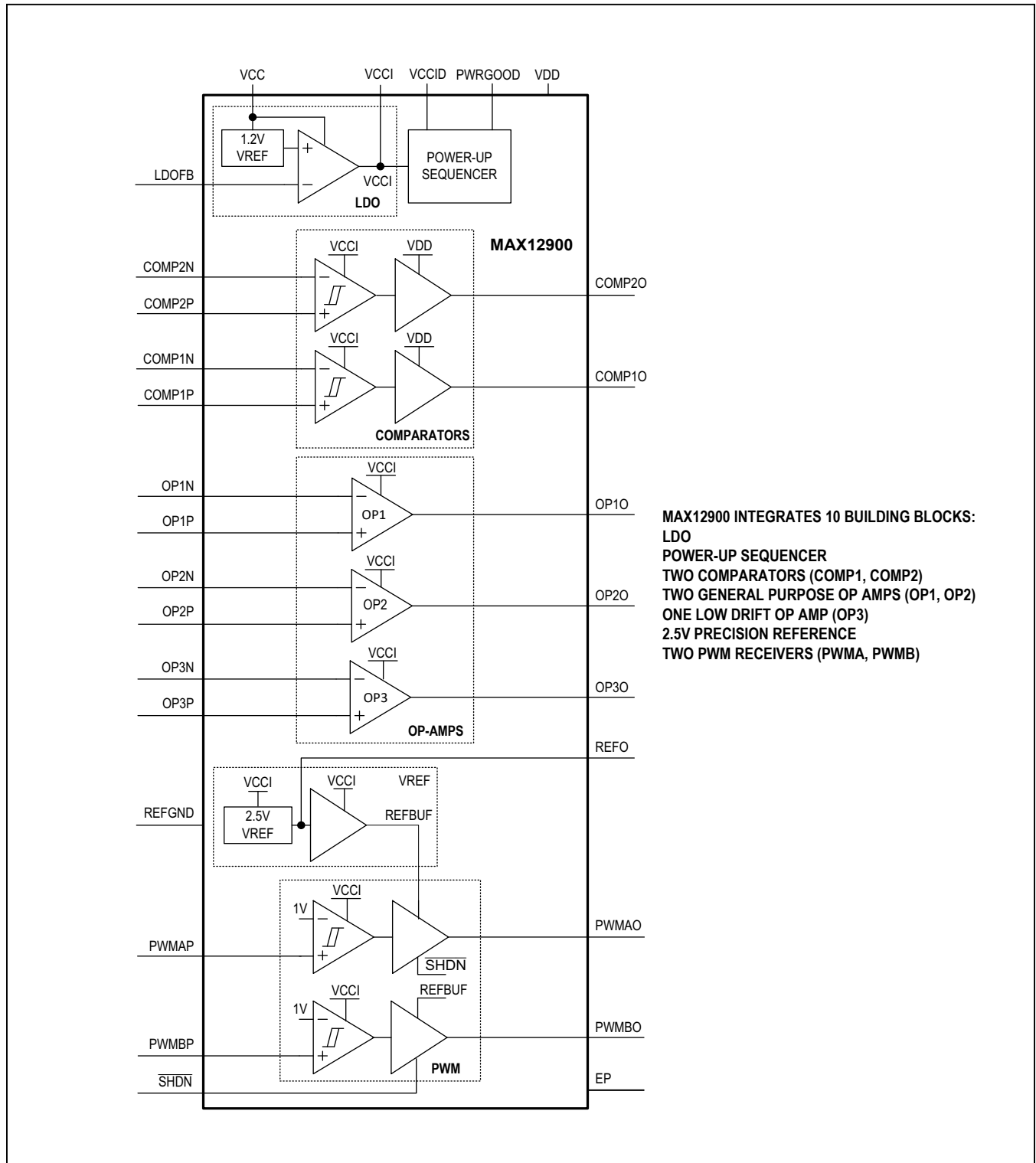
- Wide Input Supply Range: 4.0V to 36V
- Ultra-Low-Power Consumption: 170µA (typ)
- High Linearity: 0.01% (Max Error)
- High Resolution: Up to 16 Bit
- Low Drift Voltage Reference: 10ppm/°C max
- Wide Temperature Range: -40°C to +125°C
- Small Package: 5mm x 5mm x 0.8mm 32-pin TQFN

Applications

- Loop-Powered 4-20mA Current Transmitter
- Smart Sensors
- Remote Instrumentation
- Industrial Automation and Process Control

Ordering Information appears at end of data sheet.

Functional Block Diagram



Absolute Maximum Ratings

VCC to GND-0.3V to +40V
 VCC to VCCI-0.3V to +40V
 VCCI and VCCID to GND-0.3V to +6V
 VCCI to VCCID.....-0.3V to +0.3V
 VDD to GND-0.3V to +6V
 PWRGOOD to GND-0.3V to VCCI + 0.3V
 LDOFB to GND-0.3V to VCCI + 0.3V
 I/C and REFGND to GND-0.3V to + 0.3V
 SHDN to GND-0.3V to VCCI + 0.3V
 REFO to GND-0.3V to VCCI + 0.3V

Op Amps

OP10, OP20, OP30 to GND-0.3V to VCCI + 0.3V
 OP1P, OP1N, OP2P, OP2N, OP3P,
 OP3N to GND.....-0.3V to min [4.5V, VCCI + 0.3V]
 Current into OP1P, OP1N, OP2P, OP2N,
 OP3P, OP3N..... ±20mA
 Current into OP3O..... ±30mA
 Output Short-Circuit Duration for OP1 and
 OP2 to VCCI or GND Continuous

Comparators

COMP1P, COMP1N, COMP2P, COMP2N
 to GND.....-0.3V to VCCI + 0.3V
 COMP1O, COMP2O to GND-0.3V to VDD + 0.3V
 Current into COMP1P, COMP1N,
 COMP2P, COMP2N ±20mA
 Output Short-Circuit Duration to
 VDD or GND..... Continuous

PWM Conditioners

PWMAP, PWMBP to GND.....-0.3V to VCCI + 0.3V
 PWMAO, PWMBO to GND-0.3V to VCCI + 0.3V
 Current into PWMAP, PWMBP..... ±20mA
 Output Short-Circuit Duration to VCCI or GND..... Continuous

Continuous Power Dissipation (T_A = +70°C,
 derate 35.7mW/°C above +70°C).....2857.1mW
 Operating Temperature Range..... -40°C to +125°C
 Functional Temperature Range
 (Startup condition) -55°C to +125°C
 Maximum Junction Temperature +150°C
 Storage Temperature Range -65°C to +150°C
 Soldering Temperature (reflow) +260°C
 Lead Temperature +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32 TQFN

| | |
|--|-------------------------|
| PACKAGE CODE | T3255 |
| Outline Number | 21-0140 |
| Land Pattern Number | 90-0015 |
| Thermal Resistance, Four-Layer Board: | |
| Junction to Ambient (θ _{JA}) | 40.2°C/W |
| Junction to Case (θ _{JC}) | 2.0°C/W |

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

Voltage Reference

$V_{CC1} = +3.0V$ to $+5.5V$, $V_{GND} = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$, $V_{CC1} = +3.3V$. (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---|---|-------|-------|-------|-----------------|
| VOLTAGE REFERENCE 2.5V | | | | | | |
| STATIC | | | | | | |
| Supply Voltage | V_{CC1} | Guaranteed by line regulation test | 3.0 | | 5.5 | V |
| V_{CC1} Line Regulation | $\frac{\Delta V_{REF}}{\Delta V_{CC1}}$ | $3.0V \leq V_{CC1} \leq 5.5V$ | | 20 | 140 | $\mu V/V$ |
| V_{CC} Line Regulation | $\frac{\Delta V_{REF}}{\Delta V_{CC}}$ | $4.3V \leq V_{CC} \leq 36V$, $V_{CC1} = 3.3V$ | | 1.2 | | nV/V |
| Output Voltage | V_{OUT} | $T_A = +25^\circ C$ | 2.495 | 2.500 | 2.505 | V |
| Output Voltage Temperature Coefficient | TCV_{OUT} | $C_{REF} = 2nF$ (Note 2) | | 2 | 10 | ppm/ $^\circ C$ |
| Temperature Hysteresis | $\frac{\Delta V_{REF}}{\text{Cycle}}$ | $C_{REF} = 2nF$ | | -140 | | ppm |
| Load Regulation | $\frac{\Delta V_{REF}}{\Delta I_{OUT}}$ | Sourcing $0V \leq I_{OUT} \leq 500 \mu A$ | | 0.14 | 0.6 | $\mu V/\mu A$ |
| Short-Circuit Current | I_{SC} | Short to GND | | 3 | | mA |
| Maximum Capacitive Load | C_{REF} | | | 2 | | nF |
| DYNAMIC | | | | | | |
| V_{CC1} Ripple Rejection | $\frac{V_{REF}}{V_{CC1}}$ | $V_{CC1} = 3.3V$, $f = 120Hz$ | | 90 | | dB |
| V_{CC} Ripple Rejection | $\frac{V_{REF}}{V_{CC}}$ | $V_{CC} = 12V$, $V_{CC1} = 3.3V$, $f = 120Hz$ | | 160 | | dB |
| Turn-On Settling Time | t_R | From 90% of V_{CC1} to within 0.1% of V_{REF} , $C_{REF} = 2nF$ | | 85 | | μs |
| Noise Voltage | e_{REF} | 0.1Hz to 10Hz | | 40 | | μV_{p-p} |
| | | 10Hz to 10kHz | | 125 | | μV_{RMS} |

Electrical Characteristics (continued)

PWM Conditioners

$V_{CCI} = +3.0V$ to $+5.5V$, $V_{GND} = 0V$, outputs connected to $100k\Omega$ in parallel with $10pF$ terminated to $V_{REF}/2$, input pulses have 10ns rise and fall times, PWM period = $100\mu s$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$, $V_{CCI} = +3.3V$. (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------|--|-----|-----|-----------|------------------|
| PWMA, PWMB | | | | | | |
| STATIC | | | | | | |
| Supply Voltage | V_{CCI} | Guaranteed by $PSRR_{VOH}$ test | 3.0 | | 5.5 | V |
| V_{CCI} Supply Rejection Ratio of Input Threshold Voltage | $PSRR_{VTH}$ | $3.0V \leq V_{CCI} \leq 5.5V$ | | 65 | | dB |
| V_{CC} Supply Rejection Ratio of Input Threshold Voltage | | $4.3V \leq V_{CC} \leq 36V$, $V_{CCI} = 3.3V$ | | 150 | | dB |
| V_{CCI} Supply Rejection Ratio of Output Voltage High | $PSRR_{VOH}$ | $3.0V \leq V_{CCI} \leq 5.5V$, no load | 59 | 75 | | dB |
| V_{CC} Supply Rejection Ratio of Output Voltage High | | $4.3V \leq V_{CC} \leq 36V$, $V_{CCI} = 3.3V$, no load | | 160 | | dB |
| Input Voltage Range | | | 0 | | V_{CCI} | V |
| Input Voltage High | V_{IH} | PWMA, PWMB, \overline{SHDN} | 1.4 | | | V |
| Input Voltage Low | V_{IL} | PWMA, PWMB, \overline{SHDN} | | | 0.6 | V |
| PWMA, PWMB Input Threshold | V_{TH} | | | 1.0 | | V |
| PWMA, PWMB Input Threshold Accuracy | | | | 1 | | mV |
| PWMA, PWMB Hysteresis | PWM_{HYS} | | | 5 | | mV |
| SHDN Hysteresis | $SHDN_{HYS}$ | | | 50 | | mV |
| Input Bias Current | I_B | $V_{PWMA} = V_{PWMB} = 0V$ | | -1 | | nA |
| Input Capacitance | C_{IN} | | | 2 | | pF |
| Output Voltage High | V_{OH} | $V_{REF} - V_{OUT}$, $I_{SOURCE} = 100\mu A$ | | | 0.1 | V |
| Output Voltage Low | V_{OL} | $V_{OUT} - V_{GND}$, $I_{SINK} = 100\mu A$ | | | 0.1 | V |
| Short Circuit Current | I_{SC} | PWMA or PWMB short to V_{REF} | | -12 | | mA |
| | | PWMA or PWMB short to GND | | 6 | | mA |
| Output High Level Voltage Matching | | Difference between the voltage of the two PWM outputs | -2 | | +2 | mV |
| Output Low Level Voltage Matching | | Difference between the voltage of the two PWM outputs | -2 | | +2 | mV |
| PWMA, PWMB Output Voltage High Drift | | | | 7 | | $\mu V/^\circ C$ |
| Linearity | | From code 10 to code 245 (Note 2), Figure 1 | | | 0.01 | %FSR |

Electrical Characteristics (continued)

PWM Conditioners (continued)

$V_{CCI} = +3.0V$ to $+5.5V$, $V_{GND} = 0V$, outputs connected to $100k\Omega$ in parallel with $10pF$ terminated to $V_{REF}/2$, input pulses have 10ns rise and fall times, PWM period = $100\mu s$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$, $V_{CCI} = +3.3V$. (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------------|--|-----|-----|-----|----------------|
| DYNAMIC | | | | | | |
| Propagation Delay Active to Shut down | t_{SHDN} | From 50% of \overline{SHDN} to when PWM outputs are Hi-Z | | 10 | | μs |
| Propagation Delay Shut down to Active | t_{ACT} | From 50% of \overline{SHDN} to when PWM outputs are active | | 10 | | μs |
| Minimum Input Pulse Width | I_{PW} | Single high state, guaranteed by PWM timing tests | 390 | | | ns |
| Driver Rise Time for PWMAO and PWMBO | R_{TA}, R_{TB} | Single 390ns pulse, 10% to 90% | | | 7 | ns |
| Driver Fall Time for PWMAO and PWMBO | F_{TA}, F_{TB} | | | | 6 | ns |
| PWMAO to PWMBO Rise Time Matching | | Single 390ns pulse | -4 | | +4 | ns |
| PWMAO to PWMBO Fall Time Matching | | Single 390ns pulse | -2 | | +2 | ns |
| PWMAO to PWMBO Delay Matching | | Single 390ns pulse, measured at 50% FSR of rising edges | -30 | | +30 | ns |
| PWMAO and PWMBO Pulse Width Accuracy | | Single 390ns pulse, pulse width difference between input and output waveforms (measured at 50% points) | -30 | | +30 | ns |
| PWMAO and PWMBO Pulse Width Variation vs. Temperature | | Single 390ns pulse | | 25 | | ps/ $^\circ C$ |
| PWMAO and PWMBO Pulse Width Matching | | Single 390ns pulse, difference between PWMAO and PWMBO pulse widths | -30 | | +30 | ns |

Electrical Characteristics (continued)

Op Amps

$V_{CCI} = +3.0V$ to $+5.5V$, $V_{GND} = 0V$, $V_{CM} = V_{OUT} = V_{CCI}/2$, no resistive load, $C_L = 10pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$, $V_{CCI} = +3.3V$. (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------------|------------------|---|------|---------|-----------------|------------------|
| OP1, OP2 | | | | | | |
| STATIC | | | | | | |
| Supply Voltage | V_{CCI} | Guaranteed by $PSRR_{V_{CCI}}$ test | 3.0 | | 5.5 | V |
| V_{CCI} Supply Rejection Ratio | $PSRR_{V_{CCI}}$ | $3.0V \leq V_{CCI} \leq 5.5V$ | 62 | 80 | | dB |
| V_{CC} Supply Rejection Ratio | $PSRR_{V_{CC}}$ | $4.3V \leq V_{CC} \leq 36V$, $V_{CCI} = 3.3V$ | | 165 | | dB |
| Common Mode Input Voltage | V_{CMR} | Guaranteed by CMRR test $V_{CCI} \leq 4.5V$ | -0.1 | | $V_{CCI} - 0.5$ | V |
| | | Guaranteed by CMRR test $4.5V \leq V_{CCI} \leq 5.5V$ | -0.1 | | +4.0 | V |
| Common Mode Rejection Ratio | CMRR | $-0.1V \leq V_{CM} \leq \min(4.0V, V_{CCI} - 0.5V)$ | 56 | | | dB |
| Input Offset Voltage | V_{OS} | | | 1 | | mV |
| Input Offset Voltage Drift | ΔV_{OS} | (Note 2) | | | 15 | $\mu V/^\circ C$ |
| Input Bias Current | I_B | $-40^\circ C \leq T_A \leq +85^\circ C$ (Note 2) | -15 | | +15 | pA |
| | | $-40^\circ C \leq T_A \leq +125^\circ C$ (Note 2) | -125 | | +125 | pA |
| Input Offset Current | I_{OS} | $-40^\circ C \leq T_A \leq +85^\circ C$ (Note 2) | -15 | | +15 | pA |
| | | $-40^\circ C \leq T_A \leq +125^\circ C$ (Note 2) | -80 | | +80 | pA |
| Open-Loop Gain | AVOL | $150mV \leq V_{OUT} \leq V_{CCI} - 150mV$, $R_L = 100k\Omega$ connected to $V_{CCI} / 2$, $-40^\circ C \leq T_A \leq +85^\circ C$ | 78 | | | dB |
| | | $-40^\circ C \leq T_A \leq +125^\circ C$ | 72 | | | |
| Output Voltage High | V_{OH} | $V_{CCI} - V_{OUT}$, $R_L = 100k\Omega$ connected to $V_{CCI} / 2$ | | | 25 | mV |
| Output Voltage Low | V_{OL} | $V_{OUT} - V_{GND}$, $R_L = 100k\Omega$ connected to $V_{CCI} / 2$ | | | 25 | mV |
| Output Short-Circuit Current | $I_{OUT(SC)}$ | | | ± 3 | | mA |

Electrical Characteristics (continued)

Op Amps (continued)

$V_{CCI} = +3.0V$ to $+5.5V$, $V_{GND} = 0V$, $V_{CM} = V_{OUT} = V_{CCI}/2$, no resistive load, $C_L = 10pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$, $V_{CCI} = +3.3V$. (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-------------------|--|------|-----|-----------------|-----------------|
| DYNAMIC | | | | | | |
| Input Voltage Noise Density | eN | f = 1kHz | | 150 | | nV/ \sqrt{Hz} |
| Input Current Noise Density | iN | f = 1kHz | | 40 | | fA/ \sqrt{Hz} |
| Gain Bandwidth Product | GBWP | | | 200 | | kHz |
| Slew Rate | SR | | | 0.1 | | V/ μs |
| Settling Time | | To 0.1%, $V_{OUT} = 2V$ step, $A_V = -1V/V$ | | 25 | | μs |
| Maximum Capacitive Load | C_L | No sustained oscillations, $A_V = 1V/V$ | | 100 | | pF |
| OP3 ($R_L = 100k\Omega$ CONNECTED to $V_{CCI}/2$, $C_L = 20pF$) | | | | | | |
| STATIC | | | | | | |
| Supply Voltage | V_{CCI} | Guaranteed by PSRR $_{V_{CCI}}$ test | 3.0 | | 5.5 | V |
| V_{CCI} Supply Rejection Ratio | PSRR $_{V_{CCI}}$ | $3.0V \leq V_{CCI} \leq 5.5V$ | 107 | | | dB |
| V_{CC} Supply Rejection Ratio | PSRR $_{V_{CC}}$ | $4.3V \leq V_{CC} \leq 36V$, $V_{CCI} = 3.3V$ | | 195 | | dB |
| Common Mode Input Voltage | V_{CMR} | Guaranteed by CMRR test $V_{CCI} \leq 4.3V$ | -0.1 | | $V_{CCI} - 0.3$ | V |
| | | Guaranteed by CMRR test $4.3V < V_{CCI} \leq 5.5V$ | -0.1 | | +4.0 | V |
| Common Mode Rejection Ratio | CMRR | $-0.1V \leq V_{CM} \leq \min(4.0V, V_{CCI} - 0.3V)$ | 105 | | | dB |
| Input Offset Voltage | V_{OS} | $T_A = 25^\circ C$, $V_{CCI} = 3.3V$ (Note 2) | -10 | | +10 | μV |
| Input Offset Voltage Drift | ΔV_{OS} | (Note 2) | | 5 | 70 | nV/ $^\circ C$ |
| Input Bias Current | I_B | $-40^\circ C \leq T_A \leq +85^\circ C$ (Note 2) | -15 | | +15 | pA |
| | | $-40^\circ C \leq T_A \leq +125^\circ C$ (Note 2) | -125 | | +125 | pA |
| Input Offset Current | I_{OS} | | | -40 | | pA |
| Input Capacitance | C_{IN} | | | 2 | | pF |
| Open-Loop Gain | AVOL | $150mV \leq V_{OUT} \leq V_{CCI} - 150mV$, $R_L = 5k\Omega$ connected to $V_{CCI} / 2$ | 123 | 150 | | dB |
| Output Voltage High | V_{OH} | $V_{CCI} - V_{OUT}$, $R_L = 100k\Omega$ connected to $V_{CCI} / 2$ | | | 12 | mV |
| Output Voltage Low | V_{OL} | $V_{OUT} - V_{GND}$, $R_L = 100k\Omega$ connected to $V_{CCI} / 2$ | | | 12 | mV |

Electrical Characteristics (continued)

Op Amps (continued)

$V_{CCI} = +3.0V$ to $+5.5V$, $V_{GND} = 0V$, $V_{CM} = V_{OUT} = V_{CCI}/2$, no resistive load, $C_L = 10pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$, $V_{CCI} = +3.3V$. (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------|--------|---|-----|-----|-----|-----------------|
| DYNAMIC | | | | | | |
| Input Voltage Noise Density | eN | f = 1kHz | | 35 | | nV/ \sqrt{Hz} |
| Input Voltage Noise | | 0.1Hz \leq f \leq 10Hz | | 0.7 | | μV_{p-p} |
| Input Current Noise Density | iN | f = 1kHz | | 80 | | fA/ \sqrt{Hz} |
| Gain Bandwidth Product | GBWP | | | 2.2 | | MHz |
| Slew Rate | SR | | | 0.7 | | V/ μs |
| Phase Margin | | | | 57 | | $^\circ$ |
| Maximum Capacitive Load | C_L | No sustained oscillations, $A_V = 1V/V$ | | 300 | | pF |

Electrical Characteristics (continued)

Comparators

$V_{CCI} = +3.0V$ to $+5.5V$, $V_{DD} = +1.8V$ to $+3.6V$, $V_{GND} = 0V$, $V_{CM} = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$, $V_{DD} = V_{CCI} = +3.3V$. (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------------|-------------------|--|-----|-----|-----------------|-------|
| COMP1, COMP2 | | | | | | |
| STATIC | | | | | | |
| Supply Voltage | V_{CCI} | Guaranteed by PSRR $_{V_{CCI}}$ test | 3.0 | | 5.5 | V |
| Supply Voltage Output Stage | V_{DD} | | 1.8 | | 3.6 | V |
| V_{CCI} Supply Rejection Ratio | PSRR $_{V_{CCI}}$ | $3.0V \leq V_{CCI} \leq 5.5V$ | 54 | | | dB |
| V_{CC} Supply Rejection Ratio | PSRR $_{V_{CC}}$ | $4.3V \leq V_{CC} \leq 36V$, $V_{CCI} = 3.3V$ | | 160 | | dB |
| Common Mode Input Voltage | V_{CMR} | Guaranteed by CMRR test | 0 | | $V_{CCI} - 1.3$ | V |
| Common Mode Rejection Ratio | CMRR | $0V \leq V_{CM} \leq V_{CCI} - 1.3V$ | 56 | 75 | | dB |
| Input Offset Voltage | V_{OS} | | -10 | | +10 | mV |
| Hysteresis | V_{HYS} | | | 15 | | mV |
| Input Bias Current | I_B | $V_{CM} = 0V$ | -10 | -1 | | nA |
| Input Offset Current | I_{OS} | | | 1 | | nA |
| Input Capacitance | C_{IN} | | | 2 | | pF |
| Output Voltage High | V_{OH} | $V_{DD} - V_{OUT}$, $I_{SOURCE} = 100 \mu A$ | | | 0.4 | V |

Electrical Characteristics (continued)

Comparators (continued)

$V_{CCI} = +3.0V$ to $+5.5V$, $V_{DD} = +1.8V$ to $+3.6V$, $V_{GND} = 0V$, $V_{CM} = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$, $V_{DD} = V_{CCI} = +3.3V$. (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------|-----------|--|-----|-----|-----|---------|
| Output Voltage Low | V_{OL} | $V_{OUT} - V_{GND}$, $I_{SINK} = 100 \mu A$ | | | 0.4 | V |
| Short Circuit Current | I_{SC} | Short to GND | | 2 | | mA |
| | | Short to V_{DD} | | -2 | | mA |
| DYNAMIC | | | | | | |
| Propagation Delay Low to High | t_{PD+} | $C_{LOAD} = 10pF$, threshold set to $V_{CCI} - 1.4V$, input swings from $0V$ to $V_{CCI} - 1.3V$ | | 2 | | μs |
| Propagation Delay High to Low | t_{PD-} | $C_{LOAD} = 10pF$, threshold set to $0.1V$, input swings from $V_{CCI} - 1.3V$ to $0V$ | | 0.5 | | μs |
| Rise Time | T_R | $C_{LOAD} = 10pF$ | | 50 | | ns |
| Fall Time | T_F | $C_{LOAD} = 10pF$ | | 50 | | ns |

LDO

$V_{CC} = +4.0V$ to $+36V$, $V_{GND} = 0V$, $C_{LOAD} = 0.32\mu F$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$, $V_{CC} = +24V$. (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|------------------|---|------|-----|------|---------|
| LDO | | | | | | |
| STATIC | | | | | | |
| Supply Voltage | V_{CC} | Guaranteed by line regulation test | 4.0 | 24 | 36 | V |
| Dropout Voltage | | Guaranteed by line and load regulation tests | 1 | | | V |
| V_{CC} Line Regulation | | V_{CC} from $V_{CCI} + 1V$ to $36V$, $I_{LDO} = 4mA$, $V_{CCI} = 3.0V$ to $5.5V$ | | 2 | 25 | mV |
| Output Voltage | V_{CCI} | Guaranteed by block PSRR $_{V_{CCI}}$ tests | 3.0 | | 5.5 | V |
| Output Voltage Accuracy | | $V_{CC} = 24V$, no load except for LDOFB resistor divider, $V_{CCI} = 3.3V$ | -3.5 | | +3.5 | % |
| Output Current Range | I_{LDO} | Guaranteed by load regulation test | 0 | | 4 | mA |
| V_{CCI} Current Limit | I_{CCI_Limit} | V_{CCI} short to GND | | 12 | | mA |
| Load Regulation | | $V_{CC} = V_{CCI} + 1V$, I_{LDO} from $0mA$ to $4mA$, $V_{CCI} = 3.0V$ to $5.5V$ | | 1 | 10 | mV |
| Maximum Capacitive Load | C_{LOAD} | No resistive load except for LDOFB resistor divider | | 5 | | μF |
| DYNAMIC | | | | | | |
| V_{CC} Supply Rejection Ratio | PSRR | $V_{CC} = 12V$, DC to $120Hz$ | | 70 | | dB |

Electrical Characteristics (continued)

Chip-Level Specifications

$V_{CC} = +4.0V$ to $+36V$, $V_{CCI} = +3.0V$ to $+5.5V$, $V_{DD} = +1.8V$ to $+3.6V$, $V_{GND} = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$, $V_{CC} = +24V$, $V_{DD} = V_{CCI} = +3.3V$. (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|----------------------|---|-----|-----|-----|-----------------------|
| STATIC | | | | | | |
| V _{CC} Supply Current | I _{CC} | V _{CC} = 24V, V _{CCI} = 3.3V, $\overline{SHDN} = 3.3V$, no load, $-40^\circ C \leq T_A \leq +85^\circ C$ | | 170 | 250 | μA |
| | | $-40^\circ C \leq T_A \leq +125^\circ C$ | | | 265 | μA |
| V _{CC} Supply Current with PWM Conditioners Shutdown | I _{CC_SHDN} | V _{CC} = 24V, V _{CCI} = 3.3V, $\overline{SHDN} = 0V$, no load | | 142 | | μA |
| V _{DD} Supply Current | I _{DD} | | | | 1 | μA |
| PWRGOOD Turn-on Threshold | | | | 90 | | % of V _{CCI} |
| PWRGOOD Turn-off Threshold | | | | 80 | | % of V _{CCI} |
| PWRGOOD Voltage High | V _{OH} | V _{CCI} - V _{OUT} , I _{SOURCE} = 100 μA | | | 0.4 | V |
| PWRGOOD Voltage Low | V _{OL} | V _{OUT} - V _{GND} , I _{SINK} = 100 μA | | | 0.4 | V |
| PWRGOOD Short Circuit Current | I _{SC} | Short to GND | | 2 | | mA |
| | | Short to V _{CCI} | | -2 | | mA |
| DYNAMIC | | | | | | |
| PWRGOOD Turn-on Delay | | From V _{CCI} crossing turn-on threshold to PWRGOOD high | | 0.7 | | ms |

Note 1: Specifications are 100% tested at $T_A = +25^\circ C$ (exceptions noted). All temperature limits are guaranteed by design.

Note 2: Guaranteed by design, not production tested.

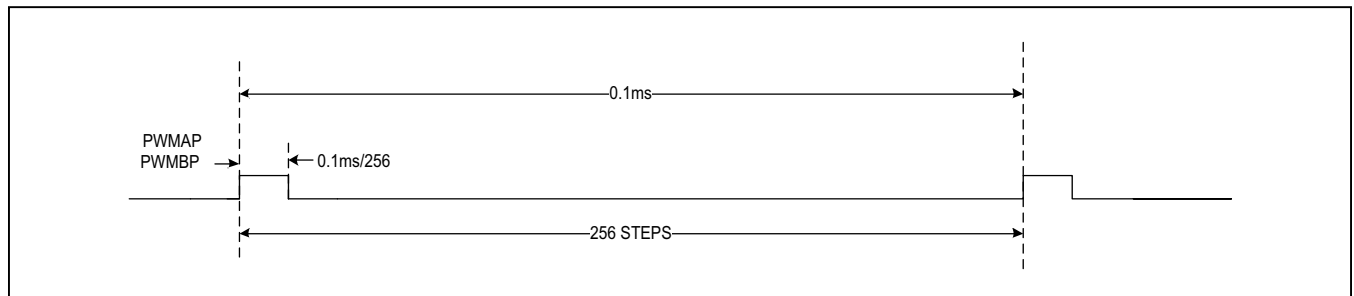
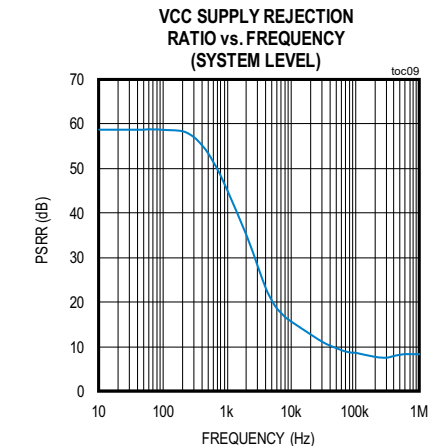
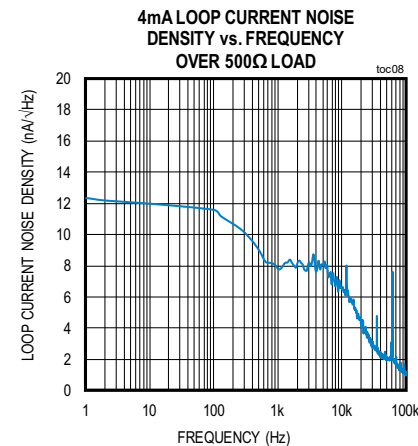
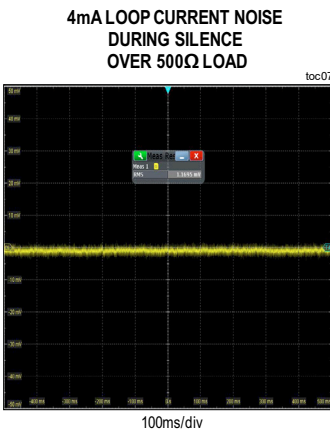
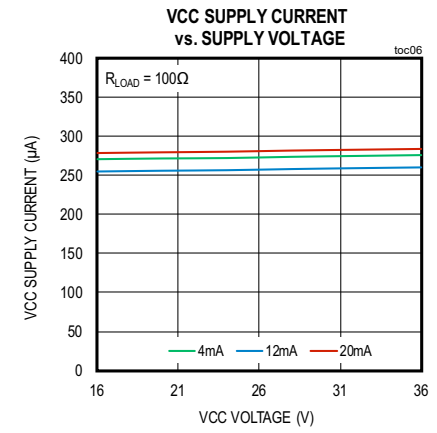
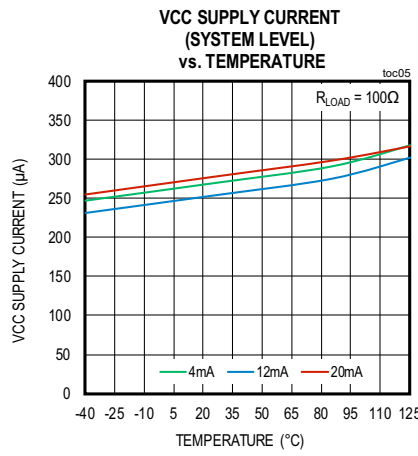
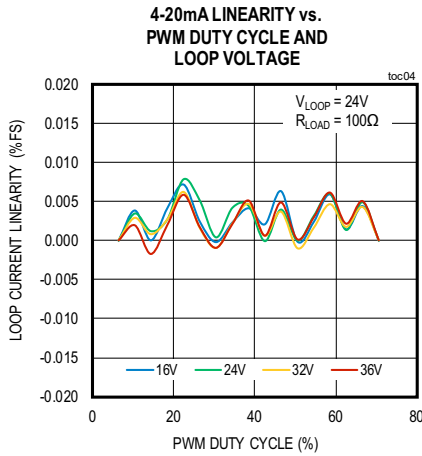
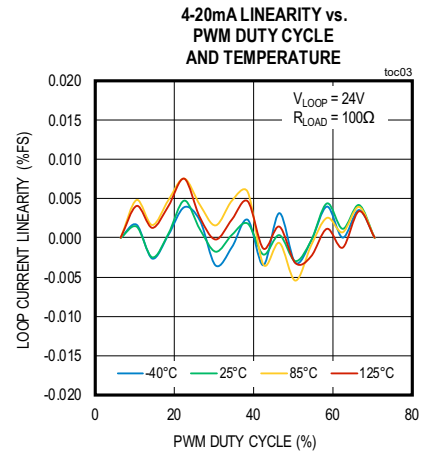
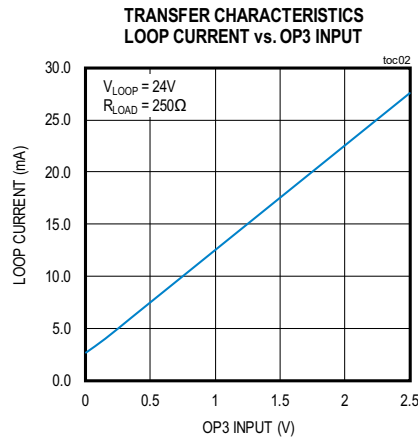
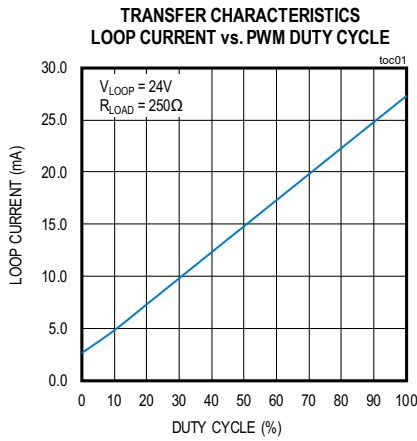


Figure 1. Typical PWM Timing Diagram

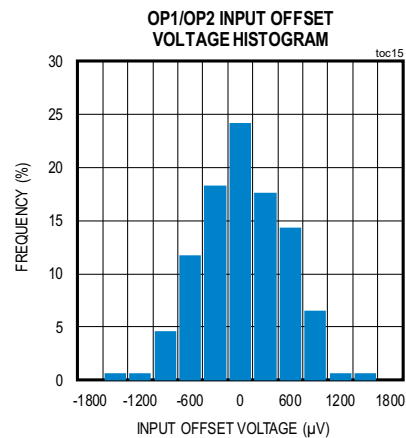
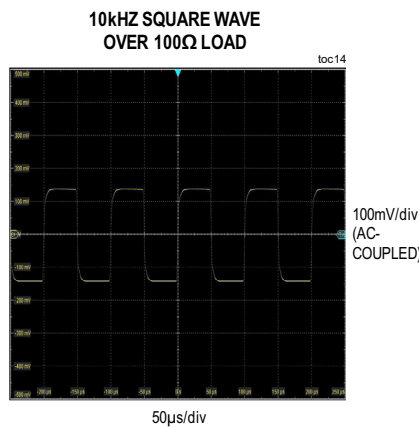
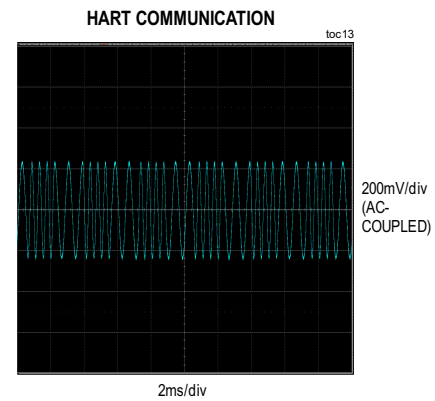
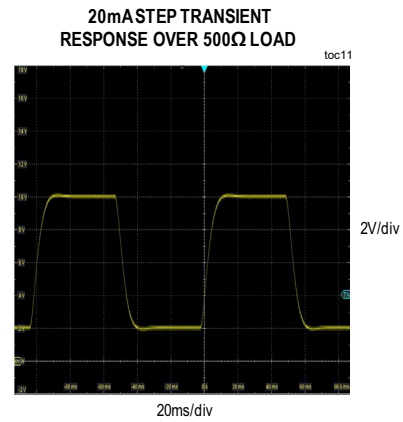
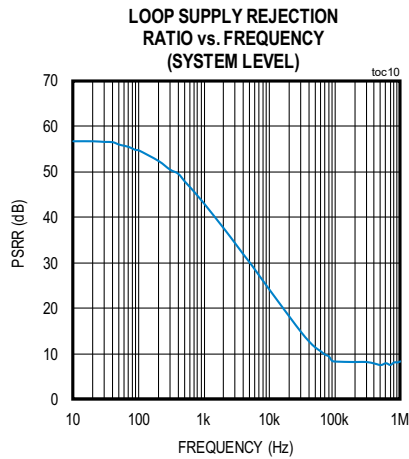
Typical Operating Characteristics

$V_{CC} = +24V$, $V_{DD} = V_{CCID} = V_{CCI} = +3.3V$, $GND = 0V$, op amp $V_{CM} = V_{OUT} = V_{CCI}/2$, op amp $C_L = 15pF$, comparator and PWM $C_L = 10pF$, LDO $C_{LOAD} = 0.32\mu F$, no resistive load on any output, $T_A = +25^\circ C$, unless otherwise noted.



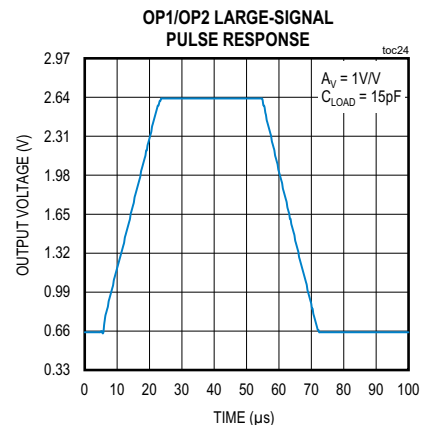
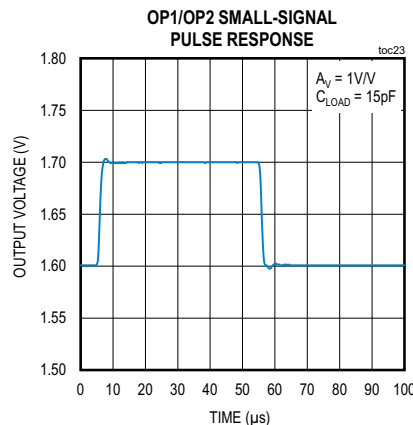
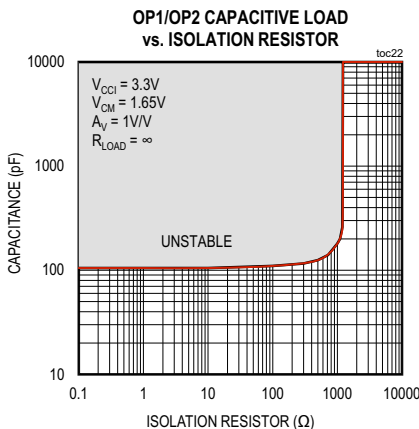
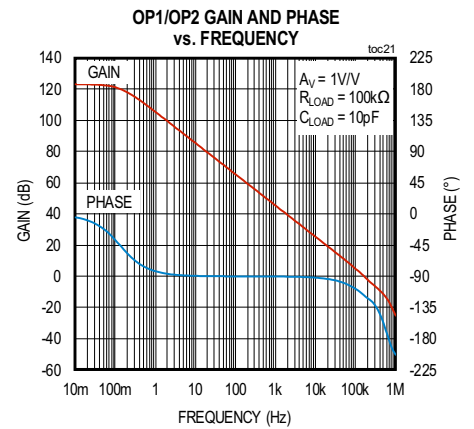
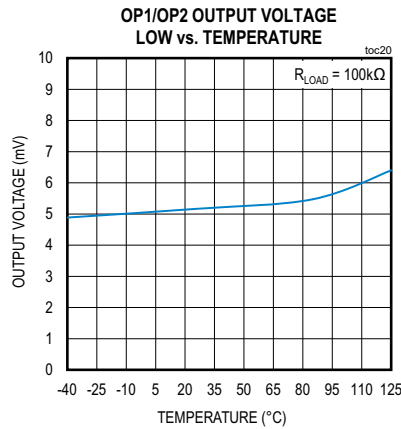
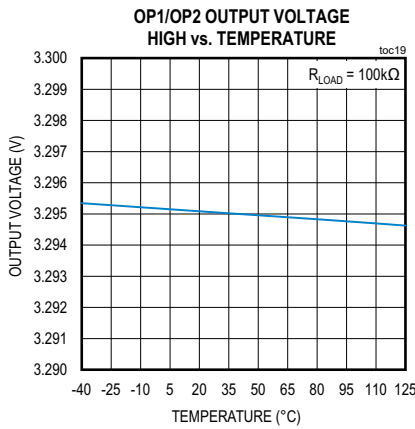
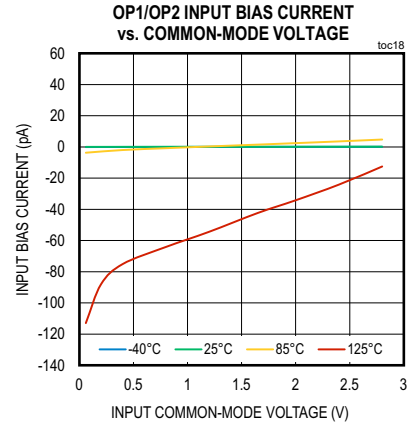
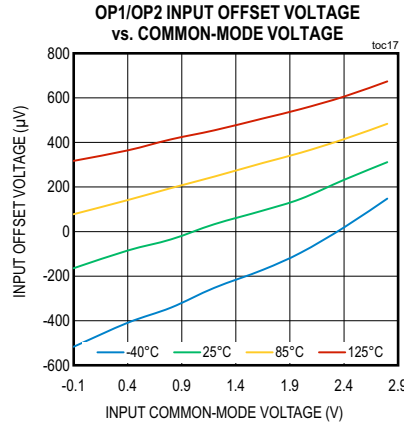
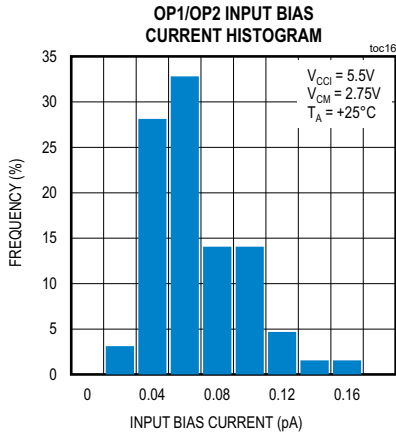
Typical Operating Characteristics (continued)

$V_{CC} = +24V$, $V_{DD} = V_{CCID} = V_{CCI} = +3.3V$, $GND = 0V$, op amp $V_{CM} = V_{OUT} = V_{CCI}/2$, op amp $C_L = 15pF$, comparator and PWM $C_L = 10pF$, LDO $C_{LOAD} = 0.32\mu F$, no resistive load on any output, $T_A = +25^\circ C$, unless otherwise noted.



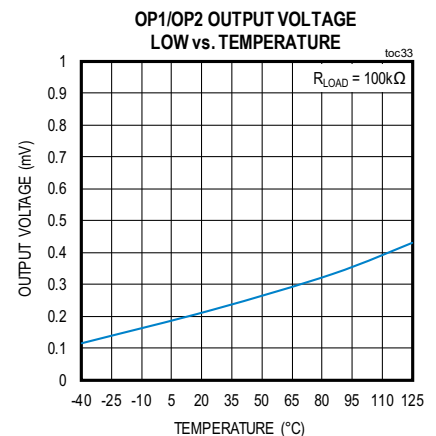
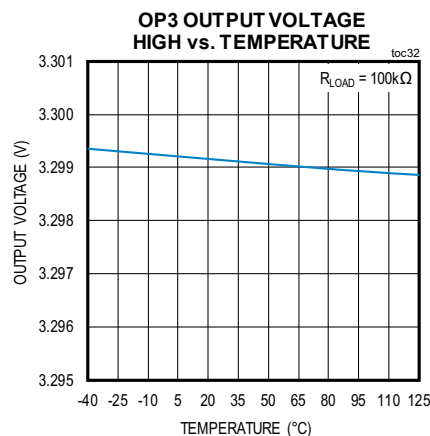
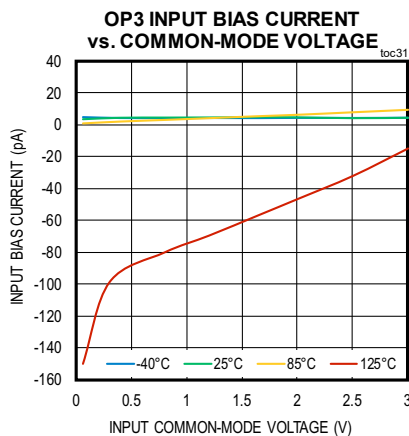
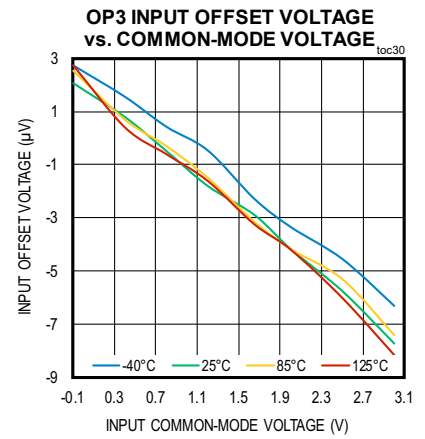
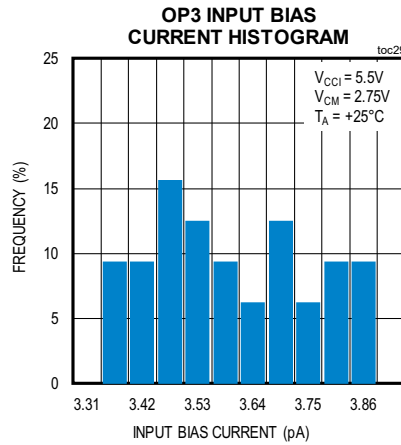
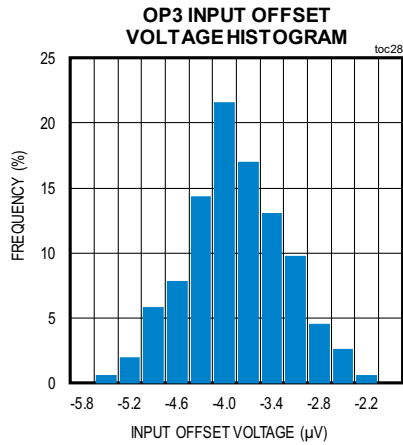
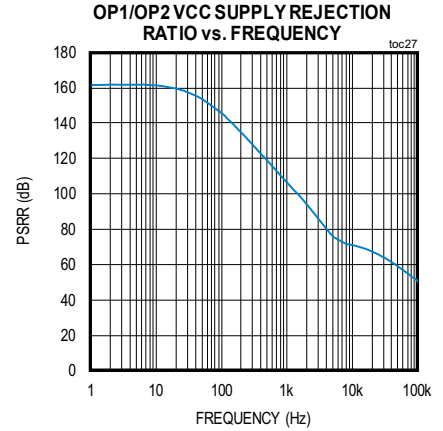
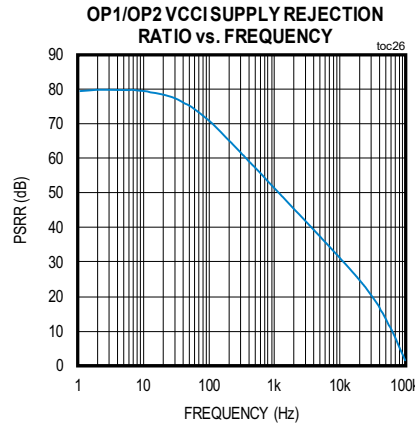
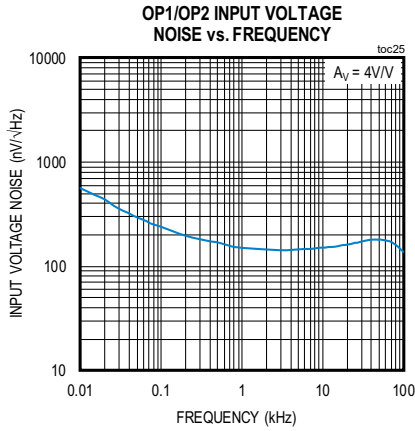
Typical Operating Characteristics (continued)

$V_{CC} = +24V$, $V_{DD} = V_{CCID} = V_{CCI} = +3.3V$, $GND = 0V$, op amp $V_{CM} = V_{OUT} = V_{CCI}/2$, op amp $C_L = 15pF$, comparator and PWM $C_L = 10pF$, LDO $C_{LOAD} = 0.32\mu F$, no resistive load on any output, $T_A = +25^\circ C$, unless otherwise noted.



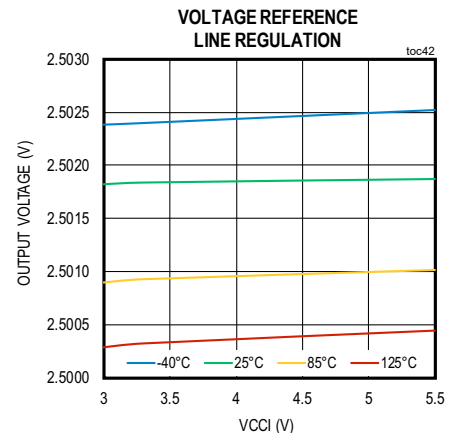
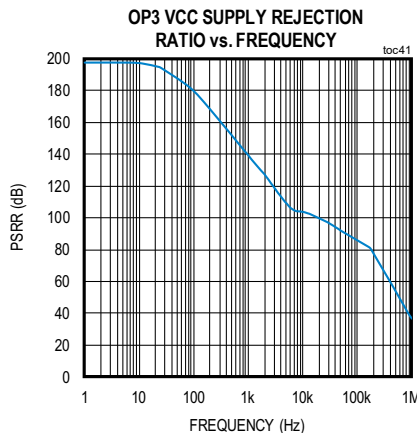
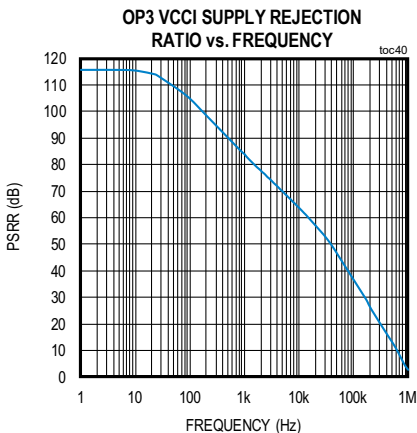
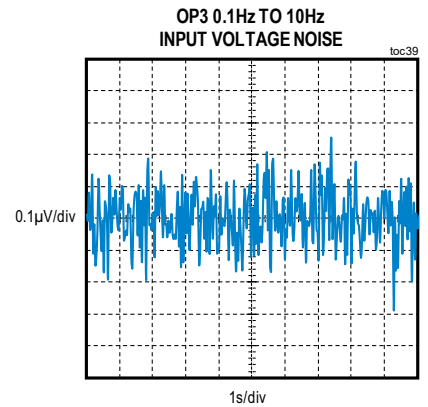
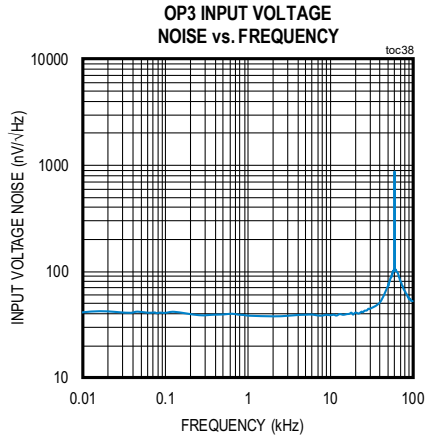
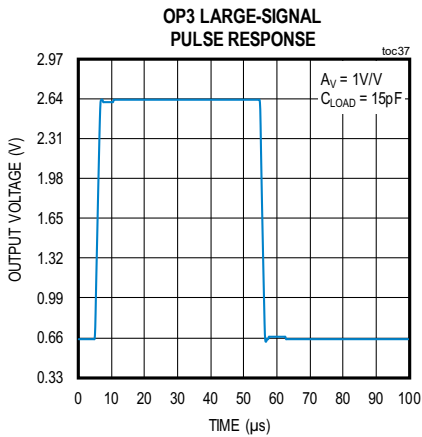
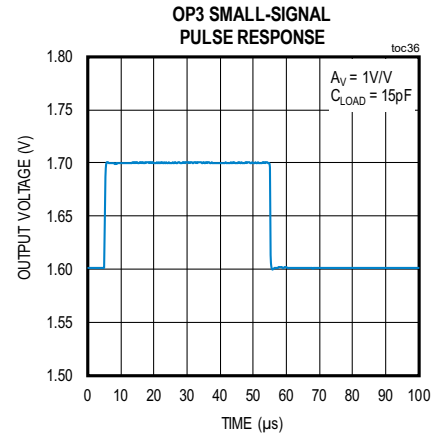
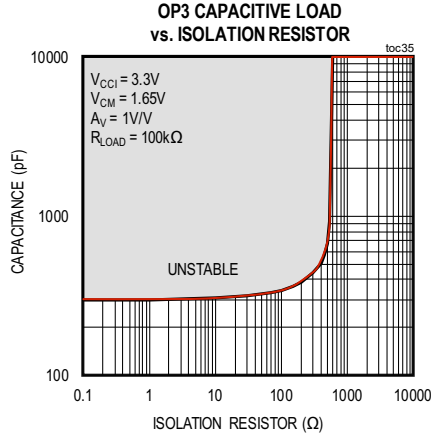
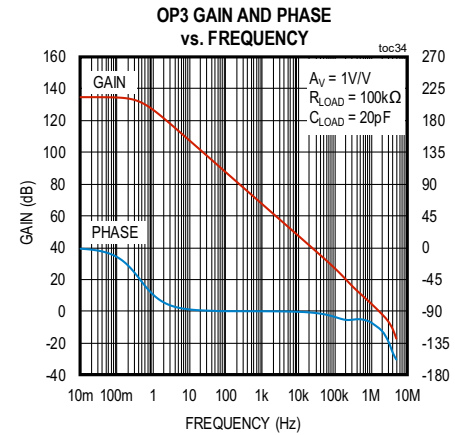
Typical Operating Characteristics (continued)

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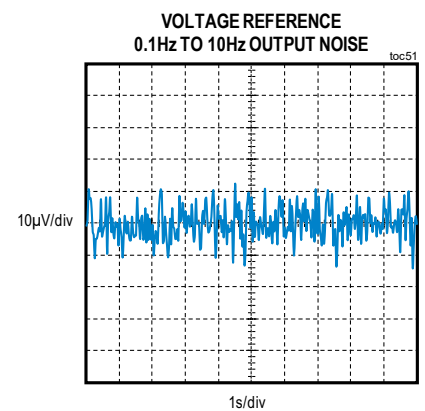
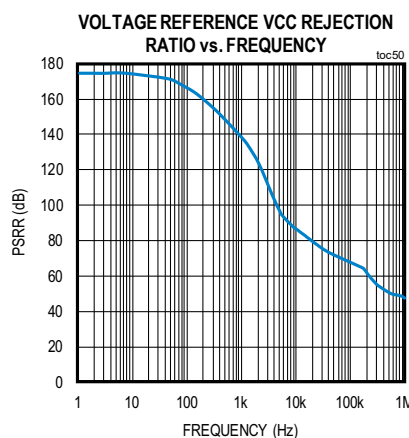
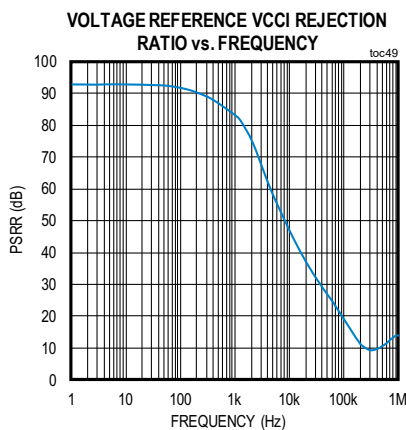
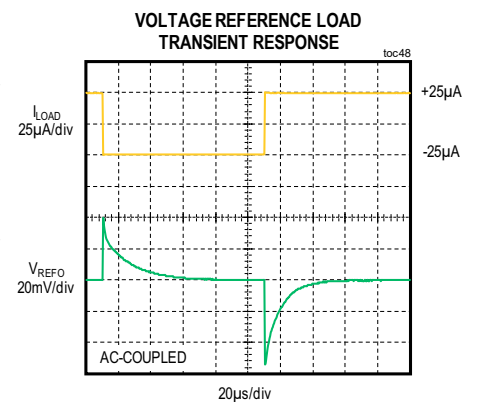
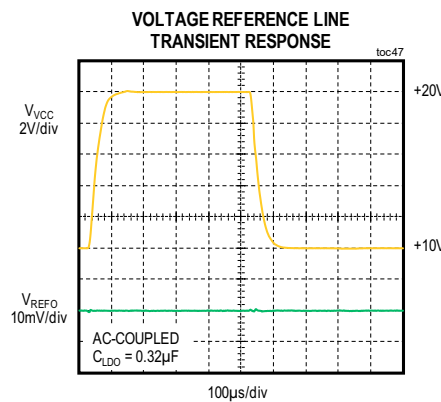
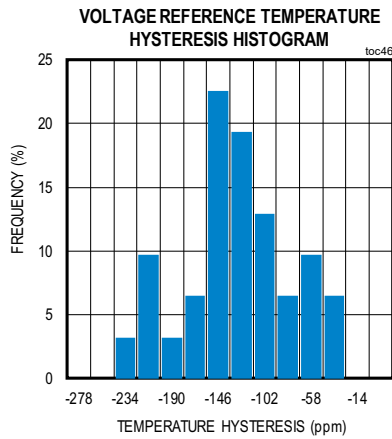
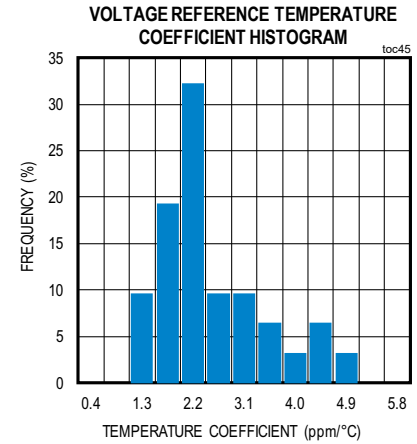
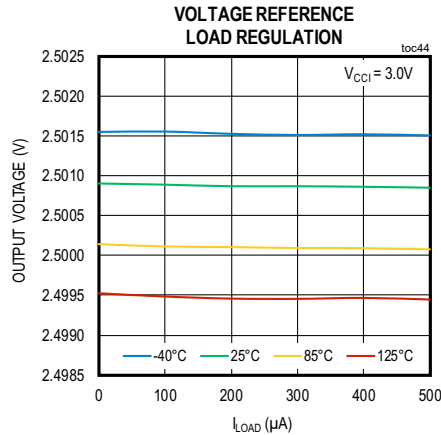
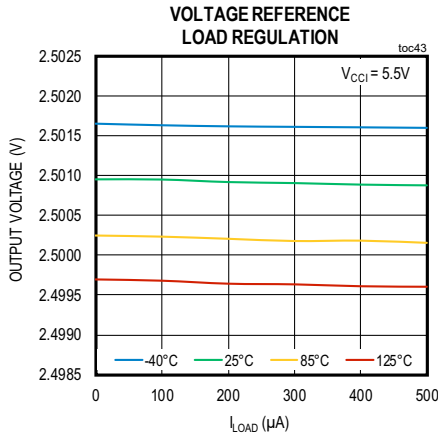
Typical Operating Characteristics (continued)

$V_{CC} = +24V$, $V_{DD} = V_{CCID} = V_{CCI} = +3.3V$, $GND = 0V$, op amp $V_{CM} = V_{OUT} = V_{CCI}/2$, op amp $C_L = 15pF$, comparator and PWM $C_L = 10pF$, LDO $C_{LOAD} = 0.32\mu F$, no resistive load on any output, $T_A = +25^\circ C$, unless otherwise noted.



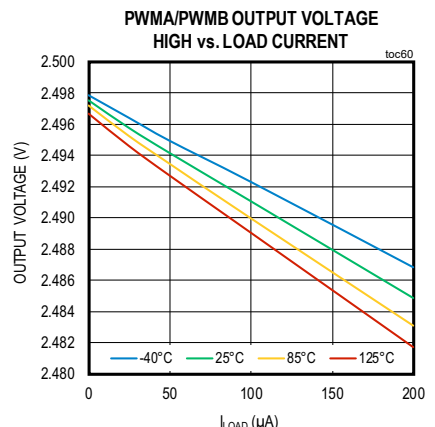
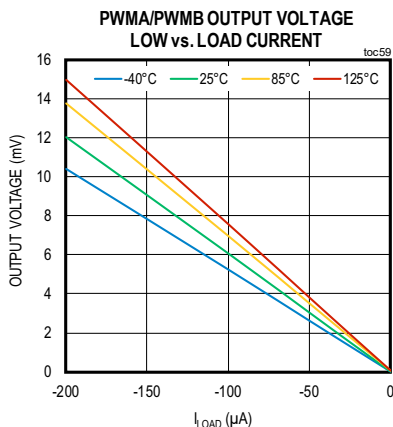
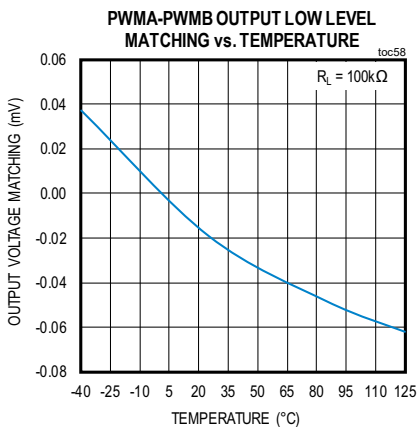
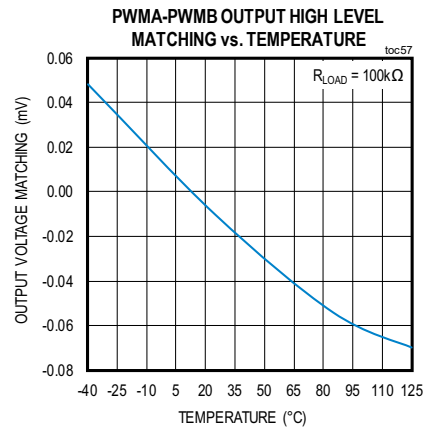
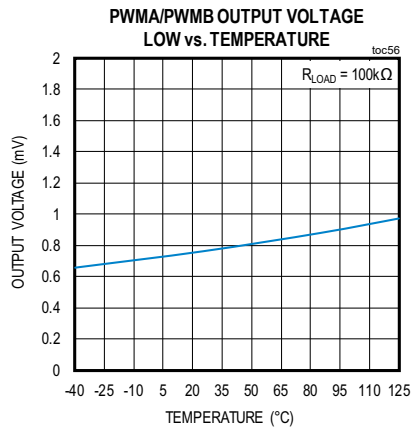
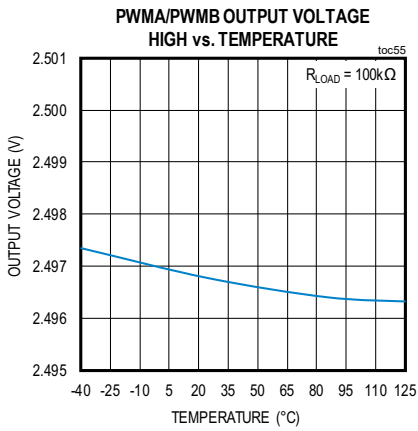
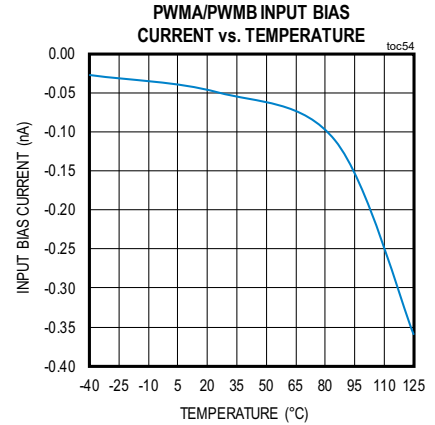
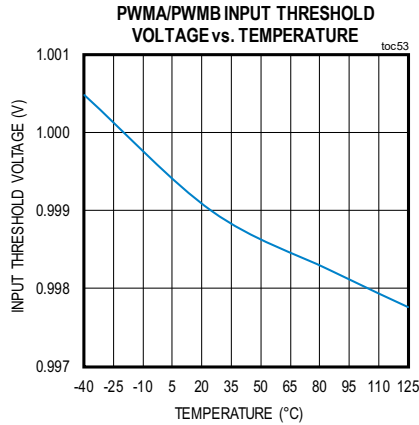
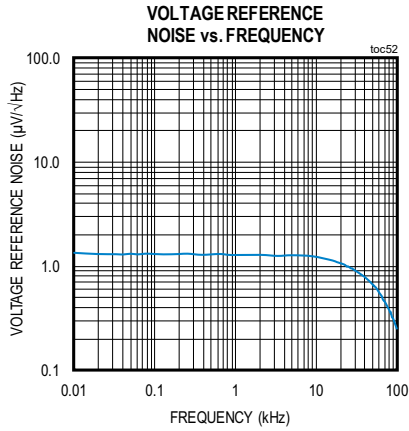
Typical Operating Characteristics (continued)

$V_{CC} = +24V$, $V_{DD} = V_{CCID} = V_{CCI} = +3.3V$, $GND = 0V$, op amp $V_{CM} = V_{OUT} = V_{CCI}/2$, op amp $C_L = 15pF$, comparator and PWM $C_L = 10pF$, LDO $C_{LOAD} = 0.32\mu F$, no resistive load on any output, $T_A = +25^\circ C$, unless otherwise noted.



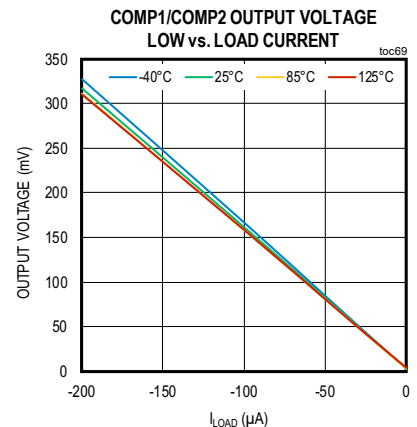
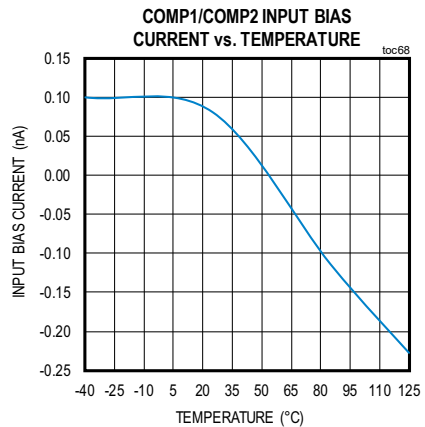
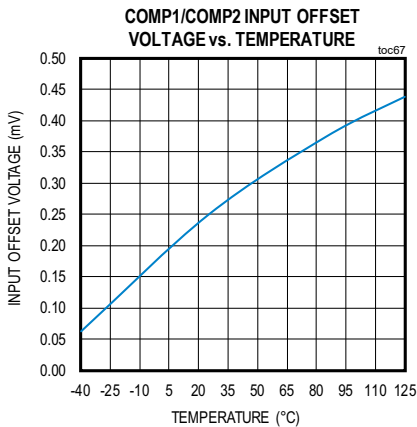
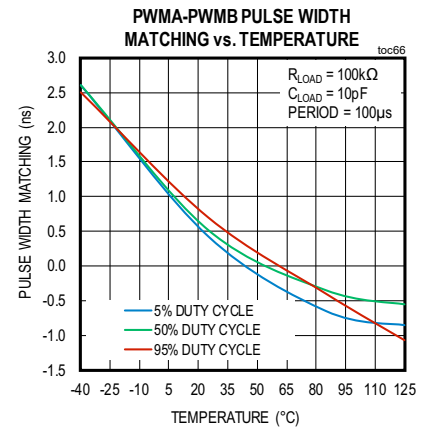
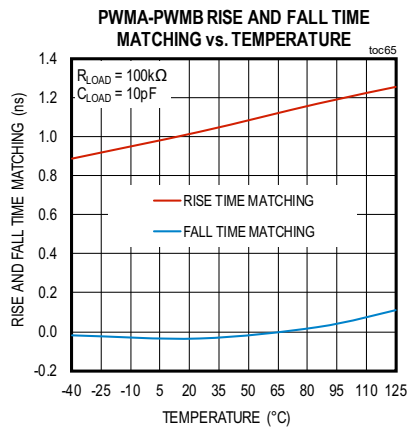
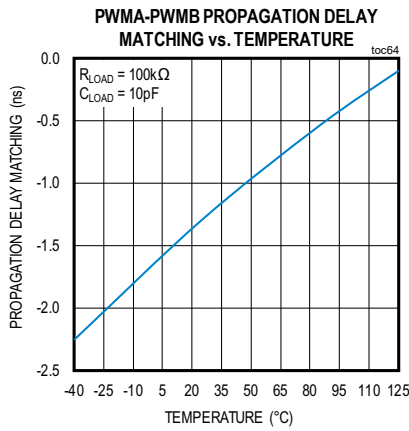
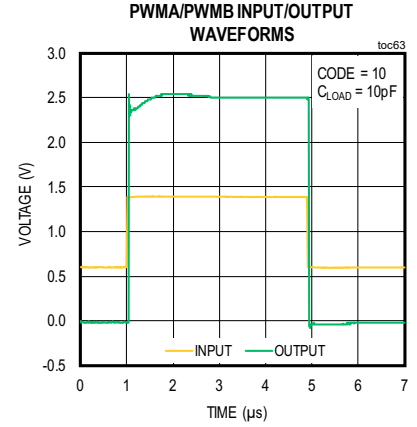
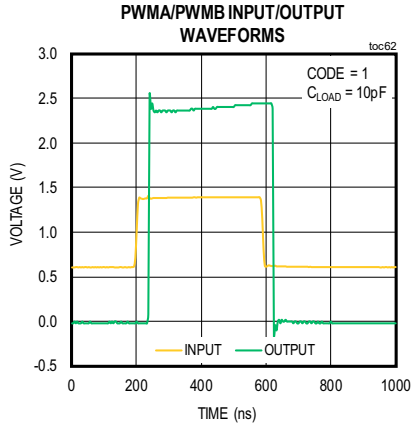
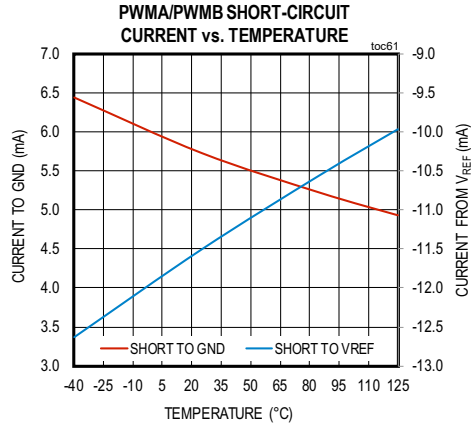
Typical Operating Characteristics (continued)

$V_{CC} = +24V$, $V_{DD} = V_{CCID} = V_{CCI} = +3.3V$, $GND = 0V$, op amp $V_{CM} = V_{OUT} = V_{CCI}/2$, op amp $C_L = 15pF$, comparator and PWM $C_L = 10pF$, LDO $C_{LOAD} = 0.32\mu F$, no resistive load on any output, $T_A = +25^\circ C$, unless otherwise noted.



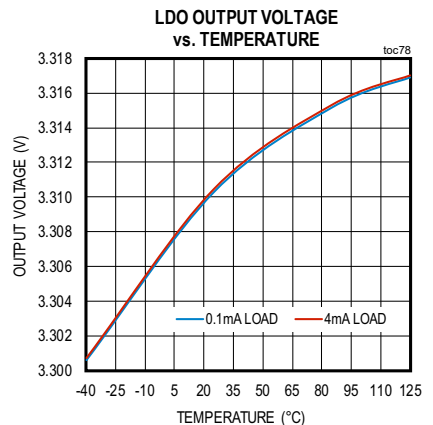
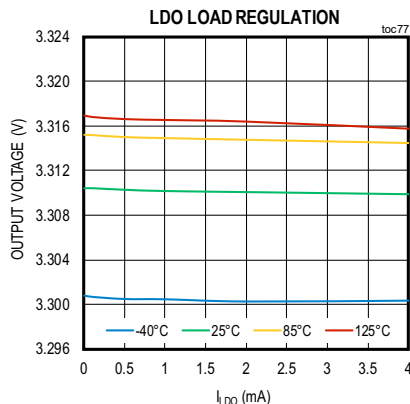
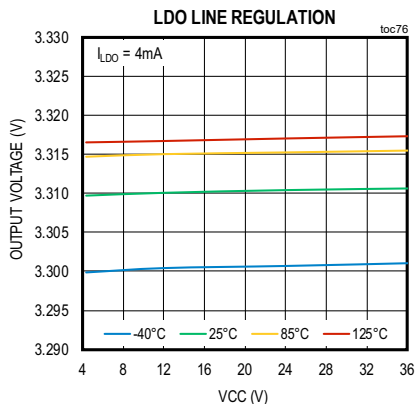
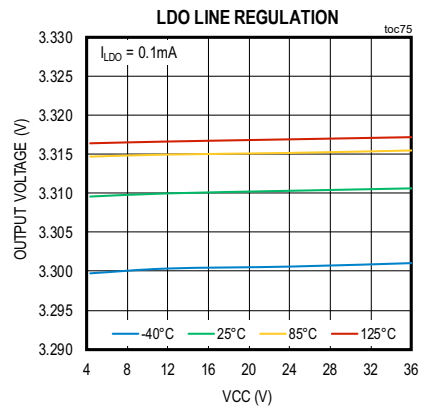
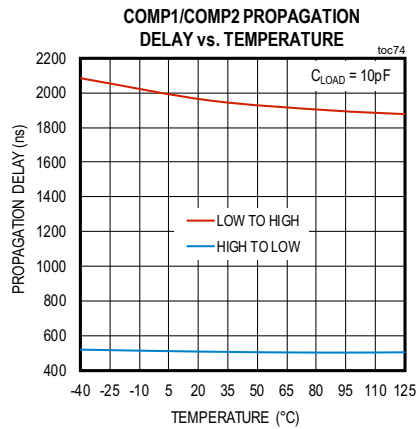
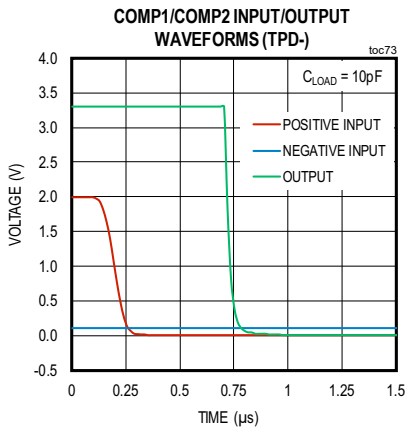
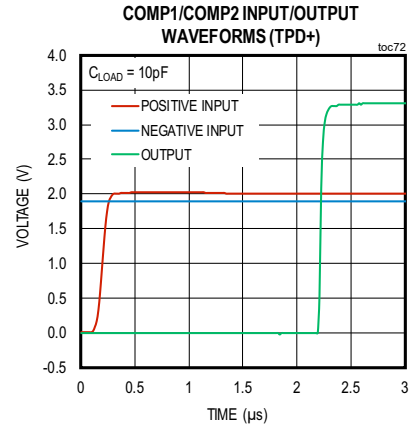
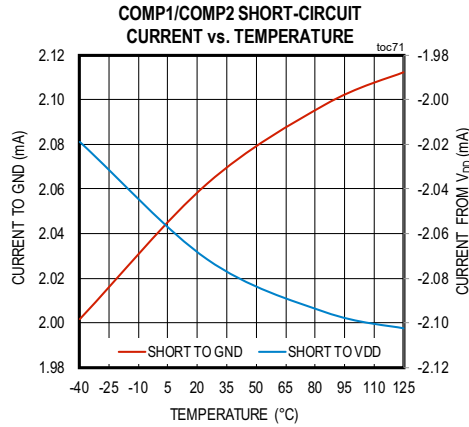
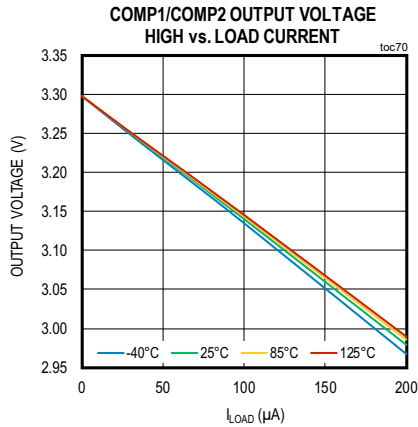
Typical Operating Characteristics (continued)

$V_{CC} = +24V$, $V_{DD} = V_{CCID} = V_{CCI} = +3.3V$, $GND = 0V$, op amp $V_{CM} = V_{OUT} = V_{CCI}/2$, op amp $C_L = 15pF$, comparator and PWM $C_L = 10pF$, LDO $C_{LOAD} = 0.32\mu F$, no resistive load on any output, $T_A = +25^\circ C$, unless otherwise noted.



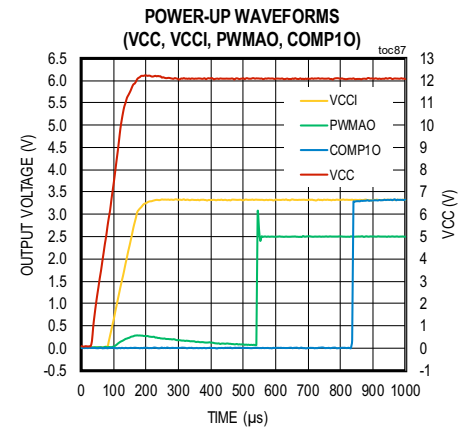
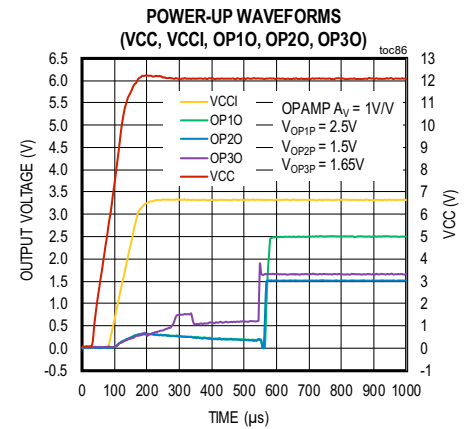
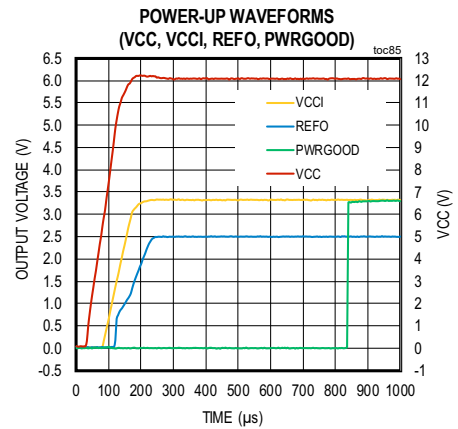
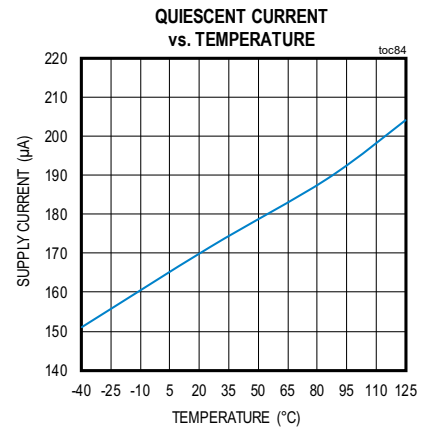
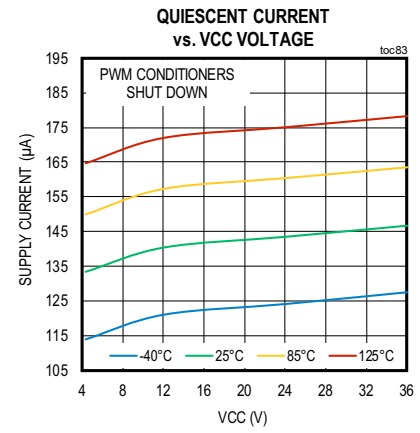
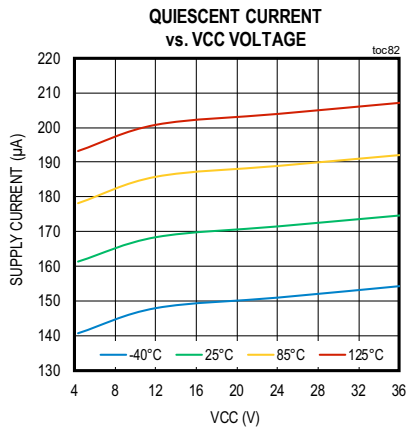
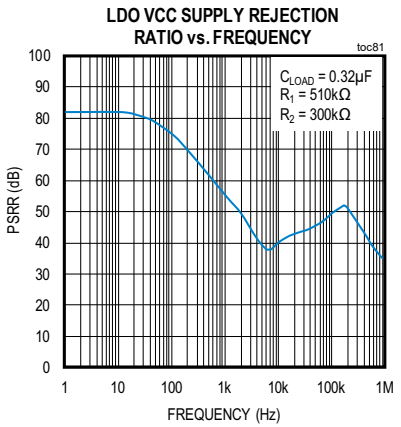
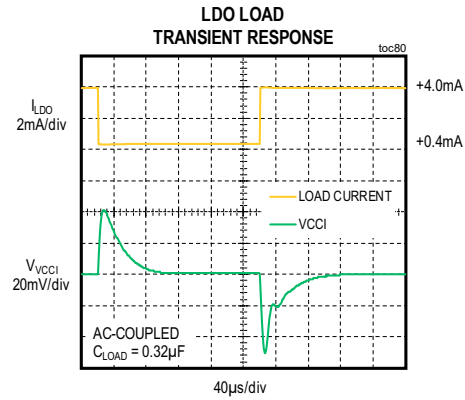
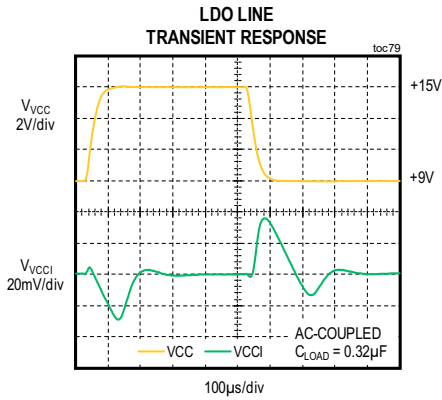
Typical Operating Characteristics (continued)

$V_{CC} = +24V$, $V_{DD} = V_{CCID} = V_{CCI} = +3.3V$, $GND = 0V$, op amp $V_{CM} = V_{OUT} = V_{CCI}/2$, op amp $C_L = 15pF$, comparator and PWM $C_L = 10pF$, LDO $C_{LOAD} = 0.32\mu F$, no resistive load on any output, $T_A = +25^\circ C$, unless otherwise noted.

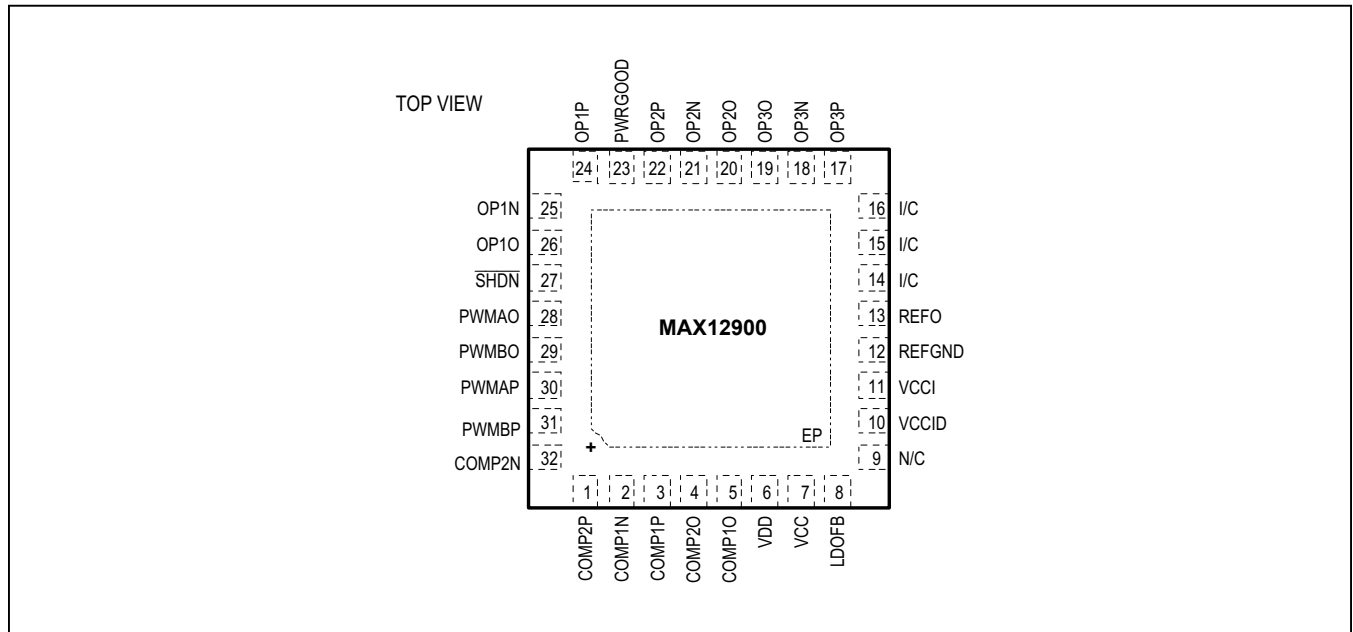


Typical Operating Characteristics (continued)

$V_{CC} = +24V$, $V_{DD} = V_{CCID} = V_{CCI} = +3.3V$, $GND = 0V$, op amp $V_{CM} = V_{OUT} = V_{CCI}/2$, op amp $C_L = 15pF$, comparator and PWM $C_L = 10pF$, LDO $C_{LOAD} = 0.32\mu F$, no resistive load on any output, $T_A = +25^\circ C$, unless otherwise noted.



Pin Configuration



Pin Description

| PIN # | NAME | DESCRIPTION |
|-------|--------|--|
| 1 | COMP2P | Comparator 2 noninverting input |
| 2 | COMP1N | Comparator 1 inverting input |
| 3 | COMP1P | Comparator 1 noninverting input |
| 4 | COMP2O | Comparator 2 output |
| 5 | COMP1O | Comparator 1 output |
| 6 | VDD | Comparator Output Supply Voltage. Add a 0.1µF bypass cap from VDD to GND. |
| 7 | VCC | Positive Supply Voltage at Internal LDO Input. Add a 1µF bypass cap from VCC to GND. |
| 8 | LDOFB | LDO feedback voltage. Connect to resistor divider between VCCI and GND. |
| 9 | N/C | Not connected |
| 10 | VCCID | Digital power input. Connect this pin to VCCI. |
| 11 | VCCI | LDO output. Add a 0.22µF bypass cap from VCCI to GND. |
| 12 | REFGND | Internal reference ground. Connect to GND. |
| 13 | REFO | Internal reference output. |
| 14 | I/C | Internally connected pin. Connect this pin to GND. |
| 15 | I/C | Internally connected pin. Connect this pin to GND. |
| 16 | I/C | Internally connected pin. Connect this pin to GND. |
| 17 | OP3P | Op Amp 3 noninverting input |
| 18 | OP3N | Op Amp 3 inverting input |
| 19 | OP3O | Op Amp 3 output |
| 20 | OP2O | Op Amp 2 output |

Pin Description (continued)

| PIN # | NAME | DESCRIPTION |
|-------|--------------------------|---|
| 21 | OP2N | Op Amp 2 inverting input |
| 22 | OP2P | Op Amp 2 noninverting input |
| 23 | PWRGOOD | Active-high output signal that indicates when the MAX12900 is ready. |
| 24 | OP1P | Op Amp 1 non-inverting input |
| 25 | OP1N | Op Amp 1 inverting input |
| 26 | OP1O | Op Amp1 output |
| 27 | $\overline{\text{SHDN}}$ | Active-Low, Shutdown Input for PWM Conditioners. PWM circuitry powers down and outputs go to Hi-Z state when this pin is low. |
| 28 | PWMAO | PWM conditioner output A |
| 29 | PWMBO | PWM conditioner output B |
| 30 | PWMAP | PWM conditioner input A |
| 31 | PWMBP | PWM conditioner input B |
| 32 | COMP2N | Comparator 2 inverting input |
| EP | GND | Exposed pad, chip ground. |

Detailed Description

The MAX12900 is an ultra-low-power, highly integrated 4-20mA transmitter. The MAX12900 integrates ten building blocks in a small package: a wide supply voltage range LDO, two comparators for PWM conditioning (PWMA and PWMB), two low-drift, general purpose op amps (OP1 and OP2), one zero-drift, wide-bandwidth op amp (OP3), two diagnostic comparators (COMP1 and COMP2), a power-up sequencer with power good output, and a low-drift voltage reference. There are many ways that one can connect these building blocks to optimize overall functionality and performance of the MAX12900 for a specific application.

Power-Up Sequencer

The power-up sequencer keeps all op amp and PWM outputs at Hi-Z, and outputs of the comparators low during power-up until VCCI reaches 90% of its final value. After that, the PWRGOOD signal is asserted and all outputs become controlled by their inputs. The PWRGOOD signal is delayed by 0.7ms (typ) after VCCI reaches 90% of its final value, thus allowing for external loops controlled by the MAX12900 to stabilize before signaling that the part is ready.

Note that external components, such as a sensor or microcontroller, should not draw load current from VCCI until the PWRGOOD signal has been asserted.

PWM Conditioners

The PWM conditioners generate ground level when the input is below the threshold voltage, and generate V_{REF} when the input is above the threshold voltage. The PWM conditioners can be powered down by setting the $\overline{\text{SHDN}}$ pin low. The PWM outputs are Hi-Z during shutdown.

General Purpose Op Amps (OP1, OP2)

The general purpose op amps, OP1 and OP2, feature a low operating supply voltage, low input bias current, rail-to-rail outputs, and a maximized ratio of Gain Bandwidth Product (GBWP) to supply current. These CMOS devices feature ultra-low input bias current up to 15pA at 85°C. They are unity-gain stable with a 200kHz GBWP, driving capacitive loads up to 100pF. The input common mode voltage range can extend 100mV below ground with excellent common-mode rejection. The OP1 and OP2 op amps can drive the output to within 25mV of both supply rails with a 100kΩ load. Op amp settling time depends primarily on the output voltage and is slew-rate limited.

The general-purpose op amps can be used as PWM filters, linear filters/amplifiers, or as linear or shunt regulator controllers, refer to the [Application Information](#) section.

Zero-Drift High Bandwidth Op Amp (OP3)

The zero-drift, wide bandwidth op amp OP3 uses an innovative auto-zero technique that allows precision and low noise with a minimum amount of power. The ultra-low input offset voltage, offset drift, and 1/f noise allow for building a highly accurate current transmitter. The high GBWP allows for noise suppression over a wider frequency band. The OP3 amplifier achieves rail-to-rail performance at the output.

Driving large capacitive loads can cause instability in many op amps. The OP3 amplifier is stable with capacitive loads up to 300pF. Stability with higher capacitive loads can be improved by adding an isolation resistor in series with the op amp output.

Low-Drift 2.5V Voltage Reference

The precision bandgap reference uses a proprietary curvature-correction circuit and laser-trimmed thin-film resistors, resulting in a low temperature coefficient of <math><10\text{ppm}/^\circ\text{C}</math>, and initial accuracy of better than 0.2%. The reference can sink and source up to 500 μA , making it attractive for use in low-voltage applications. It is stable for capacitive loads up to 2nF. In applications where the load can experience step changes, an output capacitor will reduce the amount of overshoot (or undershoot) and assist the circuit's transient response. The reference typically turns on and settles to within 0.1% of its final value in 220 μs .

General-Purpose Comparators

The comparators COMP1 and COMP2 feature a 2 μs propagation delay. Two independent rails supply each comparator. The input stage operates with V_{CCI} from 3.0V to 5.5V, and the output drivers operate with VDD from 1.8V to 3.6V. This allows for a direct connection to a microcontroller. The internal output driver allows for rail-to-rail output swings with up to 100 μA load. Both comparators offer a push-pull output that sinks and sources current.

The input common-mode voltage range for these devices extends from 0V to $V_{\text{CCI}} - 1.3\text{V}$. The MAX12900's comparators can operate at any differential input voltage within these limits. Input bias current is typically less than 1nA.

These comparators can be used for VCC, VDD or VREF voltage monitoring or other diagnostic functions, providing status information to the microcontroller.

LDO

All components of the MAX12900 are powered from an integrated LDO that generates a 3.0V to 5.5V V_{CCI} voltage from an input VCC voltage of 4.0V to 36V. The LDO provides a clean supply for sensitive analog circuitry. The output of the LDO is set by external resistors and can be selected using the following equation:

$$V_{\text{OUT}} = 1.212\text{V} \times (1 + R1/R2)$$

Where, 1.212V is an internal reference voltage, R1 and R2 form a resistor divider providing feedback voltage to close the LDO loop, refer to the typical application diagrams. It is recommended that R2 be less than or equal to 470k Ω . For example, for $V_{\text{CCI}} = 3.3\text{V}$, R1 = 698k and R2 = 402k can be used from standard 1% E96 resistor series values.

Application Information

Loop-Powered 4-20mA Sensor Transmitter with PWM inputs

One of the possible implementations of a loop powered 4-20mA sensor transmitter is shown in [Figure 2](#). In this application diagram, the PWM inputs from a microcontroller are reshaped by the conditioners, filtered by the OP1 op amp and converted to an analog voltage. The voltage is then converted to a 4-20mA loop current by OP3, an external transistor Q1 and a current sense resistor R_{SENSE} .

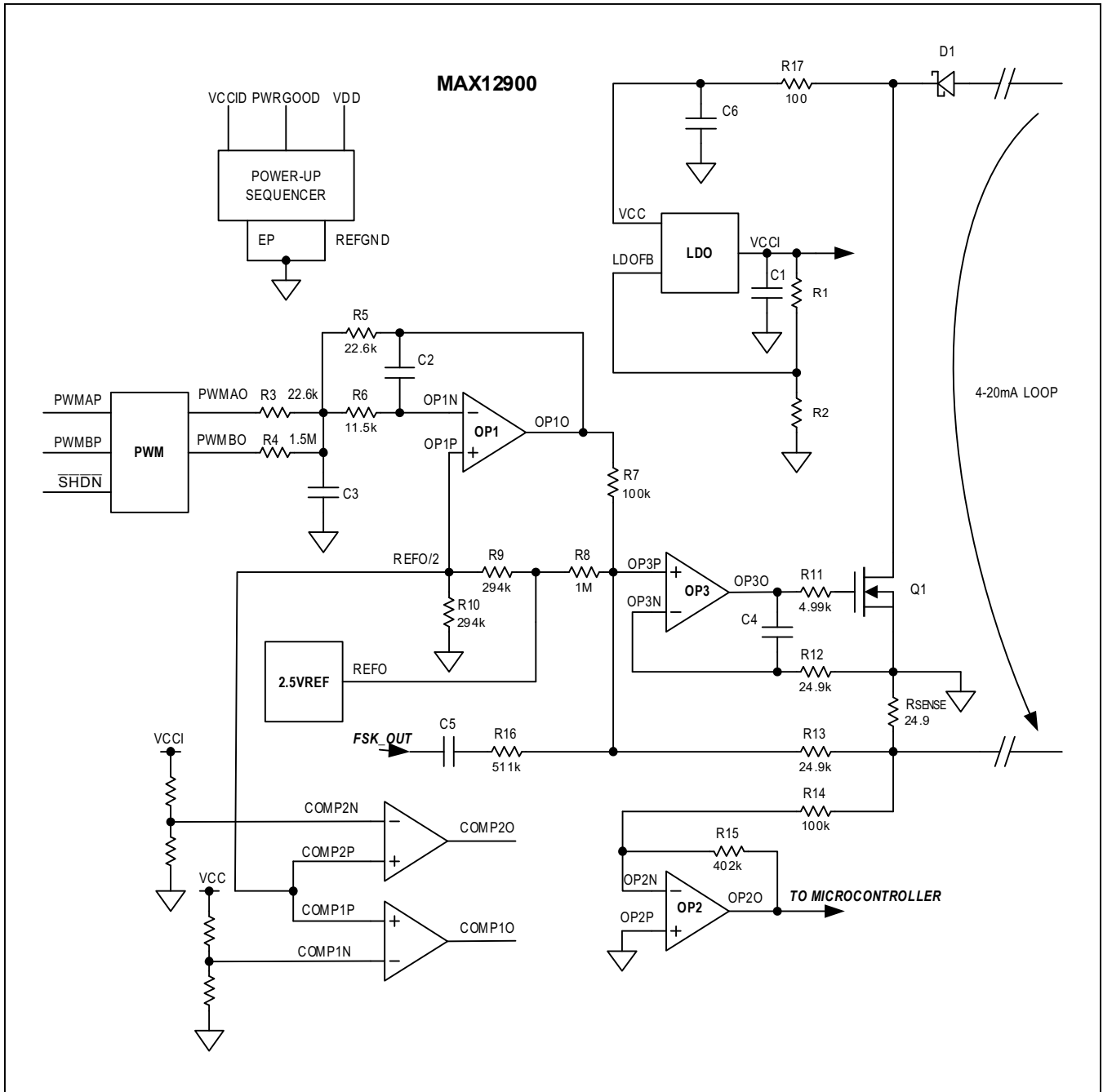


Figure 2. Loop-Powered 4-20mA Transmitter with Two PWM Inputs

The component selection of this circuit is as follows.

Let us assume the loop current range is 2.5mA to 27.5mA including NAMUR burnout detection. With the 24.9Ω R_{SENSE} resistor and the 2.5mA to 27.5mA loop current range, the non-inverting input of OP3 (OP3P) should be in the range 62.25mV (2.5mA x 24.9Ω = 62.25mV) to 684.75mV (27.5mA x 24.9Ω = 684.75mV).

The loop current (I_{loop}) has two components: offset current generated by the reference output (I_{offset}) and PWM signals converted to current (I_{PWMA}, I_{PWMB}).

$$I_{\text{loop}} = I_{\text{offset}} + I_{\text{PWMA}} + I_{\text{PWMB}}$$

After power-up, assuming the PWM signals do not contribute to the loop current, the initial 2.5mA offset current is generated by the reference voltage as follows:

$$I_{\text{offset}} = \frac{\text{REFO} \times R13}{R8 \times R_{\text{SENSE}}}$$

The PWM currents are given by

$$I_{\text{PWMA}} = \frac{\text{PWMADC} \times \text{REFO} \times \left(\frac{R5}{R3}\right) \times R13}{R7 \times R_{\text{SENSE}}}$$

$$I_{\text{PWMB}} = \frac{\text{PWMBDC} \times \text{REFO} \times \left(\frac{R5}{R4}\right) \times R13}{R7 \times R_{\text{SENSE}}}$$

where, PWMADC and PWMBDC are the PWM duty cycles.

DAC Implementation with PWM and Low-Pass Filter

The sensor data received from the microcontroller can be arranged into a coarse and a fine PWM signal.

Both the coarse and fine signals can have up to 8 bits of resolution. The PWM signals are then converted to their voltage level representations via a LPF. The PWM outputs from the MAX12900 connect to the LPF through two gain setting resistors with ratios up to 1:256; the voltage levels at the output of the LPF are proportional to the PWM duty cycles.

The application diagram in [Figure 2](#) shows an implementation of a 14-bit resolution signal path. The PWMAP input receives the coarse signal with 8-bits of resolution, and the PWMBP input receives the fine signal with 6-bits of resolution. A 1:66 ratio is used for the two gain setting resistors.

The coarse gain is set to 1 by using a 22.6kΩ gain resistor R3 and a 22.6kΩ feedback resistor R5, while the fine gain is set to 1/66 by using a 1.5MΩ gain resistor R4. The two PWM outputs are summed via the 22.6kΩ feedback resistor R5 of OP1.

The PWM frequency and filter parameters must satisfy the 4–20mA current loop noise requirements. In this example, the PWM frequency is 10kHz and the 4–20mA transmitter is designed to meet the HART specification. Consequently, the broadband noise of the current loop during silence must be below 138mV_{RMS}, and the in-band noise (500Hz–10kHz) must be below 2.2mV_{RMS} across a 500Ω loop load. In order to reduce the noise level to 2.2mV_{RMS} in-band, the LPF should suppress the noise by more than 60dB (2.5V/2.2mV = 1136.4 or 61dB). Therefore, the cut-off frequency of the LPF should be less than 70Hz with a 40dB/decade roll-off slope. OP1 implements a second-order multi-feedback LPF.

Voltage-Controlled Current Source

The integrated OP3 op amp can be combined with an external current modulating transistor Q1 to implement a precision voltage controlled current source. Q1 can be either an N-MOSFET or a bipolar NPN transistor and needs to satisfy the peak voltage and power dissipation criteria of the current loop. OP3 and Q1, in combination with a few external components, provide an optimal point to compensate the current loop.

Loop Current Diagnostic

In the application example of [Figure 2](#), the second general purpose amplifier (OP2) is used for current diagnostics and provides feedback to the microcontroller.

Connection with a Sensor

The MAX12900 can work with any kind of sensor transmitter, even though it is designed with smart sensors in mind. A smart sensor means that it has an integrated microcontroller and the ability to provide either linear analog or PWM output. If the total current consumption of the transmitter is less than 4mA, power to the sensor and the digital VDD supply can be provided directly from the VCCI pin. If the transmitter requires more than 4mA, an external dc-dc switching converter can be used. Such

a scenario is shown in the application circuit in [Figure 3](#), where OP2 is utilized as a linear voltage regulator and the dc-dc converter powers the microcontroller and drives the VDD supply pin.

Loop Powered 4-20mA Transmitter for Explosion-Proof Devices

If the sensor is to be deployed in hazardous or explosive areas, it must use additional protective components to limit the electrical energy from short circuit or failure conditions, and to prevent sparks that could cause an explosive atmosphere to ignite.

[Figure 4](#) shows an application circuit with improved protection in hazardous environments. In order to limit the electrical energy that goes to the sensor transmitter, an additional Q2 transistor and Zener diodes are added. Typically, a Zener diode should have a clamping voltage from 5V to 12V. In this case, both Q1 and Q2 transistors are the current modulating elements of the circuit. The total 4-20mA loop current is the sum of the current flowing through the Zener diodes, the Q1 transistor and the sensor. Each current path is protected by limiting resistors. Most of the power dissipation is spread out through Q1, Q2 and the Zener diodes, which makes the system design more robust.

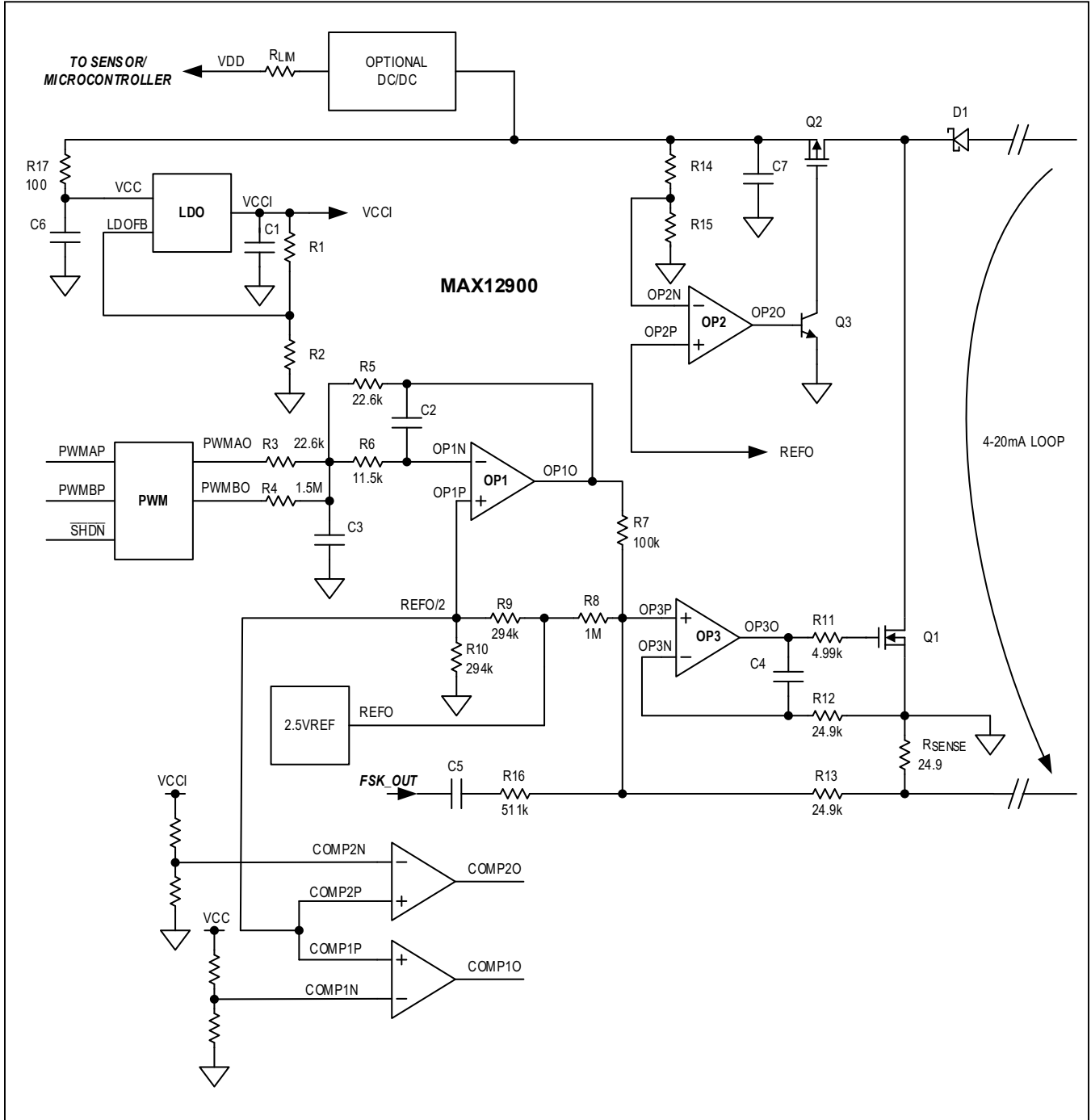


Figure 3. Loop-Powered 4-20mA Transmitter with an External Voltage Regulator

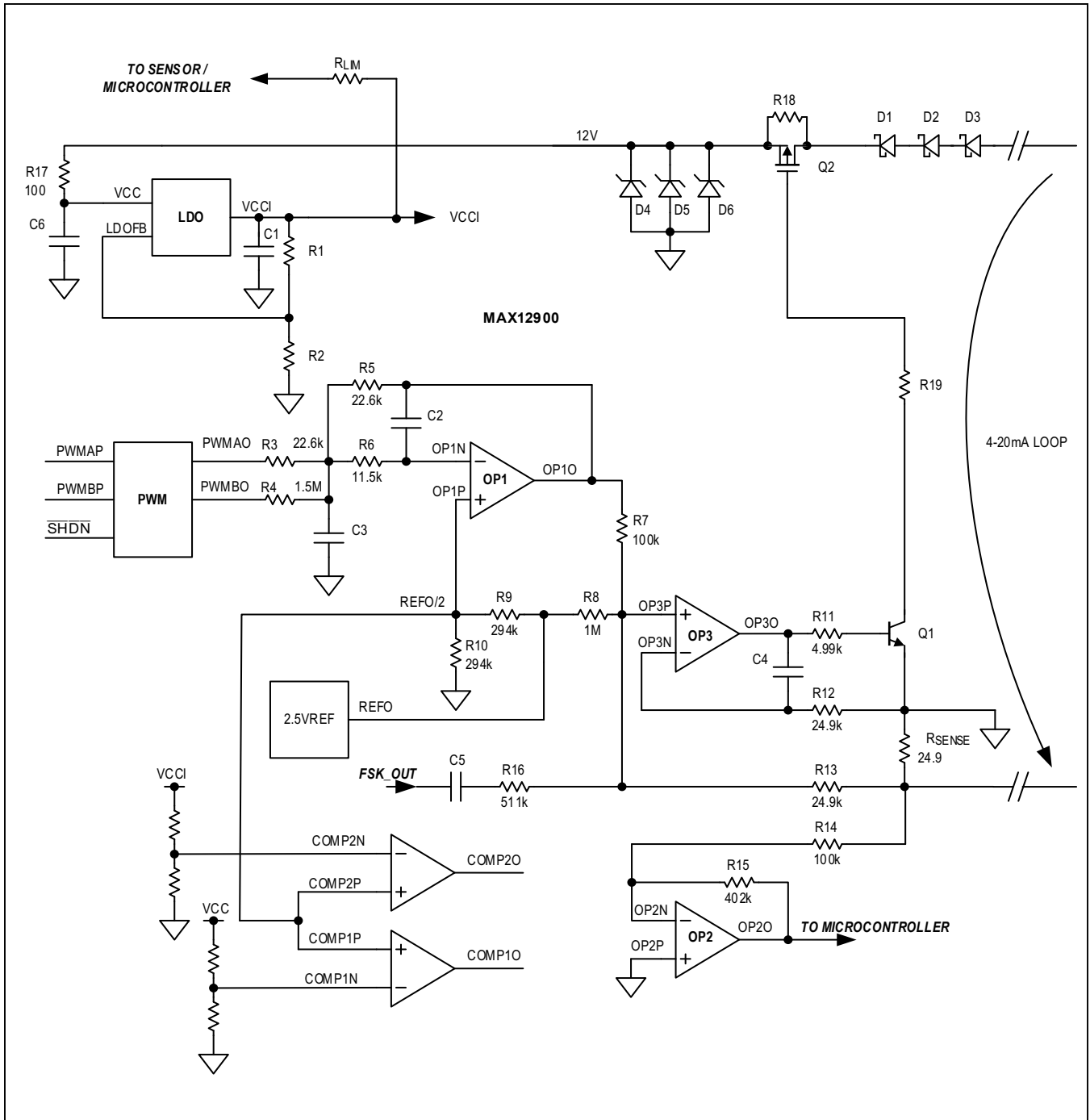


Figure 4. Loop-Powered 4-20mA Transmitter for Hazardous Environments

Ordering Information

| PART | PACKAGE | BODY SIZE | PIN PITCH | TEMP RANGE (°C) |
|----------------|---------|-----------|-----------|-----------------|
| MAX12900AATJ+ | TQFN32 | 5mm x 5mm | 0.5mm | -40 to +125 |
| MAX12900AATJ+T | TQFN32 | 5mm x 5mm | 0.5mm | -40 to +125 |

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and Reel

Chip Information

PROCESS: BiCMOS

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|-----------------------------|---------------|
| 0 | 9/17 | Initial release | — |
| 1 | 10/17 | Updated title of data sheet | 1–30 |
| 2 | 3/18 | Updated Equation 3 | 26 |

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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