19-5293; Rev 1; 3/11

EVALUATION KIT AVAILABLE

USB Host Charger Identification Analog Switches

General Description

The MAX14566E/MAX14566AE/MAX14566BE are second-generation USB devices that combine Hi-Speed USB analog switches with a USB host charger (dedicated charger) identification circuit. These devices support both the latest USB Battery Charging Specification Revision 1.2 including data contact detection and a set resistor bias for Apple-compliant devices as well as legacy USB D+/D- short detection using data line pullup. The MAX14566E has a pMOSFET open-drain control output ($\overline{CEN}$) and the MAX14566AE has an nMOSFET open-drain control output (CEN) to restart the peripheral connected to the USB host.

These devices feature high-performance Hi-Speed USB switches with low 4pF (typ) on-capacitance and low 4.0Ω (typ) on-resistance. In addition, the devices feature a single digital input (CB) to switch between pass-through mode and autodetection charger mode. The USB host charger identification circuit allows a host USB port to support USB chargers with shorted DP/DM detection and to provide support for Apple-compliant devices using a resistor bias on USB data lines. When an Apple-compliant device is attached to the port in autodetection charger mode, the devices supply the voltage to the DP and DM lines from the internal resistor-divider. If a USB Revision 1.2-compliant device is attached, the devices short DP and DM to allow correct charger detection. The MAX14566BE features an additional digital input (CB1) to allow forced charger mode.

These devices have enhanced, high electrostatic discharge (ESD) protection on the DP and DM inputs up to ±15kV Human Body Model (HBM). All the devices are available in an 8-pin (2mm x 2mm) TDFN package, and are specified over the -40°C to +85°C extended temperature range.

Features

- **Hi-Speed USB Switching**
- **Low 4.0pF (typ) On-Capacitance**
- **Low 4.0Ω (typ) On-Resistance**
- **Ultra-Low 0.1Ω (typ) On-Resistance Flatness**
- **+2.8V to +5.5V Supply Range**
- **Ultra-Low 3µA (typ) Supply Current**
- **Automatic Current-Limit Switch Control**
- **Automatic USB Charger Identification Circuit**
- **±15kV High ESD HBM Protection On DP/DM**
- **2mm x 2mm, 8-Pin TDFN Package**
- **-40°C to +85°C Operating Temperature Range**

Applications

Laptops

Netbooks

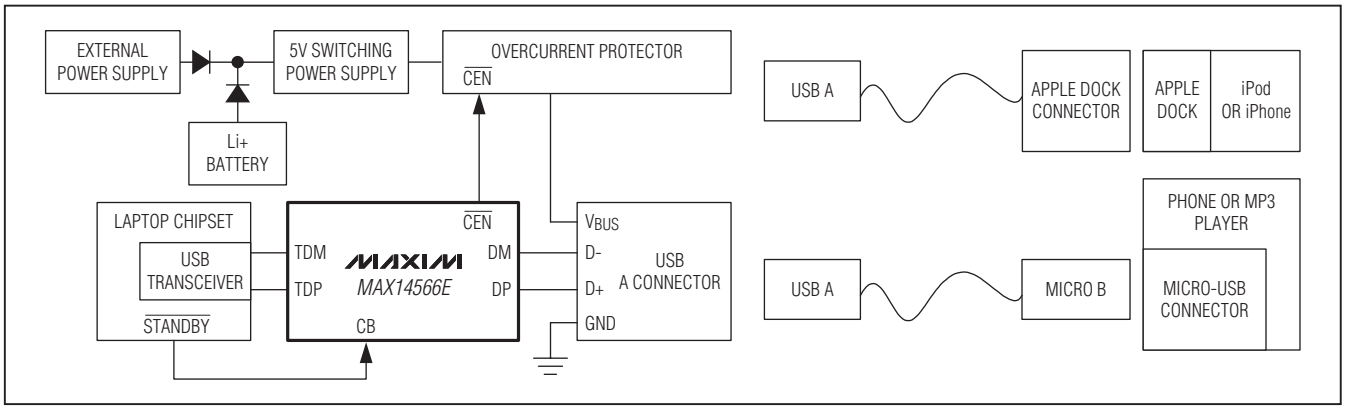
Universal Charger including iPod®/iPhone® Chargers

Ordering Information/ Selector Guide

PART	PIN-PACKAGE	CLS CONTROL	TOP MARK
MAX14566EETA+	8 TDFN-EP*	$\overline{CEN}$	ADJ
MAX14566AEETA+	8 TDFN-EP*	CEN	ADK
MAX14566BEETA+	8 TDFN-EP*	—	BMR

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Operating Circuit



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USB Host Charger Identification Analog Switches

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC}, TDP, TDM, CB, DP, DM, $\overline{CEN}$/CEN, CB1....-0.3V to +6.0V
Continuous Current into any Terminal..... ±30mA
Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 11.9mW/°C above +70°C) 954mW

Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....84°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....37°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.8V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5.0V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY (MAX14566E/MAX14566AE)							
Power-Supply Range	V_{CC}	$V_{CB} > V_{IH}$		2.8		5.5	V
		V_{CB} = 0V (Note 3)		4.75		5.25	V
Supply Current	I_{CC}	$V_{CB} = V_{CC}$	V_{CC} = 3.3V			2	µA
			V_{CC} = 5.5V			7	
		V_{CB} = 0V	V_{CC} = 4.75V		110	200	
			V_{CC} = 5.25V		120	200	
Supply Current Increase	ΔI_{CC}	$0 \le V_{CB} \le V_{IL}$ or $V_{IH} \le V_{CB} \le V_{CC}$				2	µA
POWER SUPPLY (MAX14566BE)							
Power-Supply Range	V_{CC}	$V_{CB} = V_{CC}$ and $V_{CB1} = V_{CC}$ or $V_{CB} = V_{CC}$ and V_{CB1} = 0V or V_{CB} = 0V and $V_{CB1} = V_{CC}$		2.8		5.5	V
		V_{CB} = 0V and V_{CB1} = 0V (Note 3)		4.75		5.25	V
Supply Current	I_{CC}	$V_{CB} = V_{CC}$ and $V_{CB1} = V_{CC}$ or $V_{CB} = V_{CC}$ and V_{CB1} = 0V	V_{CC} = 3.3V			2	µA
			V_{CC} = 5.5V			7	
		V_{CB} = 0V and V_{CB1} = 0V	V_{CC} = 4.75V		110	200	
			V_{CC} = 5.25V		120	200	
		V_{CB} = 0V and $V_{CB1} = V_{CC}$	V_{CC} = 5.0V for TYP V_{CC} = 5.5V for MAX		3	7	
Supply Current Increase	ΔI_{CC}	V_{CB1} = 0V; $0 \le V_{CB} \le V_{IL}$ and $V_{IH} \le V_{CB} \le V_{CC}$ (Note 4)			1		µA
		V_{CB} = 0V; $0 \le V_{CB1} \le V_{IL}$ and $V_{IH} \le V_{CB1} \le V_{CC}$ (Note 4)			1		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5.0V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG SWITCH						
Analog-Signal Range	V_{DP},V_{DM}		0		V_{CC}	V
On-Resistance TDP/TDM Switch	R_{ON}	V_{DP} = V_{DM} = 0V to V_{CC}, I_{DP} = I_{DM} = 10mA		4.0	6.5	Ω
On-Resistance Match Between Channels TDP/TDM Switch	ΔR_{ON}	V_{CC} = 5.0V, V_{DP} = V_{DM} = 400mV, I_{DP} = I_{DM} = 10mA		0.1		Ω
On-Resistance Flatness TDP/TDM Switch	R_{FLAT}	V_{CC} = 5.0V, V_{DP} = V_{DM} = 0 to V_{CC}, I_{DP} = I_{DM} = 10mA		0.1		Ω
On-Resistance of DP/DM Short	R_{SHORT}	V_{CB} = 0V, V_{DP} = 1V, I_{DP} = I_{DM} = 10mA		40	70	Ω
Off-Leakage Current	I_{TDPOFF}, I_{TDMOFF}	V_{CC} = 3.6V, V_{DP} = V_{DM} = 0.3V to 3.3V, V_{TDP} = V_{TDM} = 3.3V to 0.3V, V_{CB} = 0V	-250		+250	nA
On-Leakage Current	I_{DPON},I_{DMON}	V_{CC} = 3.6V, V_{DP} = V_{DM} = 3.3V to 0.3V, V_{CB} = V_{CC}	-250		+250	nA
DYNAMIC PERFORMANCE						
Turn-On Time	t_{ON}	V_{TDP} or V_{TDM} = 1.5V, R_L = 300Ω, C_L = 35pF, Figure 1		20	100	µs
Turn-Off Time	t_{OFF}	V_{TDP} or V_{TDM} = 1.5V, R_L = 300Ω, C_L = 35pF, Figure 1		1	5	µs
TDP, TDM Switch Propagation Delay	t_{PLH}, t_{PHL}	R_L = R_S = 50Ω		60		ps
Output Skew	$t_{SK(O)}$	Skew between DP and DM when connected to TDP and TDM, R_L = R_S = 50Ω, Figure 2		40		ps
TDP, TDM Off-Capacitance	C_{OFF}	f = 1MHz		2.0		pF
DP, DM On-Capacitance (Connected to TDP, TDM)	C_{ON}	f = 240MHz		4.0	5.5	pF
-3dB Bandwidth	BW	R_L = R_S = 50Ω (Note 4)		1000		MHz
Off-Isolation	V_{ISO}	V_{TDP}, V_{DP} = 0dBm, R_L = R_S = 50Ω, f = 250MHz, Figure 3 (Note 4)		-20		dB
Crosstalk	V_{CT}	V_{TDP}, V_{DP} = 0dBm, R_L = R_S = 50Ω, f = 250MHz, Figure 3 (Note 4)		-25		dB
INTERNAL RESISTORS						
DP/DM Short Pulldown	R_{PD}		335	500	710	kΩ
RP1/RP2 Ratio	RT_{RP}		1.485	1.5	1.515	Ratio
RP1 + RP2 Resistance	R_{RP}		95	126	176	kΩ
RM1/RM2 Ratio	RT_{RM}		0.843	0.85	0.865	Ratio
RM1 + RM2 Resistance	R_{RM}		70	94	132	kΩ
COMPARATORS						
DM1 Comparator Threshold	V_{DM1F}	DM falling	45	46	47	%V_{CC}
DM1 Comparator Hysteresis				1		%
DM2 Comparator Threshold	V_{DM2F}	DM falling	6.31	7	7.6	%V_{CC}
DM2 Comparator Hysteresis				1		%
DP Comparator Threshold	V_{DPR}	DP rising	45	46	47	%V_{CC}

USB Host Charger Identification Analog Switches

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5.0V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DP Comparator Hysteresis				1		%
LOGIC INPUT (CB, CB1)						
CB/CB1 Input Logic-High	V_{IH}		1.4			V
CB/CB1 Input Logic-Low	V_{IL}				0.4	V
CB/CB1 Input Leakage Current	I_{IN}	V_{CC} = 5.5V, 0V ≤ V_{CB} ≤ V_{IL} or V_{IH} ≤ V_{CB} ≤ V_{CC}	-1		+1	µA
$\overline{CEN}$/CEN OUTPUTS						
V_{BUS} Toggle Time (MAX14566E/ MAX14566AE)	t_{VBT}	CB = logic 0 to logic 1 or logic 1 to logic 0	0.5	1	2	s
$\overline{CEN}$ Output Logic-High Voltage		CB = logic 0 to logic 1, I_{SOURCE} = 2mA (MAX14566E only)	V_{CC} - 0.4			V
$\overline{CEN}$ Output Leakage Current		V_{CC} = 5.5V, $V_{\overline{CEN}}$ = 0V, $\overline{CEN}$ deasserted (MAX14566E only)			1	µA
CEN Output Logic-Low Voltage		CB = logic 0 to logic 1, I_{SINK} = 2mA (MAX14566AE only)			0.4	V
CEN Output Leakage Current		V_{CC} = V_{CEN} = 5.5V, CEN deasserted (MAX14566AE only)			1	µA
ESD PROTECTION						
ESD Protection Level (DP and DM Only)	V_{ESD}	HBM		±15		kV
ESD Protection Level (All Other Pins)	V_{ESD}	HBM		±2		kV

Note 2: All units are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 3: The part is operational from +2.8V to +5.5V. However, in order to have the valid Apple resistor-divider network, the V_{CC} supply must stay within the range of +4.75V to +5.25V.

Note 4: Guaranteed by design.

Test Circuits/Timing Diagrams

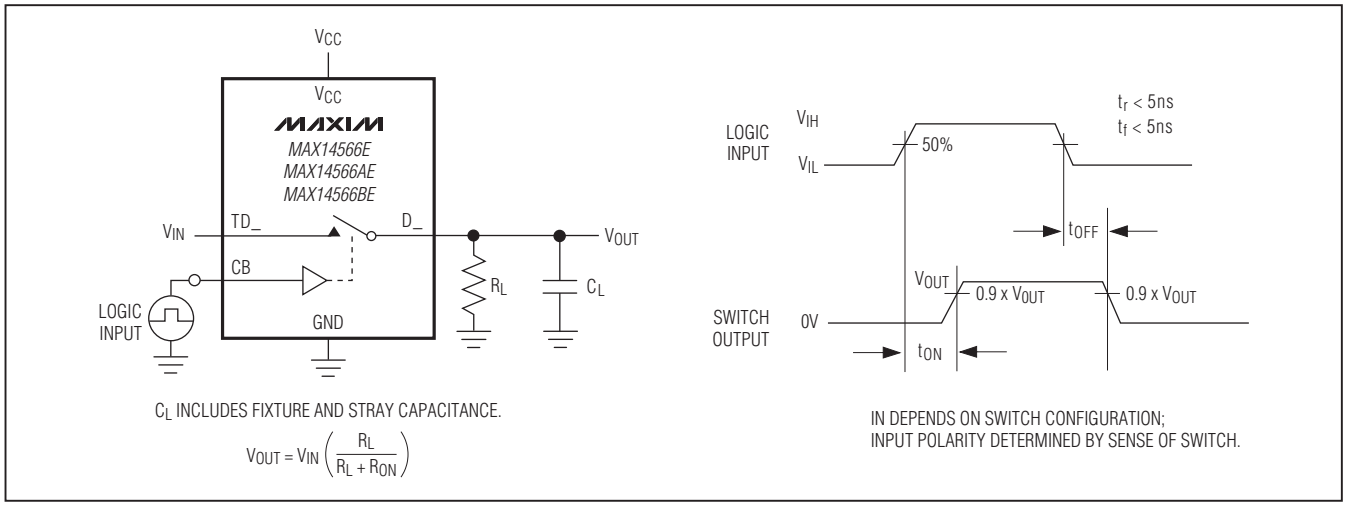


Figure 1. Switching Time

Test Circuits/Timing Diagrams (continued)

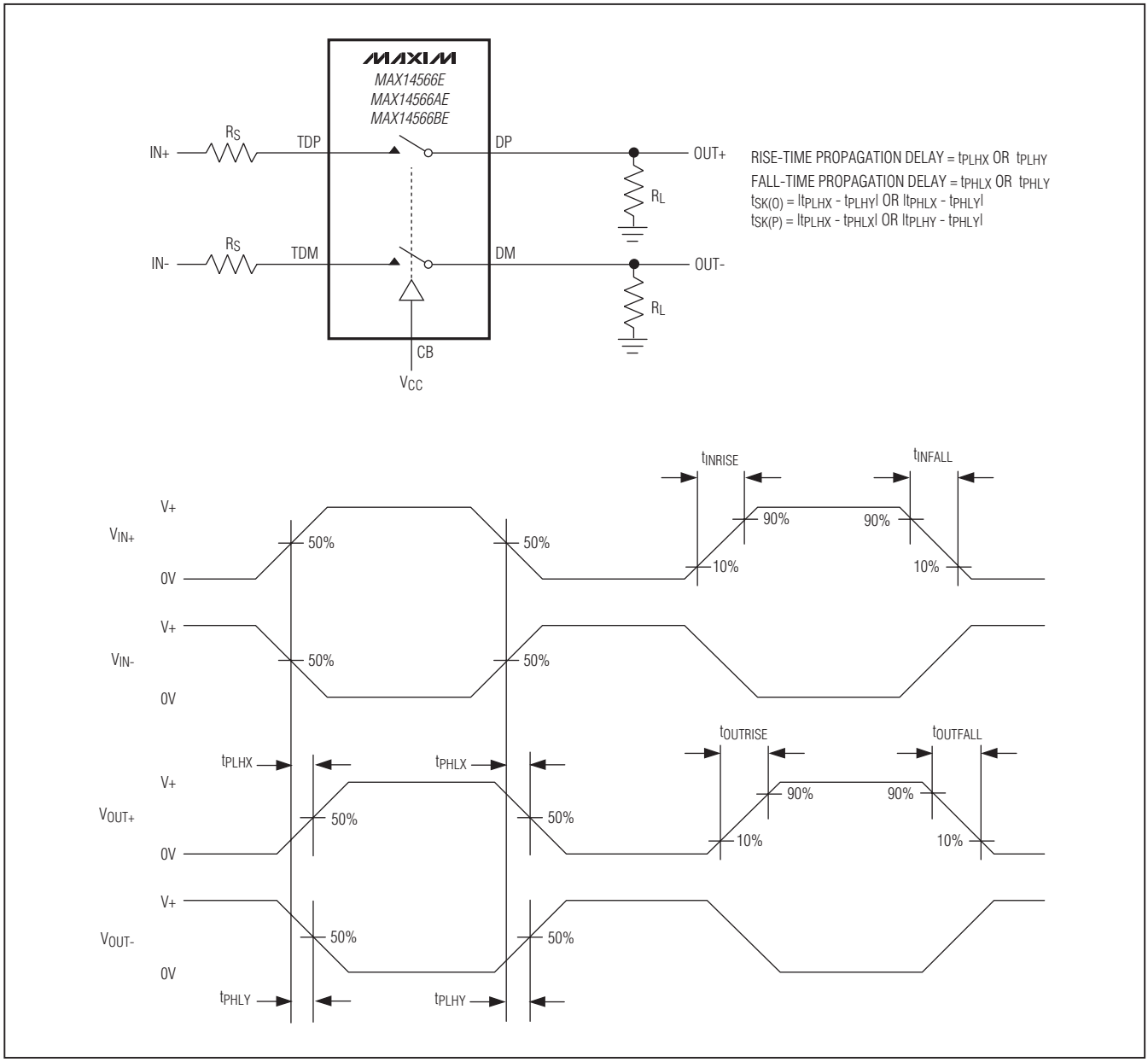


Figure 2. Output Signal Skew

USB Host Charger Identification Analog Switches

Test Circuits/Timing Diagrams (continued)

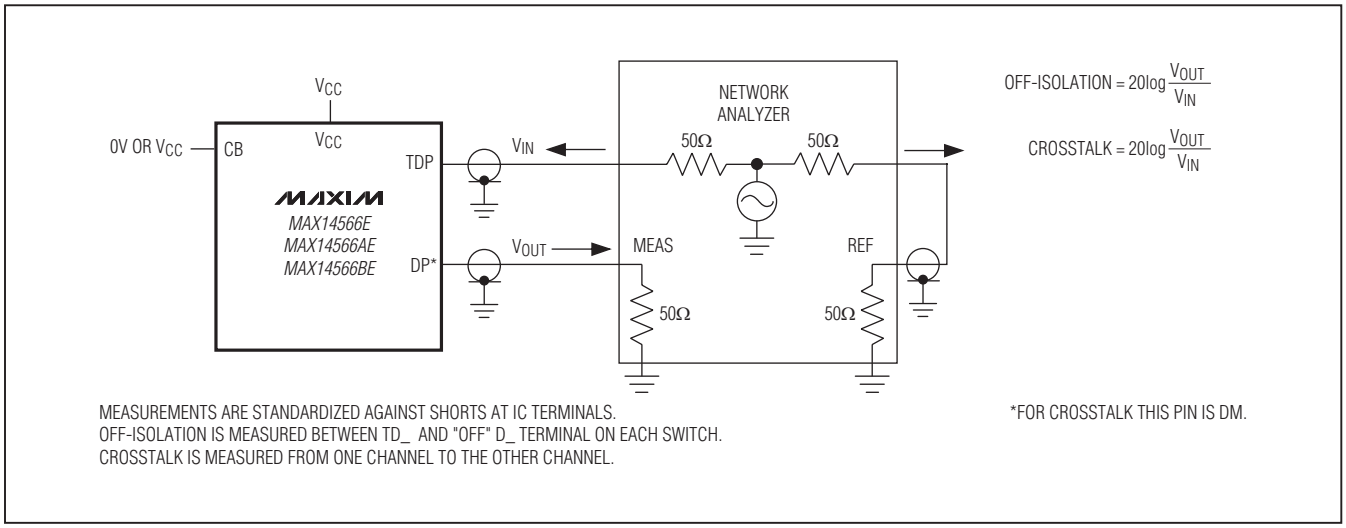
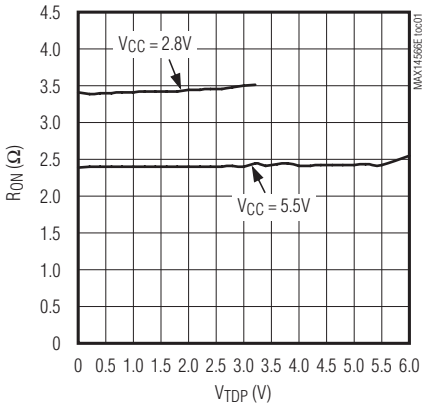


Figure 3. Off-Isolation and Crosstalk

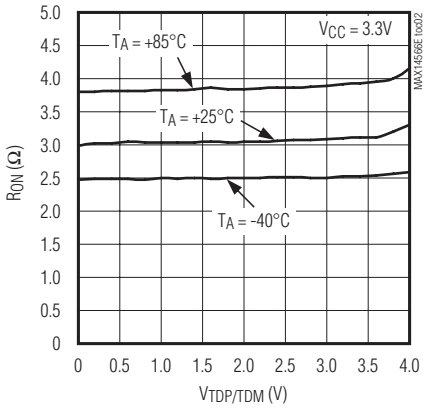
Typical Operating Characteristics

(VCC = 5V, TA = +25°C, unless otherwise noted.)

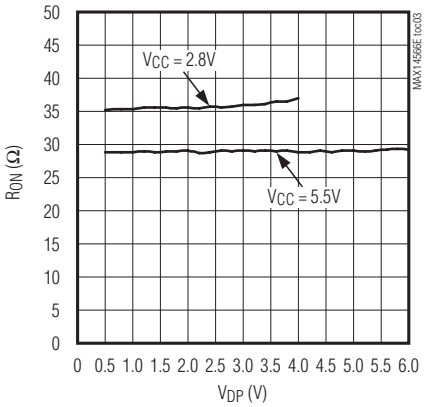
TDP/TDM ON-RESISTANCE vs. SUPPLY VOLTAGE



ON-RESISTANCE vs. VTDP/TDM



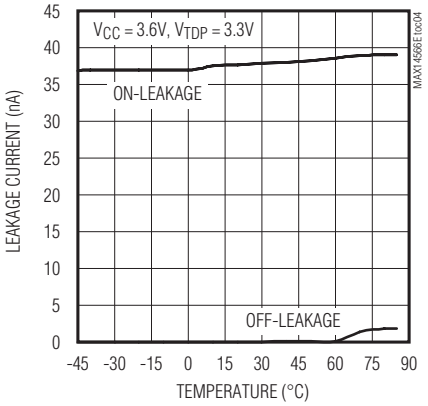
DP/DM SHORT ON-RESISTANCE vs. SUPPLY VOLTAGE



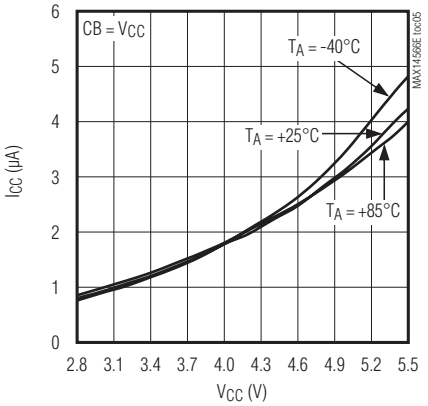
Typical Operating Characteristics (continued)

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

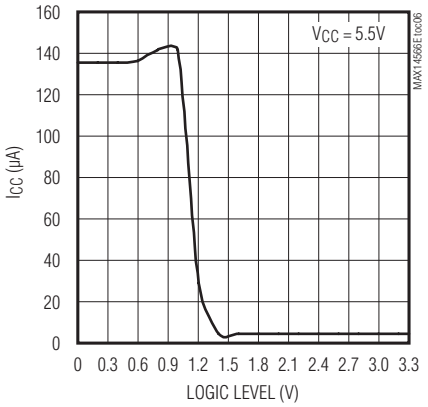
TDP/DP LEAKAGE CURRENT vs. TEMPERATURE



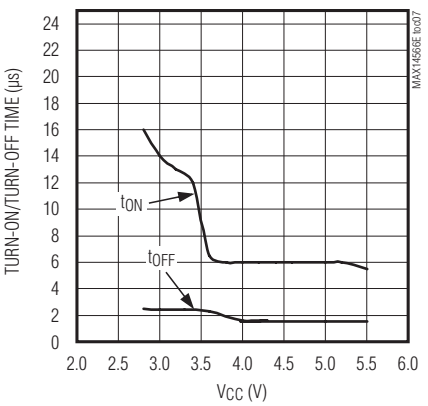
SUPPLY CURRENT vs. SUPPLY VOLTAGE



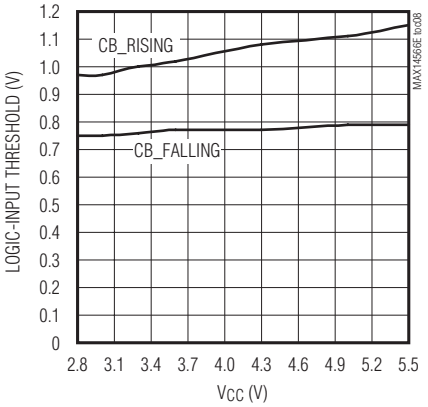
SUPPLY CURRENT vs. LOGIC LEVEL



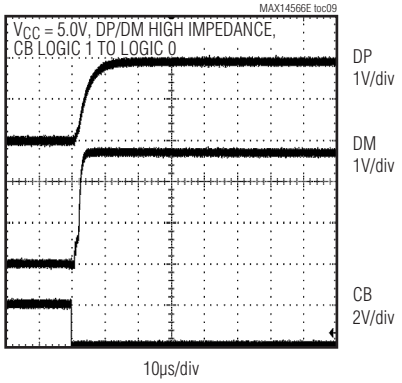
TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE



LOGIC-INPUT THRESHOLD vs. SUPPLY VOLTAGE



AUTODETECTION MODE

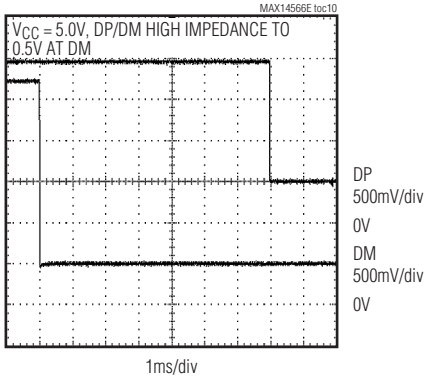


USB Host Charger Identification Analog Switches

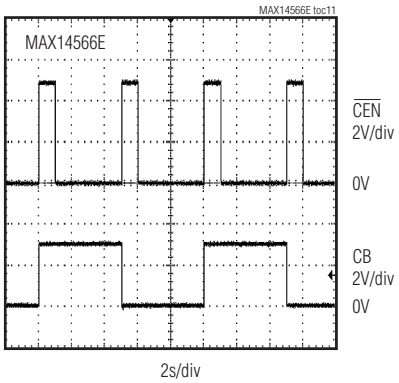
Typical Operating Characteristics (continued)

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

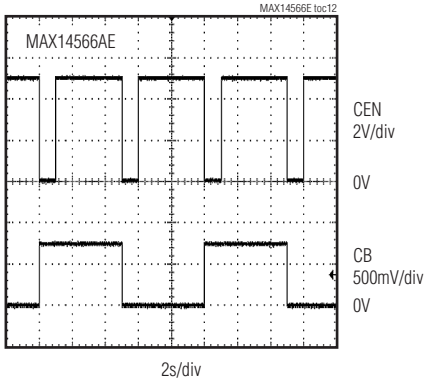
AUTODETECTION MODE



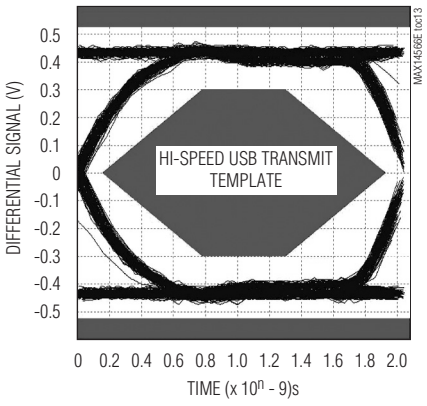
AUTO RESET



AUTO RESET

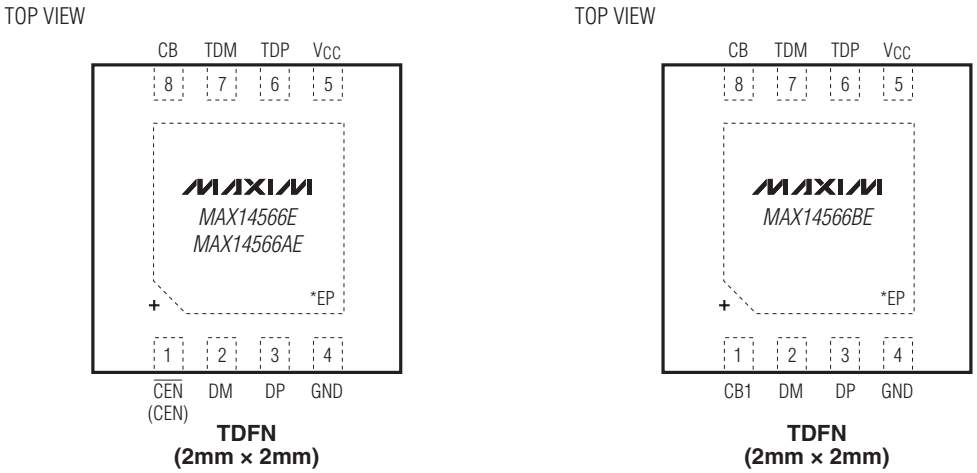


USB EYE DIAGRAM



USB Host Charger Identification Analog Switches

Pin Configuration



( ) FOR MAX14566AE ONLY

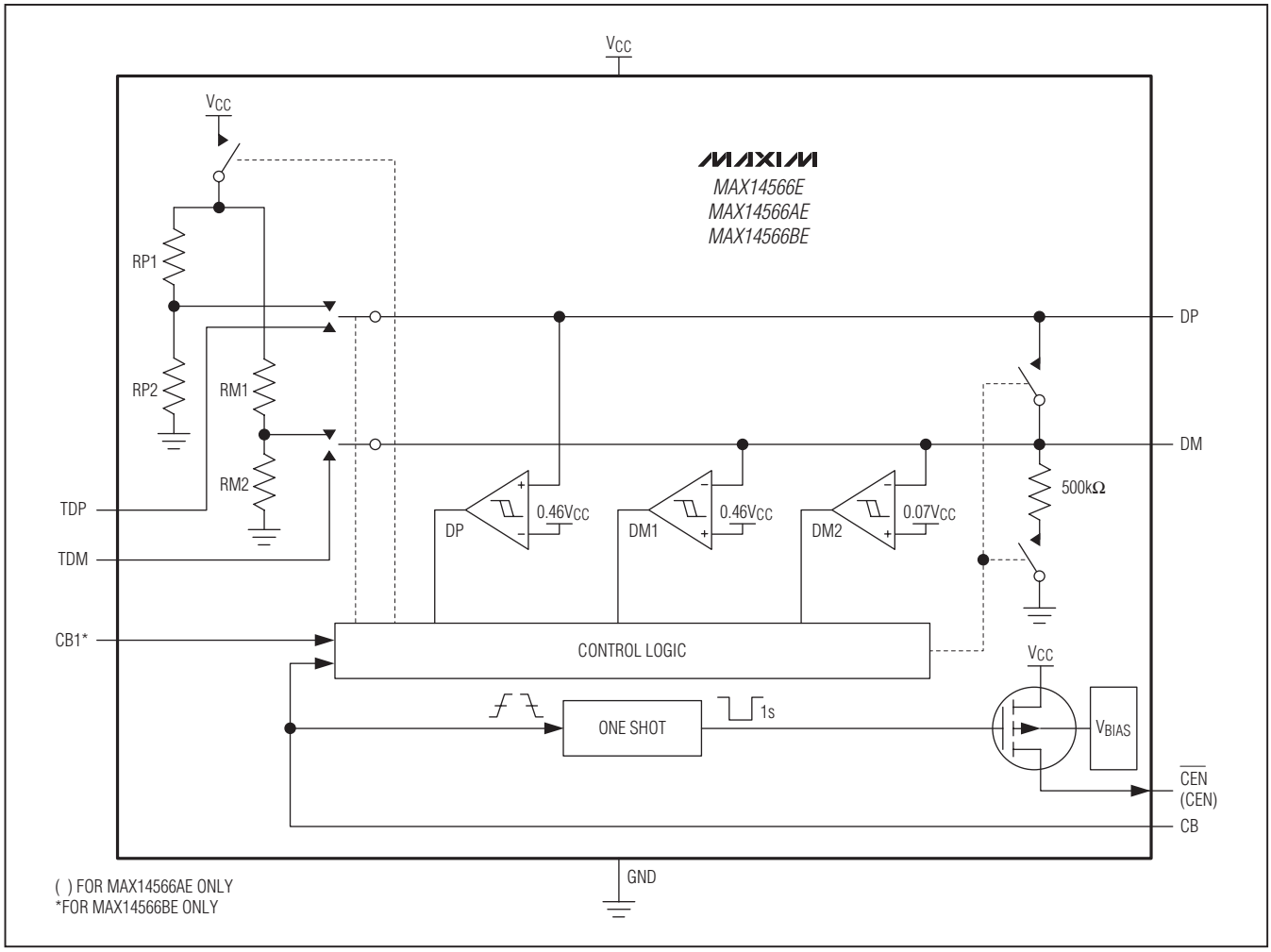
*CONNECT EP TO GND.

Pin Description

PIN			NAME	FUNCTION
MAX14566E	MAX14566AE	MAX14566BE		
—	1	—	CEN	nMOSFET Open-Drain Output, Current-Limit Switch (CLS) Control Output. If CB changes from logic 0 to logic 1 or from logic 1 to logic 0, CEN is low for 1s (typ).
1	—	—	$\overline{CEN}$	Active-Low pMOSFET Open-Drain Output, Current-Limit Switch (CLS) Control Output. If CB changes from logic 0 to logic 1 or logic 1 to logic 0, $\overline{CEN}$ is high for 1s (typ).
—	—	1	CB1	Switch Control Bit. See Table 2.
2	2	2	DM	USB Connector D- Connection
3	3	3	DP	USB Connector D+ Connection
4	4	4	GND	Ground
5	5	5	V_{CC}	Power Supply. Connect a 0.1µF capacitor between V_{CC} and GND as close as possible to the device.
6	6	6	TDP	Host USB Transceiver D+ Connection
7	7	7	TDM	Host USB Transceiver D- Connection
8	8	8	CB	Switch Control Bit. See Table 1. CB = logic 0, charger mode CB = logic 1 (PM), pass-through mode active, DP/DM connected to TDP/TDM
—	—	—	EP	Exposed Pad. Connect EP to ground. Do not use EP as the only ground connection.

USB Host Charger Identification Analog Switches

Functional Diagram



Detailed Description

The MAX14566E/MAX14566AE/MAX14566BE are Hi-Speed USB analog switches that support USB hosts to identify the USB port as a charger port when the USB host is in a low-power mode and cannot enumerate USB devices. These devices feature high-performance Hi-Speed USB switches with low 4pF (typ) on-capacitance and low 4Ω (typ) on-resistance. DP and DM can handle signals between 0V and 6V with any supply voltage.

Resistor-Dividers

All the devices feature an internal resistor-divider for biasing data lines to provide support for Apple-compliant devices. When these devices are not operated with the resistor-divider, they disconnect the resistor-dividers from the supply voltage to minimize supply current requirements. The resistor-dividers are not connected in pass-through mode.

Switch Control

The MAX14566E/MAX14566AE feature a single digital input, CB, for mode selection (Table 1). Connect CB to a logic-level low voltage for autodetection charger mode (AM). See the *Autodetection* section for more information. Connect CB to a logic-level high voltage for normal high-speed pass-through mode (PM). The MAX14566BE features dual digital inputs, CB and CB1, for mode selection (Table 2). Connect CB to a logic-level high for normal high-speed pass-through mode (PM). Connect CB to a logic-level low for different charger-mode selection

with CB1. Connect CB1 to a logic-level low for auto mode (AM) or connect CB1 to a logic-level high for forced dedicated-charger mode (FM).

Autodetection

All the devices feature autodetection charger mode for dedicated chargers and USB masters. CB must be set low to activate autodetection charger mode.

In autodetection charger mode, the MAX14566E monitors the voltages at DM and DP to determine the type of the device attached. If the voltage at DM is +2.3V (typ) or higher and the voltage at DP is +2.3V (typ) or lower, the voltage stays unchanged.

If the voltage at DM is forced below the +2.3V (typ) threshold, the internal switch disconnects DM and DP from the resistor-divider and DP and DM are shorted together for dedicated charging mode.

If the voltage at DP is forced higher than the +2.3V (typ) threshold, the internal switch disconnects DM and DP from the resistor-divider and DP and DM are shorted together for dedicated charging mode.

Once the charging voltage is removed, the short between DP and DM is disconnected for normal operation.

Automatic Peripheral Reset

The MAX14566E/MAX14566AE feature automatic current-limit switch control output. This feature resets the peripheral connected to V_{BUS} in the event the USB host switches to or from standby mode. $\overline{CEN}$/CEN provide a 1s (typ) pulse on the rising or falling edge of CB (Figures 4, 5, and 6).

Table 1. Digital Input State (MAX14566E/MAX14566AE)

CB	MODE	DP/DM	COMMENT	INTERNAL RESISTOR-DIVIDER
0	AM	Autodetection Circuit Active	Auto Mode	Connected
1	PM	Connected to TDP/TDM	USB Traffic Active	Not Connected

Table 2. Digital Input State (MAX14566BE)

CB	CB1	MODE	STATUS
0	0	AM	Auto Mode
0	1	FM	Forced Dedicated-Charger Mode: DP/DM Shorted
1	X	PM	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

X = Don't care.

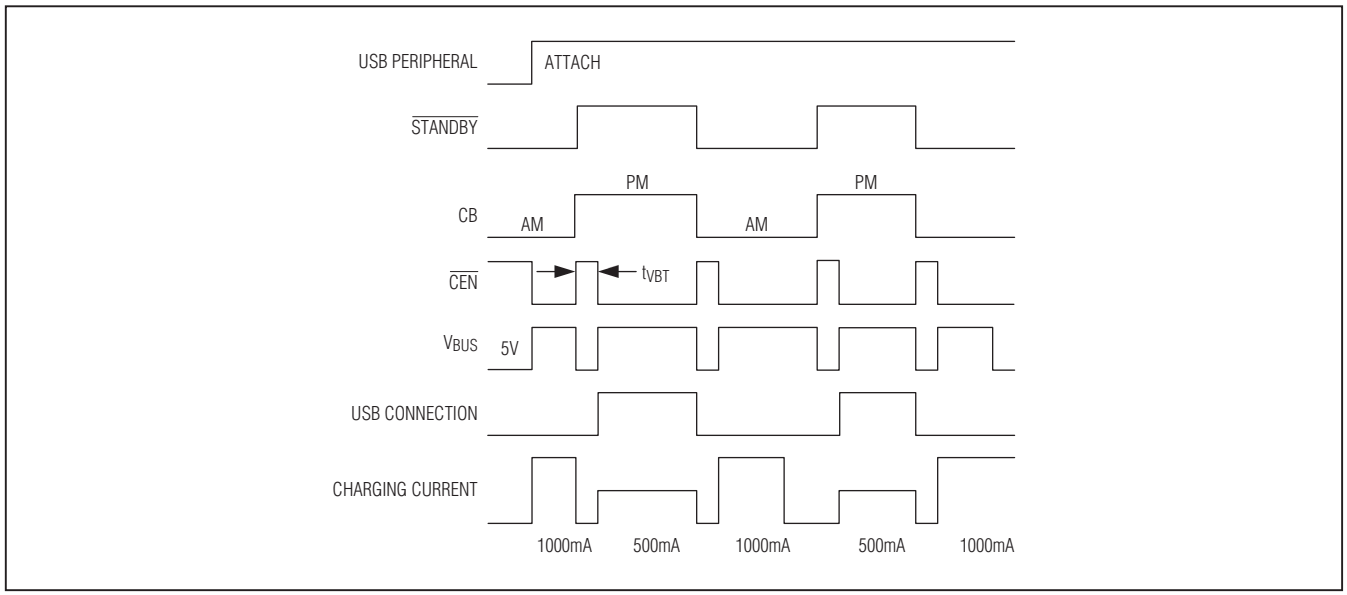


Figure 4. MAX14566E Peripheral Reset Timing Diagram

USB Host Charger Identification Analog Switches

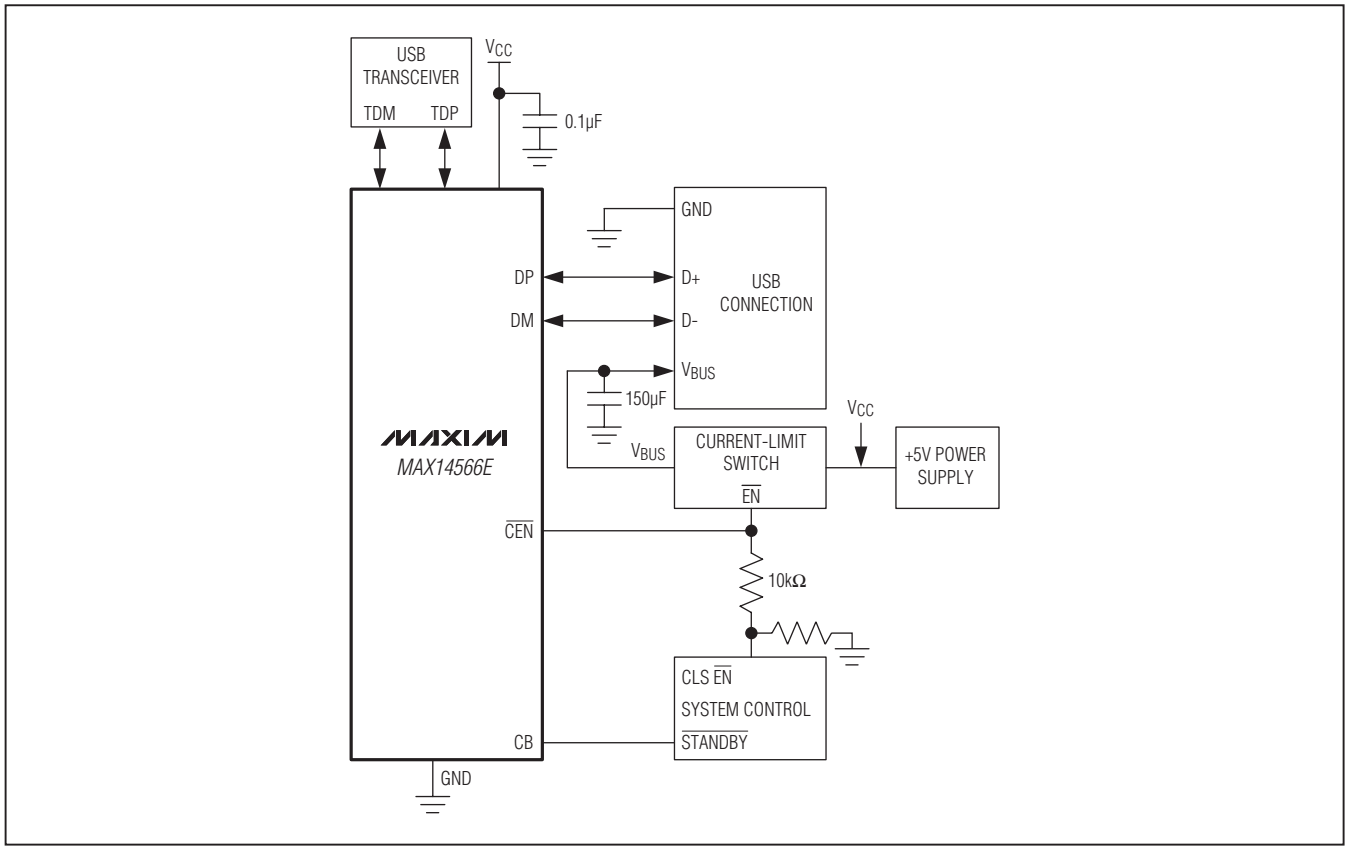


Figure 5. MAX14566E Peripheral Reset Applications Diagram

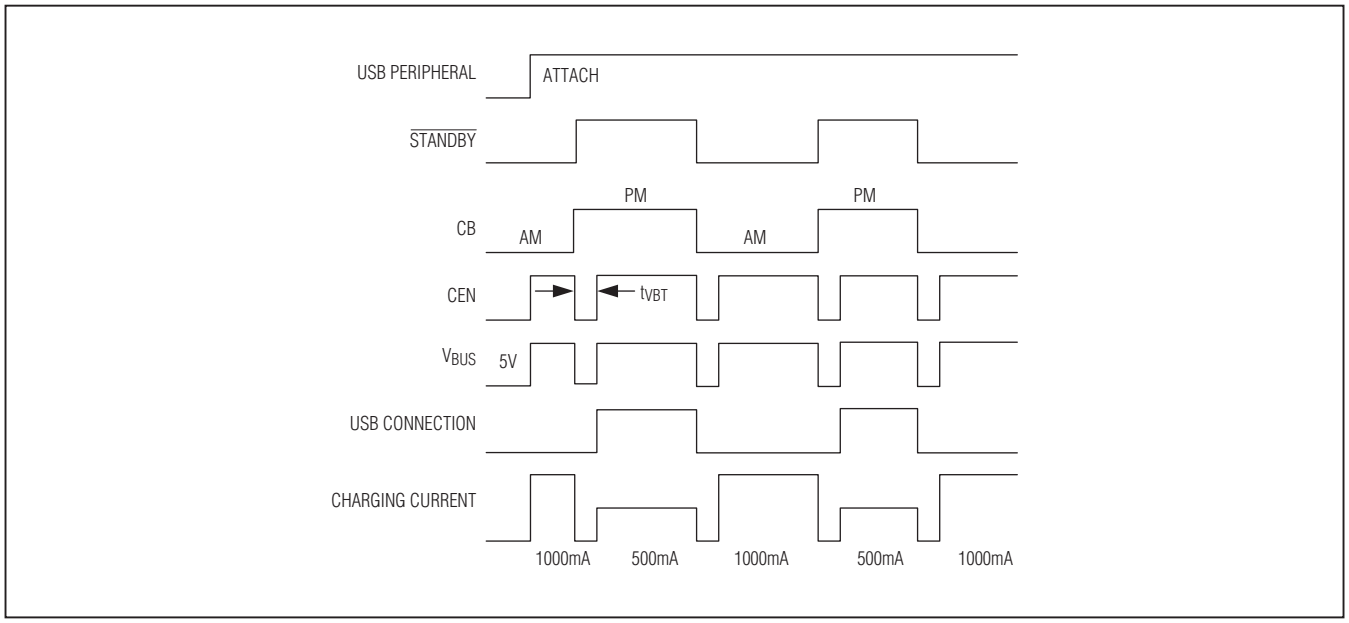


Figure 6. MAX14566AE Peripheral Reset Timing Diagram

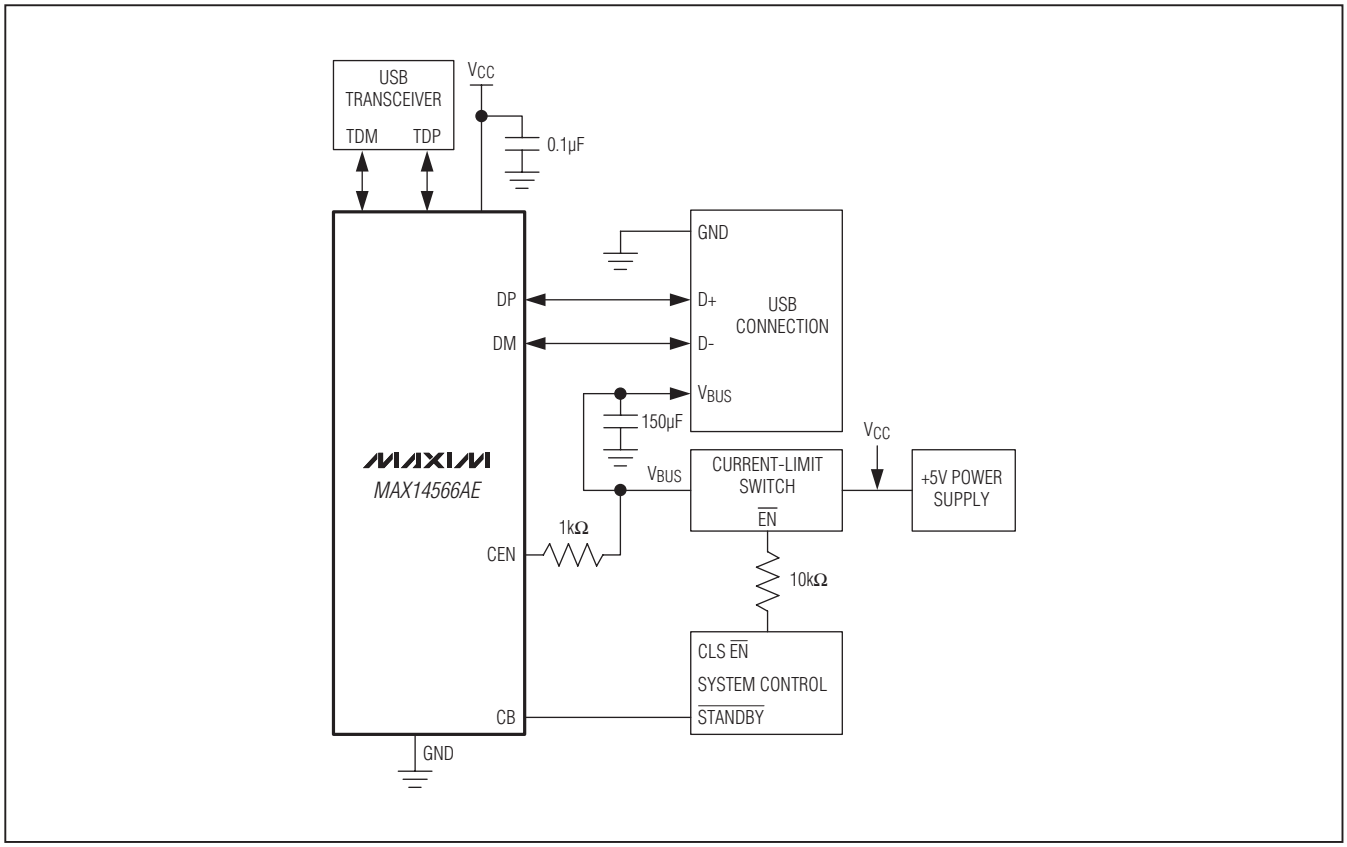


Figure 7. MAX14566AE V_{BUS} Discharge Circuit

Bus Voltage Discharge

The MAX14566AE automatic current-limit switch control output can be used to discharge the V_{BUS} during V_{BUS} reset. When the system controls the current-limit switch for V_{BUS} toggle, the output capacitor can be discharged slowly depending upon the load. If fast discharge of the V_{BUS} capacitor is desired, the CEN output can be used to achieve the fast discharge as shown in Figure 7.

Data Contact Detect

All the devices support USB devices that require detecting the USB data lines prior to charging. When a USB Revision 1.2-compliant device is attached, the USB data lines DP and DM are shorted together. The short remains until it is detected by the USB device. This feature guarantees appropriate charger detection if a USB Revision 1.2-compliant device is attached. The autodetection charger mode is activated after the data contact detect is established. CB must be set low to activate data contact detect.

ESD Test Conditions

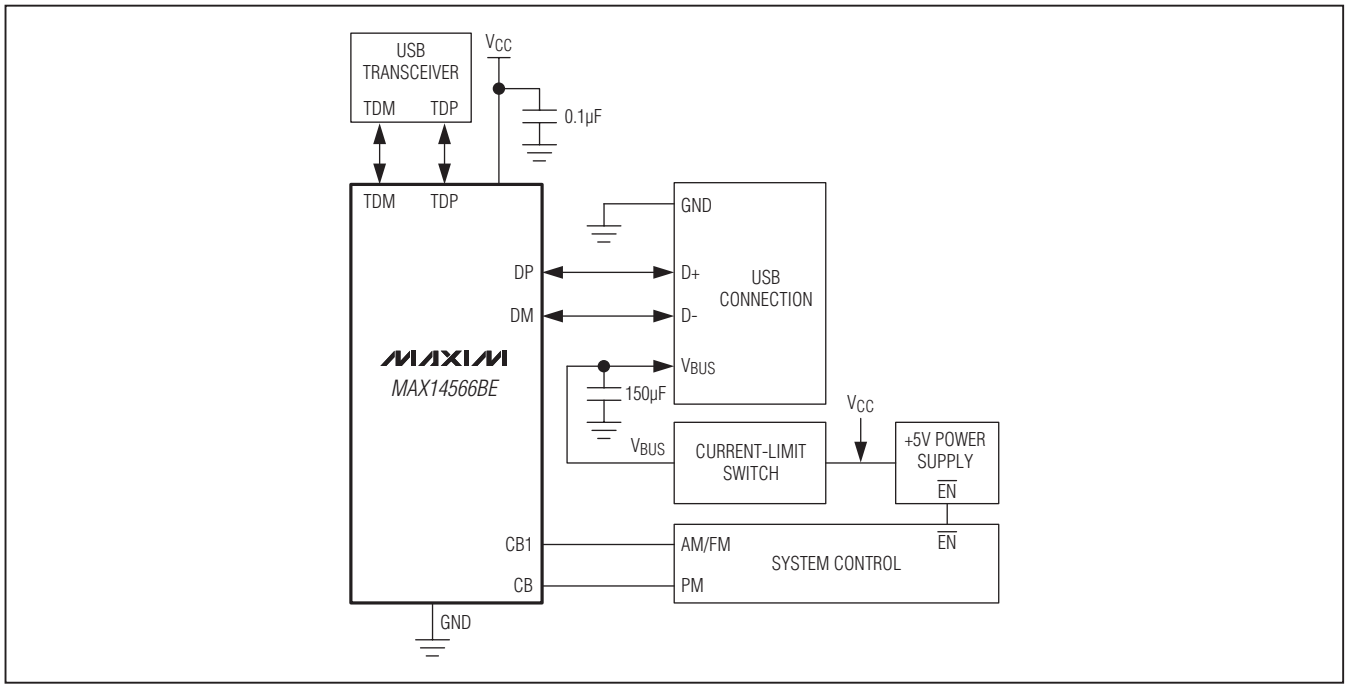
ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Extended ESD Protection (Human Body Model)

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV (HBM) encountered during handling and assembly. DP and DM are further protected against ESD up to ±15kV (HBM) without damage. The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the device continues to function without latchup (Figure 8).

USB Host Charger Identification Analog Switches

Typical Application Circuit (MAX14566BE)



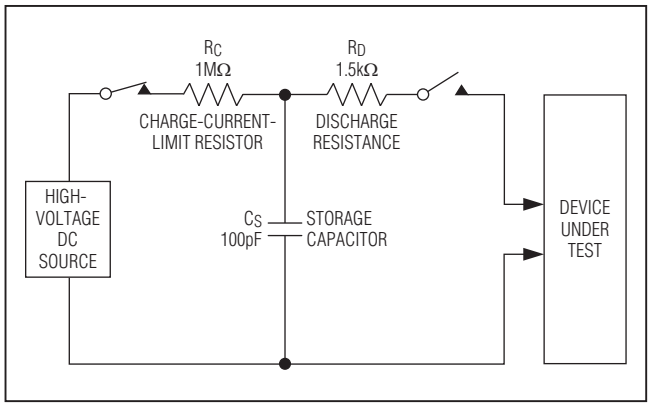


Figure 8a. Human Body ESD Test Model

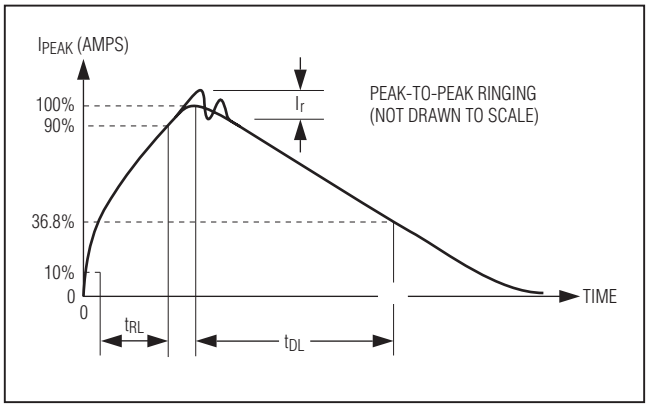


Figure 8b. Human Body Current Waveform

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 TDFN-EP	T822+1	21-0168	90-0064

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/10	Initial release	—
1	3/11	Changed the USB Battery Charging Specification Revision 1.1 to Revision 1.2	1, 13