



Dual-Pair LLT with Charge Pump and High-ESD Protection

MAX14569

General Description

The MAX14569 is a dedicated dual-pair unidirectional logic-level translator that is ideal for industrial and metering applications. Voltages VCC and VL set the logic levels on either side of the device. Logic-high signals present on the VL side of the device appear as high-voltage logic signals on the VCC side of the device and vice versa.

The device has two pairs of logic-level translators in back-to-back configuration: one logic-level translator from a low voltage to a high voltage and the other logic-level translator from a high voltage to a low voltage. The device also features a high-efficiency charge pump to boost the battery input, VBAT, to VCC (5V).

The device features an extreme power-saving mode that reduces supply current to a typical 0.01µA. The device also features thermal short-circuit protection for enhanced protection in applications that route signals externally.

In addition, the device features enhanced high electrostatic discharge (ESD) Human Body Model (HBM) protection on OUTAVCC, INBVCC, OUTCVCC, and INDVCC ports up to ±25kV. The MAX14569 is available in a 16-pin QSOP package, and is specified over the -40°C to +85°C extended temperature range.

Features

- ◆ Ultra-Low Shutdown Supply Current, 0.01µA (typ)
- ◆ Ultra-Low VL Supply Current, 1µA (max)
- ◆ Operates Down to 1.6V on VL
- ◆ Continuous Current Drive Capability > 10mA
- ◆ Extended ESD Protection on VCC Input and Output Lines
 - ±25kV Human Body Model
 - ±15kV IEC 61000-4-2 Air-Gap Discharge
 - ±12kV IEC 61000-4-2 Contact Discharge
- ◆ 16-Pin QSOP Package
- ◆ -40°C to +85°C Extended Operating Temperature Range

Applications

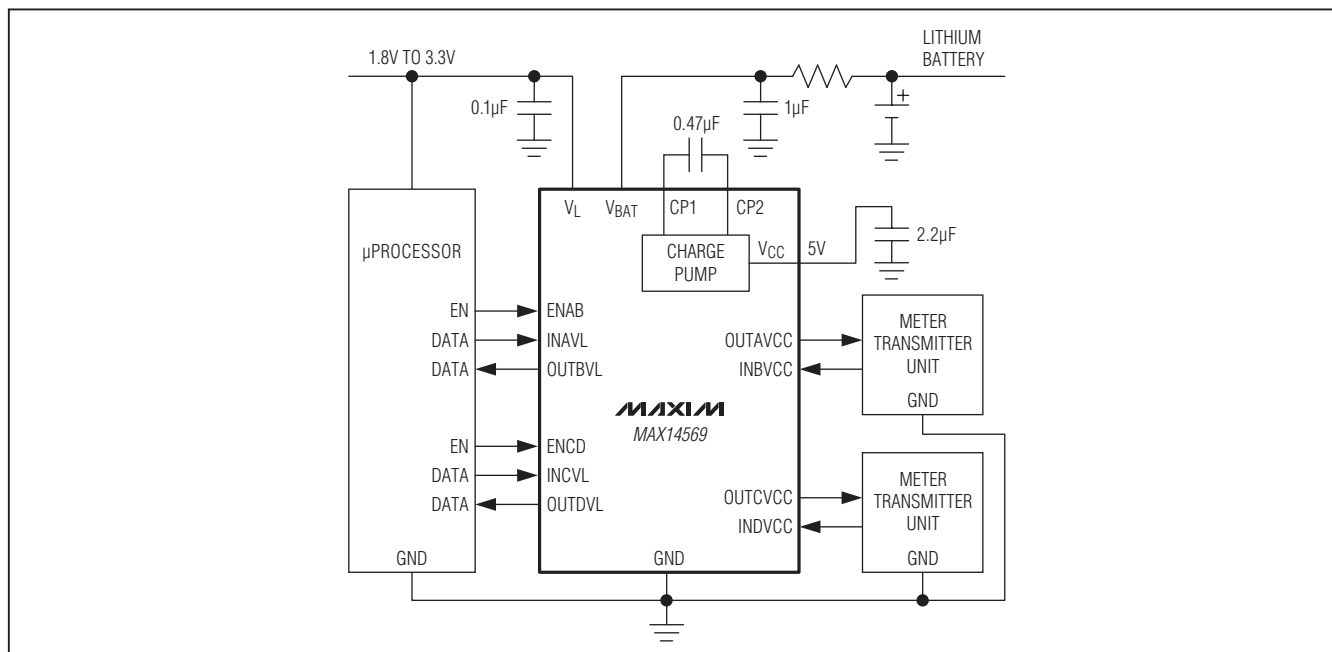
- Automatic Meter Reader
- Remote Communications System
- Industrial Networking

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14569EEE+T	-40°C to +85°C	16 QSOP

+ Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

VBAT, VL	-0.3V to +6V	Short-Circuit Duration OUTAVCC, OUTCVCC, OUTBVL, OUTDVL to GND	Continuous
VCC (no shutdown condition)	(VBAT - 0.3V) to +6V	Continuous Power Dissipation (TA = +70°C)	771.5mW
VCC (shutdown condition)	-0.3V to +6V	QSOP (derate 9.6mW/°C above +70°C)	771.5mW
CP1	-0.3V to (VBAT + 0.3V)	Junction-to-Ambient Thermal Resistance (Note 1)	103.7°C/W
CP2	-0.3V to +6V	θJA	103.7°C/W
ENAB, ENCD	-0.3V to +6V	Junction-to-Case Thermal Resistance (Note 1)	37°C/W
INAVL, INCVL	-0.3V to +6V	θJC	37°C/W
OUTBVL, OUTDVL	-0.3V to (VL + 0.3V)	Operating Temperature Range	-40°C to +85°C
INBVCC, INDVCC	-0.3V to (VCC + 0.3V)	Storage Temperature Range	-65°C to +150°C
OUTAVCC, OUTCVCC	-0.3V to (VCC + 0.3V)	Junction Temperature	+150°C
Short-Circuit Current OUTAVCC, OUTCVCC, OUTBVL, OUTDVL to GND	Continuous	Lead Temperature (soldering, 10s)	+300°C
		Soldering Temperature (reflow)	+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VBAT = 2.3V to 5.5V, VL = 1.6V to 5.5V, CVBAT = 1μF, CVCC = 2.2μF, CVL = 0.1μF, TA = -40°C to +85°C, unless otherwise noted. Typical values are at VBAT = 3.6V, VL = 3.0V, and TA = +25°C.) (Notes 2, 3, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
VBAT Supply Range	VBAT		2.3		5.5	V
VL Supply Range	VL		1.6		5.5	V
Supply Current from VL	I _{QVL}	INBVCC = INDVCC = VCC, INAVL = INCVL = VL			1	μA
VBAT Shutdown Supply Current	I _{SHDN-VBAT}	VINAVL = VINCVL = 0V, VENAB = VENCDC = 0V		0.01	0.5	μA
VL Shutdown Supply Current	I _{SHDN-VL}	VENAB = VENCDC = 0V		0.01	0.5	μA
VBAT Change in Supply Current with ENAB and ENCD at VL	ΔI _{VBAT}	VENAB = VENCDC = VL (Notes 2, 4, 5)			1	μA
OUTAVCC Shutdown Mode Leakage Current	I _{OUTAVCC_LEAK}	VENAB = 0V, VENCDC = VIH, VOUTAVCC = 5V		0.01	1	μA
OUTCVCC Shutdown Mode Leakage Current	I _{OUTCVCC_LEAK}	VENAB = VIH, VENCDC = 0V, VOUTCVCC = 5V		0.01	1	μA
OUTBVL, OUTDVL Shutdown Mode Leakage Current	I _{OUTBVL_LEAK} I _{OUTDVL_LEAK}	VENAB = VENCDC = 0V, VOUTBVL = VOUTDVL = 0V		0.01	1	μA
INBVCC Shutdown Mode Leakage Current	I _{INBVCC_LEAK}	VENAB = 0V, VENCDC = VIH, VINBVCC = 5V		0.01	1	μA
INDVCC Shutdown Mode Leakage Current	I _{INDVCC_LEAK}	VENAB = VIH, VENCDC = 0V, VINDVCC = 5V		0.01	1	μA

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ELECTRICAL CHARACTERISTICS (continued)

($V_{BAT} = 2.3V$ to $5.5V$, $V_L = 1.6V$ to $5.5V$, $C_{VBAT} = 1\mu F$, $C_{VCC} = 2.2\mu F$, $C_{VL} = 0.1\mu F$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{BAT} = 3.6V$, $V_L = 3.0V$, and $T_A = +25^\circ C$.) (Notes 2, 3, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INAVL, INCVL Leakage Current	I _{INAVL_LEAK} I _{INCVL_LEAK}	$V_{INAVL} = V_{INCVL} = V_L$		0.01	1	μA
ENAB, ENCD Input Leakage Current	I _{ENAB_LEAK} I _{ENCD_LEAK}	$V_{ENAB} = V_{ENCD} = 5V$		0.01	1	μA
OUTAVCC, OUTCVCC Short-Circuit Output Current	I _{SH}	$V_{OUTAVCC} = 0V$ or $V_{OUTCVCC} = 0V$, $V_{BAT} \geq 2.7V$	100	250		mA
LOGIC LEVELS						
INAVL, INCVL Input-Voltage High	V _{IHL}		$0.7 \times V_L$			V
INAVL, INCVL Input-Voltage Low	V _{ILL}				$0.3 \times V_L$	V
INBVCC, INDVCC Input-Voltage High	V _{IHC}		$0.7 \times V_{CC}$			V
INBVCC, INDVCC Input-Voltage Low	V _{ILC}				$0.3 \times V_{CC}$	V
ENAB, ENCD Input-Voltage High	V _{IH}		1.2			V
ENAB, ENCD Input-Voltage Low	V _{IL}				0.4	V
ENAB, ENCD Input-Voltage Hysteresis	V _{HYS}			120		mV
OUTBVL, OUTDVL Output-Voltage High	V _{OHL}	OUTBVL or OUTDVL source current = $100\mu A$, INBVCC or INDVCC > V _{IHC}	$V_L - 0.1$			V
		OUTBVL or OUTDVL source current = $4mA$, INBVCC or INDVCC > V _{IHC}	$V_L - 0.4$			
OUTBVL, OUTDVL Output-Voltage Low	V _{OLL}	OUTBVL or OUTDVL sink current = $100\mu A$, INBVCC or INDVCC < V _{ILC}			0.1	V
		OUTBVL or OUTDVL sink current = $4mA$, INBVCC or INDVCC < V _{ILC}			0.4	
OUTAVCC, OUTCVCC Output-Voltage High	V _{OHC}	OUTAVCC or OUTCVCC source current = $100\mu A$, INAVL or INCVL > V _{IHL} , $2.7V \leq V_{BAT} \leq 4.5V$		4.6		V
		OUTAVCC or OUTCVCC source current = $20mA$, INAVL or INCVL > V _{IHL} , $2.7V \leq V_{BAT} \leq 4.5V$		4.3		

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ELECTRICAL CHARACTERISTICS (continued)

($V_{BAT} = 2.3V$ to $5.5V$, $V_L = 1.6V$ to $5.5V$, $C_{VBAT} = 1\mu F$, $C_{VCC} = 2.2\mu F$, $C_{VL} = 0.1\mu F$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{BAT} = 3.6V$, $V_L = 3.0V$, and $T_A = +25^\circ C$.) (Notes 2, 3, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTAVCC, OUTCVCC Output-Voltage Low	VOLC	OUTAVCC or OUTCVCC sink current = $100\mu A$, INAVL or INCVL < V_{ILL} , $2.7V \leq V_{BAT} \leq 4.5V$			0.1	V
		OUTAVCC or OUTCVCC sink current = $20mA$, INAVL or INCVL < V_{ILL} , $2.7V \leq V_{BAT} \leq 4.5V$			0.4	
TIMING CHARACTERISTICS (Note 6)						
OUTAVCC, OUTCVCC Rise Time	trVCC	Figure 1			25	ns
OUTAVCC, OUTCVCC Fall Time	tFVCC	Figure 1			25	ns
OUTBVL, OUTDVL Rise Time	trVL	Figure 2			25	ns
OUTBVL, OUTDVL Fall Time	tFVL	Figure 2			25	ns
Propagation Delay (Driving INAVL, INCVL) Low-to-High	tpVL-VCC-LH	Figure 1			30	ns
Propagation Delay (Driving INAVL, INCVL) High-to-Low	tpVL-VCC-HL	Figure 1			30	ns
Propagation Delay (Driving INBVCC, INDVCC) Low-to-High	tpVCC-VL-LH	Figure 2			30	ns
Propagation Delay (Driving INBVCC, INDVCC) High-to-Low	tpVCC-VL-HL	Figure 2			30	ns
Maximum Data Rate			12			Mbps
CHARGE PUMP						
VCC Output Voltage	VCC	$I_{CC} = 10mA$, $2.7V \leq V_{BAT} \leq 4.5V$	4.7	5.0	5.3	V
		$I_{CC} = 40mA$, $3.0V \leq V_{BAT} \leq 4.5V$	4.7	5.0	5.3	
VCC Output Voltage Ripple		$I_{CC} = 40mA$		45		mVp-P
VCC Line Regulation		$I_{CC} = 10mA$, $2.7V \leq V_{BAT} \leq 4.5V$	-1		+1	%
VCC Load Regulation	ΔV_{CC}	$0 \leq I_{CC} \leq 40mA$, $V_{BAT} = 3.6V$		-1		%
Quiescent Current	I_Q	$I_{CC} = 0mA$, $V_{BAT} = 3.6V$			200	μA
CP_ Leakage Current	I_{CP_LEAK}	$V_{BAT} = 3.6V$, $V_{CC} = 0V$ $V_{ENAB} = V_{ENCD} = 0V$		0.01	0.5	μA

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ELECTRICAL CHARACTERISTICS (continued)

($V_{BAT} = 2.3V$ to $5.5V$, $V_L = 1.6V$ to $5.5V$, $C_{VBAT} = 1\mu F$, $C_{VCC} = 2.2\mu F$, $C_{VL} = 0.1\mu F$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{BAT} = 3.6V$, $V_L = 3.0V$, and $T_A = +25^\circ C$.) (Notes 2, 3, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CP_Switching Frequency	f_{CP}	No capacitor between CP1 and CP2, $2.7V \leq V_{BAT} \leq 4.5V$	0.5	1	1.5	MHz
Efficiency	η	$I_{CC} = 10mA$, $V_{BAT} = 2.7V$, $V_{CC} = 5.0V$		90		%
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			+150		$^\circ C$
Thermal Hysteresis	T_{HYST}			+20		$^\circ C$
ESD PROTECTION						
OUTAVCC, INBVCC, OUTCVCC, INDVCC		Human Body Model		± 25		kV
		IEC 61000-4-2 Air Gap Discharge		± 15		
		IEC 61000-4-2 Contact Discharge		± 12		
All Other Pins		Human Body Model		± 2		kV

Note 2: V_L must be less than or equal to V_{CC} during normal operation. However, V_L can be greater than V_{CC} during startup and shutdown conditions.

Note 3: All units are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 4: Connect a $0.47\mu F$ capacitor between CP1 and CP2.

Note 5: $\Delta I_{VBAT} = [I_{VBAT}(V_{ENAB} = V_{ENC D} = V_{IL}) - I_{VBAT}(V_{ENAB} = V_{ENC D} = 0V)]$. Guaranteed by design and not production tested.

Note 6: $V_{CC} = 5.0V$, $V_L = 1.6V$ to V_{CC} , $V_{BAT} = 2.7V$ to $3.6V$, $V_{ENAB} = V_{ENC D} > V_{IH}$, $R_S = 50\Omega$, $R_L = 1M\Omega$, $C_L = 15pF$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{BAT} = 3.6V$, $V_L = 3.0V$, and $T_A = +25^\circ C$.

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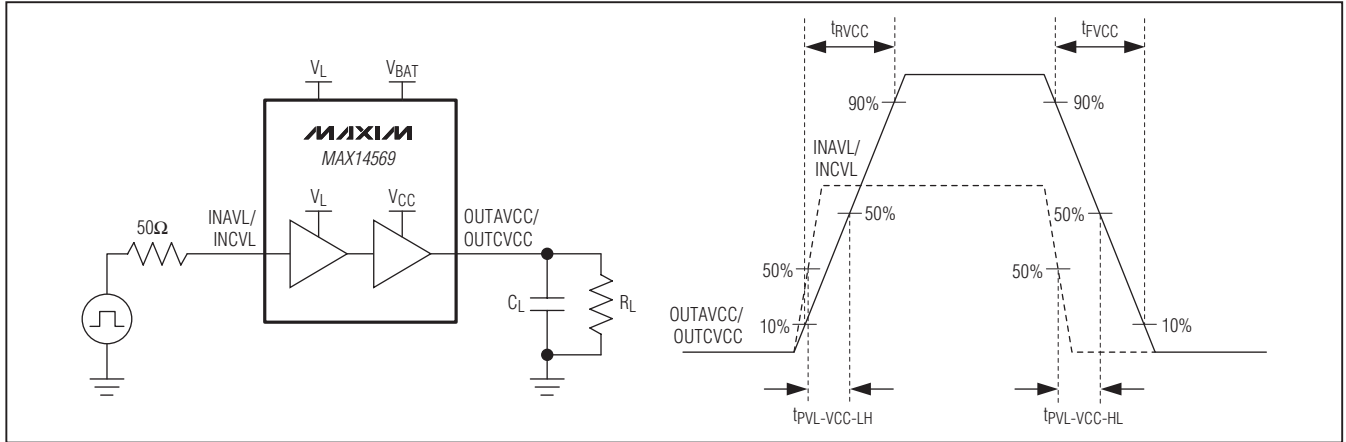


Figure 1. Push-Pull Driving INAVL/INCVL Test Circuit and Timing

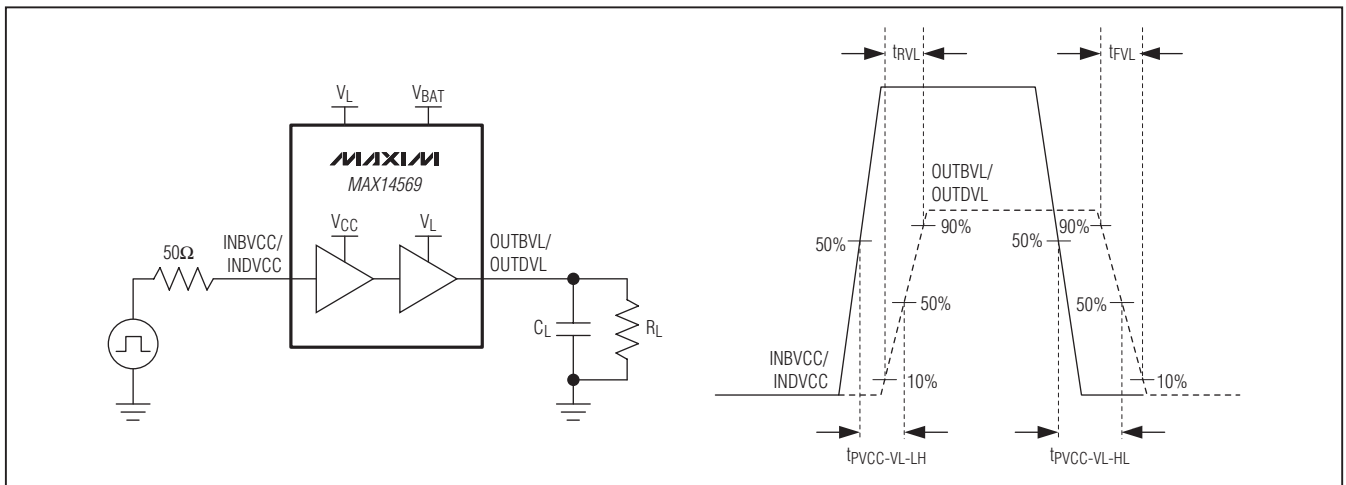


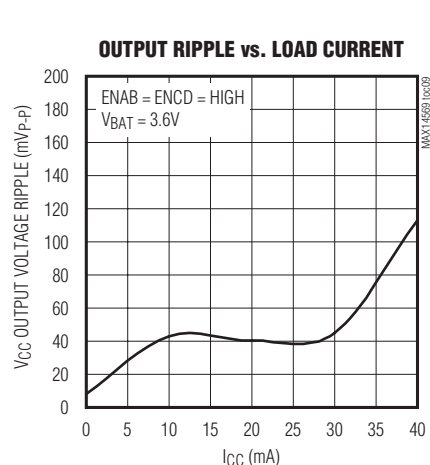
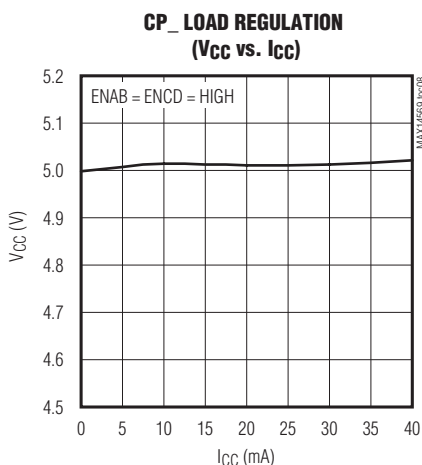
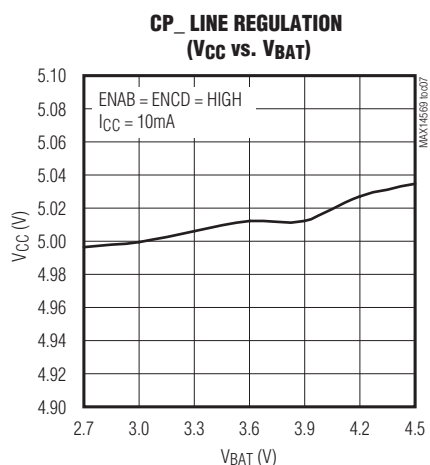
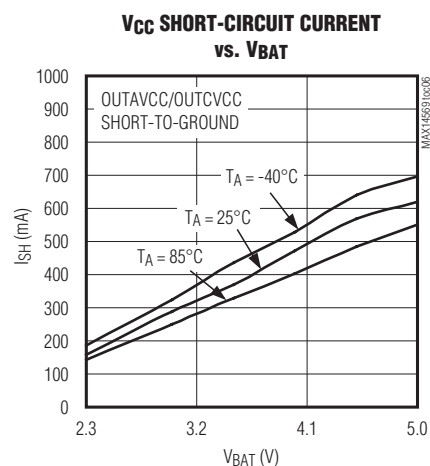
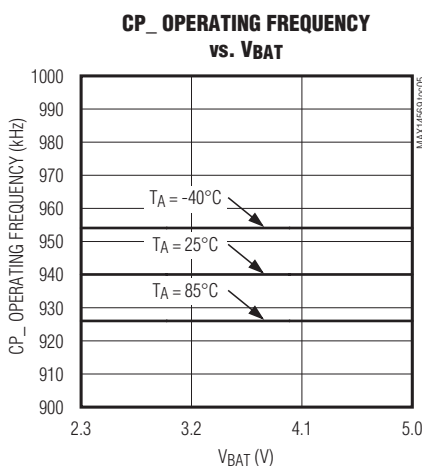
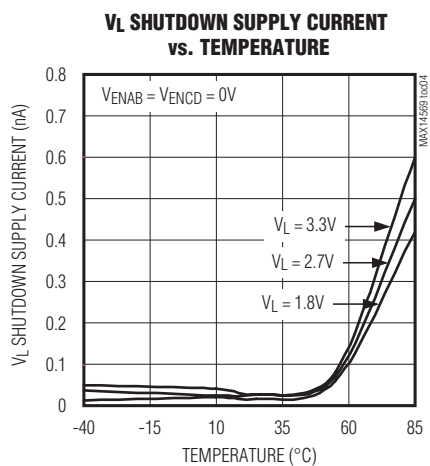
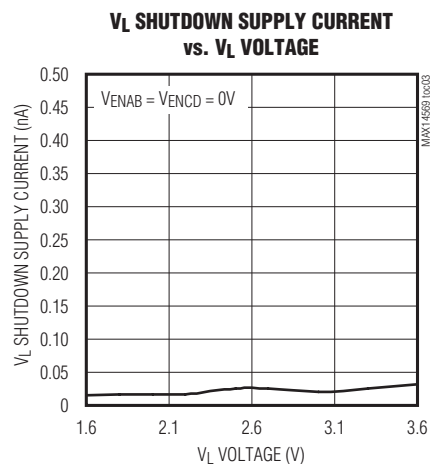
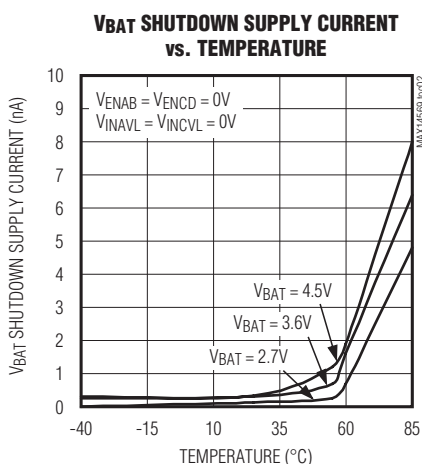
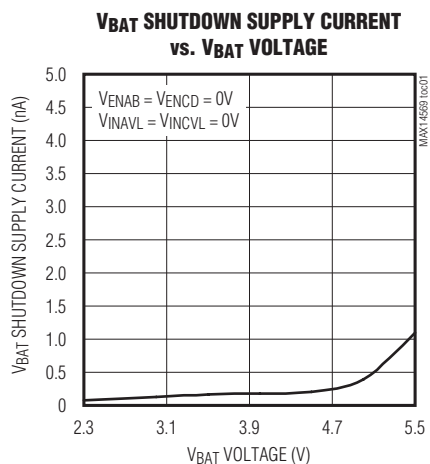
Figure 2. Push-Pull Driving INBVCC/INDVCC Test Circuit and Timing

Dual-Pair LLT with Charge Pump and High-ESD Protection

Typical Operating Characteristics

($V_{BAT} = 3.6V$, $V_L = 3V$, $C_{VBAT} = 1\mu F$, $C_{VCC} = 2.2\mu F$, $C_{VL} = 0.1\mu F$, connect $0.47\mu F$ capacitor between CP1 and CP2, data rate = 1Mbps, $T_A = +25^\circ C$, unless otherwise noted.)

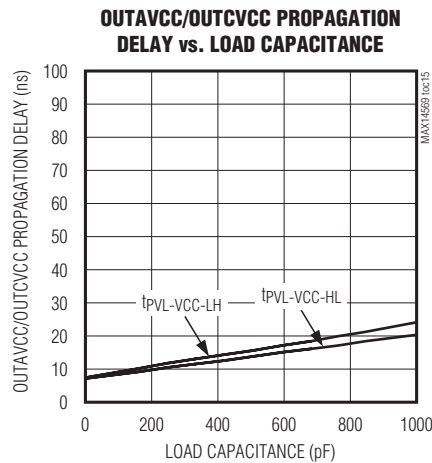
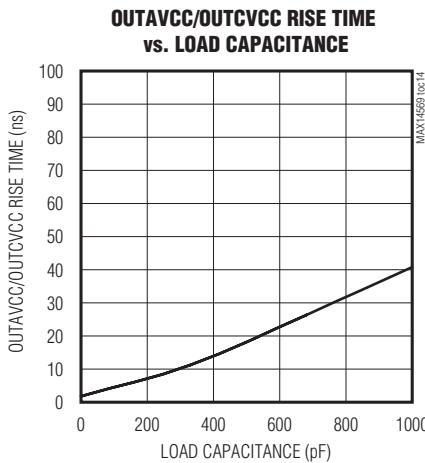
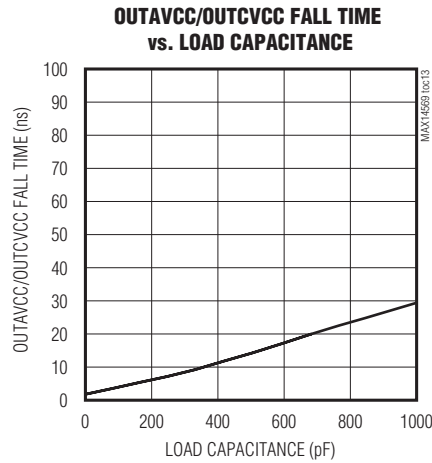
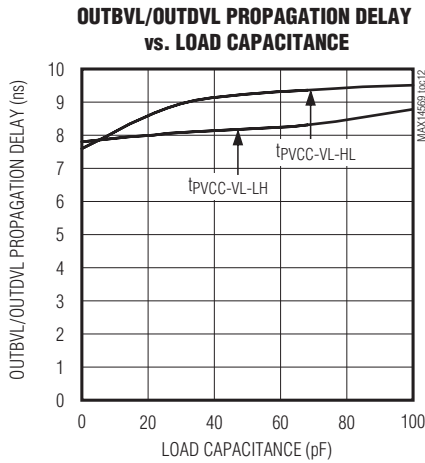
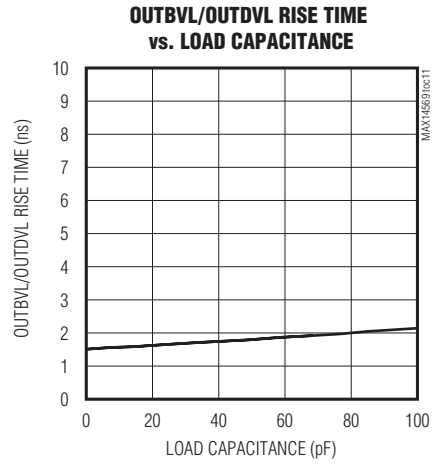
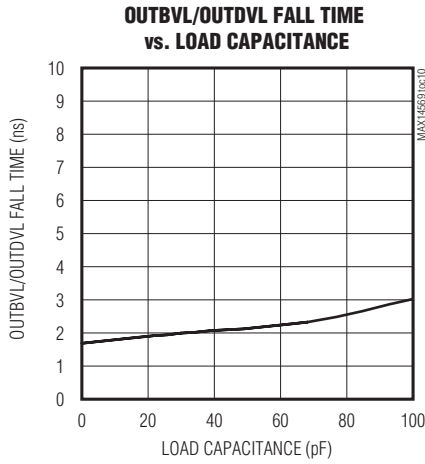
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Dual-Pair LLT with Charge Pump and High-ESD Protection

Typical Operating Characteristics (continued)

($V_{BAT} = 3.6V$, $V_L = 3V$, $C_{VBAT} = 1\mu F$, $C_{VCC} = 2.2\mu F$, $C_{VL} = 0.1\mu F$, connect $0.47\mu F$ capacitor between CP1 and CP2, data rate = 1Mbps, $T_A = +25^\circ C$, unless otherwise noted.)

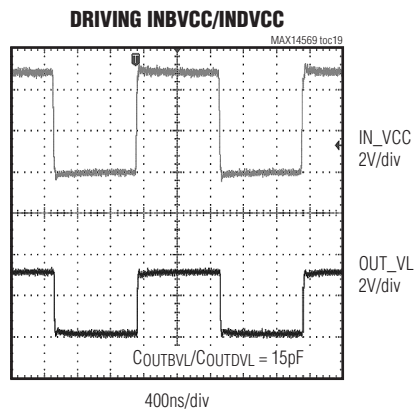
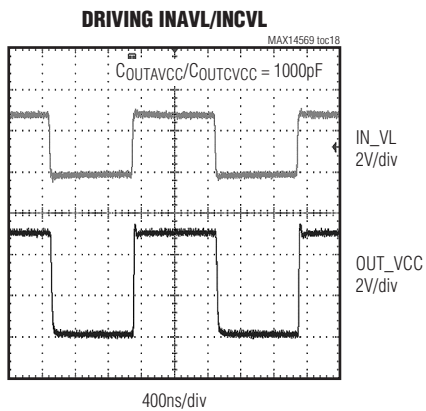
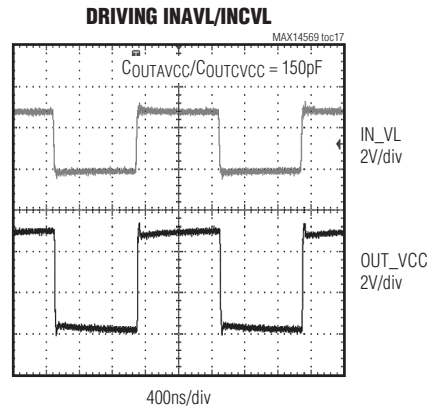
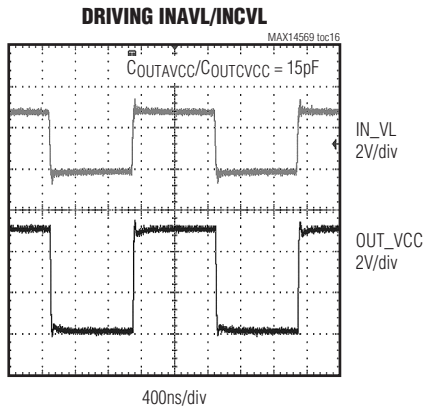


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Typical Operating Characteristics (continued)

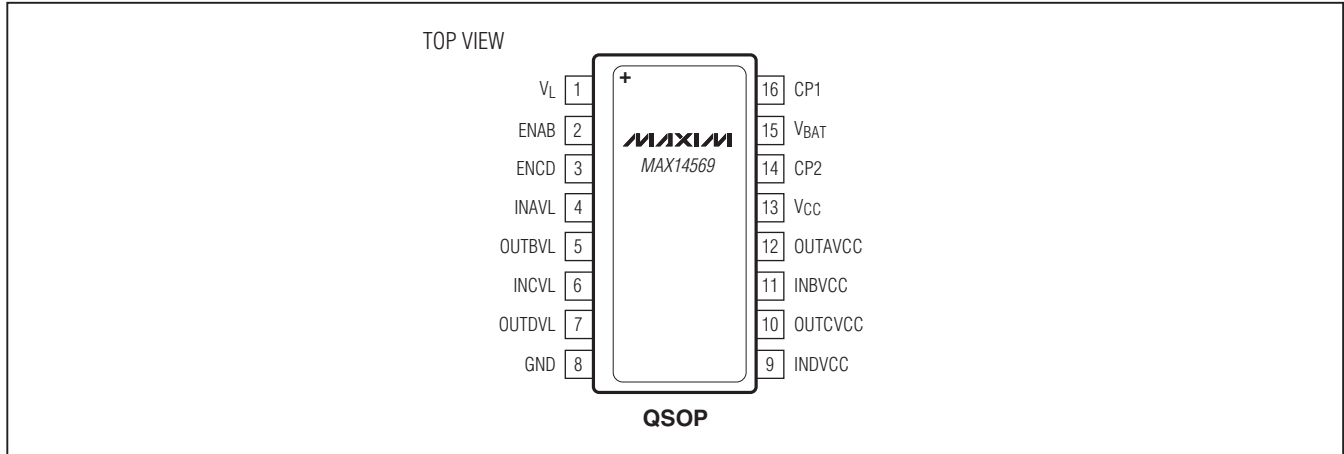
($V_{BAT} = 3.6V$, $V_L = 3V$, $C_{VBAT} = 1\mu F$, $C_{VCC} = 2.2\mu F$, $C_{VL} = 0.1\mu F$, connect $0.47\mu F$ capacitor between CP1 and CP2, data rate = 1Mbps, $T_A = +25^\circ C$, unless otherwise noted.)

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Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	VL	Logic Supply Voltage, +1.6V to +5.5V. Bypass VL to GND with a 0.1μF capacitor placed as close as possible to the device.
2	ENAB	Enable Input for A and B Ports. Drive ENAB low for shutdown mode, or drive ENAB high for normal operation.
3	ENCD	Enable Input for C and D Ports. Drive ENCD low for shutdown mode, or drive ENCD high for normal operation.
4	INAVL	Input A Port. Referenced to VL.
5	OUTBVL	Output B Port. Referenced to VL.
6	INCVL	Input C Port. Referenced to VL.
7	OUTDVL	Output D Port. Referenced to VL.
8	GND	Ground
9	INDVCC	Input D Port. Referenced to VCC.
10	OUTCVCC	Output C Port. Referenced to VCC.
11	INBVCC	Input B Port. Referenced to VCC.
12	OUTAVCC	Output A Port. Referenced to VCC.
13	VCC	Charge-Pump Output. Bypass VCC to GND with a 2.2μF ceramic capacitor placed as close as possible to the VCC pin to have high ESD protection on OUTAVCC, INBVCC, OUTCVCC, and INDVCC pins.
14	CP2	External Charge-Pump Capacitor Connection
15	VBAT	Battery Input, +2.3V to +5.5V. Bypass VBAT to GND with a 1μF capacitor placed as close as possible to the device.
16	CP1	External Charge-Pump Capacitor Connection

Dual-Pair LLT with Charge Pump and High-ESD Protection

Detailed Description

The MAX14569 is a dedicated dual-pair unidirectional logic-level translator that is ideal for automatic remote-metering applications. Externally applied voltage V_L and regulated output voltage V_{CC} set the logic levels on either side of the device.

The device boosts the V_{BAT} supply input voltage to a charge-pump-regulated output, V_{CC} . Logic-high signals present on the V_L side of the device appear as a high-voltage logic signals on the V_{CC} side of the device and vice versa.

The device has two pairs of logic-level translators in back-to-back configuration: one logic-level translator from a low voltage to a high voltage and the other logic-level translator from a high voltage to a low voltage.

The device features an extreme power-saving mode that reduces supply current to a typical $0.01\mu A$. The device also features thermal short-circuit protection on the V_{CC} side for enhanced protection in applications that route signals externally.

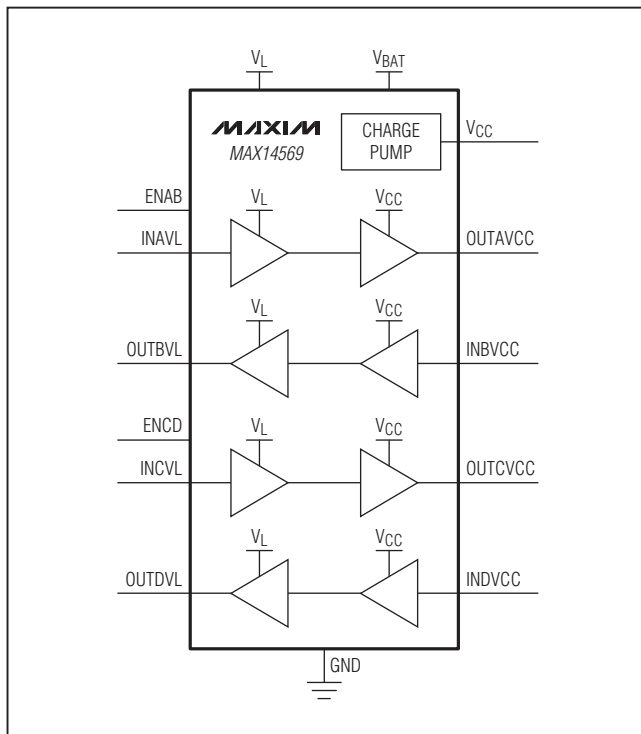
Level Translation

For proper operation, ensure that $2.3V \leq V_{BAT} \leq 5.5V$, $1.6V \leq V_L \leq 5.5V$. The device enters low-power shutdown mode when $ENAB = ENCD = GND$ (see the *Functional Table*). In shutdown mode, the $INAVL$, $INBVCC$, $INCVL$, $INDVCC$, $OUTAVCC$ and $OUTCVCC$ are in high-impedance mode and the $OUTBVL$ and $OUTDVL$ are pulled down to GND. The maximum data rate depends heavily on the load capacitance (see the rise/fall times in the *Typical Operating Characteristics*), output impedance of the driver, and the operating voltage range.

Output Load Requirements

The device is designed to drive a wide variety of load types including a high capacitive load. To protect the V_{CC} outputs ($OUTAVCC$, $OUTCVCC$) from a harsh external environment, the V_{CC} outputs are ruggedized with a high ESD-capable output structure. When the high capacitive load is connected to the V_{CC} output side, the current is limited by the charge-pump circuit along with the output driver impedance. The device is also protected by the thermal protection.

Functional Diagram



Functional Table

INPUTS		DRIVERS OUTPUT EVENTS
ENAB	ENCD	
Low	Low	Device is in shutdown OUTAVCC, OUTCVCC: high impedance OUTBVL, OUTDVL: pulldown to GND
Low	High	OUTAVCC: high impedance OUTBVL: pulldown to GND INCVL to OUTCVCC INDVCC to OUTDVL
High	Low	INAVL to OUTAVCC INBVCC to OUTBVL OUTCVCC: high impedance OUTDVL: pulldown to GND
High	High	INAVL to OUTAVCC INBVCC to OUTBVL INCVL to OUTCVCC INDVCC to OUTDVL

Dual-Pair LLT with Charge Pump and High-ESD Protection

Shutdown Mode

The device features two enable inputs (ENAB, ENCD) that place the device into a low-power shutdown mode when both are driven low. If either ENAB or ENCD is pulled high, the internal charge pump starts working and generates 5V on VCC. When both ENAB and ENCD are driven low, the MAX14569 enters shutdown mode and draws a minimum current from V_L and V_{BAT}. To minimize supply current in shutdown mode, connect INAVL and INCVL to ground.

Charge Pump

The internal charge pump provides 5V on VCC when V_{BAT} is between 2.7V and 4.5V. When V_{BAT} is between 2.3V and 2.7V, VCC is twice the voltage of V_{BAT}. The output is regulated to 5V as long as the battery voltage supports it.

Thermal Protection

The device features thermal shutdown function necessary to protect the device. When the junction temperature exceeds +150°C (typ), the charge pump turns off and OUTAVCC, OUTBVL, OUTCVCC, OUTDVL are low. This limits the device temperature from rising further. When the temperature drops 20°C (typ) below +150°C (typ), the device resumes normal operation.

Applications Information

Layout Recommendations

Use standard high-speed layout practices when laying out a board with the device. For example, to minimize line coupling, place all other signal lines not connected to the device at least 1x the substrate height of the PCB away from the input and output lines of the device.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_L to ground with a 0.1μF ceramic capacitor, V_{BAT} to ground with a 1μF ceramic capacitor, and VCC to ground with a 2.2μF ceramic capacitor. Place all capacitors as close as possible to the power-supply inputs.

±25kV ESD Protection

As with all Maxim devices, ESD protection structures are incorporated on all pins to protect against electrostatic

discharges encountered during handling and assembly. The OUTAVCC, INBVCC, OUTCVCC, INDVCC pins have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±25kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the device keeps working without latchup or damage.

ESD protection can be tested in various ways. The OUTAVCC, INBVCC, OUTCVCC, and INDVCC pins are characterized for protection to the following limits:

- ±25kV using the Human Body Model
- ±15kV using the Air-Gap Discharge Method specified in IEC 61000-4-2
- ±12kV using the Contact Discharge Method specified in IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 3 shows the Human Body Model, and Figure 4 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2, because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 5 shows the IEC 61000-4-2 model, and Figure 6 shows the current waveform for the ±8kV, IEC 61000-4-2, level 4, ESD Contact Discharge Method.

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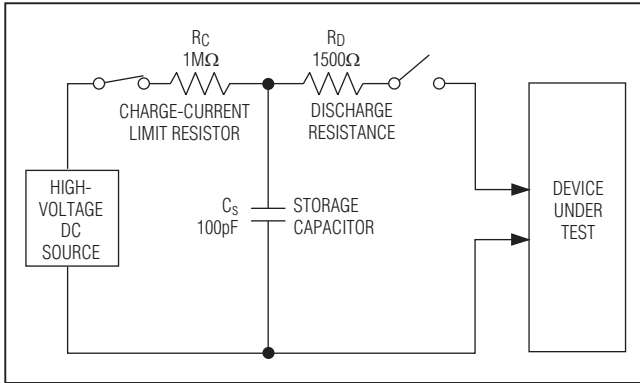


Figure 3. Human Body ESD Test Model

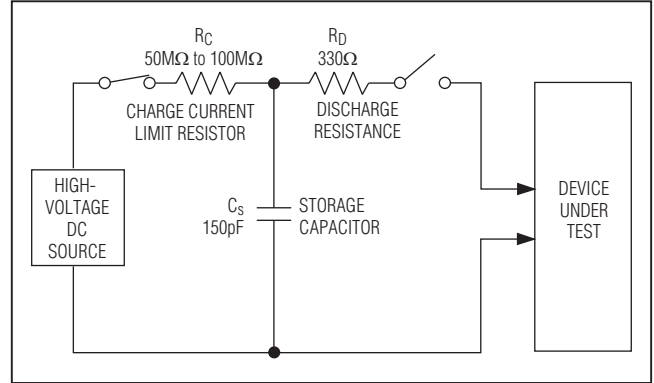


Figure 5. IEC 61000-4-2 ESD Test Model

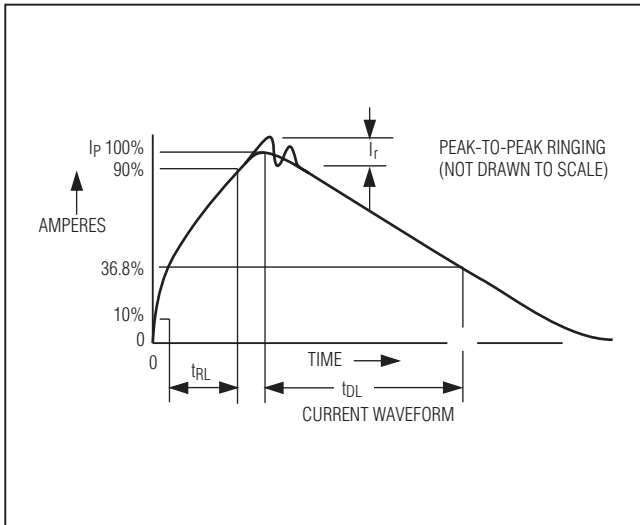


Figure 4. Human Body Current Waveform

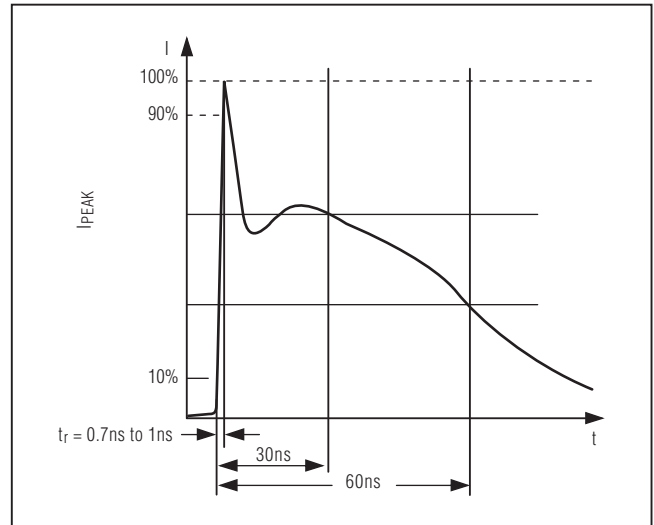


Figure 6. IEC 61000-4-2 ESD Generator Current Waveform

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 QSOP	E16+4	21-0055	90-0167

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/10	Initial release	—

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