MAX14982

All-In-One Ruggedized 5GT/s 2:1/1:2 PCIe Mux and Redriver with Equalization

General Description

The MAX14982 integrates MUX and redriver functionalities, offering an all-in-one solution capable of switching between multiple hosts or sinks and overcoming circuit-board losses. The solution is ideal for switching and redriving high-speed PCIe® 5.0GT/s (Gigatransfers per second) signals and operates from a single +3.3V supply.

The IC features bidirectional redrivers with built-in independent programmable equalization, output preemphasis, and boost that overcome transmission line noise while preserving signal integrity at the receiver.

The MAX14982 utilizes advanced power-saving techniques where power consumption is reduced by entering standby mode when no drive is connected. The device also features flow-through pin outs to simplify routing and increase layout flexibility.

The MAX14982 is available in a space-saving, 42-pin 3.5mm x 9mm, TQFN package optimal reducing layout complexity as compared to stand-alone mux and redriver solutions. The MAX14982 is specified over the -40°C to +85°C industrial operating temperature range.

Applications

- Industrial/Embedded PCs
- Ruggedized Server/Carrier Boards
- Test Equipment
- Medical Equipment

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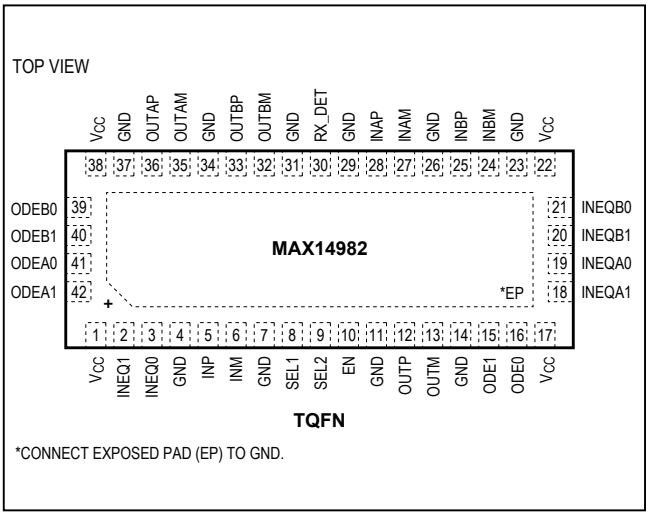
Benefits and Features

- Fully Integrated for Ease of Use and Design Flexibility
  - Capable of Switching Between Multiple Hosts and Sinks While Overcoming Board Losses
  - Optimized for PCIe Gen II (5.0GT/s); Gen I (2.5GT/s) Compatible
  - Three Levels of Independent Programmable Input Equalization and Output Deemphasis Up to 6bB
- High Level of Performance to Overcome Noise in Lossy Channels
  - Random Jitter: 0.5ps$_{RMS}$ (typ)
  - Deterministic Jitter: 20ps$_{p-p}$ (typ)
  - Equalization Permits Placement Up to 30in FR4
- Robust Solution for Harsh Environments
  - Industrial Temperature Rated: -40°C to +85°C
  - ±2.5kV Human Body Model (HBM) Protection on All Pins
  - Housed in a Flow-Through (3.5mm x 9.5mm) TQFN Package for Resistance to Vibrations/ Shocks

Pin Configuration



***Ordering Information* appears at end of data sheet.**

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Absolute Maximum Ratings

(Voltages referenced to GND.)
V_{CC} ..... -0.3V to +4.0V
All Other Pins (Note 1) ..... -0.3V to (V_{CC} + 0.3V)
Continuous Current, IN_P, IN_M, OUT_P, OUT_M..... ±30mA
Peak Current, IN_P, IN_M, OUT_P, OUT_M (for 10kHz, 1% duty cycle) ..... ±100mA
Continuous Power Dissipation (T_A = +70°C)
42-Pin TQFN (derate 34.5mW/°C above +70°C) 2758mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 2) ..... +2°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 2) ..... +29°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature Range ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Note 1: All I/O pins are clamped by internal diodes.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = +3.0V to +3.6V, C_{CL} = 75nF coupling capacitor on each output, R_L = 50Ω on each output, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PERFORMANCE							
Power-Supply Range	V_{CC}			3.0		3.6	V
Supply Current	I_{CC}	EN = V_{CC}	INEQ_ = ODE_ = GND		120	150	mA
			INEQ_ = ODE_ = V_{CC}		160	205	
		EN = GND			50		
Input Impedance, Differential	$Z_{RX-DIFF-DC}$	DC		80	100	120	Ω
Output Impedance, Differential	$Z_{TX-DIFF-DC}$	DC		80	100	120	Ω
Common-Mode Resistance to GND, Input Terminations Not Powered	$Z_{RX-HIGH-IMP-DC}$	V_{IN_P} = V_{IN_M} = -150mV to +200mV		50			kΩ
Common-Mode Resistance to GND, Input Terminations Powered	Z_{RX-DC}	DC		40	50	60	Ω
Output Short-Circuit Current	$I_{TX-SHORT}$	Single-ended (Note 4)		90			mA
Common-Mode Delta, Between Active and Idle States	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$			-100		+100	mV
DC Output Offset, During Active State	$V_{TX-ACTIVE-DIFF-DC}$	ABS(V_{OUT_P} - V_{OUT_M})		-25		+25	mV
DC Output Offset, During Electrical Idle	$V_{TX-IDLE-DIFF-DC}$	ABS(V_{OUT_P} - V_{OUT_M})		-10		+10	mV
AC PERFORMANCE							
Input Return Loss, Differential	$RL_{RX-DIFF}$	0.05GHz < f ≤ 1.25GHz (Note 4)		10			dB
		1.25GHz < f ≤ 2.5GHz (Note 4)		8			

Electrical Characteristics (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 75nF coupling capacitor on each output, R_L = 50Ω on each output, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Return Loss, Common Mode	RL_{RX-CM}	0.05GHz < f ≤ 2.5GHz (Note 4)	6			dB
Output Return Loss, Differential	$RL_{TX-DIFF}$	0.05GHz < f ≤ 1.25GHz (Note 4)	10			dB
		1.25GHz < f ≤ 2.5GHz (Note 4)	8			
Output Return Loss, Common Mode	RL_{TX-CM}	0.05GHz < f ≤ 2.5GHz (Note 4)	6			dB
Differential Input Signal Range, Redriver Operation	$V_{RX-DIFF-PP}$	0.05GHz < f ≤ 2.5GHz	150		1200	mV_{P-P}
Differential Output Voltage, Full Swing, No Deemphasis	$V_{TX-DIFF-PP}$	2 x ABS(V_{OUT_P} - V_{OUT_M}), ODE_1 = GND, ODE_0 = V_{CC} (see Table 1), f = 500MHz	800	1000	1300	mV_{P-P}
Differential Output Voltage, Low Swing, No Deemphasis	$V_{TX-DIFF-PP-LOW}$	2 x ABS(V_{OUT_P} - V_{OUT_M}), ODE_1 = ODE_0 = GND (see Table 1), f = 500MHz	600	750	1000	mV_{P-P}
Output Deemphasis Ratio, 0dB	$V_{TX-DE-RATIO-0dB}$	ODE_1 = GND, ODE_0 = V_{CC} or GND, Figure 1 (see Table 1)		0		dB
Output Deemphasis Ratio, 3.5dB	$V_{TX-DE-RATIO-3.5dB}$	ODE_1 = V_{CC}, ODE_0 = GND, Figure 1 (see Table 1)		3.5		dB
Output Deemphasis Ratio, 6dB	$V_{TX-DE-RATIO-6dB}$	ODE_1 = V_{CC}, ODE_0 = V_{CC}, Figure 1 (see Table 1)		6		dB
Input Equalization, 0dB	$V_{RX-EQ-0dB}$	INEQ_1 = GND, INEQ_0 = GND or V_{CC} (see Table 2)		0		dB
Input Equalization, 3.5dB	$V_{RX-EQ-3.5dB}$	INEQ_1 = V_{CC}, INEQ_0 = GND (see Table 2)		3.5		dB
Input Equalization, 6dB	$V_{RX-EQ-6dB}$	INEQ_1 = V_{CC}, INEQ_0 = V_{CC} (see Table 2)		6		dB
Output Common-Mode Voltage	$V_{TX-CM-AC-PP}$	MAX(V_{OUT_P} + V_{OUT_M})/2 - MIN(V_{OUT_P} + V_{OUT_M})/2 (Note 4)			100	mV_{P-P}
Propagation Delay	t_{PD}	(Note 4)	160	280	400	ps
Rise/Fall Time	$t_{TX-RISE-FALL}$	(Note 5)	30			ps
Rise/Fall Time Mismatch	$t_{TX-RF-MISMATCH}$	(Notes 4, 5)			20	ps
Deterministic Jitter	$t_{TX-DJ-DD}$	K28.5 ≤ pattern, AC-coupled, R_L = 50Ω, effects of deemphasis deembedded (Note 4), 5GT/s		20		ps_{P-P}
Random Jitter	$t_{TX-RJ-DD}$	D10.2 pattern, f > 1.5MHz		0.5	1.4	ps_{RMS}
Electrical Idle Entry Delay	$t_{TX-IDLE-SET-TO-IDLE}$	From input to output		15		ns

Electrical Characteristics (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 75nF coupling capacitor on each output, R_L = 50Ω on each output, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Electrical Idle Exit Delay	$t_{TX-IDLE-TO-DIFF-DATA}$	From input to output		8		ns
Electrical Idle Detect Threshold	$V_{TX-IDLE-THRESH}$		40	100	130	mV_{P-P}
Output Voltage During Electrical Idle (AC)	$V_{TX-IDLE-DIFF-AC-P}$	ABS(V_{OUT_P} - V_{OUT_M})			35	mV_{P-P}
Receiver Detect Pulse Amplitude	$V_{TX-RCV-DETECT}$	Voltage change in positive direction (Note 4)		600		mV
Receiver Detect Pulse Width				100		ns
Receiver Detect Retry Period				200		ns
CONTROL LOGIC						
Input Logic-Level Low	V_{IL}				0.6	V
Input Logic-Level High	V_{IH}		1.4			V
Input Logic Hysteresis	V_{HYST}			130		mV
Input Pulldown Resistor	R_{DOWN}		37.5	60	150	kΩ
ESD PROTECTION						
ESD Voltage		Human Body Model		±2.5		kV

Note 3: All devices are 100% production tested at T_A = -40°C to +85°C. Specifications for all temperature limits are guaranteed by design.

Note 4: Guaranteed by design.

Note 5: Rise and fall times are measured using 20% and 80% levels.

Timing Diagram

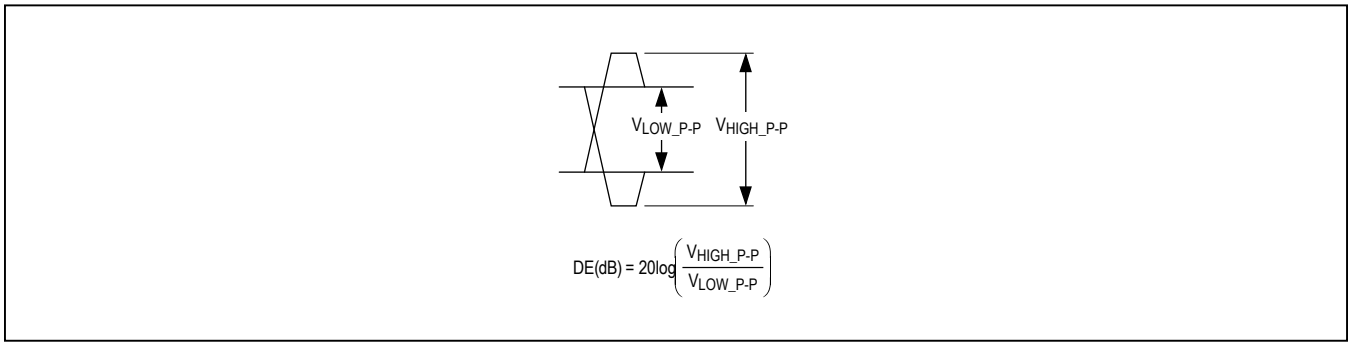
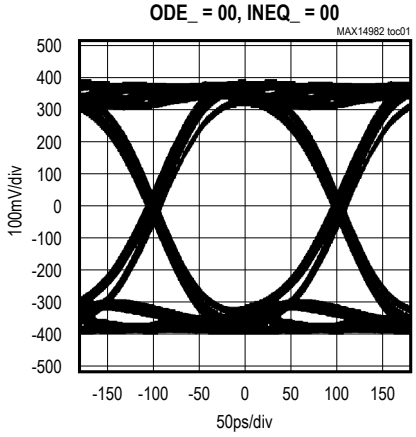


Figure 1. Illustration of Output Deemphasis

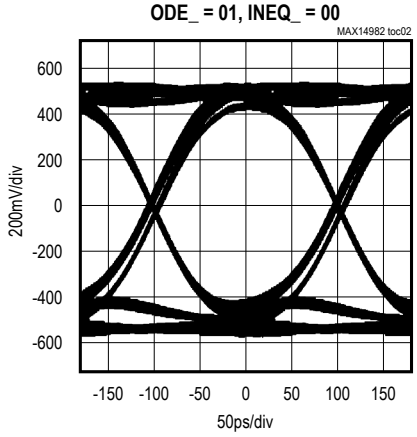
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

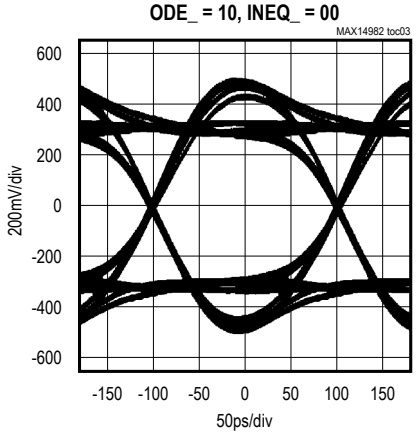
V_{IN} = 200mV$_{P-P}$, 5GT/s, ODE_ = 00, INEQ_ = 00



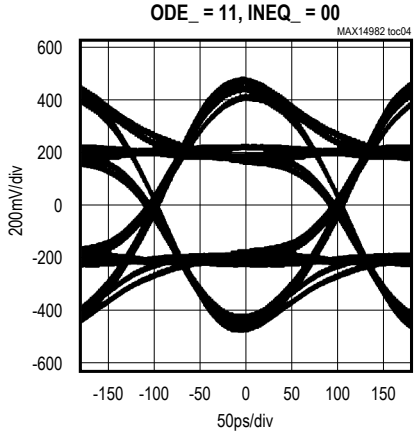
V_{IN} = 200mV$_{P-P}$, 5GT/s, ODE_ = 01, INEQ_ = 00



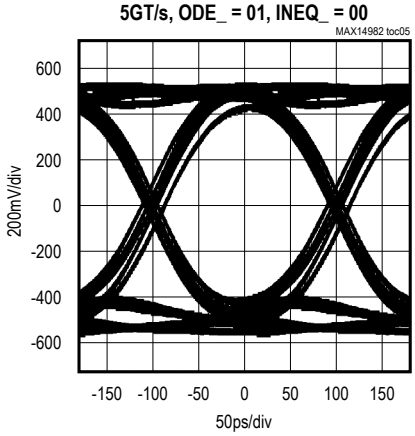
V_{IN} = 200mV$_{P-P}$, 5GT/s, ODE_ = 10, INEQ_ = 00



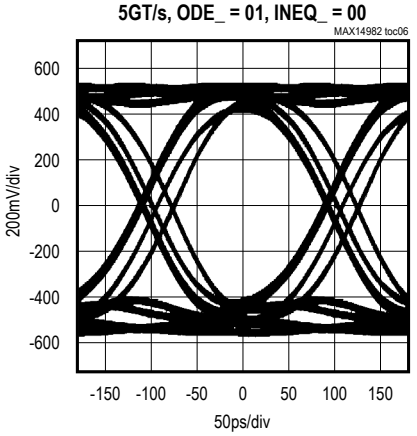
V_{IN} = 200mV$_{P-P}$, 5GT/s, ODE_ = 11, INEQ_ = 00



V_{IN} = 500mV$_{P-P}$ WITH 6in STRIPLINE, 5GT/s, ODE_ = 01, INEQ_ = 00



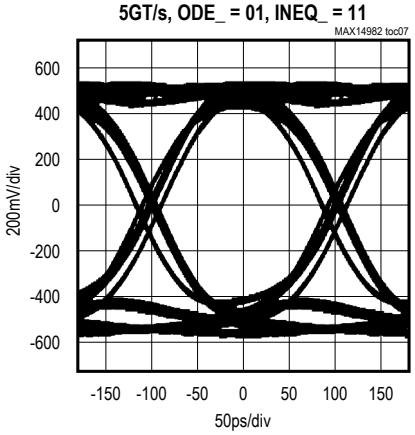
V_{IN} = 500mV$_{P-P}$ WITH 19in STRIPLINE, 5GT/s, ODE_ = 01, INEQ_ = 00



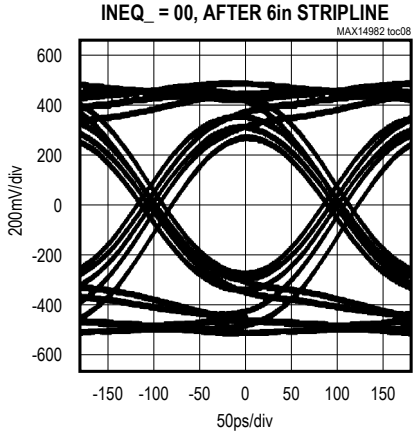
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

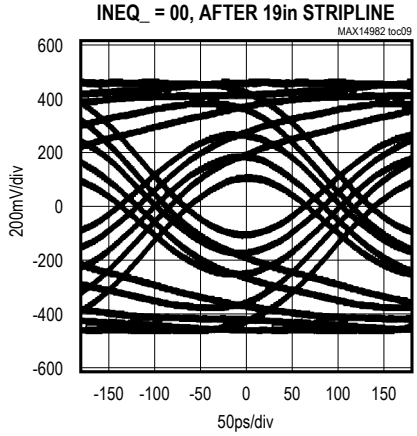
V_{IN} = 500mV$_{P-P}$ WITH 19in STRIPLINE, 5GT/s, ODE_ = 01, INEQ_ = 11



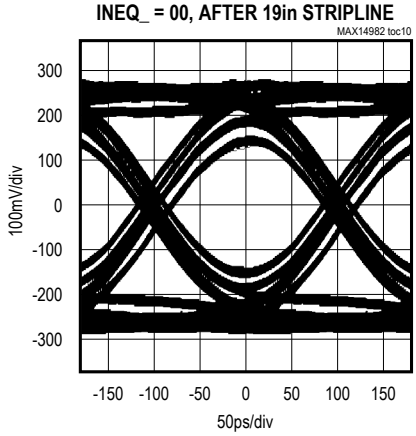
V_{IN} = 500mV$_{P-P}$, 5GT/s, ODE_ = 01, INEQ_ = 00, AFTER 6in STRIPLINE



V_{IN} = 500mV$_{P-P}$, 5GT/s, ODE_ = 01, INEQ_ = 00, AFTER 19in STRIPLINE



V_{IN} = 500mV$_{P-P}$, 5GT/s, ODE_ = 11, INEQ_ = 00, AFTER 19in STRIPLINE



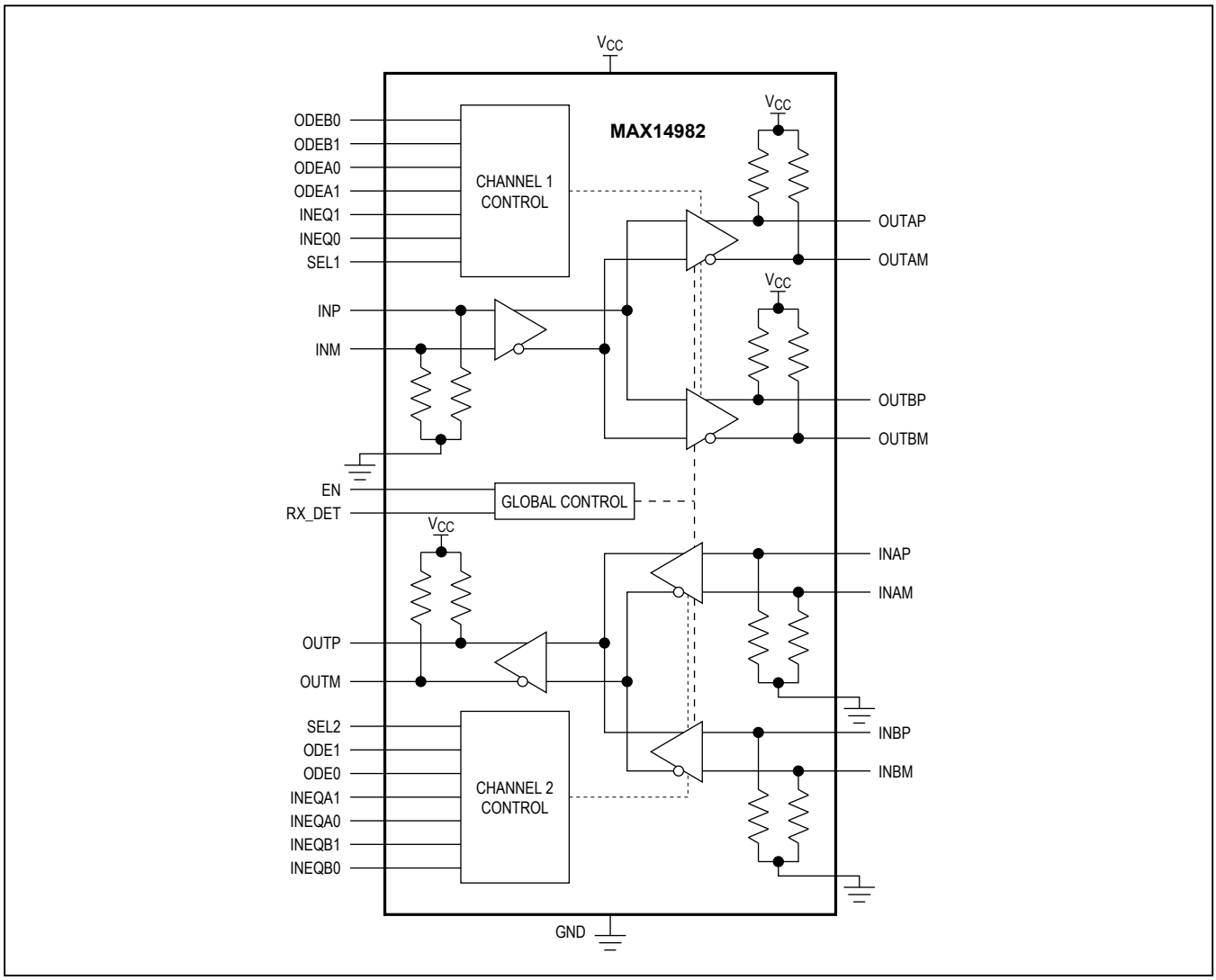
Pin Description

PIN	NAME	FUNCTION
1, 17, 22, 38	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with 1µF and 0.01µF capacitors in parallel as close to the device as possible, recommended on each V_{CC} pin.
2	INEQ1	Channel 1 Input Equalization Control MSB. See Table 2. INEQ1 is internally pulled down by a 60kΩ (typ) resistor.
3	INEQ0	Channel 1 Input Equalization Control LSB. See Table 2. INEQ0 is internally pulled down by a 60kΩ (typ) resistor.
4, 7, 11, 14, 23, 26, 29, 31, 34, 37	GND	Ground
5	INP	Channel 1 Noninverting Input
6	INM	Channel 1 Inverting Input
8	SEL1	Channel 1 Active Output Selection Input. Drive SEL1 low to activate A outputs. Drive SEL1 high to activate B outputs. SEL1 is internally pulled down by a 60kΩ (typ) resistor.
9	SEL2	Channel 2 Active Input Selection Input. Drive SEL2 low to activate A inputs. Drive SEL2 high to activate B inputs. SEL2 is internally pulled down by a 60kΩ (typ) resistor.
10	EN	Enable Input. Drive EN low for reduced power standby mode. Drive EN high for normal operation. EN is internally pulled down by a 60kΩ (typ) resistor.
12	OUTP	Channel 2 Noninverting Output
13	OUTM	Channel 2 Inverting Output
15	ODE1	Channel 2 Output Deemphasis Control MSB. See Table 1. ODE1 is internally pulled down by a 60kΩ (typ) resistor.
16	ODE0	Channel 2 Output Deemphasis Control LSB. See Table 1. ODE0 is internally pulled down by a 60kΩ (typ) resistor.
18	INEQA1	Channel 2 Input A Equalization Control MSB. See Table 2. INEQA1 is internally pulled down by a 60kΩ (typ) resistor.
19	INEQA0	Channel 2 Input A Equalization Control LSB. See Table 2. INEQA0 is internally pulled down by a 60kΩ (typ) resistor.
20	INEQB1	Channel 2 Input B Equalization Control MSB. See Table 2. INEQB1 is internally pulled down by a 60kΩ (typ) resistor.
21	INEQB0	Channel 2 Input B Equalization Control LSB. See Table 2. INEQB0 is internally pulled down by a 60kΩ (typ) resistor.
24	INBM	Channel 2 Inverting Input B
25	INBP	Channel 2 Noninverting Input B
27	INAM	Channel 2 Inverting Input A
28	INAP	Channel 2 Noninverting Input A
30	RX_DET	Receiver Detection Control Bit. Toggle RX_DET to initiate receiver detection. RX_DET is internally pulled down by a 60kΩ (typ) resistor.
32	OUTBM	Channel 1 Inverting Output B
33	OUTBP	Channel 1 Noninverting Output B
35	OUTAM	Channel 1 Inverting Output A
36	OUTAP	Channel 1 Noninverting Output A
39	ODEB0	Channel 1 Output B Deemphasis Control LSB. See Table 1. ODEB0 is internally pulled down by a 60kΩ (typ) resistor.

Pin Description (continued)

PIN	NAME	FUNCTION
40	ODEB1	Channel 1 Output B Deemphasis Control MSB. See Table 1. ODEB1 is internally pulled down by a 60kΩ (typ) resistor.
41	ODEA0	Channel 1 Output A Deemphasis Control LSB. See Table 1. ODEA0 is internally pulled down by a 60kΩ (typ) resistor.
42	ODEA1	Channel 1 Output A Deemphasis Control MSB. See Table 1. ODEA1 is internally pulled down by a 60kΩ (typ) resistor.
—	EP	Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to maximize thermal performance as well as good ground conductivity to the device.

Functional Diagram



Detailed Description

The MAX14982 is an active 2:1/1:2 multiplexer designed to equalize and redrive PCIe signals up to 5.0GT/s. The device features PCIe-required electrical idle and receiver detection on each channel, and improves signal integrity at the receiver through independent programmable input equalization and output deemphasis.

Enable Input (EN)

The MAX14982 features an active-high enable input (EN). EN has an internal pulldown resistor of 60kΩ (typ). When EN is driven low or left unconnected, the IC enters reduced power standby mode and the redrivers are disabled. Drive EN high for normal operation.

Active Input/Output Select (SEL1, SEL2)

SEL1 selects the active output for channel 1 and SEL2 selects the active input for channel 2. Drive SEL1 or SEL2 low or leave unconnected to activate A inputs or outputs. Drive SEL1 or SEL2 high to activate B inputs or outputs. SEL1 and SEL2 have internal pulldown resistors of 60kΩ (typ).

Table 1. Output Deemphasis

ODE_1	ODE_0	OUTPUT DEEMPHASIS (dB)
0	0	0, low swing
0	1	0, full swing
1	0	3.5, full swing
1	1	6, full swing

Table 2. Input Equalization

INEQ_1	INEQ_0	INPUT EQUALIZATION (dB)
0	X	0
1	0	3.5
1	1	6

X = Don't Care

Table 3. Receiver Detection

RX_DET/ SEL1/SEL2	EN	DESCRIPTION
X	0	Receiver detection inactive
0	1	Following a rising or falling edge; indefinite retry until receiver detected
Rising or falling edge	1	Initiate receiver detection
1	1	Following a rising or falling edge; indefinite retry until receiver detected

X = Don't Care

Programmable Output Deemphasis (ODE_0, ODE_1)

The MAX14982 features independent programmable output deemphasis capable of providing 0dB, 3.5dB, or 6dB deemphasis on any channel. When both ODE_0 and ODE_1 are driven low or left unconnected, the output is in low-swing mode (750mV typ) (see Table 1). ODE0, ODE1, ODEA0, ODEA1, ODEB0, and ODEB1 have internal pulldown resistors of 60kΩ (typ).

Programmable Input Equalization (INEQ_0, INEQ_1)

The MAX14982 features independent programmable input equalization capable of providing 0dB, 3.5dB, or 6dB of high-frequency equalization on any channel (see Table 2.) INEQ0, INEQ1, INEQA0, INEQA1, INEQB0, and INEQB1 have internal pulldown resistors of 60kΩ (typ).

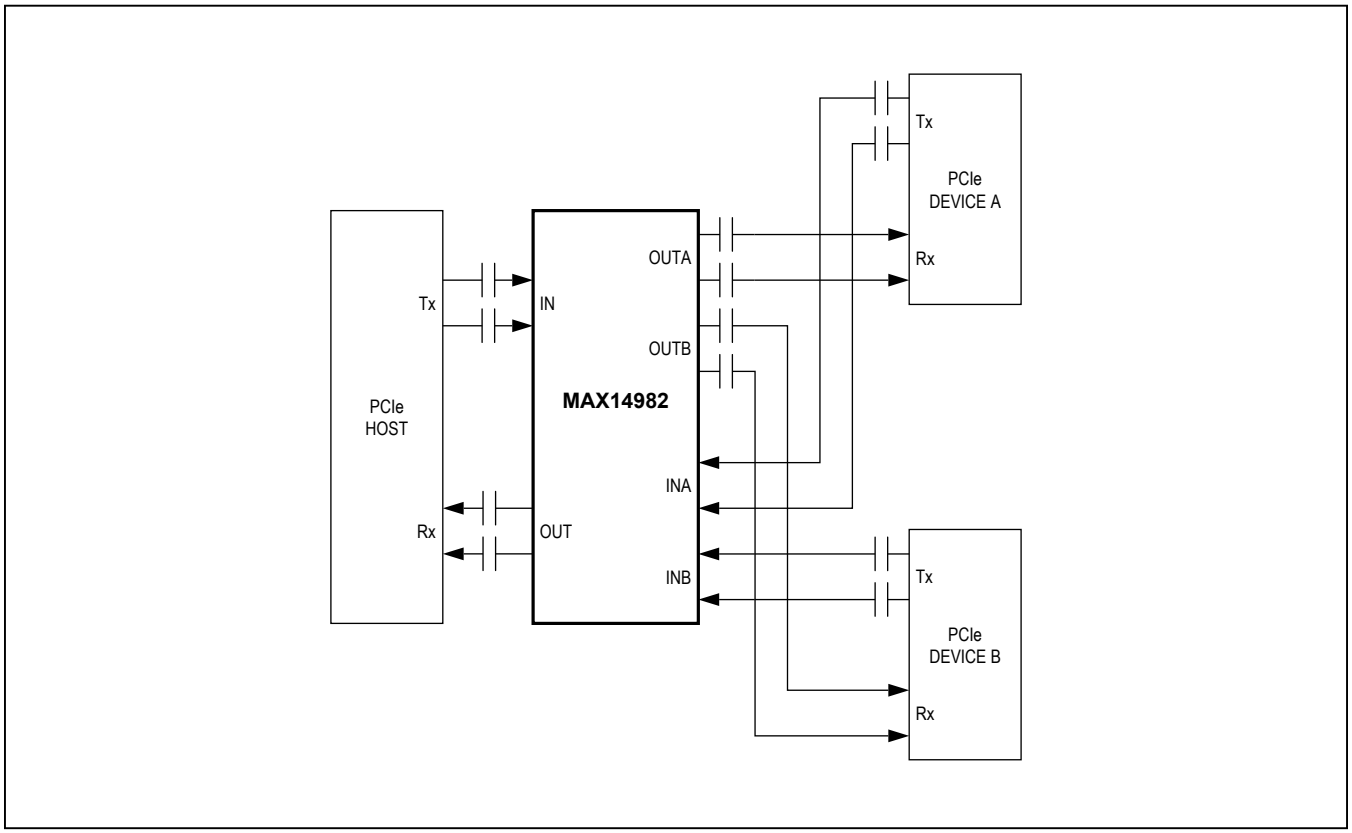
Receiver Detection (RX_DET)

The MAX14982 features receiver detection on each channel. Receiver detection initializes on the rising edge of EN, or upon initial power-up if EN is high. Receiver detection can also be initiated on a rising or falling edge of the RX_DET, SEL1, or SEL2 inputs when EN is high. During this time, the part remains in reduced power standby mode and the outputs are squelched, despite the logic-high state of EN. Once started, receiver detection repeats indefinitely on each channel. Once a receiver is detected on one of the channels, up to 2^{16} more attempts are made on the other channel. Upon receiver detection, channel output and electrical idle detection are enabled (see Table 3). RX_DET has an internal pulldown resistor of 60kΩ (typ).

Electrical Idle Detection

The IC features electrical idle detection to prevent unwanted noise from being redriven at the output. If the MAX14982 detects that the differential input has fallen below $V_{TX\text{-}IDLE\text{-}THRESH}$, the MAX14982 squelches the output. For differential input signals that are above $V_{TX\text{-}IDLE\text{-}THRESH}$, the MAX14982 turns on the output and redrives the signal.

Typical Application Circuit



Applications Information

Layout

Circuit board layout and design can significantly affect the performance of the MAX14982. Use good high-frequency design techniques, including minimizing ground inductance and using controlled-impedance transmission lines on data signals. It is recommended to run receive and transmit on different layers to minimize crosstalk and to place 1µF and 0.01µF power-supply bypass capacitors in parallel as close to V_{CC} as possible on each V_{CC} pin. Always connect V_{CC} to a power plane.

Exposed Pad Package

The exposed-pad, 42-pin TQFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed pad on the MAX14982 must be soldered to the circuit board ground plane for proper thermal performance. For more information on exposed-pad packages, refer to Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Always apply GND then V_{CC} before applying signals, especially if the signal is not current limited.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14982ETO+	-40ºC to +85ºC	42 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+4	21-0140	90-0012

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/13	Initial release	—
1	1/15	Updated *Ordering Information* table	11