EVALUATION KIT AVAILABLE

MAX15003

Triple-Output Buck Controller with Tracking/Sequencing

General Description

The MAX15003 is a triple-output, pulse-width-modulated (PWM), step-down DC-DC controller with tracking and sequencing capability. The device operates over the input voltage range of 5.5V to 23V or 5V ±10%. Each PWM controller provides an adjustable output down to 0.6V and delivers up to 15A for each output with excellent load and line regulation. The MAX15003 is optimized for high-performance, small-size power management solutions.

The options of coincident tracking, ratiometric tracking, and output sequencing allow the tailoring of the power-up/power-down sequence depending on the system requirements. Each of the MAX15003 PWM sections utilizes a voltage-mode control scheme with external compensation allowing for good noise immunity and maximum flexibility with a wide selection of inductor values and capacitor types. Each PWM section operates at the same, fixed switching frequency that is programmable from 200kHz to 2.2MHz and can be synchronized to an external clock signal using the SYNC input. Each converter operating at up to 2.2MHz with 120° out-of-phase, increases the input capacitor ripple frequency up to 6.6MHz, thereby reducing the RMS input ripple current and the size of the input bypass capacitor requirement significantly.

The MAX15003 includes internal input undervoltage lockout with hysteresis, digital soft-start/soft-stop for glitch-free power-up and power-down of each converter. The power-on reset ($\overline{RESET}$) with an adjustable timeout period monitors all three outputs and provides a $\overline{RESET}$ signal to the processor when all outputs are within regulation. Protection features include lossless valley-mode current limit and hiccup mode output short-circuit protection.

The MAX15003 is available in a space-saving, 7mm x 7mm, 48-pin TQFN-EP package and is specified for operation over the -40°C to +125°C automotive temperature range. See the MAX15002 data sheet for a dual version of the MAX15003.

Applications

PCI Express® Host Bus Adapter Power Supplies

Networking/Server Power Supplies

Point-of-Load DC-DC Converters

Features

- **5.5V to 23V or 5V ±10% Input Voltage Range**
- **Triple-Output Synchronous Buck Controller**
- **Selectable In-Phase or 120° Out-of-Phase Operation**
- **Output Voltages Adjustable from 0.6V to 0.85V_{IN}**
- **Lossless Valley-Mode Current Sensing or Accurate Valley Current Sensing Using R_{SENSE}**
- **External Compensation for Maximum Flexibility**
- **Digital Soft-Start and Soft-Stop**
- **Sequencing or Coincident/Ratiometric V_{OUT} Tracking**
- **Individual PGOOD Outputs**
- **$\overline{RESET}$ Output with a Programmable Timeout Period**
- **200kHz to 2.2MHz Programmable Switching Frequency**
- **External Frequency Synchronization**
- **Hiccup Mode Short-Circuit Protection**
- **Space-Saving (7mm x 7mm) 48-Pin TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX15003ATM+	-40°C to +125°C	48 TQFN-EP* (7mm x 7mm)

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

***Note:** Devices are also available in a tape-and-reel packaging. Specify tape and reel by adding "T" to the part number when ordering. Tape-and-reel orders are available in 2.5k increments.*

Pin Configuration appears at end of data sheet.

PCI Express is a registered trademark of PCI-SIG Corporation.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-1048; Rev 1; 8/12

ABSOLUTE MAXIMUM RATINGS

IN, LX_, CSN_ to SGND .....-0.3V to +30V
BST_ to SGND .....-0.3V to +30V
BST_ to LX_ .....-0.3V to +6V
REG, DREG_, SYNC, EN_, RT, CT, $\overline{RESET}$, PHASE, SEL to SGND .....-0.3V to +6V
ILIM_, PGOOD_, FB_, COMP_, CSP_ to SGND .....-0.3V to +6V
DL_ to PGND_ .....-0.3V to ($V_{DREG\_}$ + 0.3V)
DH_ to LX_ .....-0.3V to ($V_{BST\_}$ + 0.3V)
PGND_ to SGND, PGND_ to Any Other PGND_ .....-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFN (derate 38.5mW/°C above +70°C) 3076.9mW*
Operating Junction Temperature Range .....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

**As per JEDEC51 standard (multilayer board).*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

48 TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....26°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1.3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 5.5V to 23V or V_{IN} = V_{REG} = 4.5V to 5.5V, $V_{DREG\_}$ = V_{REG}, $V_{PGND\_}$ = V_{SYNC} = V_{PHASE} = V_{SEL} = 0V, C_{REG} = 2.2µF, R_{RT} = 100kΩ, C_{CT} = 0.1µF, $R_{ILIM\_}$ = 60kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = 12V and T_A = T_J = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM SPECIFICATIONS						
Input Voltage Range	V_{IN}		5.5		23.0	V
		V_{IN} = V_{REG} = $V_{DREG\_}$ (Note 2)	4.5		5.5	V
Input Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} rising	3.95	4.05	4.15	V
Input Undervoltage Lockout Hysteresis				0.35		V
Operating Supply Current		V_{IN} = 12V, $V_{FB\_}$ = 0.8V, no switching		5	8	mA
Shutdown Supply Current		V_{IN} = 12V, EN_ = 0V, PGOOD_ unconnected		150	300	µA
REG VOLTAGE REGULATOR						
Output-Voltage Setpoint	V_{REG}	V_{IN} = 5.5V to 23V	4.9		5.2	V
Load Regulation		I_{REG} = 0 to 120mA, V_{IN} = 12V			0.2	V
DIGITAL SOFT-START/SOFT-STOP						
Soft-Start/Soft-Stop Duration				2048		Clocks
Reference Voltage Steps				64		Steps
ERROR TRANSCONDUCTANCE AMPLIFIER						
FB_, TRACK_ Input Bias Current			-250		+250	nA
FB_ Voltage Setpoint	V_{FB}	T_A = T_J = 0°C to +85°C	0.5945	0.6	0.6065	V
		T_A = T_J = -40°C to +125°C	0.590	0.6	0.608	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5.5V to 23V or V_{IN} = V_{REG} = 4.5V to 5.5V, $V_{DREG\_}$ = V_{REG}, $V_{PGND\_}$ = V_{SYNC} = V_{PHASE} = V_{SEL} = 0V, C_{REG} = 2.2µF, R_{RT} = 100kΩ, C_{CT} = 0.1µF, $R_{ILIM\_}$ = 60kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = 12V and T_A = T_J = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FB_ to COMP_ Transconductance				2.1		mS
COMP_ Output Swing			0.75		3.50	V
Open-Loop Gain				80		dB
Unity-Gain Bandwidth				10		MHz
DRIVERS						
DL_, DH_ Break-Before-Make Time		C_{LOAD} = 5nF		20		ns
DH1 On-Resistance		Low, sinking 100mA		0.9		Ω
		High, sourcing 100mA		1.3		
DH2 On-Resistance		Low, sinking 100mA		0.9		Ω
		High, sourcing 100mA		0.3		
DH3 On-Resistance		Low, sinking 100mA		0.9		Ω
		High, sourcing 100mA		1.3		
DL1 On-Resistance		Low, sinking 100mA		0.9		Ω
		High, sourcing 100mA		1.3		
DL2 On-Resistance		Low, sinking 100mA		0.9		Ω
		High, sourcing 100mA		1.3		
DL3 On Resistance		Low, sinking 100mA		0.9		Ω
		High, sourcing 100mA		1.3		
LX_ to PGND_ On-Resistance		Sinking 10mA		8		Ω
CURRENT-LIMIT AND HICCUP MODE						
Cycle-By-Cycle Valley Current-Limit Adjustment Range	V_{CL}	$V_{CL\_}$ = $V_{ILIM\_}$ / 10	50		300	mV
Cycle-By-Cycle Valley Current-Limit Threshold Tolerance		$V_{ILIM\_}$ = 0.5V	44		54	mV
		$V_{ILIM\_}$ = 3V	290		310	
ILIM_ Reference Current		$V_{ILIM\_}$ = 0 to 3V, T_A = T_J = +25°C		20		µA
ILIM_ Reference Current Temperature Coefficient				3333		ppm/°C
CSP_, CSN_ Input Bias Current		$V_{CSP\_}$ = 0V, $V_{CSN\_}$ = -0.3V	-20		+20	µA
Number of Cumulative Current-Limit Events to Hiccup	N_{CL}			8		
Number of Consecutive Non-Current-Limit Cycles to Clear N_{CL}	N_{CLR}			3		
Hiccup Timeout				4096		Clock periods
ENABLE/PHASE/SEL						
EN_ Threshold	V_{EN-TH}	EN_ rising	1.19	1.215	1.24	V
EN_ Threshold Hysteresis				0.12		V
EN_ Input Bias Current			-1		+1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5.5V to 23V or V_{IN} = V_{REG} = 4.5V to 5.5V, $V_{DREG\_}$ = V_{REG}, $V_{PGND\_}$ = V_{SYNC} = V_{PHASE} = V_{SEL} = 0V, C_{REG} = 2.2µF, R_{RT} = 100kΩ, C_{CT} = 0.1µF, $R_{ILIM\_}$ = 60kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = 12V and T_A = T_J = +25°C, unless otherwise noted.) (Note 1)

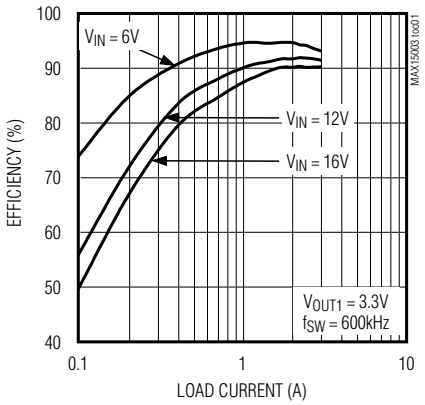
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PHASE Input Logic High			2			V
PHASE Input Logic Low					0.8	V
PHASE Input Bias Current			-1		+1	µA
SEL High Threshold			80			%V_{REG}
SEL Low Threshold					20	%V_{REG}
SEL Input Bias Current		Present only during startup	-100		+100	µA
PGOOD, $\overline{\text{RESET}}$ OUTPUTS						
FB_ For Threshold PGOOD_		FB_ falling	0.540	0.555	0.570	V
$\overline{\text{RESET}}$, PGOOD_ Output Low Level		Sinking 3mA			0.1	V
$\overline{\text{RESET}}$, PGOOD_ Leakage			-1		+1	µA
CT Charging Current			1.8	2.0	2.2	µA
CT Pulldown Resistance		Sinking 3mA			33	Ω
CT Threshold for $\overline{\text{RESET}}$ Delay		CT rising	1.8		2.6	V
		CT failling		1.2		
OSCILLATOR						
Switching Frequency Range (Each Converter)	f_{SW}	V_{SYNC} = 0V, f_{CLK} = 10^{11} / (R_{RT} + 1.75kΩ)	200		2200	kHz
Switching Frequency Accuracy (Each Converter)		f_{SW} ≤ 1500kHz	-5		+5	%
		f_{SW} ≥ 1500kHz	-7		+7	
Phase Delay		V_{PHASE} = 0V (DH1 rising to DH2 rising and DH2 rising to DH3 rising)		120		degrees
		V_{PHASE} = V_{REG} (DH1 rising to DH2 rising and DH2 rising to DH3 rising)		0		degrees
RT Voltage	V_{RT}	40kΩ < R_{RT} < 500kΩ		2		V
Minimum Controllable On-Time	$t_{ON(MIN)}$			75		ns
Minimum Off-Time	$t_{OFF(MIN)}$			150		ns
SYNC High-Level Voltage			2			V
SYNC Low-Level Voltage					0.8	V
SYNC Internal Pulldown Resistor			50	100	200	kΩ
SYNC Frequency Range		(Note 3)	0.6		6.9	MHz
SYNC Minimum On-Time				30		ns
SYNC Minimum Off-Time				30		ns
PWM Ramp Amplitude (Peak-to-Peak)				2		V
PWM Ramp Valley				1		V

Note 1: 100% production tested at T_A = T_J = +25°C and T_A = T_J = +125°C. Limits at other temperature are guaranteed by design.
Note 2: For 5V applications, connect REG directly to IN.
Note 3: The switching frequency is 1/3 of the SYNC frequency.

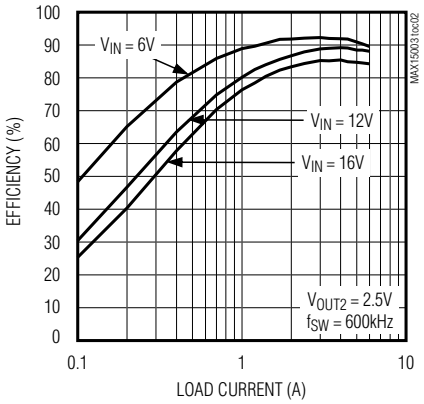
Typical Operating Characteristics

(Figure 8, V_{IN} = 12V, C_{REG} = 2.2µF, T_A = +25°C, unless otherwise noted.)

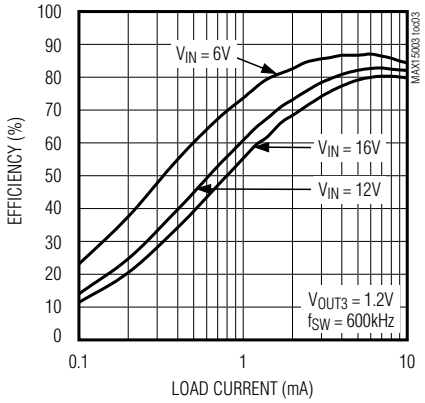
CONVERTER 1 EFFICIENCY vs. LOAD CURRENT



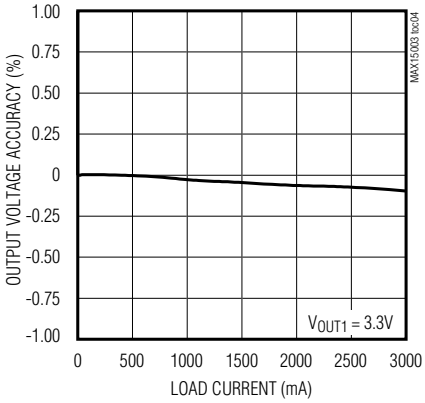
CONVERTER 2 EFFICIENCY vs. LOAD CURRENT



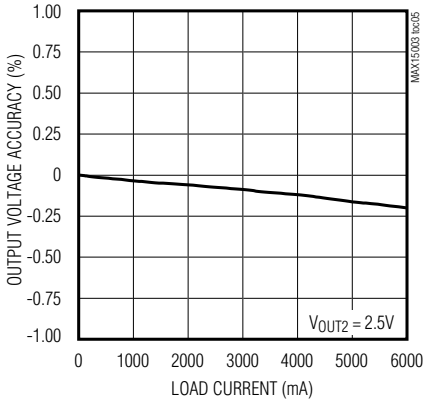
CONVERTER 3 EFFICIENCY vs. LOAD CURRENT



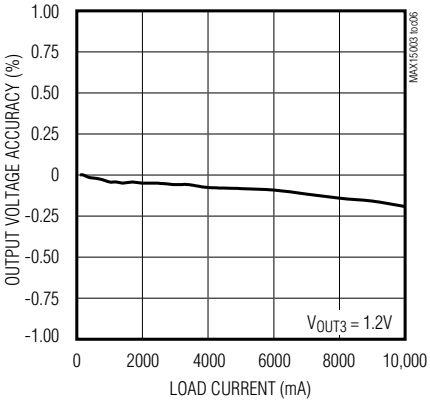
CONVERTER 1 LOAD REGULATION



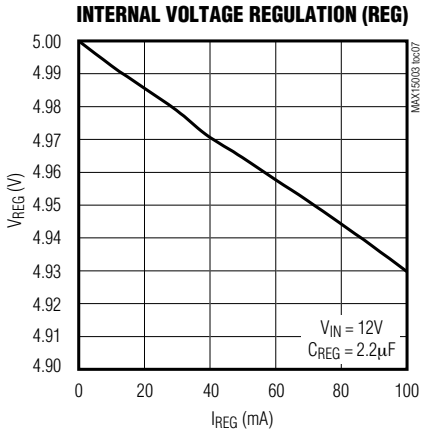
CONVERTER 2 LOAD REGULATION



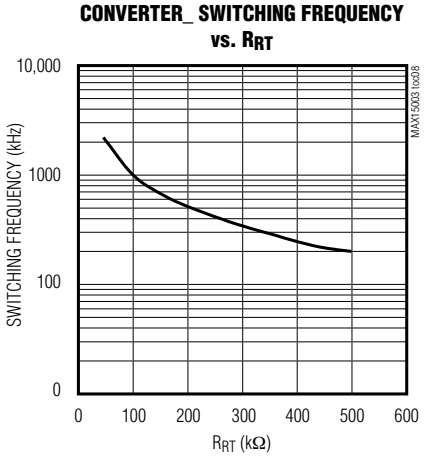
CONVERTER 3 LOAD REGULATION



INTERNAL VOLTAGE REGULATION (REG)



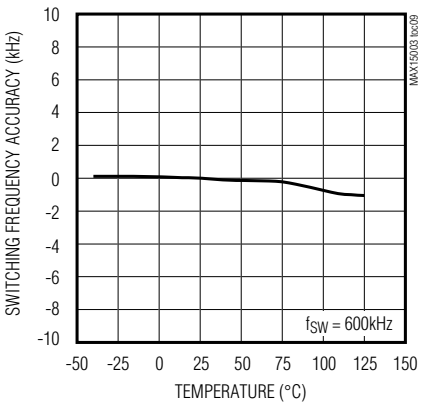
CONVERTER_ SWITCHING FREQUENCY vs. R_{RT}



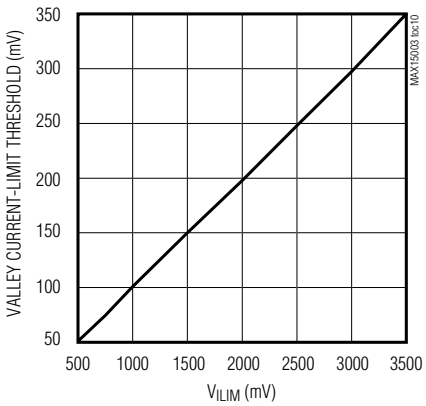
Typical Operating Characteristics (continued)

(Figure 8, V_{IN} = 12V, C_{REG} = 2.2µF, T_A = +25°C, unless otherwise noted.)

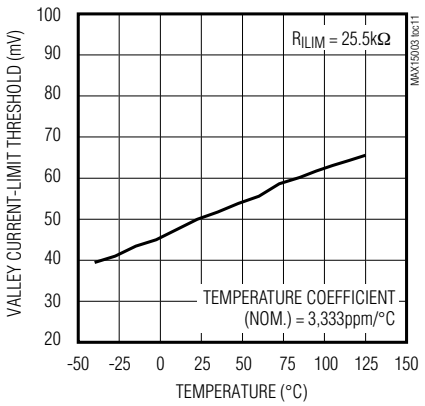
SWITCHING FREQUENCY ACCURACY vs. TEMPERATURE



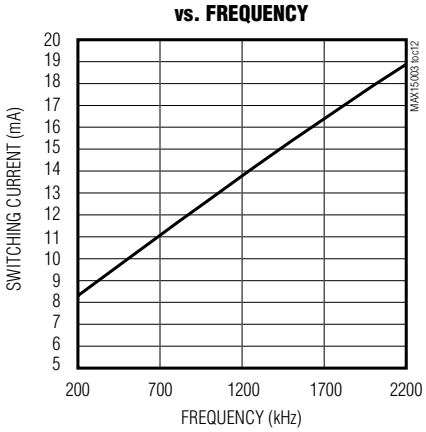
VALLEY CURRENT-LIMIT THRESHOLD vs. V_{ILIM}



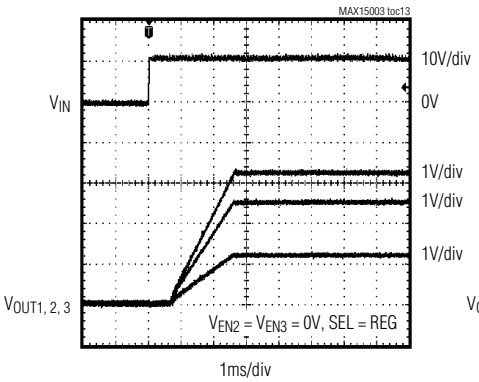
VALLEY CURRENT-LIMIT THRESHOLD vs. TEMPERATURE



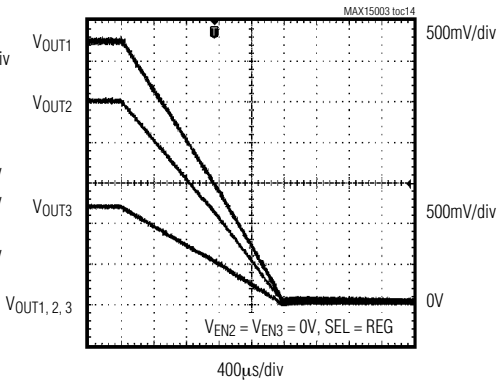
SWITCHING CURRENT vs. FREQUENCY



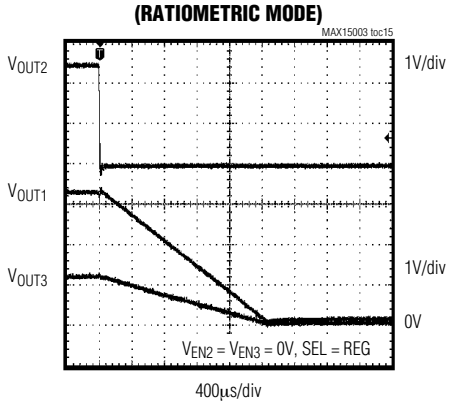
RATIOMETRIC STARTUP



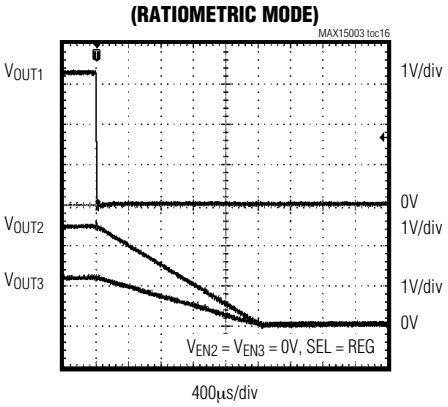
RATIOMETRIC SHUTDOWN



CHANNEL 2 SHORT CIRCUIT (RATIOMETRIC MODE)



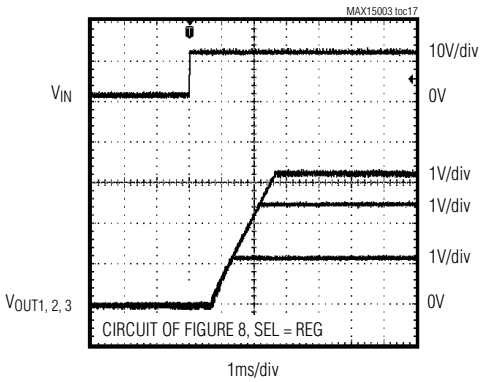
CHANNEL 1 SHORT CIRCUIT (RATIOMETRIC MODE)



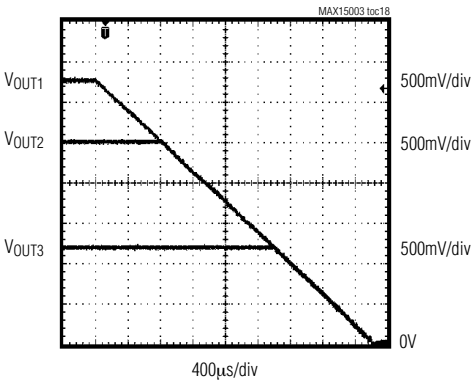
Typical Operating Characteristics (continued)

(Figure 8, V_{IN} = 12V, C_{REG} = 2.2µF, T_A = +25°C, unless otherwise noted.)

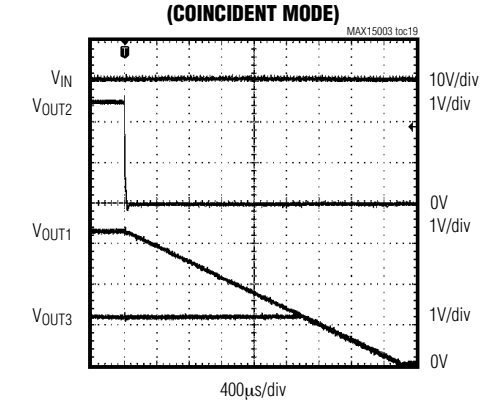
COINCIDENT STARTUP



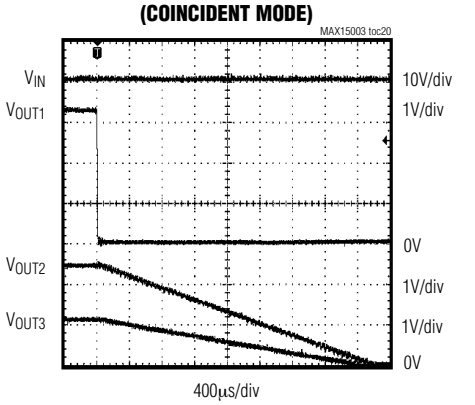
COINCIDENT SHUTDOWN



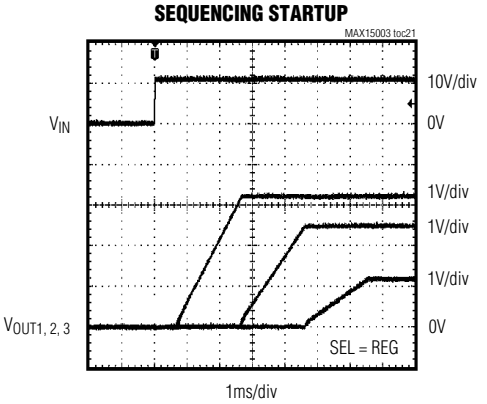
CHANNEL 2 SHORT CIRCUIT (COINCIDENT MODE)



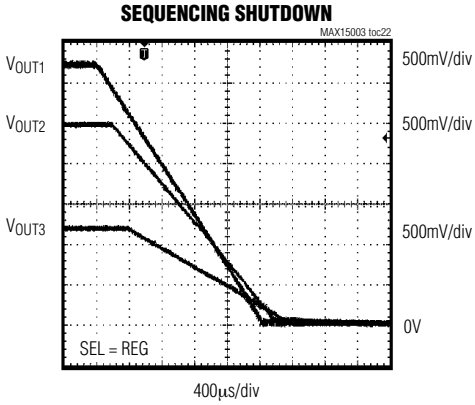
CHANNEL 1 SHORT CIRCUIT (COINCIDENT MODE)



SEQUENCING STARTUP



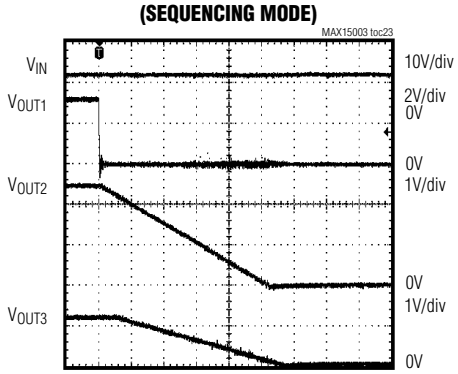
SEQUENCING SHUTDOWN



Typical Operating Characteristics (continued)

(Figure 8, V_{IN} = 12V, C_{REG} = 2.2µF, T_A = +25°C, unless otherwise noted.)

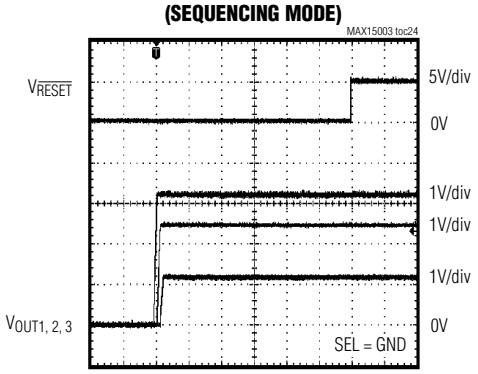
CHANNEL 1 OUTPUT SHORT CIRCUIT (SEQUENCING MODE)



SEL = GND

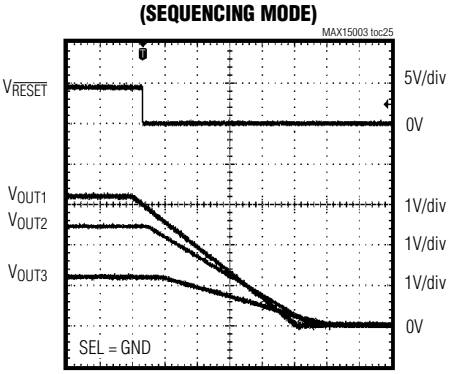
EN/TRACK2 = PGOOD1
EN/TRACK3 = PGOOD2

$\overline{\text{RESET}}$ AT STARTUP (SEQUENCING MODE)



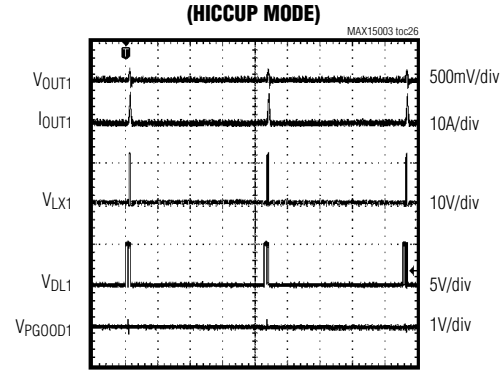
EN/TRACK2 = PGOOD1
EN/TRACK3 = PGOOD2

$\overline{\text{RESET}}$ AT SHUTDOWN (SEQUENCING MODE)

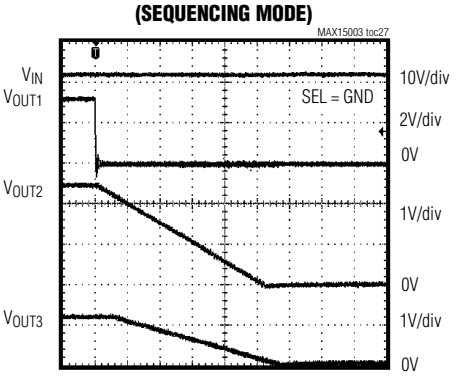


EN/TRACK2 = PGOOD1
EN/TRACK3 = PGOOD2

CONVERTER 1 SHORT-CIRCUIT CONDITION (HICCUP MODE)

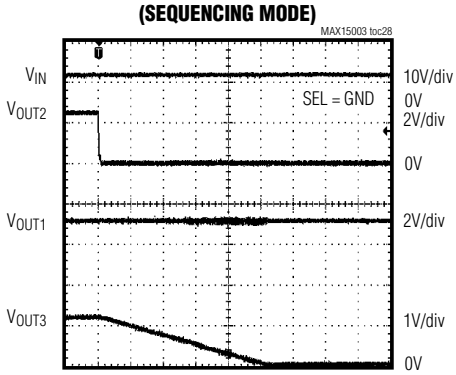


CONVERTER 1 OUTPUT SHORT-CIRCUIT (SEQUENCING MODE)



EN/TRACK2 = PGOOD1
EN/TRACK3 = PGOOD2

CONVERTER 2 OUTPUT SHORT-CIRCUIT (SEQUENCING MODE)

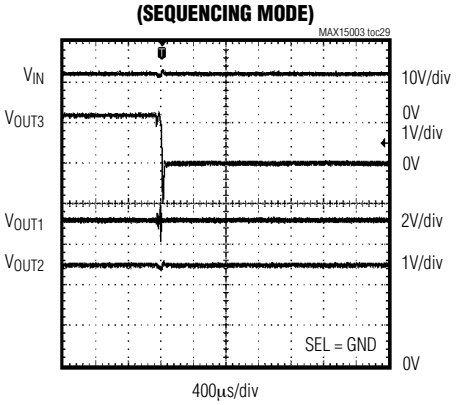


EN/TRACK2 = PGOOD1
EN/TRACK3 = PGOOD2

Typical Operating Characteristics (continued)

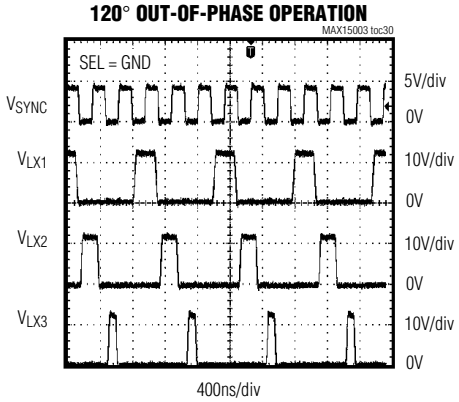
(Figure 8, V_{IN} = 12V, C_{REG} = 2.2µF, T_A = +25°C, unless otherwise noted.)

CONVERTER 3 OUTPUT SHORT-CIRCUIT (SEQUENCING MODE)

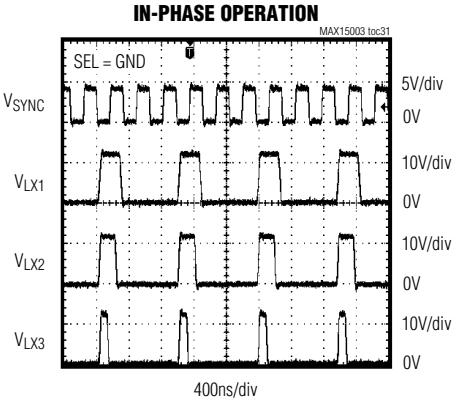


EN/TRACK2 = PGOOD1
EN/TRACK3 = PGOOD2

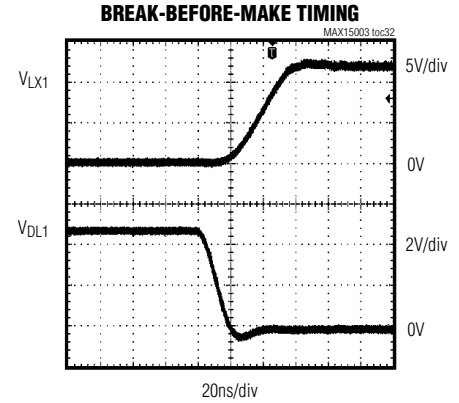
120° OUT-OF-PHASE OPERATION



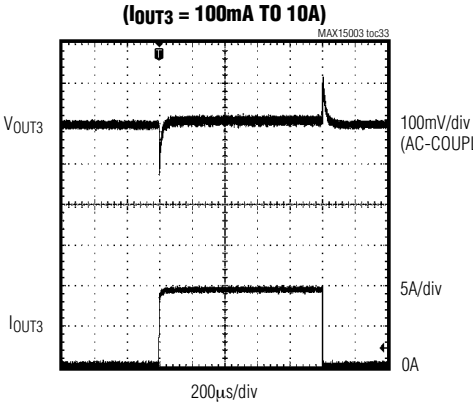
IN-PHASE OPERATION



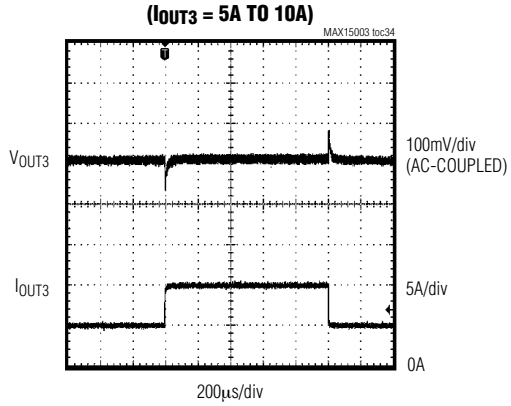
BREAK-BEFORE-MAKE TIMING



LOAD-TRANSIENT RESPONSE (I_{OUT3} = 100mA TO 10A)



LOAD-TRANSIENT RESPONSE (I_{OUT3} = 5A TO 10A)



Pin Description

PIN	NAME	FUNCTION
1	CT	$\overline{\text{RESET}}$ Timeout Capacitor Connection. Connect a timing capacitor from CT to SGND to set the $\overline{\text{RESET}}$ delay. CT sources 2µA into the timing capacitor. When the voltage at CT passes 2V, open-drain $\overline{\text{RESET}}$ goes high impedance.
2	IN	Supply Input Connection. Connect to an external voltage source from 5.5V to 23V. For 4.5V to 5.5V input application, connect IN and REG together.
3	REG	5V Regulator Output. Bypass with a 2.2µF ceramic capacitor to SGND.
4	SEL	Track/Sequence Select Input. Connect SEL to REG to configure as a triple tracker at startup or connect SEL to SGND to configure as a triple sequencer or leave SEL unconnected to configure as a dual tracker and independent sequencer. **Note:** When configured as a triple sequencer, each rail is independently enabled using the EN_.
5	PGND1	Controller 1 Power-Ground Connection. Connect the input filter capacitor's negative terminal, the source of the synchronous MOSFET, and the output filter capacitor's return to PGND1. Connect externally to SGND at a single point near the input capacitor return terminal.
6	DL1	Controller 1 Low-Side Gate Driver Output. DL1 is the gate driver output for the synchronous MOSFET.
7	DREG1	Controller 1 Low-Side Gate Driver Supply. Connect externally to REG and the anode of the boost diode. Connect a minimum of 0.1µF ceramic capacitor from DREG1 to PGND1.
8	LX1	Controller 1 High-Side MOSFET Source Connection/Synchronous MOSFET Drain Connection. Connect the inductor and the negative side of the boost capacitor to LX1.
9	DH1	Controller 1 High-Side Gate Driver Output. DH1 drives the gate of the high-side MOSFET.
10	BST1	Controller 1 High-Side Gate Driver Supply. Connect BST1 to the cathode of the boost diode and to the positive terminal of the boost capacitor.
11	CSN1	Controller 1 Negative Current-Sense Input. Connect CSN1 to the synchronous MOSFET drain (connected to LX1). When using a current-sense resistor, connect CSN1 to the junction of a low-side MOSFET's source and the current-sense resistor. See Figure 11.
12	CSP1	Controller 1 Positive Current-Sense Input. Connect CSP1 to the synchronous MOSFET source (connected to PGND1). When using a current-sense resistor, connect CSP1 to the PGND1 end of the current-sense resistor.
13	ILIM1	Controller 1 Valley Current-Limit Set Output. Connect a 25kΩ to 150kΩ resistor, R_{ILIM1}, from ILIM1 to SGND to program the valley current-limit threshold from 50mV to 300mV. ILIM1 sources 20µA out to R_{ILIM1}. The resulting voltage divided by 10 is the valley current-limit threshold. When using a precision current-sense resistor, connect a resistive divider from REG to ILIM1 to SGND to set the valley current limit. See Figure 11.
14	COMP1	Controller1 Error Transconductance Amplifier Output. Connect COMP1 to the compensation feedback network.
15	EN1	Controller 1 Enable Input. EN1 must be above 1.24V, V_{EN-TH}, for the PWM controller to start Output 1. Controller 1 is the master. Use the master as the highest output voltage in a coincident tracking configuration.

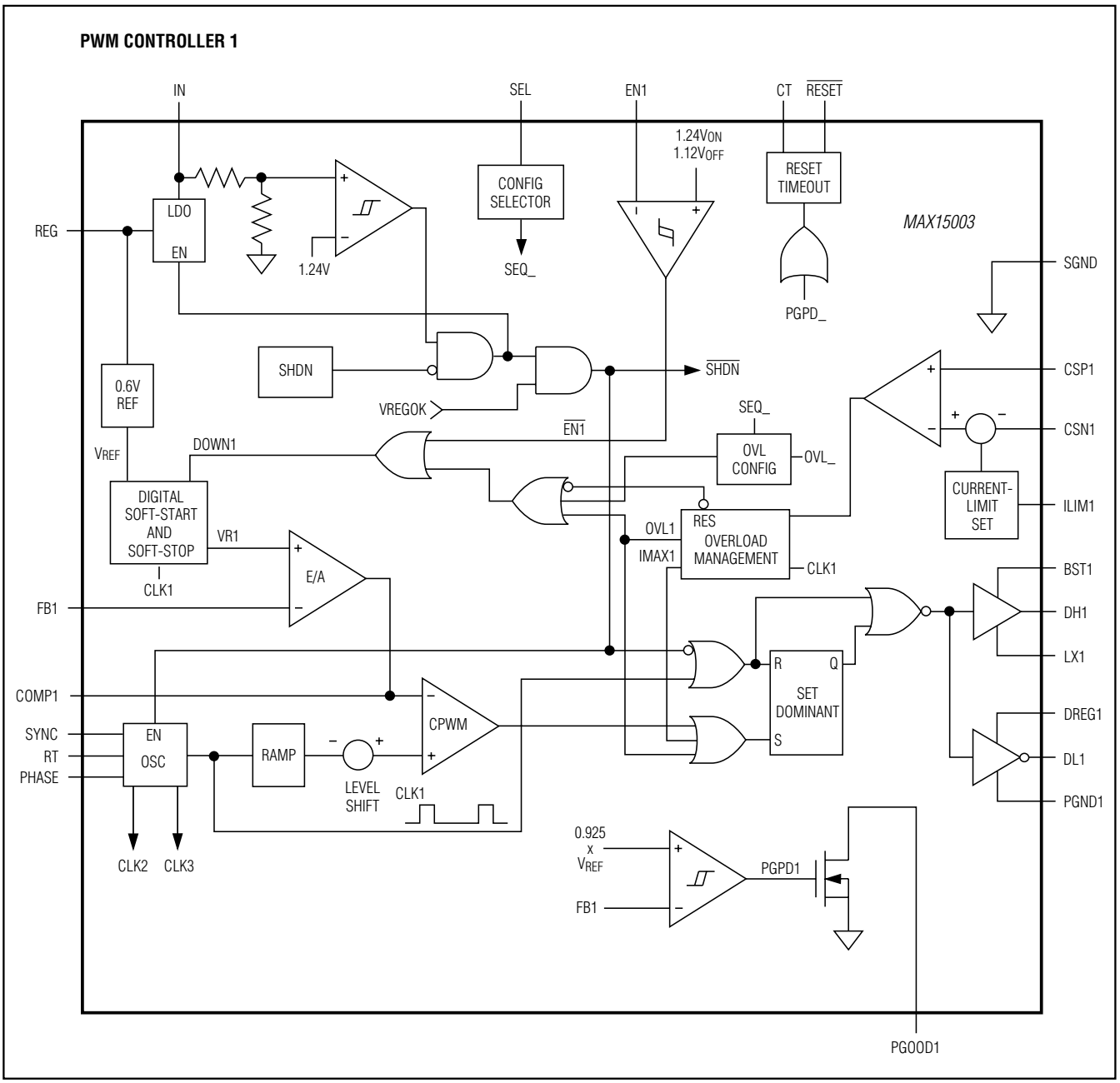
Pin Description (continued)

PIN	NAME	FUNCTION
16	FB1	Controller 1 Feedback Regulation Point. Connect to the center tap of a resistive divider from the converter output to SGND to set the output voltage. The FB1 voltage regulates to V_{FB} (0.6V).
17	PGOOD1	Controller 1 Power-Good Output. Open-drain PGOOD1 output goes high impedance (releases) when FB1 is above 0.925 x V_{FB} = 0.555V.
18	PGND2	Controller 2 Power Ground Connection. Connect the input filter capacitor's negative terminal, the source of the synchronous MOSFET, and the output filter capacitor's return to PGND2. Connect externally to SGND at a single point near the input capacitor return terminal.
19	DL2	Controller 2 Low-Side Gate Driver Output. DL2 is the gate driver output for the synchronous MOSFET.
20	DREG2	Controller 2 Low-Side Gate Driver Supply. Connect externally to REG and the anode of the boost diode. Connect at minimum, a 0.1µF ceramic capacitor from DREG2 to PGND2.
21	LX2	Controller 2 High-Side MOSFET Source Connection/Synchronous MOSFET Drain Connection. Connect the inductor and the negative side of the boost capacitor to LX2.
22	DH2	Controller 2 High-Side Gate Driver Output. DH2 drives the gate of the high-side MOSFET.
23	BST2	Controller 2 High-Side Gate Driver Supply. Connect BST2 to the cathode of the boost diode and to the positive terminal of the boost capacitor.
24	CSN2	Controller 2 Negative Current-Sense Input. Connect CSN2 to the synchronous MOSFET drain (connected to LX2). When using a current-sense resistor, connect CSN2 to the junction of the low-side MOSFET's source and the current-sense resistor. See Figure 11.
25	CSP2	Controller 2 Positive Current-Sense Input. Connect CSP2 to the synchronous MOSFET source (connected to PGND2). When using a current-sense resistor, connect CSP2 to the PGND2 end of the current-sense resistor.
26	ILIM2	Controller 2 Valley Current-Limit Set Output. Connect a 25kΩ to 150kΩ resistor, R_{ILIM2}, from ILIM2 to SGND to program the valley current-limit threshold from 50mV to 300mV. ILIM2 sources 20µA out to R_{ILIM2}. The resulting voltage divided by 10 is the valley current-limit threshold. When using a precision current-sense resistor, connect a resistive divider from REG to ILIM2 to SGND to set the valley current limit. See Figure 11.
27	COMP2	Controller 2 Error Transconductance Amplifier Output. Connect COMP2 to the compensation feedback network.
28	EN/TRACK2	Controller 2 Enable/Tracking Input. See Figure 2. When sequencing, EN/TRACK2 must be above 1.24V for the PWM controller 2 to start. Coincident tracking—connect the same resistive divider used for FB2, from Output 1 to EN/TRACK2 to SGND. Ratiometric tracking—connect EN/TRACK2 to analog ground.
29	FB2	Controller 2 Feedback Regulation Point. Connect to the center tap of a resistive divider from the converter output to SGND to set the output voltage. The FB2 voltage regulates to V_{FB} (0.6V).
30	PGOOD2	Controller 2 Power-Good Output. Open-drain PGOOD2 output goes high impedance (releases) when FB2 is above 0.925 x V_{FB} = 0.555V.
31	PGOOD3	Controller 3 Power-Good Output. Open-drain PGOOD3 output goes high impedance (releases) when FB3 is above 0.925 x V_{FB} = 0.555V.
32	FB3	Controller 3 Feedback Regulation Point. Connect to the center tap of a resistive divider from the converter output to SGND to set the output voltage. The FB3 voltage regulates to V_{FB} (0.6V).

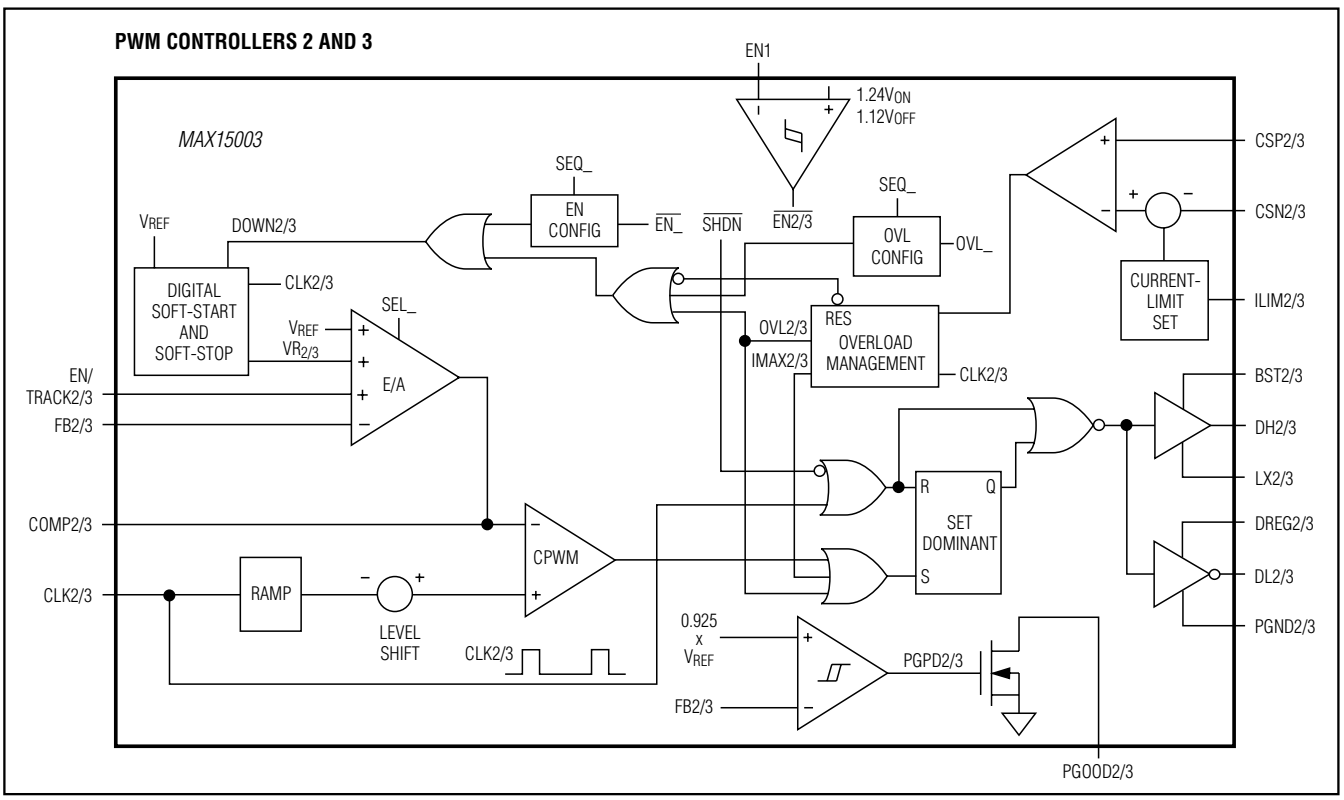
Pin Description (continued)

PIN	NAME	FUNCTION
33	EN/TRACK3	Controller 3 Enable/Tracking Input. See Figure 2. When sequencing, EN/TRACK3 must be above 1.24V for the PWM controller 3 to start. Coincident tracking—connect the same resistive divider used for FB3, from Output 1 to EN/TRACK3 to SGND. Ratiometric tracking—connect EN/TRACK3 to analog ground.
34	COMP3	Controller 3 Error Transconductance Amplifier Output. Connect COMP3 to the compensation feedback network.
35	ILIM3	Controller 3 Valley Current-Limit Set Output. Connect a 25kΩ to 150kΩ resistor, R_{ILIM3}, from ILIM3 to SGND to program the valley current-limit threshold from 50mV to 300mV. ILIM3 sources 20µA out to R_{ILIM3}. The resulting voltage divided by 10 is the valley current-limit threshold. When using a precision current-sense resistor, connect a resistive divider from REG to ILIM3 to SGND to set the valley current limit. See Figure 11.
36	CSP3	Controller 3 Positive Current-Sense Input. Connect CSP3 to the synchronous MOSFET source (connected to PGND3). When using a current-sense resistor, connect CSP3 to the PGND3 end of the current-sense resistor.
37	CSN3	Controller 3 Negative Current-Sense Input. Connect CSN3 to the synchronous MOSFET drain (connected to LX3). When using a current-sense resistor, connect CSN3 to the junction of low-side MOSFET's source and the current-sense resistor. See Figure 11.
38	BST3	Controller 3 High-Side Gate Driver Supply. Connect BST3 to the cathode of the boost diode and to the positive terminal of the boost capacitor.
39	DH3	Controller 3 High-Side Gate Driver Output. DH3 drives the gate of the high-side MOSFET.
40	LX3	Controller 3 High-Side MOSFET Source Connection/Synchronous MOSFET Drain Connection. Connect the inductor and the negative side of the boost capacitor to LX3.
41	DREG3	Controller 3 Low-Side Gate Driver Supply. Connect externally to REG and anode of the boost diode. Connect a minimum of 0.1µF ceramic capacitor from DREG3 to PGND3.
42	DL3	Controller 3 Low-Side Gate Driver Output. DL3 is the gate driver output for the synchronous MOSFET.
43	PGND3	Controller 3 Power-Ground Connection. Connect the input filter capacitor's negative terminal, the source of the synchronous MOSFET, and the output filter capacitor's return to PGND3. Connect externally to SGND at a single point near the input capacitor return terminal.
44	SYNC	Synchronization Input. Drive with a frequency at least 20% higher than three times the frequency programmed using the RT pin. The switching frequency is 1/3 the SYNC frequency. Connect SYNC to SGND when not used.
45	SGND	Analog Ground Connection. Connect SGND and PGND_ together at one point near the input bypass capacitor return terminal.
46	RT	Oscillator Timing Resistor Connection. Connect a 500kΩ to 45kΩ resistor from RT to SGND to program the switching frequency from 200kHz to 2.2MHz.
47	PHASE	Phase Select Input. Connect PHASE to SGND for 120° out-of-phase operation between the controllers. Connect to REG for in phase operation.
48	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ Output. Open-drain $\overline{\text{RESET}}$ output releases after all PGOODs are released and timeout programmed by CT finishes.
—	EP	Exposed Pad. Solder the exposed pad to a large SGND plane.

Functional Diagrams



Functional Diagrams (continued)



Detailed Description

The MAX15003 is a triple-output, pulse-width-modulated (PWM), step-down, DC-DC controller with tracking and sequencing options. The device operates over the input voltage range of 5.5V to 23V or 5V ±10%. Each PWM controller provides an adjustable output down to 0.6V and delivers up to 15A load current with excellent load and line regulation.

Each of the MAX15003 PWM sections utilizes a voltage-mode control scheme for good noise immunity and offers external compensation allowing for maximum flexibility with a wide selection of inductor values and capacitor types. The device operates at a fixed switching frequency that is programmable from 200kHz to 2.2MHz and can be synchronized to an external clock signal using the SYNC input. Each converter, operating at up to 2.2MHz with 120° out-of-phase, increases the input capacitor ripple frequency up to 6.6MHz, reducing the RMS input ripple current and the size of the input bypass capacitor requirement significantly.

The MAX15003 provides either coincident tracking, ratiometric tracking, or sequencing. This allows tailoring of the power-up/power-down sequence depending on the system requirements.

The MAX15003 features lossless valley-mode current-limit protection by monitoring the voltage drop across the synchronous MOSFET's on-resistance to sense the inductor current. The MAX15003's internal current source exhibits a positive temperature coefficient to help compensate for the MOSFET's temperature coefficient. Use an external voltage-divider when a more precise current limit is desired. This divider along with a precision shunt resistor allows for more accurate current limit.

The MAX15003 includes internal undervoltage lockout with hysteresis, digital soft-start/soft-stop for glitch-free power-up and power-down of the converters. The power-on reset ($\overline{\text{RESET}}$) with adjustable timeout period monitors all three outputs and provides a $\overline{\text{RESET}}$ signal to a system controller/processor indicating when all outputs are within regulation. Protection features include lossless valley-mode current limit and hiccup mode output short-circuit protection.

Internal Undervoltage Lockout (UVLO)

V_{IN} must exceed the default UVLO threshold before any operation can commence. The UVLO circuitry keeps the MOSFET drivers, oscillator, and all the internal circuitry shut down to reduce current consumption. The UVLO rising threshold is 4.05V with 350mV hysteresis.

Digital Soft-Start/Soft-Stop

The MAX15003 soft-start feature allows the load voltage to ramp up in a controlled manner, eliminating output-voltage overshoot. Soft-start begins after V_{IN} exceeds the undervoltage lockout threshold and the enable input is above 1.24V. The soft-start circuitry gradually ramps up the reference voltage. This controls the rate of rise of the output voltage and reduces input surge currents during startup. The soft-start duration is 2048 clock cycles. The output voltage is incremented through 64 equal steps. The output reaches regulation when soft-start is completed, regardless of output capacitance and load.

Soft-stop commences when the enable input falls below 1.12V. The soft-stop circuitry ramps down the reference voltage controlling the output voltage rate of fall. The output voltage is decremented through 64 equal steps in 2048 clock cycles.

Internal Linear Regulator (REG)

REG is the output terminal of a 5V LDO powered from IN that provides power to the IC. Connect REG externally to DREG to provide power for the low-side MOSFET gate driver. Bypass REG to SGND with a minimum 2.2µF ceramic capacitor. Place the capacitor physically close to the MAX15003 to provide good bypassing. REG is intended for powering only the internal circuitry and should not be used to supply power to external loads.

REG can source up to 120mA. This current, I_{REG}, includes quiescent current (I_Q) and gate drive current (I_{DREG}):

$$I_{REG} = I_Q + [f_{SW} \times \Sigma(Q_{GHS\_} + Q_{GLS\_})]$$

where $Q_{GHS\_}$ to $Q_{GLS\_}$ are the total gate charge of each of the respective high- and low-side external MOSFETs at V_{GATE} = 5V. f_{SW} is the switching frequency of the converter and I_Q is the quiescent current of the device at the switching frequency.

MOSFET Gate Drivers

DREG_ is the supply input for the low-side MOSFET driver. Connect DREG_ to REG externally. Everytime the low-side MOSFET switches on, high peak current is drawn from DREG for a short amount of time. Adding an RC filter (1Ω to 3.3Ω and 2.2µF in parallel to 0.1µF ceramic capacitors are typical) from REG to DREG_ filters out high-peak currents.

BST_ supplies the power for the high-side MOSFET drivers. Connect the bootstrap diode from BST_ to DREG_ (anode at DREG_ and cathode at BST_). Connect a bootstrap 0.1µF or higher ceramic capacitor between BST_ and LX_. Though not always necessary, it may be useful to insert a small resistor (4.7Ω to 22Ω) in series with the BST_ pin and the cathode of the bootstrap diode for additional noise immunity.

The high-side (DH_) and low-side (DL_) drivers drive the gates of the external n-channel MOSFETs. The drivers' 2A peak source- and sink-current capability provides ample drive for the fast rise and fall times of the switching MOSFETs. Faster rise and fall times result in reduced switching losses.

The gate driver circuitry also provides a break-before-make time (20ns typ) to prevent shoot-through currents during transition.

Oscillator/Synchronization Input/Phase Staggering (RT, SYNC, PHASE)

Use an external resistor at RT to program the MAX15003 switching frequency from 200kHz to 2.2MHz. Choose the appropriate resistor at RT to calculate the desired output switching frequency (f_{SW}):

$$f_{SW}\ (Hz) = 10^{11}/(R_{RT} + 1750)\ (\Omega)$$

Connect an external clock at SYNC for external clock synchronization. A rising clock edge on SYNC is interpreted as a synchronization input. If the SYNC signal is lost, the internal oscillator takes control of the switching rate, returning the switching frequency to that set by R_{RT}. This maintains output regulation even with intermittent SYNC signals. For proper synchronization, the external frequency must be at least 20% higher than three times the frequency programmed through the RT input. The switching frequency is 1/3 the SYNC frequency. Connect SYNC to SGND when not used.

Connect PHASE to SGND for 120° out-of-phase operation between the controllers. Connect PHASE to REG for in-phase operation.

Coincident/Ratiometric Tracking (SEL, EN/TRACK_)

The enable/tracking input in conjunction with digital soft-start and soft-stop provides coincident/ratiometric tracking (see Figure 1). Track an output voltage by connecting a resistive divider from the output being tracked to the enable/tracking input. For example, for V_{OUT2} to coincidentally track V_{OUT1}, connect the same resistive divider used for FB2, from OUT1 to EN/TRACK2 to SGND. See Figure 2 and the Coincident Startup and Coincident Shutdown graphs in the *Typical Operating Characteristics*.

Track ratiometrically by connecting EN/TRACK_ to SGND. This synchonizes the soft-start and soft-stop of all the controllers' references, and hence their respective output voltages track ratiometrically. See Figure 2 and the *Typical Operating Characteristics* (Ratiometric Startup and Ratiometric Shutdown graphs).

Connect SEL to REG to configure as a triple tracker.

When the MAX15003 converter is configured as a tracker, the output short-circuit fault situations at master or slave outputs are handled carefully so that either the master or slave output does not stay on when the other outputs are shorted to the ground. When the slave is shorted and enters in hiccup mode, both the master and the other slave soft-stop. When the master is shorted and the part enters in hiccup mode, the slaves ratiometrically soft-stop. Coming out of the hiccup, all outputs soft-start coincidently or ratiometrically depending on their initial configuration. See the *Typical Operating Characteristics* for the output behaviour during the fault conditions. During power-off, when the input falls below its UVLO, the output voltages fall down at the rate depending on the respective output capacitor and load.

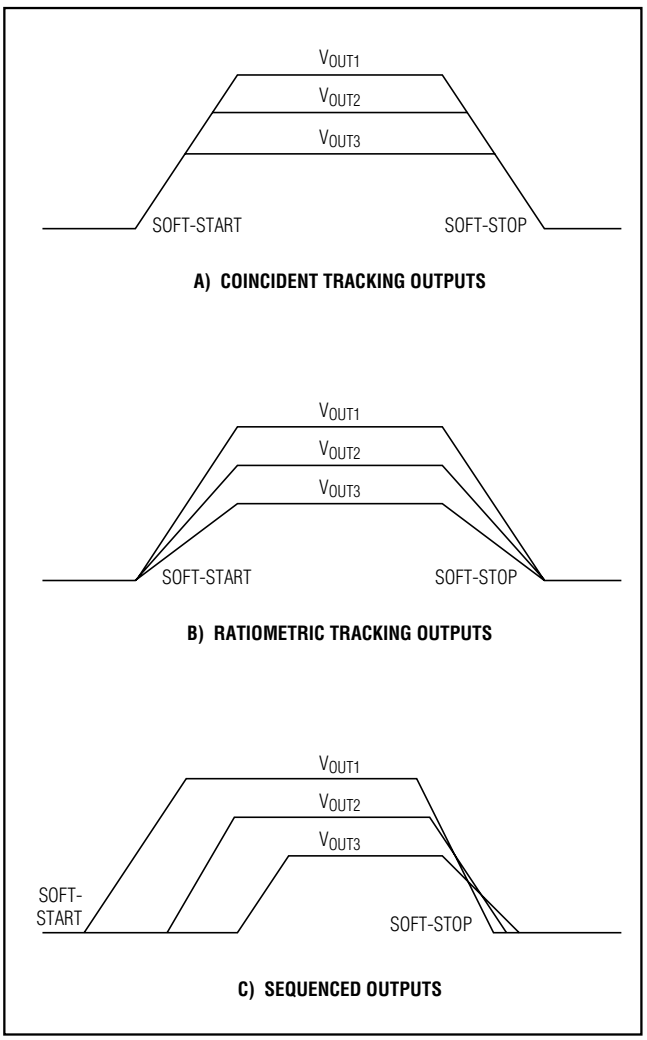


Figure 1. Graphical Representation of Coincident Tracking, Ratiometric Tracking, or PGOOD Sequencing

Output-Voltage Sequencing (SEL, EN/TRACK_, PGOOD)

Referring to Figure 1c, when sequencing, the enable/tracking input must be above 1.24V for each PWM controller to start. The PGOOD_ outputs and EN/TRACK_ inputs can be daisy-chained to generate power sequencing. Open-drain PGOOD_ outputs go high impedance when FB_ is above the PGOOD_ threshold (555mV typ). Connect a resistive divider from the power-good output to the enable/tracking input to SGND to set when each controller will start. See Figure 2. Connect SEL to SGND to configure as a triple sequencer.

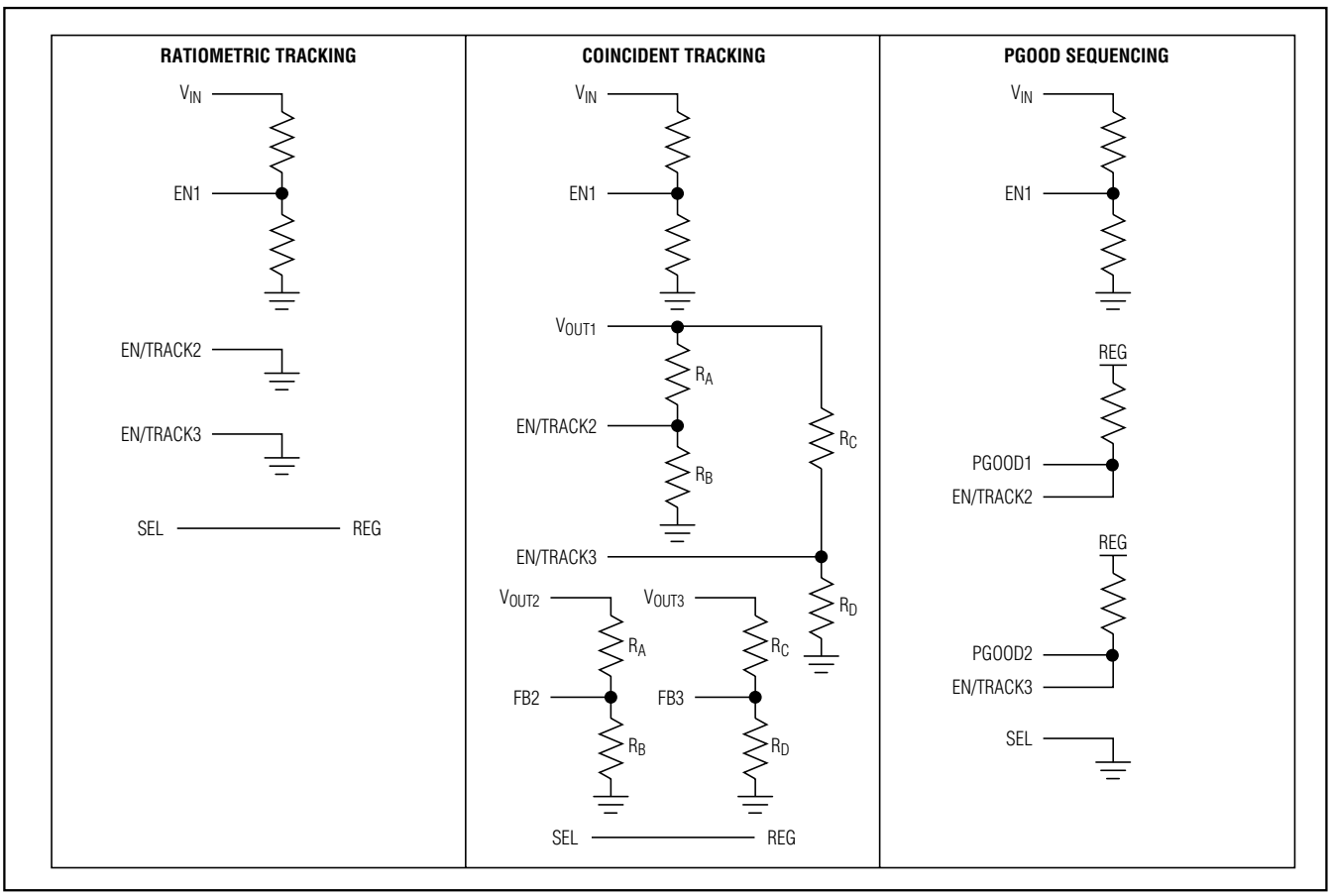


Figure 2. Ratiometric Tracking, Coincident Tracking, PGOOD Sequencing Configurations

Error Amplifier

The output of the internal error transconductance amplifier (COMP_) is provided for frequency compensation (see the *Compensation Design Guidelines* section). The inverting input is FB_ and the output COMP_. The error transamplifier has an 80dB open-loop gain and a 10MHz GBW product.

Output Short-Circuit Protection (Hiccup Mode)

The current-limit circuit employs a valley current-limiting algorithm that either uses a shunt or the synchronous MOSFET's on-resistance as the current-sensing element. Once the high-side MOSFET turns off, the voltage across the current-sensing element is monitored. If this voltage does not exceed the current-limit threshold, the high-side MOSFET turns on normally at the start of the next cycle. If the voltage exceeds the current-limit threshold just before the beginning of a new PWM cycle, the controller skips that cycle. During severe overload or short-circuit conditions, the switching frequency of the device appears to decrease because the on-time of the low-side MOSFET extends beyond a clock cycle.

If the current-limit threshold is exceeded for more than eight cumulative clock cycles (N_{CL}), the device shuts down (both DH and DL are pulled low) for 4096 clock cycles (hiccup timeout) and then restarts with a soft-start sequence. If three consecutive cycles pass without a current-limit event, the count of NCL is cleared (see Figure 3). Hiccup mode protects against a continuous output short circuit.

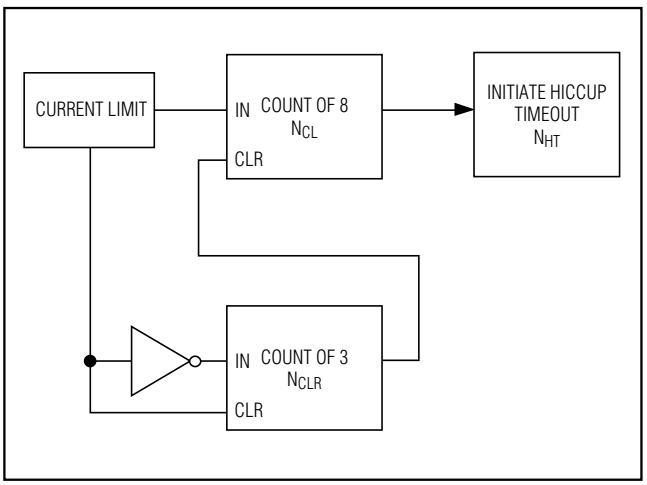


Figure 3. Hiccup-Mode Block Diagram

PWM Controller Design Procedures

Setting the Switching Frequency

Connect a 500kΩ to 45kΩ resistor from RT to SGND to program the switching frequency from 200kHz to 2.2MHz. Calculate the switching frequency using the following equation:

$$f_{SW} = 10^{11}/(R_{RT} + 1750)$$

Higher frequencies allow designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate-charge currents, and switching losses increase.

Effective Input Voltage Range

Although the MAX15003 converters can operate from input supplies ranging from 5.5V to 23V, the input voltage range can be effectively limited by the MAX15003 duty-cycle limitations for a given output voltage. The maximum input voltage is limited by the minimum on-time ($t_{ON(MIN)}$):

$$V_{IN(MAX)} \leq \frac{V_{OUT}}{t_{ON(MIN)} \times f_{SW}}$$

where $t_{ON(MIN)}$ is 75ns.

The minimum input voltage is limited by the maximum duty cycle and is calculated using the following equation:

$$V_{IN(MIN)} \geq \frac{V_{OUT}}{1-\left(t_{OFF(MIN)} \times f_{SW}\right)}$$

where $t_{OFF(MIN)}$ typically is equal to 150ns.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX15003: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the peak-to-peak inductor current (ΔI_{P-P}). Higher ΔI_{P-P} allows for a lower inductor value. A lower inductance value minimizes size and cost and improves large-signal and transient response. However, efficiency is reduced due to higher peak currents and higher peak-to-peak output voltage ripple for the same output capacitor. A higher inductance increases efficiency by reducing the ripple current, however resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels especially when the inductance is increased without also allowing for larger inductor dimensions. A good rule of thumb is to choose ΔI_{P-P} equal to 30% of the full load current. Calculate the inductance using the following equation:

$$L = \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{V_{IN} \times f_{SW} \times \Delta I_{P-P}}$$

V_{IN} and V_{OUT} are typical values so that efficiency is optimum for typical conditions. The switching frequency is programmable between 200kHz and 2.2MHz (see *Oscillator/Synchronization Input/Phase Staggering (RT, SYNC, PHASE)* section). The peak-to-peak inductor current, which reflects the peak-to-peak output ripple, is worst at the maximum input voltage. See the *Output Capacitor Selection* section to verify that the worst-case output current ripple is acceptable. The inductor saturation current (I_{SAT}) is also important to avoid runaway current during continuous output short-circuit conditions. Select an inductor with an I_{SAT} specification higher than the maximum peak current.

Input Capacitor Selection

The discontinuous input current of the buck converter causes large input ripple currents, and therefore, the input capacitor must be carefully chosen to withstand the input ripple current and keep the input voltage ripple within design requirements. The 120° ripple phase operation increases the frequency of the input capacitor ripple current to thrice the individual converter switching frequency. When using ripple phasing, the worst-case input capacitor ripple current is when the one converter with the highest output current is on.

The input voltage ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR} which peaks at the end of the on-cycle. Calculate the input capacitance and ESR required for a specified ripple using the following equations:

$$ESR = \frac{\Delta V_{ESR}}{\left(I_{LOAD(MAX)} + \frac{\Delta I_{P-P}}{2}\right)}$$

$$C_{IN} = \frac{I_{LOAD(MAX)} \times \left(\frac{V_{OUT}}{V_{IN}}\right)}{\Delta V_Q \times f_{SW}}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

$I_{LOAD(MAX)}$ is the maximum output current, ΔI_{P-P} is the peak-to-peak inductor current, and f_{SW} is the switching frequency.

For the condition with only one converter is on, calculate the input ripple current using the following equation:

$$I_{CIN(RMS)} = I_{LOAD(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

The MAX15003 includes UVLO hysteresis to avoid possible unintentional chattering during turn-on. Use additional bulk capacitance if the input source impedance is high. At lower input voltage, additional input capacitance helps avoid possible undershoot below the undervoltage lockout threshold during transient loading.

Output Capacitor Selection

The allowed output voltage ripple and the maximum deviation of the output voltage during load steps determine the required output capacitance and its ESR. The output ripple is mainly composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the voltage drop across the equivalent series resistance of the output capacitor). The equations for calculating the output capacitance and its ESR are:

$$C_{OUT} = \frac{\Delta I_{P-P}}{8 \times \Delta V_Q \times f_{SW}}$$

$$ESR = \frac{2 \times \Delta V_{ESR}}{\Delta I_{P-P}}$$

ΔV_{ESR} and ΔV_Q are not directly additive because they are out of phase from each other. If using ceramic capacitors, which generally have low ESR, ΔV_Q dominates. If using electrolytic capacitors, ΔV_{ESR} dominates.

The allowable deviation of the output voltage during fast load transients also affects the output capacitance, its ESR, and its equivalent series inductance (ESL). The output capacitor supplies the load current during a load step until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the gain bandwidth of the converter (see the *Compensation Design Guidelines* section). The resistive drop across the output capacitor's ESR, the drop across the capacitor's ESL, and the capacitor discharge cause a voltage droop during the load-step (I_{STEP}). Use a combination of low-ESR tantalum/aluminum electrolytic and ceramic capacitors for better load-transient and voltage-ripple performance. Surface-mount capacitors and capacitors in parallel help reduce the ESL. Keep the maximum output voltage deviation below the tolerable limits of the electronics being powered.

Use the following equations to calculate the required ESR, ESL, and capacitance value during a load step:

$$ESR = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

$$ESL = \frac{\Delta V_{ESL} \times t_{STEP}}{I_{STEP}}$$

where I_{STEP} is the load step, t_{STEP} is the rise time of the load step, and $t_{RESPONSE}$ is the response time of the controller.

Setting the Current Limit

Connect a 25kΩ to 150kΩ resistor, R_{ILIM}, from ILIM to SGND to program the valley current-limit threshold (V_{CL}) from 50mV to 300mV. ILIM sources 20µA out to R_{ILIM}. The resulting voltage divided by 10 is the valley current-limit threshold.

The MAX15003 uses a valley current-sense method for current limiting. The voltage drop across the low-side MOSFET due to its on-resistance is used to sense the inductor current. The voltage drop (V_{VALLEY}) across the low-side MOSFET at the valley point and at I_{LOAD} is:

$$V_{VALLEY} = R_{DS(ON)} \times \left(I_{LOAD} - \frac{\Delta I_{P-P}}{2} \right)$$

$R_{DS(ON)}$ is the on-resistance of the low-side MOSFET, I_{LOAD} is the rated load current, and ΔI_{P-P} is the peak-to-peak inductor current.

The $R_{DS(ON)}$ of the MOSFET varies with temperature. Calculate the $R_{DS(ON)}$ of the MOSFET at its operating junction temperature at full load using the MOSFET datasheet. To compensate for this temperature variation, the 20µA ILIM reference current has a temperature coefficient of 3333ppm/°C. This allows the valley current-limit threshold (V_{CL}) to track and partially compensate for the increase in the synchronous MOSFET's $R_{DS(ON)}$ with increasing temperature. Use the following equation to calculate R_{ILIM}:

$$R_{ILIM} = \frac{R_{DS(ON)} \times \left(I_{CL(MAX)} - \frac{\Delta I_{P-P}}{2} \right) \times 10}{20 \times 10^{-6} \left[1 + 3.333 \times 10^{-3} (T - 25°C) \right]}$$

Figure 4 illustrates the effect of the MAX15003 ILIM reference current temperature coefficient to compensate for the variation of the MOSFET $R_{DS(ON)}$ over the operating junction temperature range.

Power MOSFET Selection

When choosing the MOSFETs, consider the total gate charge, $R_{DS(ON)}$, power dissipation, the maximum drain-to-source voltage and package thermal impedance. The product of the MOSFET gate charge and on-resistance is a figure of merit, with a lower number signifying better performance. Choose MOSFETs that are optimized for high-frequency switching applications. The average gate-drive current from the MAX15003's output is proportional to the frequency and gate charge required to drive the MOSFET. The power dissipated in the MAX15003 is proportional to the input voltage and the average drive current (see the *Power Dissipation* section).

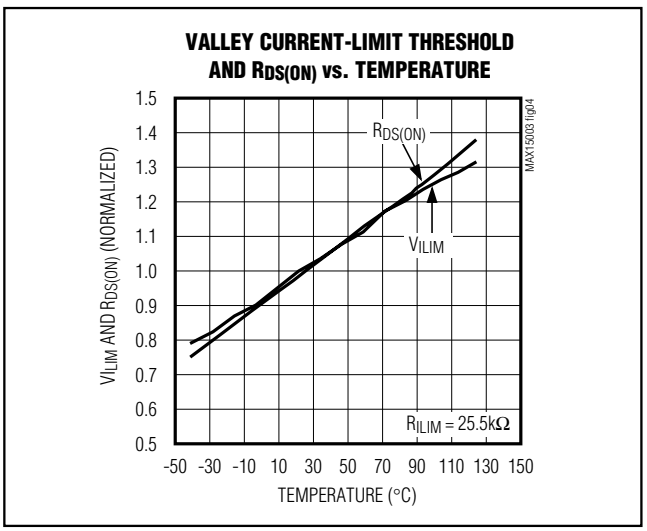


Figure 4. Current-Limit Trip Point and $V_{RDS(ON)}$ vs. Temperature

Compensation Design Guidelines

The MAX15003 uses a fixed-frequency, voltage-mode control scheme that regulates the output voltage by differentially comparing the "sampled" output voltage against a fixed reference. The subsequent error voltage that appears at the error amplifier output (COMP) is compared against an internal ramp voltage to generate the required duty cycle of the pulse-width modulator. A second order lowpass LC filter removes the switching harmonics and passes the DC component of the pulse-width-modulated signal to the output. The LC filter, which has an attenuation slope of -40dB/decade, introduces 180° of phase shift at frequencies above the LC resonant frequency. This phase shift, in addition to the inherent 180° of phase shift of the regulator's self-governing (negative) feedback system, poses the potential for positive feedback. The error amplifier and its associated circuitry are designed to compensate for this instability to achieve a stable closed-loop system.

The basic regulator loop consists of a power modulator (comprises the regulator's pulse-width modulator, associated circuitry, and LC filter), an output feedback divider, and an error amplifier. The power modulator has a DC gain set by V_{IN} / V_{RAMP}, with a double pole and a single zero set by the output inductance (L), the output capacitance (C_{OUT}), and its equivalent series resistance (ESR). A second, higher frequency zero also exists, which is a function of the output capacitor's ESR and ESL); though only taken into account when using very high-quality filter components and/or frequencies of operation.

Below are equations that define the power modulator:

$$G_{MOD(DC)} = \frac{V_{IN}}{V_{RAMP}}$$

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}}$$

$$f_{ZERO,ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

$$f_{ZERO,ESL} = \frac{ESR}{2\pi \times ESL}$$

The switching frequency is programmable between 200kHz and 2.2MHz using an external resistor at RT. Typically, the crossover frequency (f_{CO}), which is the frequency when the system's closed-loop gain is equal to unity crosses the 0dB axis—should be set at or below one-tenth the switching frequency ($f_{SW}/10$) for stable, closed-loop response.

The MAX15003 provides an internal transconductance amplifier with its inverting input and its output available to the user for external frequency compensation. The flexibility of external compensation for each converter offers wide selection of output filtering components, especially the output capacitor. For cost-sensitive applications, use aluminum electrolytic capacitors and for space-sensitive applications, use low-ESR tantalum or multilayer ceramic chip (MLCC) capacitors at the output. The higher switching frequencies of the MAX15003 allow the use of MLCC as the primary filter capacitor(s).

First, select the passive and active power components that meet the application's output ripple, component size, and component cost requirements. Second, choose the small-signal compensation components to achieve the desired closed-loop frequency response and phase margin as outlined below.

Closed-Loop Response and Compensation of Voltage-Mode Regulators

The power modulator's LC lowpass filter exhibits a variety of responses, depending on the value of the L and C (and their parasitics).

One such response is shown in Figure 5a. In this example the power modulator's uncompensated crossover is approximately 1/6th the desired crossover frequency, f_{CO}. Note also, the uncompensated roll-off through the 0dB plane follows the double-pole, -40dB/decade slope and approaches 180° of phase shift, indicative of a potentially unstable system. Together with the inherent 180° of phase delay in the negative feedback system, this may lead to near 360° or positive feedback—an unstable system.

The desired (compensated) roll-off follows a -20dB/decade slope (and commensurate 90° of phase shift), and, in this example, occurs at approximately 6x the uncompensated crossover frequency, f_{CO}. In this example, a Type II compensator provides for stable closed-loop operation, leveraging the +20dB/decade slope of the capacitor's ESR zero (see Figure 5b).

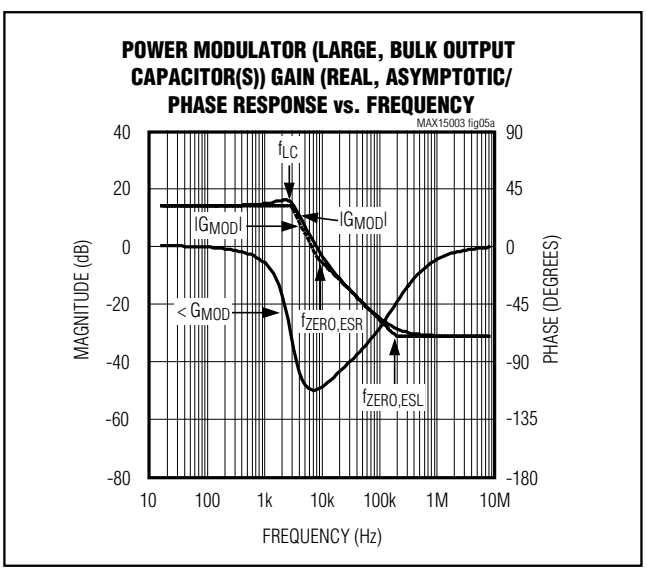


Figure 5a. Power Modulator Gain and Phase Response (Large, Bulk C_{OUT})

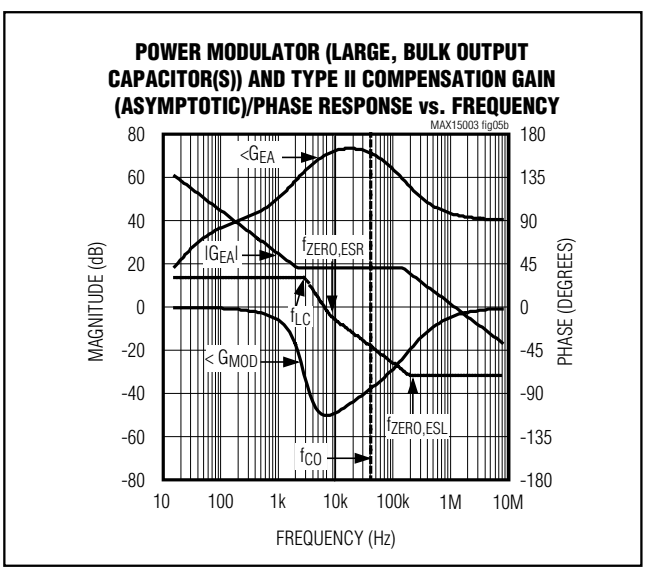


Figure 5b. Power Modulator (Large, Bulk C_{OUT}) and Type II Compensator Responses

The Type II compensator's mid-frequency gain (approximately 18dB shown here) is designed to compensate for the power modulator's attenuation at the desired crossover frequency, f_{CO} ($G_{E/A}$ + G_{MOD} = 0dB at f_{CO}). In this example, the power modulator's inherent -20dB/decade roll-off above the ESR zero ($f_{ZERO, ESR}$) is leveraged to extend the active regulation gain-bandwidth of the voltage regulator. As shown in Figure 5b, the net result is a 6x increase in the regulator's gain bandwidth while providing greater than 75° of phase margin (the difference between $G_{E/A}$ and G_{MOD} respective phases at crossover, f_{CO}).

Other filter schemes pose their own problems. For instance, when choosing high-quality filter capacitor(s), e.g., MLCCs, and an inductor with minimal parasitics, the inherent ESR zero may occur at a much higher frequency, as shown in Figure 5c.

As with the previous example, the actual gain and phase response is overlaid on the power modulator's asymptotic gain response. One readily observes the more dramatic gain and phase transition at or near the power modulator's resonant frequency, f_{LC}, versus the gentler response of the previous example. This is due to the component's lower parasitics leading to the higher frequency of the inherent ESR zero of the output capacitor. In this example, the desired crossover frequency occurs *below* the ESR zero frequency.

In this example, a compensator with an inherent mid-frequency double-zero response is required to mitigate the effects of the filter's double-pole. Such is available with the Type III topology.

As demonstrated in Figure 5d, the Type III's mid-frequency double-zero gain (exhibiting a +20dB/decade slope, noting the compensator's pole at the origin) is designed to compensate for the power modulator's double-pole -40dB/decade attenuation at the desired crossover frequency, f_{CO} (again, $G_{E/A}$ + G_{MOD} = 0dB at f_{CO}). (See Figure 5d).

In the above example, the power modulator's inherent (mid-frequency) -40dB/decade roll-off is mitigated by the mid-frequency double zero's +20dB/decade gain to extend the active regulation gain-bandwidth of the voltage regulator. As shown in Figure 5d, the net result is an approximate doubling in the regulator's gain bandwidth while providing greater than 60° of phase margin (the difference between $G_{E/A}$ and G_{MOD} respective phases at crossover, f_{CO}).

Design procedures for both Type II and Type III compensators are shown below.

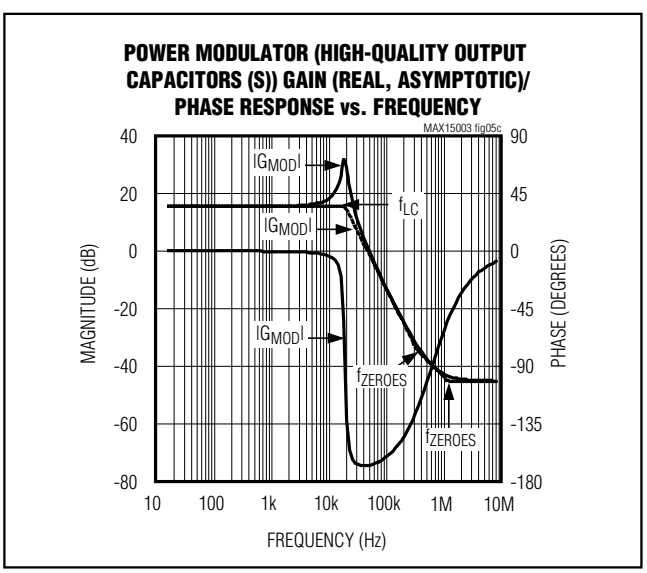


Figure 5c. Power Modulator Gain and Phase Response (High-Quality C_{OUT})

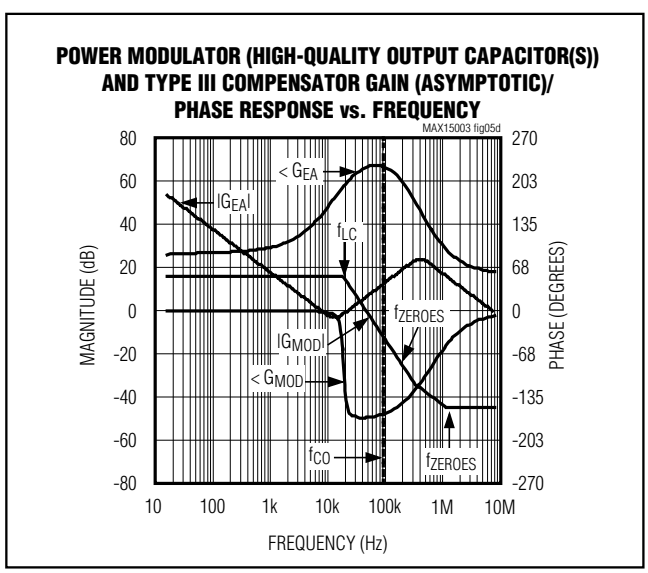


Figure 5d. Power Modulator (High-Quality C_{OUT}) and Type III Compensator Responses

Type II: Compensation When $f_{CO} > f_{ZERO, ESR}$

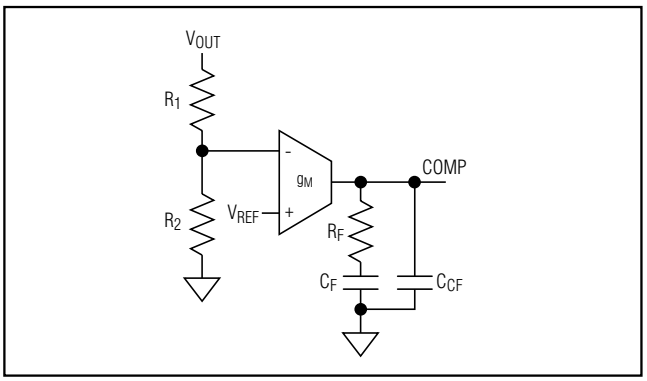


Figure 6a. Type II Compensation Network

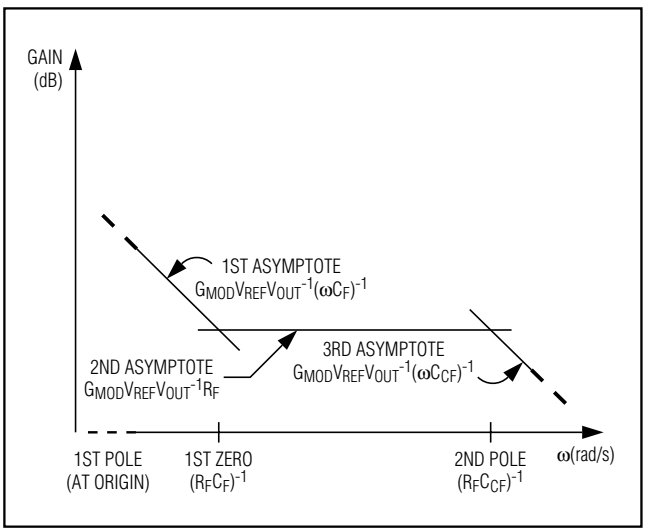


Figure 6b. Type II Compensation Network Response

When the $f_{ZERO,ESR}$ is lower than f_{CO} and close to f_{LC}, a Type II compensation network provides the necessary closed-loop response. The Type II compensation network provides a mid-band compensating zero and high-frequency pole (see Figures 6a and 6b).

R_FC_F provides the mid-band zero $f_{MID,ZERO}$, and R_FC_{CF} provides the high-frequency pole. Use the following procedure to calculate the compensation network components.

1) Calculate the $f_{ZERO,ESR}$ and LC double pole, f_{LC}:

$$f_{ZERO,ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}}$$

2) Calculate the unity-gain crossover frequency as:

$$f_{CO} \le \frac{f_{SW}}{10}$$

3) Determine R_F from the following:

$$R_F = \frac{V_{RAMP}(2\pi \times f_{CO} \times L)V_{OUT}}{V_{FB} \times V_{IN} \times g_m \times ESR}$$

Note: R_F is derived by setting the total loop gain at crossover frequency to unity, e.g., $G_{EA}(f_{CO}) \times G_M(f_{CO}) = 1V/V$. The transconductance error amplifier gain is $G_{EA}(f_{CO}) = g_M \times R_F$ while the modulator gain is:

$$G_{MOD}(f_{CO}) = \frac{V_{IN}}{V_{RAMP}} \times \frac{ESR}{2\pi \times f_{CO} \times L} \times \frac{V_{FB}}{V_{OUT}}$$

The total loop gain can be expressed logarithmically as follows:

$$20\log_{10}[g_m R_F] +$$

$$20\log_{10}\left[\frac{ESR \times V_{IN} \times V_{FB}}{(2\pi \times f_{CO} \times L) \times V_{OUT} \times V_{RAMP}}\right] = 0dB$$

where V_{RAMP} is the peak-to-peak ramp amplitude equal to 2V.

4) Place a zero at or below the LC double pole, f_{LC}:

$$C_F = \frac{1}{2\pi \times R_F \times f_{LC}}$$

5) Place a high-frequency pole at or below $f_P = 0.5 \times f_{SW}$:

$$C_{CF} = \frac{1}{\pi \times R_F \times f_{SW}}$$

6) Choose an appropriately sized R1 (connected from OUT_ to FB_, start with a 10kΩ). Once R1 is selected, calculate R2 using the following equation:

$$R_2 = R_1 \times \frac{V_{FB}}{V_{OUT} - V_{FB}}$$

where $V_{FB} = 0.6V$.

Type III: Compensation When $f_{CO} < f_{ZERO, ESR}$

As indicated above, the position of the output capacitor's inherent ESR zero is critical in designing an appropriate compensation network. When low-ESR ceramic output capacitors are used, the ESR zero frequency ($f_{ZERO, ESR}$) is usually much higher than unity crossover frequency (f_{CO}). In this case, a Type III compensation network is recommended (see Figure 7a).

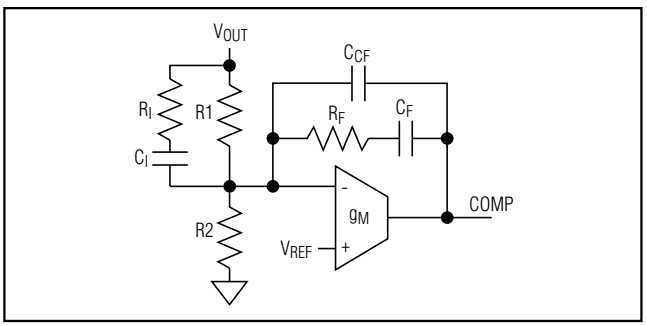


Figure 7a. Type III Compensation Network

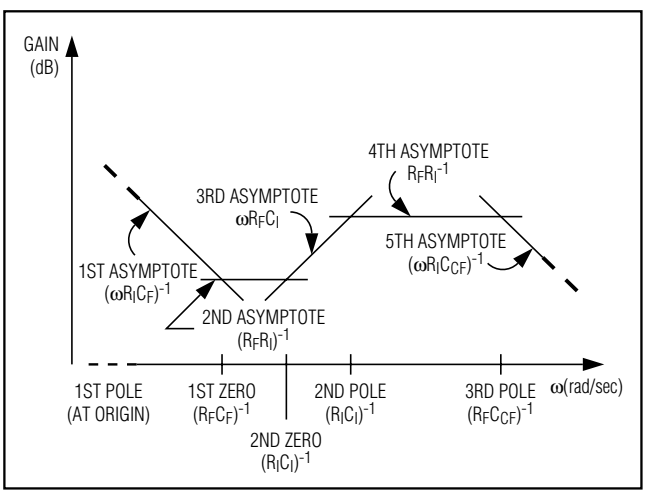


Figure 7b. Type III Compensation Network Response

As shown in Figure 7b, a Type III compensation network introduces two zeros and three poles into the control loop. The error amplifier has a low-frequency pole at the origin, two zeros, and higher frequency poles. The locations of the zeros and poles should be such that the phase margin peaks at f_{CO}.

Set the ratios of f_{CO}-to-f_Z and f_P-to-f_{CO} equal to one another, e.g., $\frac{f_{CO}}{f_Z} = \frac{f_P}{f_{CO}} = 5$ is a good number to get about 60° of phase margin at f_{CO}. Whichever technique, it is important to place the two zeros at or below the double pole to avoid the conditional stability issue.

Use the following procedure to calculate the compensation network components.

1) Select a crossover frequency, f_{CO}:

$$f_{CO} \le \frac{f_{SW}}{10}$$

2) Calculate the LC double-pole frequency, f_{LC} :

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}}$$

3) Select $R_F \ge 10k\Omega$.

4) Place a zero $f_{Z1} = \frac{1}{2\pi \times R_F \times C_F}$ at 0.75 x f_{LC} where

$$C_F = \frac{1}{2\pi \times R_F \times 0.75 \times f_{LC}}$$

5) Calculate C_I for a target unity-gain crossover frequency, f_C:

$$C_I = \frac{2\pi \times f_{CO} \times L \times C_{OUT} \times V_{RAMP}}{V_{IN} \times R_F}$$

Note: C_I is derived by setting the total loop gain at crossover frequency to unity, e.g., $G_{EA}(f_{CO})$ x $G_{MOD}(f_{CO})$ = 1V/V. The total loop gain can be expressed logarithmically as follows:

$$20 \times \log_{10}\left[2\pi \times f_{CO} \times R_F \times C_I\right] +$$

$$20 \times \log_{10}\left[\frac{G_{MOD(DC)}}{\left(2\pi \times f_{CO}\right)^2 \times L \times C_{OUT}}\right] = 0dB$$

6) Place a second zero, f_{Z2}, at or below f_{LC} thereby determining R_1.

$$R_1 = \frac{1}{2\pi \times f_{Z2} \times C_I}$$

7) Place a pole ($f_{P1} = \frac{1}{(2\pi \times R1 \times CI)}$), at or below $f_{ZERO,ESR}$.

$$R_1 = \frac{1}{2\pi \times f_{ZERO,ESR} \times C_I}$$

8) Place a second pole ($f_{P2} = \frac{1}{2\pi \times R_F \times C_{CF}}$) at or below one-half the switching frequency.

$$C_{CF} = \frac{1}{\pi \times f_{SW} \times R_F}$$

9) Calculate R2 using the following equation:

$$R_2 = R_1 \times \frac{V_{FB}}{V_{OUT} - V_{FB}}$$

where V_{FB} = 0.6V.

Typical Operating Circuits

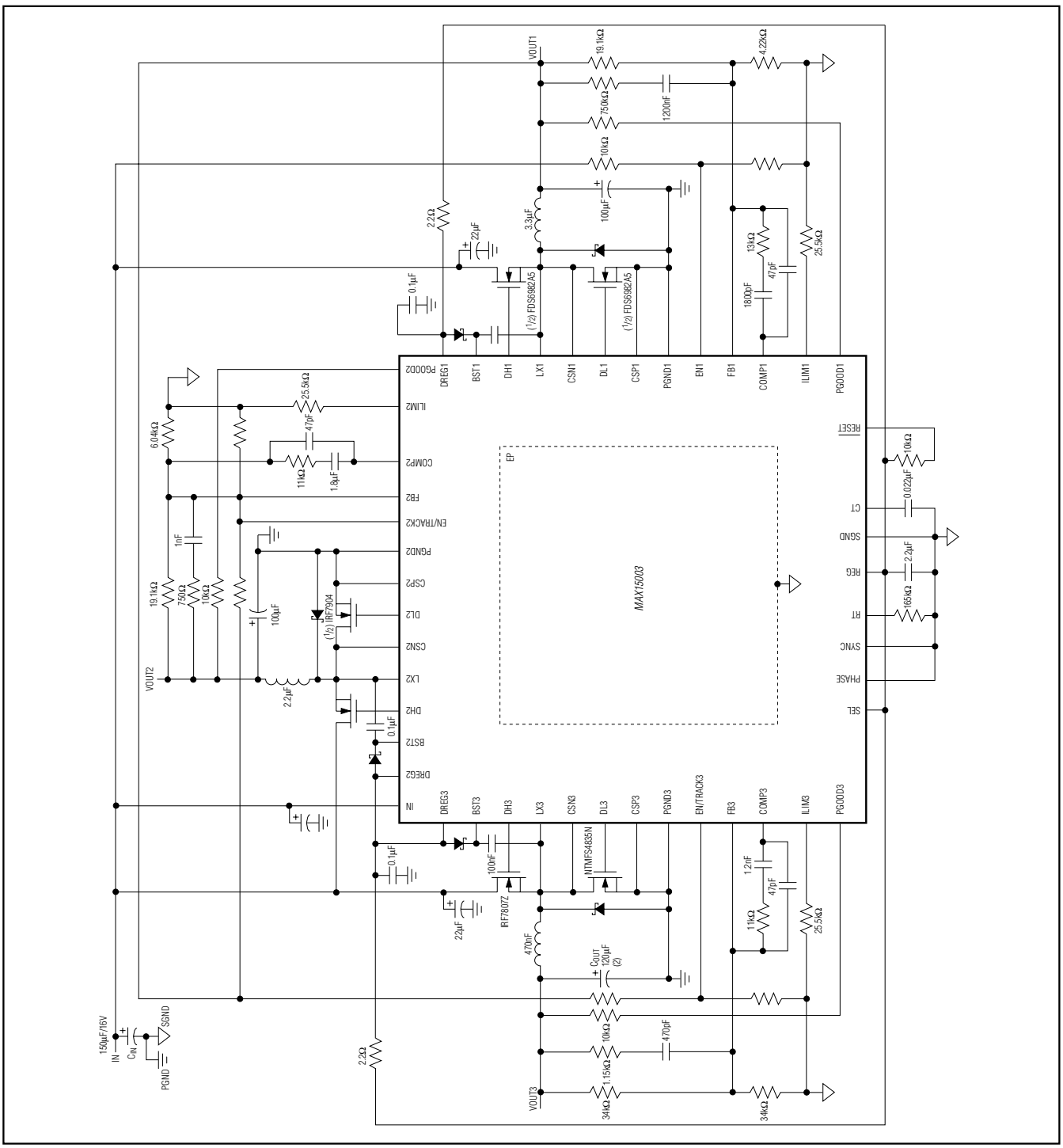


Figure 8. Coincident Triple Tracker with Lossless Current Sense

Typical Operating Circuits (continued)

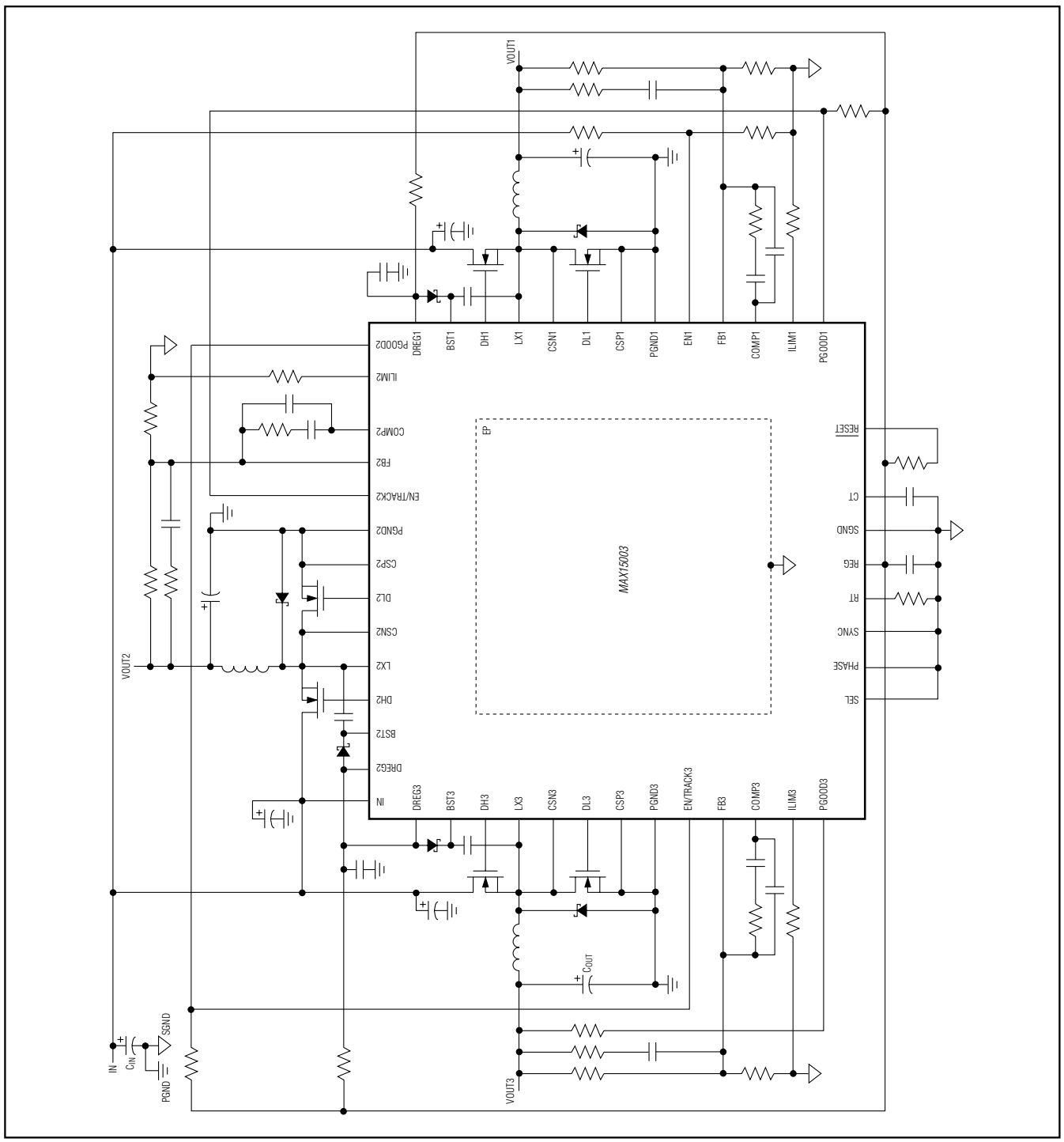


Figure 9. Triple Sequencer with Lossless Current Sense

Typical Operating Circuits (continued)

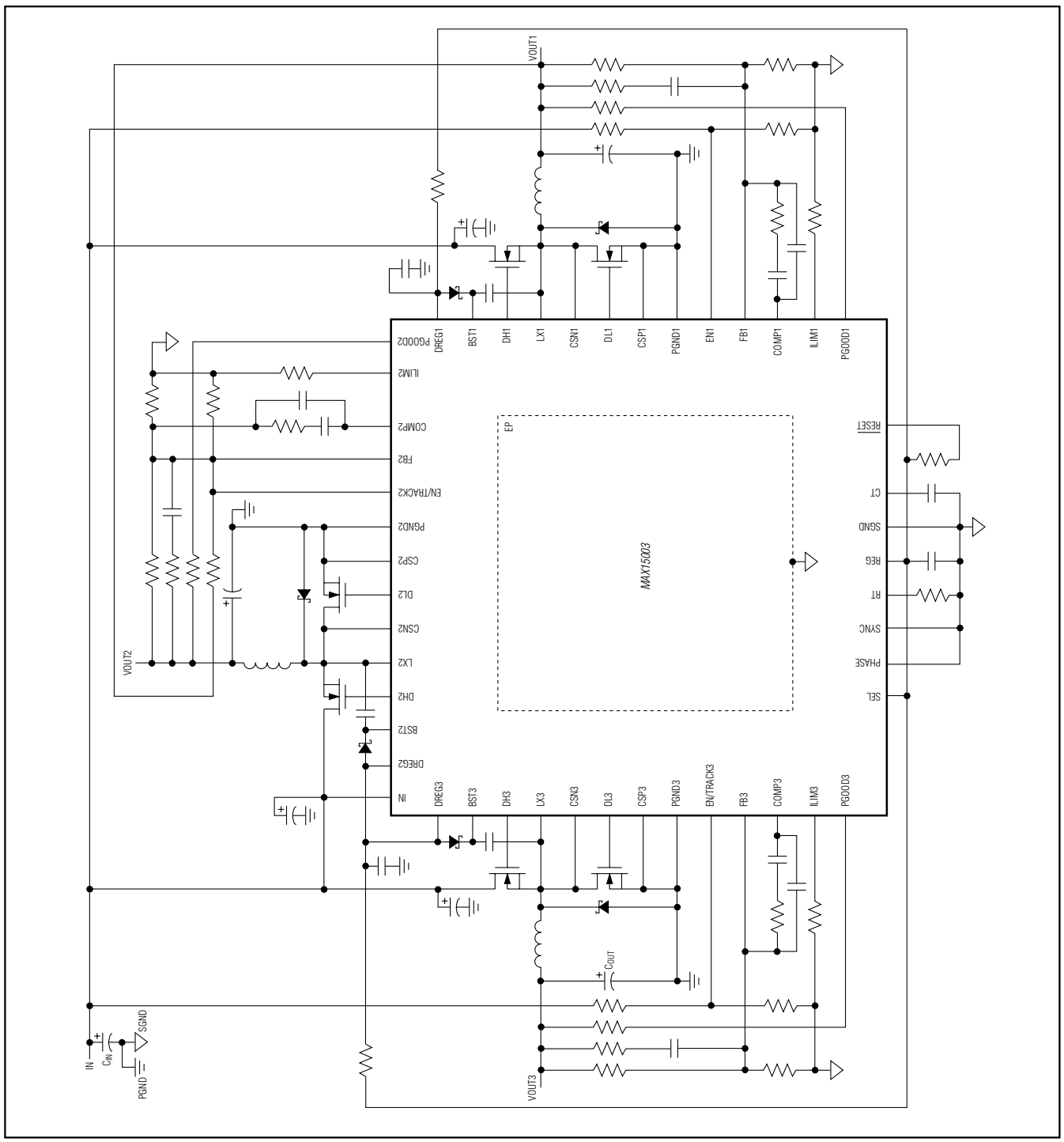


Figure 10. Coincident Dual Tracker and a Sequencer with Lossless Current Sense

Typical Operating Circuits (continued)

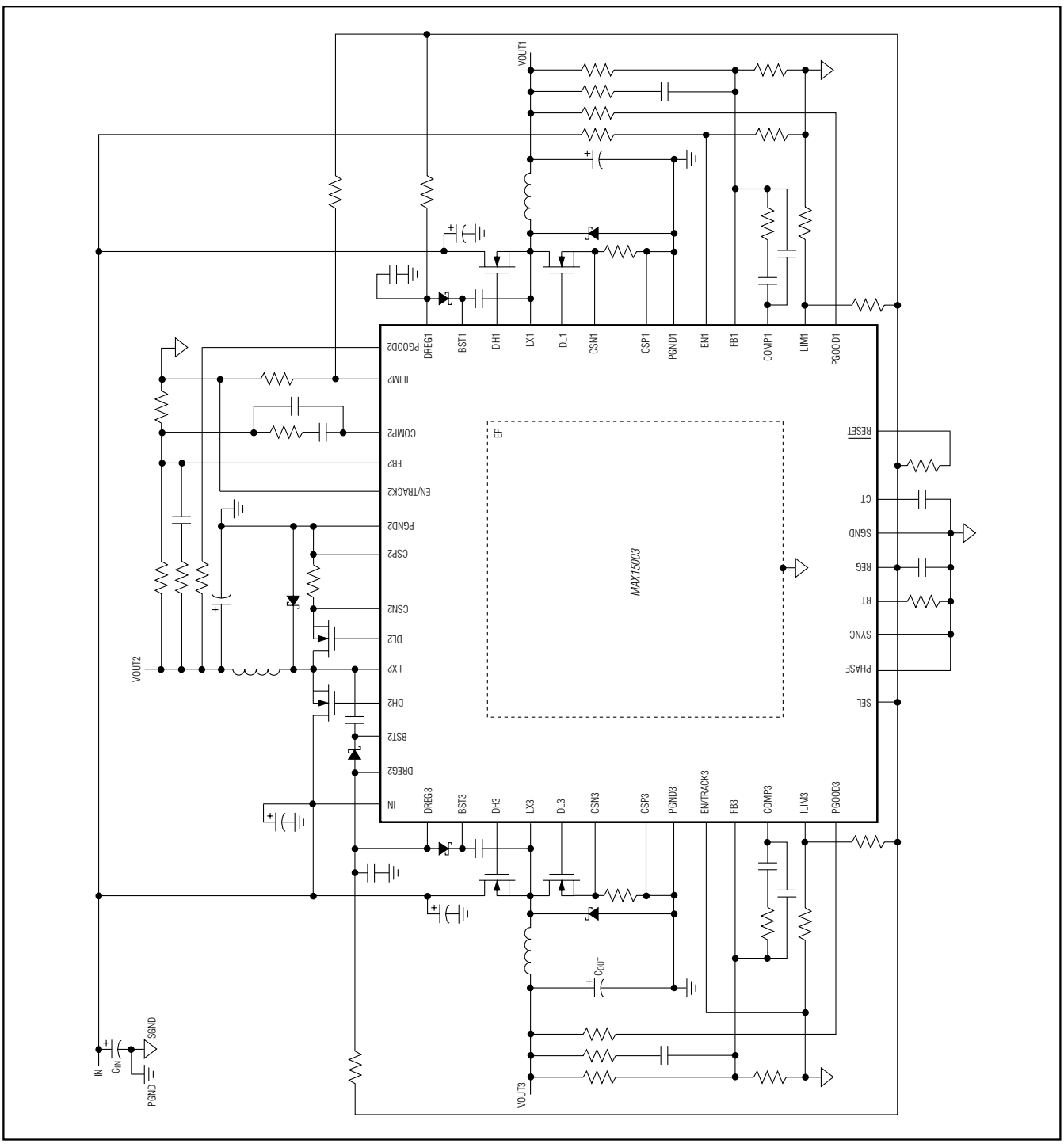


Figure 11. Ratiometric Triple Tracker with Accurate Valley-Mode Current Sense

PWM Controller Applications Information

Power Dissipation

The 48-pin TQFN thermally enhanced package can dissipate up to 3.08W. Calculate power dissipation in the MAX15003 as a product of the input voltage and the total REG output current (I_{REG}). I_{REG} includes quiescent current (I_Q) and the total gate drive current (I_{DREG}):

$$P_D = V_{IN} \times I_{REG}$$

$$I_{REG} = I_Q + [f_{SW} \times (Q_{G1} + Q_{G2} + Q_{G3} + Q_{G4} + Q_{G5} + Q_{G6})]$$

where Q_{G1} to Q_{G6} are the total gate charge of the low-side and high-side external MOSFETs. f_{SW} is the switching frequency of the converter and I_Q is the quiescent current of the device at the switching frequency.

Use the following equation to calculate the maximum power dissipation (P_{DMAX}) in the chip at a given ambient temperature (T_A):

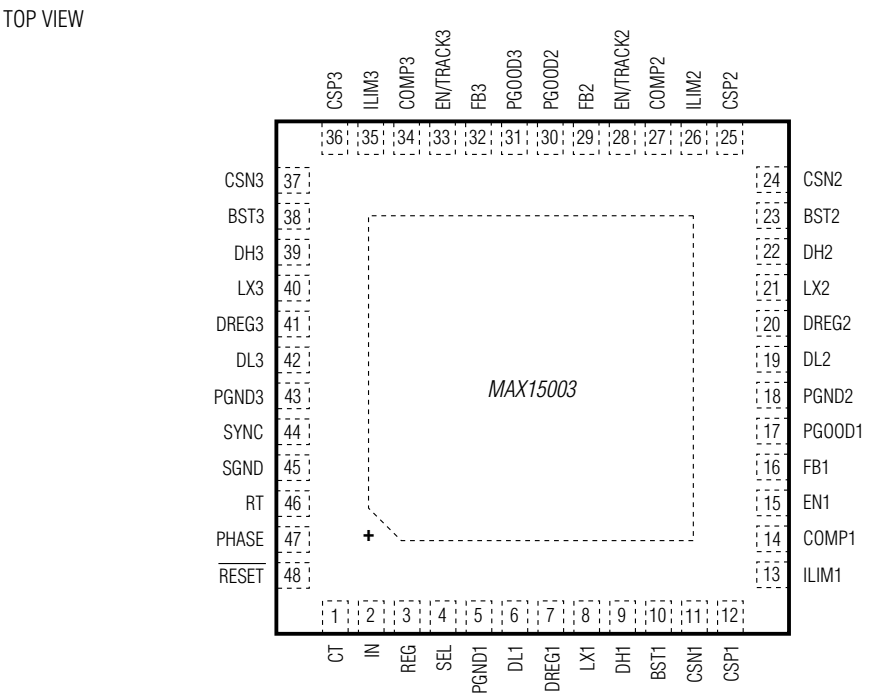
$$P_{DMAX} = 38.5 \times (150 - T_A)\text{.....mW}$$

PCB Layout Guidelines

Use the following guidelines to layout the switching voltage regulator.

1) Place the IN, REG, and DREG_ bypass capacitors close to the MAX15003.
2) Minimize the area and length of the high-current loops from the input capacitor, upper switching MOSFET, inductor, and output capacitor back to the input capacitor negative terminal.
3) Keep the current loop formed by the lower switching MOSFET, inductor, and output capacitor short.
4) Keep SGND and PGND isolated and connect them at one single point close to the negative terminal of the input filter capacitor.
5) Run the current-sense lines CSP_ and CSN_ close to each other to minimize the loop area.
6) Avoid long traces between the DREG_ bypass capacitor, low-side driver outputs of the MAX15003, MOSFET gate, and PGND. Minimize the loop formed by the DREG_ bypass capacitor, bootstrap diode, bootstrap capacitor, high-side driver output of the MAX15003, and upper MOSFET gates.
7) Place the bank of output capacitors close to the load.
8) Distribute the power components evenly across the board for proper heat dissipation.
9) Provide enough copper area at and around the switching MOSFETs, and inductor to aid in thermal dissipation.
10) Connect the MAX15003 exposed paddle to a large copper plane to maximize its power dissipation capability. Connect the exposed paddle to SGND. Do not connect the exposed paddle to the SGND pin (pin 45) directly underneath the IC.
11) Use 2oz copper to keep the trace inductance and resistance to a minimum. Thin copper PCBs compromise efficiency because high currents are involved in the application. Also, thicker copper conducts heat more effectively, thereby reducing thermal impedance.

Pin Configuration



THIN QFN
(7mm x 7mm)

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN-EP	T4877+3	21-0144	90-0129

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/07	Initial release	—
1	8/12	Updated *MOSFET Gate Drivers* section	15