19-1308; Rev 2; 9/06

EVALUATION KIT AVAILABLE

Digitally Controlled Fuel-Gauge Interface

General Description

The MAX1660 digitally controlled fuel-gauge interface executes two essential functions for rechargeable battery-pack management: fuel gauging and pack overcurrent protection. It accurately monitors a battery pack's charge and discharge current flow, and records each using two independent, on-board Coulomb counters. Each counter's contents are externally accessible via a System Management Bus (SMBus™)-compatible 2-wire serial interface. An optional third wire interrupts the microcontroller (µC) when the charge or discharge counters reach a preset value, or when an overcurrent condition (charge or discharge) occurs. In the event of an overcurrent or short-circuit condition, the MAX1660 disconnects the load and alerts its host. The MAX1660's flexibility allows accurate fuel gauging for any battery chemistry, using any desired control algorithm.

The MAX1660 operates with battery voltages from +4V to +28V and provides two micropower shutdown modes, increasing battery lifetime. To minimize total parts count, the device integrates a precision 2.00V system-reference output, a 3.3V linear-regulator output that can supply up to 5mA to power external circuitry, and a power-on reset output for the system µC. The MAX1660 is available in a 16-pin QSOP package.

Applications

Smart-Battery Packs

Battery-Pack Fuel Gauging

Battery-Pack Overcurrent Protection

Digital Current-Sense Instrumentation

Industrial-Control System Interfaces

Analog-to-Digital Conversion

Features

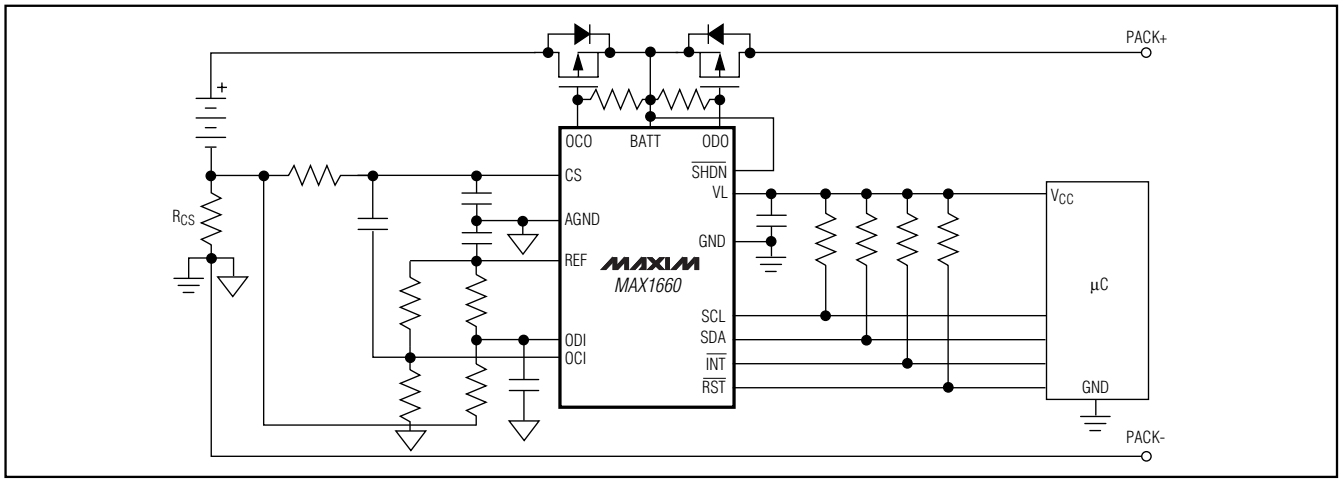
- **1% Accuracy over a 600µA to 4A Current Range (R_{SENSE} = 30mΩ)**
- **5µV Input Offset Voltage (28µV max)**
- **SMBus 2-Wire (Plus Optional Interrupt) Serial Interface**
- **2.00V Precision System Reference Output**
- **3.3V Linear-Regulator Output Powers External Circuitry**
- **Two Micropower Shutdown Modes**
- **Independent 32-Bit Charge and Discharge Coulomb Counters**
- **Battery-Overcharge/Overdischarge Protection**
- **Battery Short-Circuit/Overcurrent Protection**
- **On-Board Power MOSFET Drivers**
- **80µA Quiescent Current**
- **<1µA Shutdown Current**
- **Small 16-Pin QSOP Package (Same Board Area as 8-Pin SO)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX1660EEE	-40°C to +85°C	16 QSOP	E16

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



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For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Digitally Controlled Fuel-Gauge Interface

ABSOLUTE MAXIMUM RATINGS

BATT, ODO, OCO, $\overline{SHDN}$ to GND .....-0.3V to +30V
SCL, SDA, $\overline{INT}$, $\overline{RST}$ to GND .....-0.3V to +6V
REF, ODI, OCI to GND.....-0.3V to (VL + 0.3V)
VL to GND .....-0.3V to +6V
CS to GND.....-2V to +6V
AGND to GND .....-1V to +1V

Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{\overline{SHDN}}$ = V_{BATT} = 12V, V_{SCL} = V_{SDA} = 3.6V, C_{REF} = 10nF, C_{VL} = 0.1µF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND REFERENCES						
BATT Input Voltage Range	V_{BATT}		4		28	V
BATT Supply Current	I_{BATT}	$V_{\overline{SHDN}}$ = 3.3V, SOFTSHDN = 0, I_{VL} = 0		80	135	µA
		$V_{\overline{SHDN}}$ = 3.3V, SOFTSHDN = 1, I_{VL} = 0		15	30	
		$V_{\overline{SHDN}} \le 0.4V$		0.02	1	
VL Output Voltage	V_{VL}	SOFTSHDN = 0, 0 ≤ I_{VL} ≤ 5mA	3.1	3.25	3.4	V
		SOFTSHDN = 1, 0 ≤ I_{VL} ≤ 5mA	3.1	3.25	3.6	
REF Output Voltage	V_{REF}	I_{REF} = 0	1.96	2.00	2.04	V
REF Load Regulation		0 ≤ I_{REF} ≤ 200µA		10	50	µV/µA
FUEL GAUGE						
CS to AGND Input Resistance				100		kΩ
Discharge Coulomb-Counter Accumulation Rate		V_{CS} = 0	0	2	12	Counts/s
		V_{CS} = -120mV	49,500	50,000	50,500	
Charge Coulomb-Counter Accumulation Rate		V_{CS} = 0	0	2	12	Counts/s
		V_{CS} = 120mV	49,500	50,000	50,500	
OVERCURRENT COMPARATOR						
OCI, ODI Input Offset Voltage			-7	0	7	mV
OCI, ODI Input Offset Current		(Note 1)	-1	0.01	1	µA
Propagation Delay				1		µs
ODO Sink Current		V_{ODO} = 0.4V	1	2.5		mA
ODO Off-Leakage Current		V_{ODO} = 28V		0.01	1	µA
OCO Sink Current		V_{OCO} = 0.4V	1	2.5		mA
OCO Off-Leakage Current		V_{OCO} = 28V		0.01	1	µA
INTERFACE-LOGIC LEVELS						
Input High Voltage	V_{IH}	$\overline{SHDN}$, SCL, SDA	2.2			V
Input Low Voltage	V_{IL}	SCL, SDA			0.8	V
		$\overline{SHDN}$			0.6	
SDA Output Low Sink Current	V_{OL}	V_{SDA} = 0.6V	6			mA
$\overline{INT}$ Output Low Sink Current	V_{OL}	$V_{\overline{INT}}$ = 0.4V	2			mA

ELECTRICAL CHARACTERISTICS (continued)

($V_{\overline{SHDN}}$ = V_{BATT} = 12V, V_{SCL} = V_{SDA} = 3.6V, C_{REF} = 10nF, C_{VL} = 0.1µF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL, SDA, $\overline{INT}$, $\overline{RST}$ Leakage Current		Output forced to 5V		0.01	1	µA
$\overline{SHDN}$ Input Bias Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ forced to 3.6V		0.7	3.0	µA
		$\overline{SHDN}$ forced to 28V		20	100	
$\overline{RST}$ Active Timeout Period				25		ms
$\overline{RST}$ Output Voltage	$V_{\overline{RST}}$	V_{VL} = 1V, I_{SINK} = 50µA			0.3	V
		V_{VL} = 3V, I_{SINK} = 1.2mA			0.3	
$\overline{RST}$ Threshold Voltage	V_{TH1}, V_{TH2}	V_{TH2}, VL falling	1.0	1.7	2.2	V
		V_{TH1}, VL rising	2.75	2.90	3.05	

ELECTRICAL CHARACTERISTICS

($V_{\overline{SHDN}}$ = V_{BATT} = 12V, V_{SCL} = V_{SDA} = 3.6V, C_{REF} = 10nF, C_{VL} = 0.1µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND REFERENCES						
BATT Input Voltage Range	V_{BATT}		4		28	V
BATT Supply Current	I_{BATT}	$V_{\overline{SHDN}}$ = 3.3V, SOFTSHDN = 0, I_{VL} = 0			135	µA
		$V_{\overline{SHDN}}$ = 3.3V, SOFTSHDN = 1, I_{VL} = 0			30	
		$V_{\overline{SHDN}} \le$ 0.4V			1	
VL Output Voltage	V_{VL}	SOFTSHDN = 0, 0 ≤ I_{VL} ≤ 5mA	3.1		3.4	V
		SOFTSHDN = 1, 0 ≤ I_{VL} ≤ 5mA	3.1		3.6	
REF Output Voltage	V_{REF}	I_{REF} = 0	1.96		2.04	V
REF Load Regulation		0 ≤ I_{REF} ≤ 200µA			50	µV/µA
FUEL GAUGE						
Discharge Coulomb-Counter Accumulation Rate		V_{CS} = 0	0		12	Counts/s
		V_{CS} = -120mV	49,250		50,750	
Charge Coulomb-Counter Accumulation Rate		V_{CS} = 0	0		12	Counts/s
		V_{CS} = 120mV	49,250		50,750	
OVERCURRENT COMPARATOR						
OCI, ODI Input Offset Voltage			-10		10	mV
OCI, ODI Input Offset Current		(Note 1)	-1		1	µA
ODO Sink Current		V_{ODO} = 0.4V	1			mA
ODO Off-Leakage Current		V_{ODO} = 28V			1	µA
OCO Sink Current		V_{ODO} = 0.4V	1			mA
OCO Off-Leakage Current		V_{ODO} = 28V			1	µA

ELECTRICAL CHARACTERISTICS (continued)

($V_{\overline{SHDN}}$ = V_{BATT} = 12V, V_{SCL} = V_{SDA} = 3.6V, C_{REF} = 10nF, C_{VL} = 0.1µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERFACE-LOGIC LEVELS						
Input High Voltage	V_{IH}	$\overline{SHDN}$, SCL, SDA	2.2			V
Input Low Voltage	V_{IL}	SCL, SDA			0.8	V
		$\overline{SHDN}$			0.6	
SDA Output Low Sink Current	V_{OL}	V_{SDA} = 0.6V	6			mA
$\overline{INT}$, $\overline{RST}$ Output Low Sink Current	V_{OL}	$V_{\overline{INT}}$ = 0.4V	2			mA
SCL, SDA, $\overline{INT}$, $\overline{RST}$ Leakage Current		Output forced to 5V			1	µA
$\overline{SHDN}$ Input Bias Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ forced to 3.6V			3.0	µA
		$\overline{SHDN}$ forced to 28V			120	
$\overline{RST}$ Output Voltage	$V_{\overline{RST}}$	V_{VL} = 1V, I_{SINK} = 50µA			0.3	V
		V_{VL} = 3V, I_{SINK} = 1.2mA			0.3	
$\overline{RST}$ Threshold Voltage	V_{TH1}, V_{TH2}	V_{TH2}, VL falling	1.0		2.2	V
		V_{TH1}, VL rising	2.75		3.05	

TIMING CHARACTERISTICS

(**T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Serial-Clock High Period	t_{HIGH}		4			µs
SCL Serial-Clock Low Period	t_{LOW}		4.7			µs
START Condition Setup Time	$t_{SU:STA}$		4.7			µs
START Condition Hold Time	$t_{HD:STA}$		4			µs
SDA Valid to SCL Rising-Edge Setup Time, Slave Clocking in Data	$t_{SU:DAT}$		800			ns
SCL Falling Edge to SDA Transition	$t_{HD:DAT}$		0			ns
SCL Falling Edge to SDA Valid, Master Clocking in Data	t_{DV}				1	µs

TIMING CHARACTERISTICS

(**T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Serial-Clock High Period	t_{HIGH}		4			µs
SCL Serial-Clock Low Period	t_{LOW}		4.7			µs
START Condition Setup Time	$t_{SU:STA}$		4.7			µs
START Condition Hold Time	$t_{HD:STA}$		4			µs
SDA Valid to SCL Rising-Edge Setup Time, Slave Clocking in Data	$t_{SU:DAT}$		800			ns
SCL Falling Edge to SDA Transition	$t_{HD:DAT}$		0			ns
SCL Falling Edge to SDA Valid, Master Clocking in Data	t_{DV}				1	µs

Note 1: OCI and ODI are MOSFET inputs. Minimum and maximum limits are for production screening only. Actual performance is indicated in typical value.

Note 2: Specifications to -40°C are guaranteed by design, not production tested.

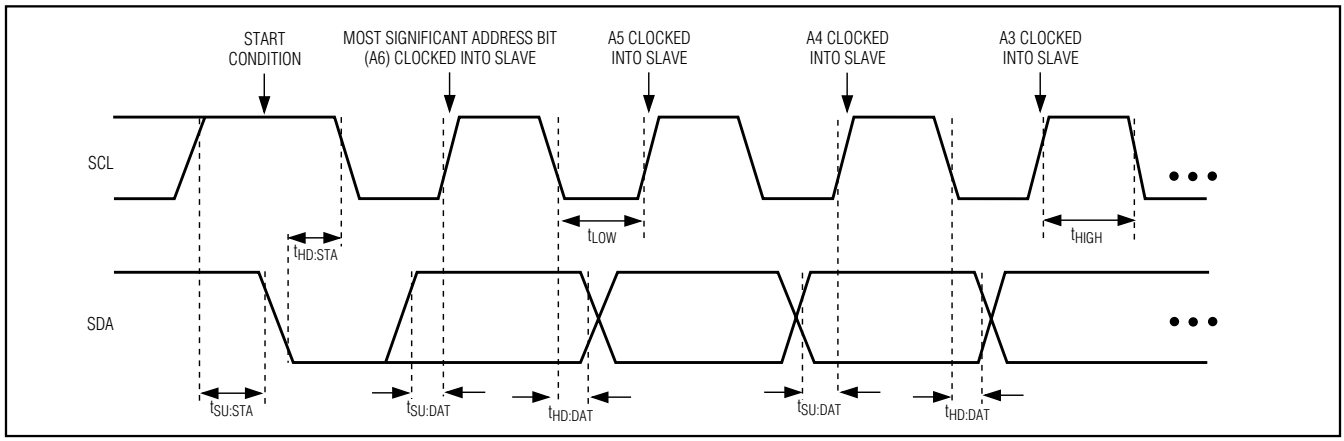


Figure 1. SMBus Serial-Interface Timing—Address

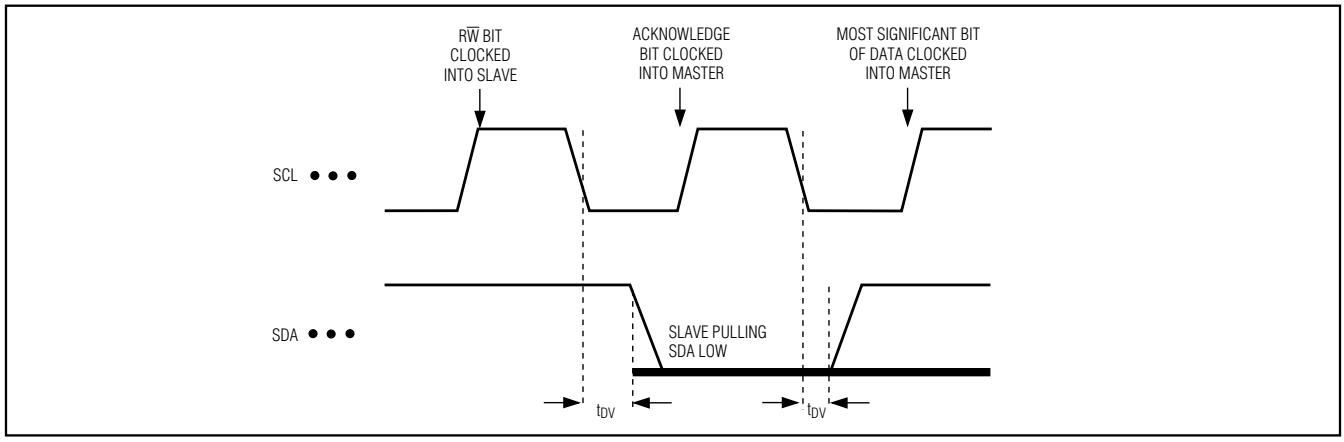


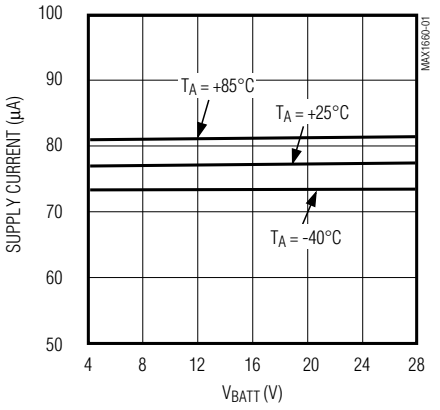
Figure 2. SMBus Serial-Interface Timing—Acknowledge

Digitally Controlled Fuel-Gauge Interface

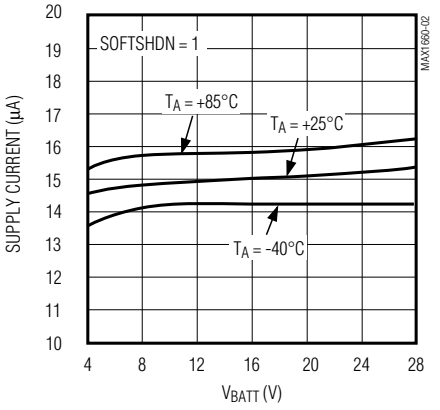
Typical Operating Characteristics

(V_{BATT} = $V_{\overline{SHDN}}$ = 12V, C_{REF} = 10nF, C_{VL} = 0.1µF, T_A = +25°C, unless otherwise noted.)

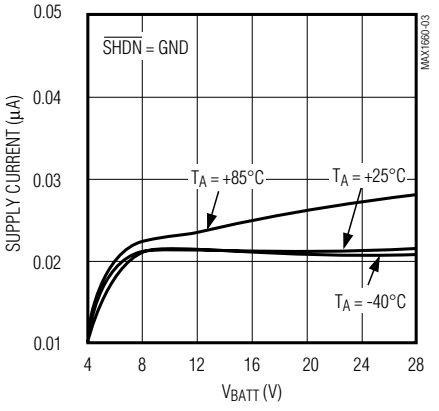
SUPPLY CURRENT vs. V_{BATT}



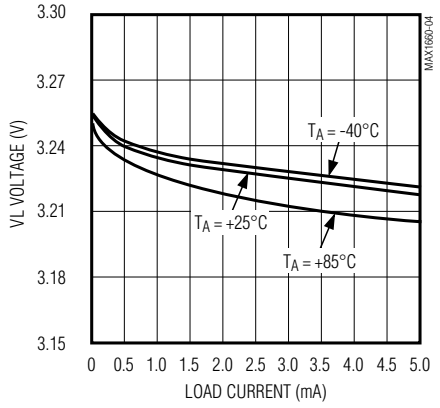
SHUTDOWN SUPPLY CURRENT vs. V_{BATT}



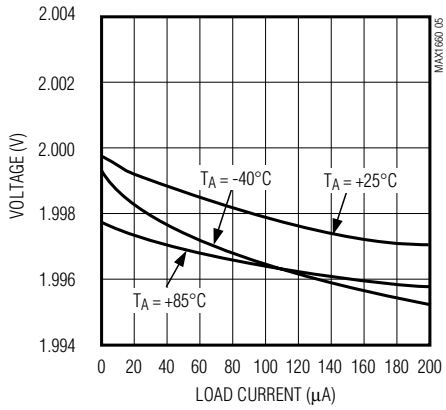
SHUTDOWN SUPPLY CURRENT vs. V_{BATT}



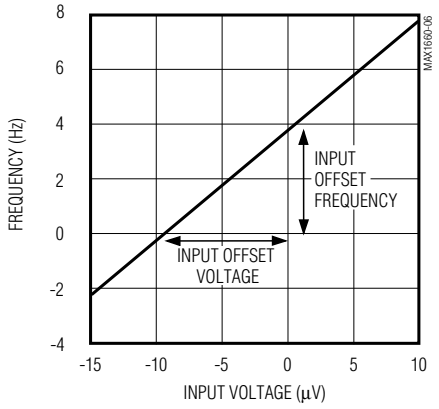
VL VOLTAGE vs. VL LOAD CURRENT



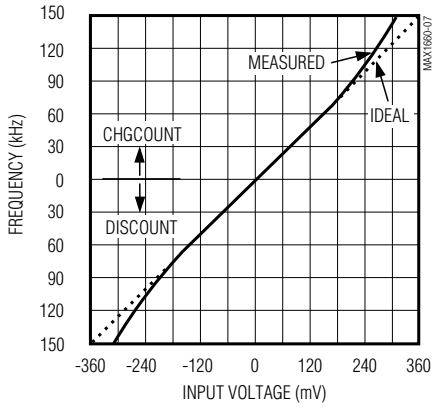
REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT



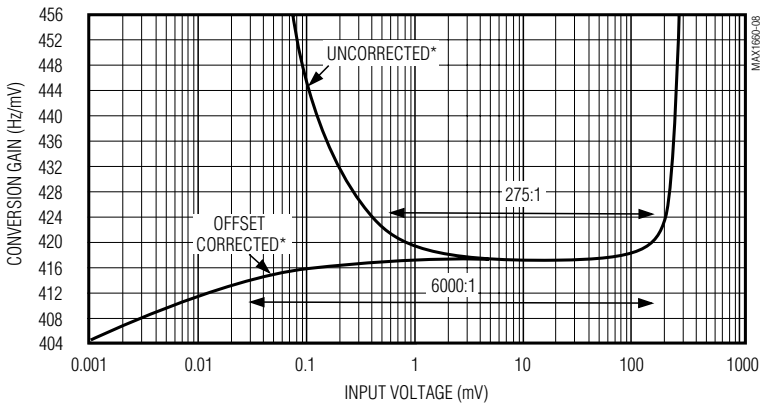
FREQUENCY vs. INPUT VOLTAGE



FREQUENCY vs. INPUT VOLTAGE



CONVERSION GAIN vs. INPUT VOLTAGE



*SEE INTERNAL OFFSET MEASUREMENT SECTION

Pin Description

PIN	NAME	FUNCTION
1	$\overline{INT}$	Open-Drain Host-Interrupt Output. $\overline{INT}$ sinks current when active, otherwise high-impedance (see *$\overline{INT}$ Output* section). $\overline{INT}$ is compatible with the SMBus SMBALERT# (the "#" indicates asserted low) signal. Connect a 100kΩ pullup resistor between $\overline{INT}$ and VL. Leave $\overline{INT}$ unconnected if host interrupt is not used.
2	$\overline{SHDN}$	Active-Low Shutdown Input (see *Shutdown Modes* section)
3	N.C.	No Connection. Not internally connected.
4	CS	Current-Sense Resistor Input
5	AGND	Analog Ground
6	REF	2.00V Reference Output. Bypass REF to AGND with a 10nF capacitor (see *Internal Regulator and Reference* section).
7	ODI	Discharge Overcurrent-Detection Input (see *Overcurrent Detection* section)
8	OCI	Charge Overcurrent-Detection Input (see *Overcurrent Detection* section)
9	GND	Ground
10	VL	3.3V Linear-Regulator Output. Bypass VL with a 0.33µF capacitor to GND (see *Internal Regulator and Reference* section).
11	BATT	Supply Input
12	ODO	High-Voltage, Open-Drain MOSFET Gate-Driver Output. ODO controls activation of the battery-discharge path (see *OCO and ODO Gate Drivers* section).
13	OCO	High-Voltage, Open-Drain MOSFET Gate-Driver Output. OCO controls activation of the battery-charge path (see *OCO and ODO Gate Drivers* section).
14	$\overline{RST}$	Active-Low Reset Output. Connect a 100kΩ pullup resistor between $\overline{RST}$ and VL. Leave $\overline{RST}$ unconnected if the power-on reset function is not used (see *$\overline{RST}$ Output* section).
15	SDA	Serial-Data Input/Output. Connect a 10kΩ resistor between SDA and VL (see *SMBus Interface* section).
16	SCL	Serial-Clock Input. Connect a 10kΩ resistor between SDA and VL (see *SMBus Interface* section).

Detailed Description

The MAX1660 measures the cumulative charge into (charging) and out of (discharging) the system battery pack and stores the information in one of two internal, independent charge and discharge counters. It achieves battery-pack overcharge and overdischarge protection through a powerful digital compare function that interrupts the host CPU when the charge or discharge counter reaches a host-programmed value. The device also informs the host of changes in the direction of current flow and protects the battery pack from short-circuit and overcurrent conditions.

The MAX1660 incorporates a 2-wire SMBus-compliant serial interface, allowing access to charge/discharge counters and internal registers. An optional third wire provides an SMBALERT#-compliant interrupt signal, or it may be used as a simple, stand-alone host interrupt.

Coulomb-Counting Interface

The MAX1660's Coulomb-counting interface monitors the charge flowing in either the charging or discharging direction, and counts the Coulombs of charge by incrementing either the charge counter (CHGCOUNT) or the discharge counter (DISCOUNT) accordingly. The number of counter increments generated per Coulomb of charge sensed (conversion gain) is given by the following equation:

$$A_C = 416.7 \times 10^3 \, R_{CS} \, \frac{Counts}{Coulomb}$$

where R_{CS} is the current-sense resistor (see the *Typical Operating Circuit*). The gain factor is the constant of proportionality that relates the counter values stored in CHGCOUNT and DISCOUNT to the amount of charge flow into or out of the battery pack. A higher conversion gain (larger R_{CS}) increases resolution at low currents,

Digitally Controlled Fuel-Gauge Interface

but limits the maximum measurable current. Likewise, a smaller conversion gain (smaller R_{CS}) decreases resolution at low currents, but increases the maximum measurable current. A 30mΩ current-sense resistor (A_C = 12.5 x 10^3 counts per Coulomb) provides a good balance between resolution and input current range for many applications. With this current-sense resistance, the MAX1660 typically measures currents from 600µA to 4A with better than 1% accuracy (see the section *Choosing R_{CS}*).

Charge and Discharge Counters

Figure 3 shows the functional diagram of the MAX1660's Coulomb-counter section. The Coulomb counter's output increments (but never decrements) one of two independent 32-bit counters: CHGCOUNT for charging currents, and DISCOUNT for discharging currents. By independently counting the charge and discharge currents, the MAX1660 can accommodate any algorithm to account for a battery pack's energy-conversion efficiency. A 2x1 multiplexer, gated by the configuration word's SETCOUNT bit, determines which counter's contents are passed to the COUNT register when COUNT updates. The 32-bit COUNT register is divided into 4 bytes: COUNT0 (the least significant) through COUNT3 (the most significant). See Table 1 for a description of the different registers.

CHGCOUNT and DISCOUNT reset to zero whenever a power-on reset executes, or when the configuration word's CLRCOUNTER bit is set. Each counter also resets any time an overflow condition occurs. The counters' 32-bit capacity allows them to continually monitor 4A for almost 24 hours before overflowing (with R_{CS} = 30mΩ). When a counter overflows, it simply clears and begins counting from 0; no interrupts are generated.

Execute the ReadCount01 and ReadCount23 commands to read the active counter's contents at any time (Table 2). Since the Read-Word protocol supports only 16-bit data transfers, issue these commands sequentially to read the entire 32-bit COUNT register. First issue ReadCount01 to read COUNT0 and COUNT1, and then issue ReadCount23 to read COUNT2 and COUNT3. Executing ReadCount01 enables updating of the COUNT register; the COUNT register updates on SCL's falling edge after the command-byte ACK bit

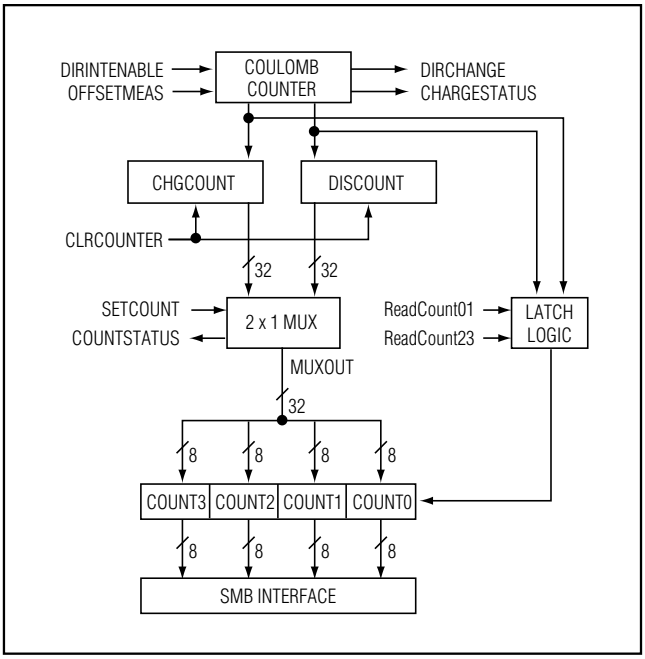


Figure 3. Coulomb-Counter Functional Diagram

Table 1. Register Descriptions

REGISTER NAME	DESCRIPTION
CHGCOUNT	The 32-bit counter that accumulates the number of units of charge that have passed through R_{CS} in the charging direction since CHGCOUNT was last cleared. CHGCOUNT clears on a power-on reset, or when the configuration word's CLEARCOUNTER bit is set. CHGCOUNT is unaffected by discharging currents.
DISCOUNT	The 32-bit counter that accumulates the number of units of charge that have passed through R_{CS} in the discharging direction since DISCOUNT was last cleared. DISCOUNT clears on a power-on reset, or when the configuration word's CLEARCOUNTER bit is set. DISCOUNT is unaffected by charging currents.
COUNT	The 32-bit register that stores the value held in the counter selected by the configuration word's SETCOUNT bit when updating has been enabled by the ReadCount01 command. Data transfers to COUNT from the selected CHGCOUNT or DISCOUNT register whenever the MAX1660's SMBus interface detects a new command. See the *Charge and Discharge Counters* section.
COMP	The 32-bit register that stores the host-defined COUNT threshold. The contents of COMP are continuously compared with the contents of either CHGCOUNT or DISCOUNT (whichever is selected by the SETCOUNT bit) for equality. When an equality occurs, the configuration word's COMPSTATUS bit is set, and an interrupt is generated ($\overline{INT}$ goes low).

Table 2. Read Word Commands

COMMAND NAME	COMMAND CODE	DESCRIPTION
ReadCount01	0x82	Enables updating of the COUNT register; returns COUNT0 in the LSB and COUNT1 in the MSB of the Read-Word protocol. COUNT updating remains enabled until the ReadCount23 command is executed. See the *Charge and Discharge Counters* section.
ReadCount23	0x83	Disables COUNT register updating; returns COUNT2 in the LSB and COUNT3 in the MSB of the Read-Word protocol. See the *Charge and Discharge Counters* section.
ReadStatus()	0x84	Returns the status word's contents in the Read-Word protocol's LSB. The MSB's contents are all 1s. See Table 5 for a description of the status bits.

clocks in (Figure 4). COUNT0 returns in the least significant byte (LSB), and COUNT1 returns in the most significant byte (MSB) of the Read-Word protocol. After the ReadCount01 command is executed (updating is enabled), any command executed by the MAX1660 prior to execution of the ReadCount23 command updates the COUNT contents, potentially corrupting the data read by ReadCount23 (if a 16th-bit carry occurs). ReadCount23 disables COUNT updating and then returns COUNT2 and COUNT3 in the Read-Word protocol's LSB and MSB. To ensure proper execution, issue these commands in the correct order, with no commands executed between them (ReadCount01 first, followed by ReadCount23).

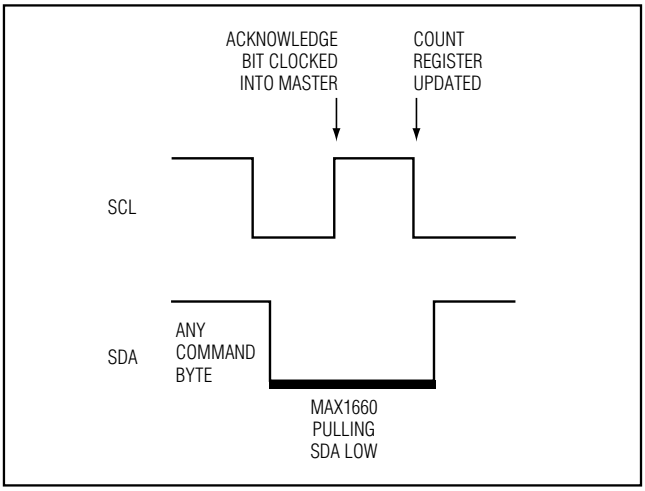


Figure 4. COUNT Register Updating

Digital Compare Function

The MAX1660's digital compare function simplifies implementation of end-of-charge and end-of-discharge detection, relieving the host from having to constantly monitor the counters. The host simply programs a value into the COMP register, and the MAX1660 generates an interrupt ($\overline{INT}$ goes low) when this condition is met.

Figure 5 shows the MAX1660's digital compare section functional diagram. When the digital compare function is enabled, the MAX1660 continuously compares the contents of the counter selected by the configuration word's SETCOUNT bit with the 32-bit word stored in the COMP register (Table 1). The 32-bit COMP register is divided into 4 bytes: COMP0 (the least significant) through COMP3 (the most significant). When COMP is equal to MUXOUT, the configuration word's COMPSTATUS bit is set, and the MAX1660 generates an interrupt ($\overline{INT}$ goes low). The host defines any action taken as a result of this interrupt. The COMP register contents remain valid until either the host redefines the value stored in COMP, or a power-on reset is executed. Executing a power-on reset disables the digital compare function. Enable the digital compare function by setting the configuration word's COMPENABLE bit.

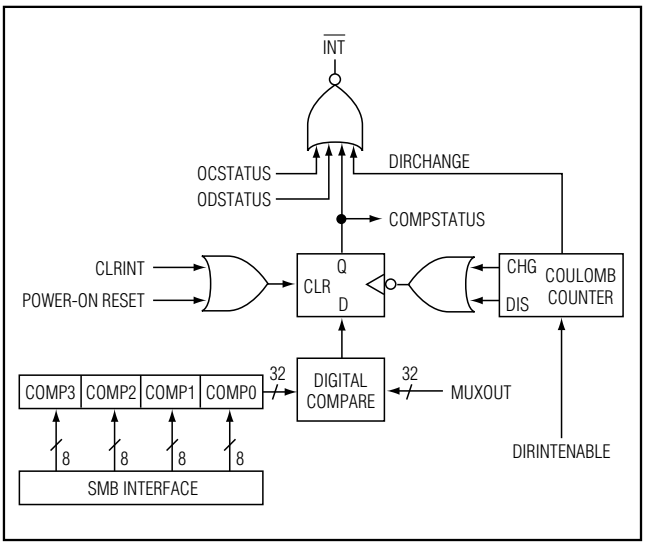


Figure 5. Digital Compare Section Functional Diagram

Digitally Controlled Fuel-Gauge Interface

Use the WriteComp01 and WriteComp23 commands to define the COMP register contents (Table 3). Since the Write-Word protocol supports only 16-bit data transfers, sequentially execute these commands to write the entire 32-bit COMP word. First execute WriteComp01 to write COMP0 and COMP1, and then execute WriteComp23 to write COMP2 and COMP3. Executing WriteComp01 internally disables the COMPINT interrupt and writes the Write-Word protocol's LSB into COMP0 and its MSB into COMP1. The COMPINT interrupt disables on SCL's 18th rising edge during WriteComp01 execution (Figure 6). Executing WriteComp23 writes the Write-Word protocol's LSB and MSB into COMP2 and COMP3, and enables the COMPINT interrupt. The COMPINT interrupt reenables on the falling edge following SCL's 36th rising edge during WriteComp23 execution. Disabling the COMPINT interrupt with the WriteComp01 command prevents an erroneous interrupt, due to incomplete data in the COMP register. To ensure proper execution, issue these commands in the correct sequence.

Direction-Change Detection Function

The MAX1660's direction-change detection function informs the host whenever the current flow changes direction. When it is used in conjunction with the MAX1660's digital compare function and CHARGE-STATUS bit in end-of-charge and end-of-discharge detection routines, the host can ensure that the digital compare function continues to monitor the proper counter when the current flow changes direction.

The direction-change function is simple: the status word's DIRCHANGE bit sets any time the current flow changes direction. Once DIRCHANGE is set, it remains set until it is cleared; additional changes in the current-flow direction do not affect the bit. To clear the DIRCHANGE bit, write a 1 to the configuration word's CLRINT bit. DIRCHANGE also clears when the MAX1660 enters soft-shutdown mode and after a power-on reset. In end-of-charge and end-of-discharge routines, in which the host must be informed immediately of a change in current-flow direction, set the configuration word's DIRINTENABLE bit to generate an interrupt whenever the status word's DIRCHANGE bit is set.

Table 3. Write-Word Commands

COMMAND NAME	COMMAND CODE	DESCRIPTION
WriteComp01	0x00	Disables the COMPINT interrupt; writes the Write-Word protocol's LSB into COMP0 and its MSB into COMP1.
WriteComp23	0x01	Writes the Write-Word protocol's LSB into COMP2 and its MSB into COMP3, and enables the COMPINT interrupt.
WriteConfig()	0x04	Writes the Write-Word protocol's data bytes into the configuration word. See Table 6 for a description of the configuration bits.

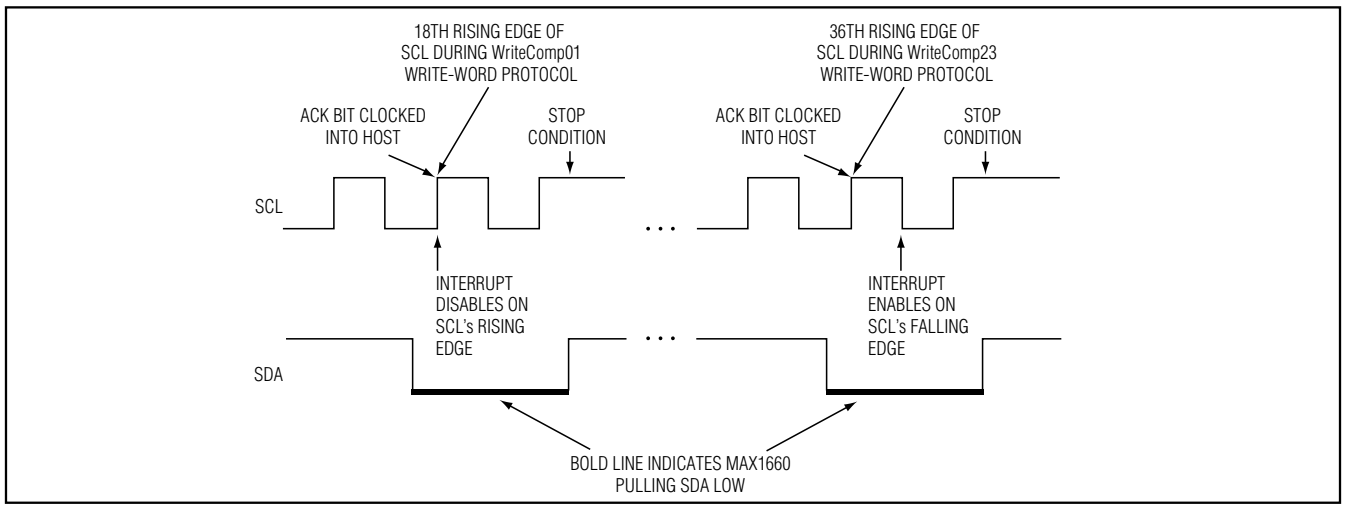


Figure 6. Automatic Interrupt Enable/Disable During COMP Update

Overcurrent Detection

The MAX1660's precision analog interface continuously monitors the input current to detect an overcurrent condition. Figure 7 shows the functional diagram of the overcurrent comparator section.

An overcurrent condition occurs whenever the voltage on CS exceeds the voltage on OCI (for charging currents), or when ODI falls below ground (for discharging currents). When an overcurrent condition occurs, the overcurrent comparators generate an interrupt ($\overline{INT}$ goes low) and set the OD (discharging) or OC (charging) latch, which remains set until either the configuration word's CLRINT bit is set, the MAX1660 enters soft-shutdown mode, or the MAX1660 initiates a power-on reset. The host defines any action taken upon receipt of this interrupt. A logic block follows the latch, which sets the gate-driver output's appropriate state, as defined in Table 4, and drives the n-channel MOSFET open-drain gate drivers.

Although the host has complete control over the MAX1660's response to an overcurrent condition, take care to ensure adequate overcurrent protection. In general, the configuration word's OCLO and ODLO bits should *always* remain cleared. This ensures that either the MAX1660 will be in overcurrent autodetect mode (the power-on-reset state), or the external FETs are forced off (the load is disconnected). Regardless of the OCLO and ODLO bit settings, the MAX1660 interrupts the host ($\overline{INT}$ goes low) if the current flow exceeds the overcurrent threshold.

When OCHI = OCLO = 1 or ODHI = ODLO = 1, the corresponding overcurrent comparator operates in free-running mode, driving OCO and ODO directly. When the current exceeds the overcurrent threshold, the appropriate MOSFET turns off, and when the current is below the overcurrent threshold, it turns on. Forcing the MOSFET off prevents current from flowing, which in turn decreases the current flow to below the overcurrent threshold. A persistent overcurrent condition, therefore, produces a pulsed output as the current flow repeatedly crosses the overcurrent threshold. In free-running mode, $\overline{INT}$ pulls low when the first overcurrent condition occurs, and stays low until the interrupt is cleared, as described in the *$\overline{INT}$ Output* section. Operation in this mode requires that OCO and ODO be buffered to ensure fast MOSFET turn-off and slow MOSFET turn-on times. The relatively slow turn-off response of the OCO and ODO open-drain outputs alone is unsuitable for driving MOSFETs directly in this mode.

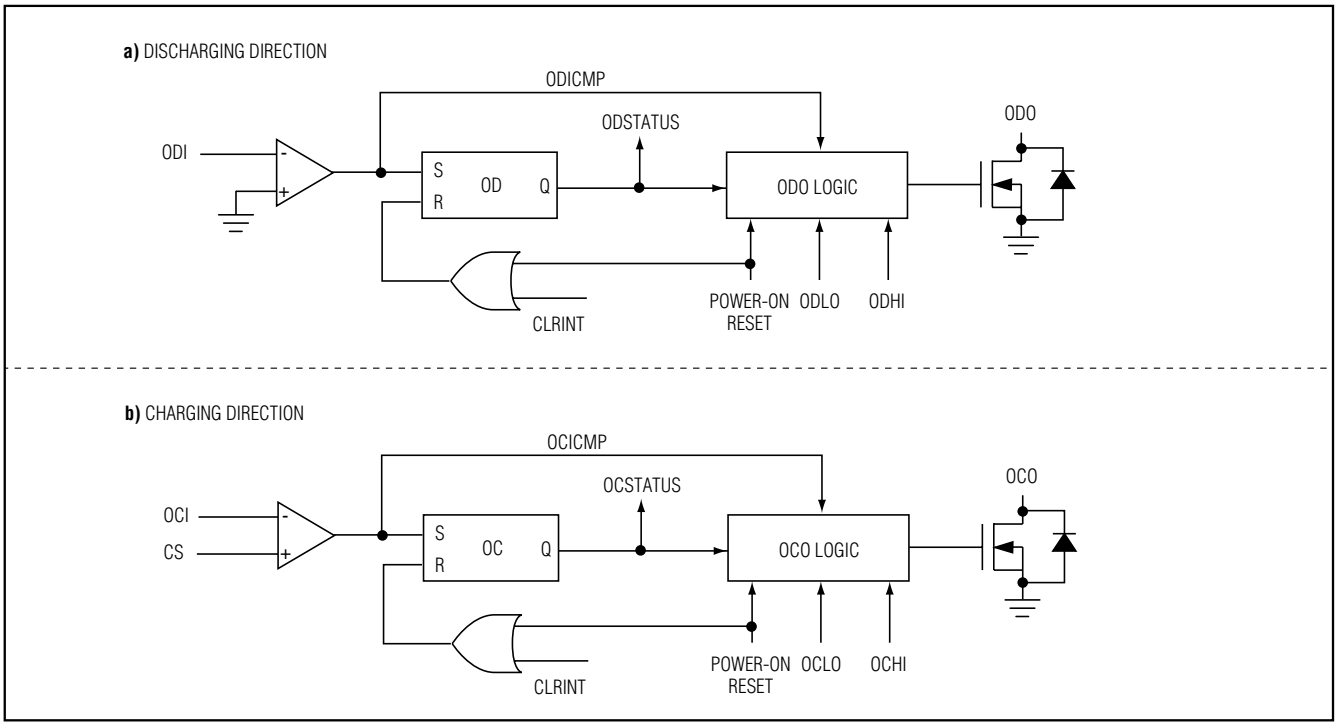


Figure 7. Overcurrent Comparator Section Functional Diagram

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Table 4a. OCO Logic Truth Table

OCHI BIT	OCLO BIT	OCSTATUS BIT	OCO OUTPUT	STATE
0	0	0	GND	Automatic overcurrent protection (default)
0	0	1	HI-Z	Overcurrent detected
0	1	X	GND	Force-charge path on
1	0	X	HI-Z	Force-charge path off
1	1	X	OCICMP	Free running

Table 4b. ODO Logic Truth Table

ODHI BIT	ODLO BIT	ODSTATUS BIT	ODO OUTPUT	STATE
0	0	0	GND	Automatic overcurrent protection (default)
0	0	1	HI-Z	Overcurrent detected
0	1	X	GND	Force-discharge path on
1	0	X	HI-Z	Force-discharge path off
1	1	X	ODICMP	Free running

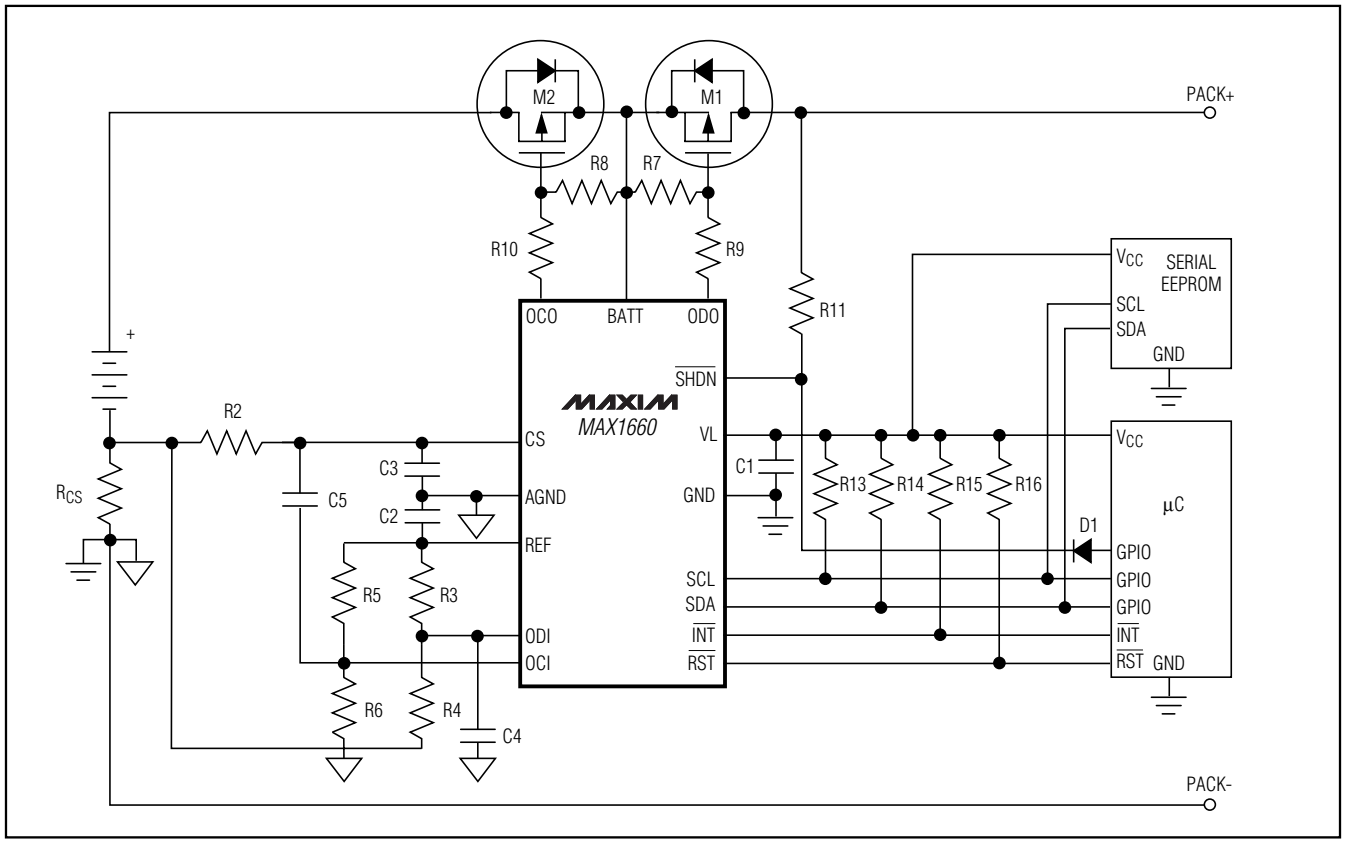

Figure 8. Typical Application Circuit

OCO and ODO Gate Drivers

OCO and ODO are open-drain n-channel MOSFET outputs that drive the external p-channel MOSFET gates. Connect pullup resistors in the 500kΩ to 1MΩ range from OCO and ODO to BATT to reduce current draw when OCO and ODO are driven low. For additional protection of OCO and ODO from voltage spikes coupled through the MOSFET gate capacitance, place 10kΩ resistors (R9 and R10) from OCO and ODO to the respective MOSFET gates (Figure 8). To protect the battery pack and load during power-up, OCO and ODO are forced into a high-Z state during the power-on-reset timeout period. Table 4 shows the truth tables defining the OCO and ODO output states with respect to the overcurrent comparators and the MAX1660's configuration bits.

$\overline{INT}$ Output

The MAX1660's $\overline{INT}$ output drives an optional third wire that interrupts the host whenever an alert condition occurs. The MAX1660's host-interrupt procedure is compatible with the SMBus SMBALERT# signal, but it is equally useful as a simple host-interrupt output.

By default, an interrupt is triggered ($\overline{INT}$ is pulled low) any time an overcurrent condition occurs (see the *Overcurrent Detection* section). The MAX1660 may also be configured to generate an interrupt whenever a digital compare equality occurs and/or when a change in the current-flow direction is detected (see the *Digital Compare Function* and *Direction-Change Detection Function* sections).

Once triggered, $\overline{INT}$ stays low until the interrupt is cleared. An interrupt is cleared when one of three conditions is true: a 1 is written into the configuration word's CLRINT bit, the MAX1660 acknowledges the SMBus Alert Response Address (ARA), or a power-on reset occurs. The MAX1660 acknowledges the ARA with the 0x8F byte.

$\overline{INT}$ is an open-drain output; connect a 100kΩ pullup resistor between $\overline{INT}$ and VL.

Alert Response Address (0001100)

The Alert Response address provides quick fault identification for single slave devices that lack the complex, expensive logic needed to be a BusMaster.

When a slave device generates an interrupt, the host (BusMaster) interrogates the bus slave devices via a special receive-byte operation that includes the Alert Response address. The data returned by this read-byte operation is the address of the interrupting slave device. The MAX1660 when interrupted, will respond with 0x8F.

$\overline{RST}$ Output

$\overline{RST}$ is an open-drain, active-low power-on reset output provided for the MAX1660's host controller and other external circuitry. $\overline{RST}$ drives low on power-up whenever the MAX1660 enters hard-shutdown mode, or whenever the VL regulator output is below V_{TH1} (typically 1.7V). In hard-shutdown mode, $\overline{RST}$ goes low and remains low as long as the VL regulator provides sufficient gate drive to the $\overline{RST}$ output switch (typically until VL falls to 1V), after which $\overline{RST}$ drifts slightly upward. On power-up or when exiting hard-shutdown mode, $\overline{RST}$ drives low until 25ms (typ) after VL exceeds V_{TH2} (typically 2.9V). Although $\overline{RST}$ offers a reliable power-on reset function, it does not detect brownout conditions (V_{TH1} < VL < V_{TH2}). For applications that require brownout detection, refer to Maxim's complete line of precision microprocessor supervisory products. Connect a 100kΩ pullup resistor between $\overline{RST}$ and VL. Leave $\overline{RST}$ unconnected if the power-on reset function is not used.

Internal Regulator and Reference

The 3.3V VL internal linear regulator powers the MAX1660 control circuitry, logic, and reference, and can supply up to 5mA to power external loads, such as a microcontroller or other circuitry. Bypass VL to GND with a 0.33µF capacitor.

The 2.00V precision reference (REF) is accurate to ±2%, making it useful as a system reference. REF can supply up to 200µA to external circuitry. Bypass REF to GND with a 10nF capacitor.

Shutdown Modes

Hard Shutdown

Driving $\overline{SHDN}$ low puts the MAX1660 into hard-shutdown mode and forces the power-on reset state. In hard-shutdown mode, the VL regulator and the reference turn off, reducing supply current to 1µA (max). To protect the battery pack and load during the power-on-reset timeout period, the OCO and ODO outputs are forced into their high-Z states. $\overline{SHDN}$ is a logic-level input, but can be safely driven by voltages up to V_{BATT}.

Soft Shutdown

Drive the MAX1660 into soft-shutdown mode by setting the configuration word's SHDNSTATUS bit. All interrupts clear in soft-shutdown mode. In this mode, only the VL regulator and the SMBus interface remain active, reducing the supply current to just 15µA.

To prevent current from flowing undetected while the MAX1660 remains in soft-shutdown mode, ensure that the command to enter soft-shutdown mode contains a

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low byte of 0xA (ODHI = OCHI = 1, ODLO = OCLO = 0) to force the FETs off and disconnect the load. The MAX1660 does not perform a power-on reset when exiting soft-shutdown mode.

SMBus Interface

The MAX1660's 2-wire serial interface is compatible with Intel's SMBus interface. An interrupt output ($\overline{INT}$) allows the MAX1660 to immediately interrupt its host in the event of an overcurrent condition. This interrupt complies with the SMBALERT# signal of the SMBus specification. Although each of the MAX1660's pins are designed to protect against ±2kV ESD strikes, SDA and SCL pins have extended ESD-protection structures designed to provide protection for ±4kV ESD.

The MAX1660 operates as an SMBus slave only, never as a master. It does not initiate communication on the bus; it only receives commands and responds to queries for status information. Although the MAX1660 offers the host an array of configuration commands, providing complete control over many of its functions, it performs its functions automatically. The host needs to communicate with the MAX1660 only to retrieve data and change configurations as necessary.

Each communication with the MAX1660 begins with a start condition, defined as a falling edge on SDA with SCL high. The device address follows the start condition. The MAX1660 device address is fixed at 0b1000111 (where 0b indicates a binary number), which may also be denoted as 0x8E (where 0x indicates a hexadecimal number) for Read-Word commands, or 0x8F for Write-Word commands. Figure 9 shows examples of SMBus Write-Word and Read-Word protocols.

ReadStatus() Command

The host determines the MAX1660's status by executing the ReadStatus() command. This command returns the MAX1660's status, including the state of its interrupts, as well as the present direction of current flow. Table 5 describes each of the status word's bits.

Status information is retrieved from the MAX1660 using the Read-Word protocol; however, the device's flexible implementation of the SMBus standard also allows the Receive-Byte protocol to be substituted when status is being read. When the MAX1660 receives a command, its command code is latched, remaining valid until it is overwritten by a new command code. When status information is repeatedly being read, polling time can be significantly decreased by using the Receive-Byte protocol to read the status word's LSB after the initial ReadStatus() command.

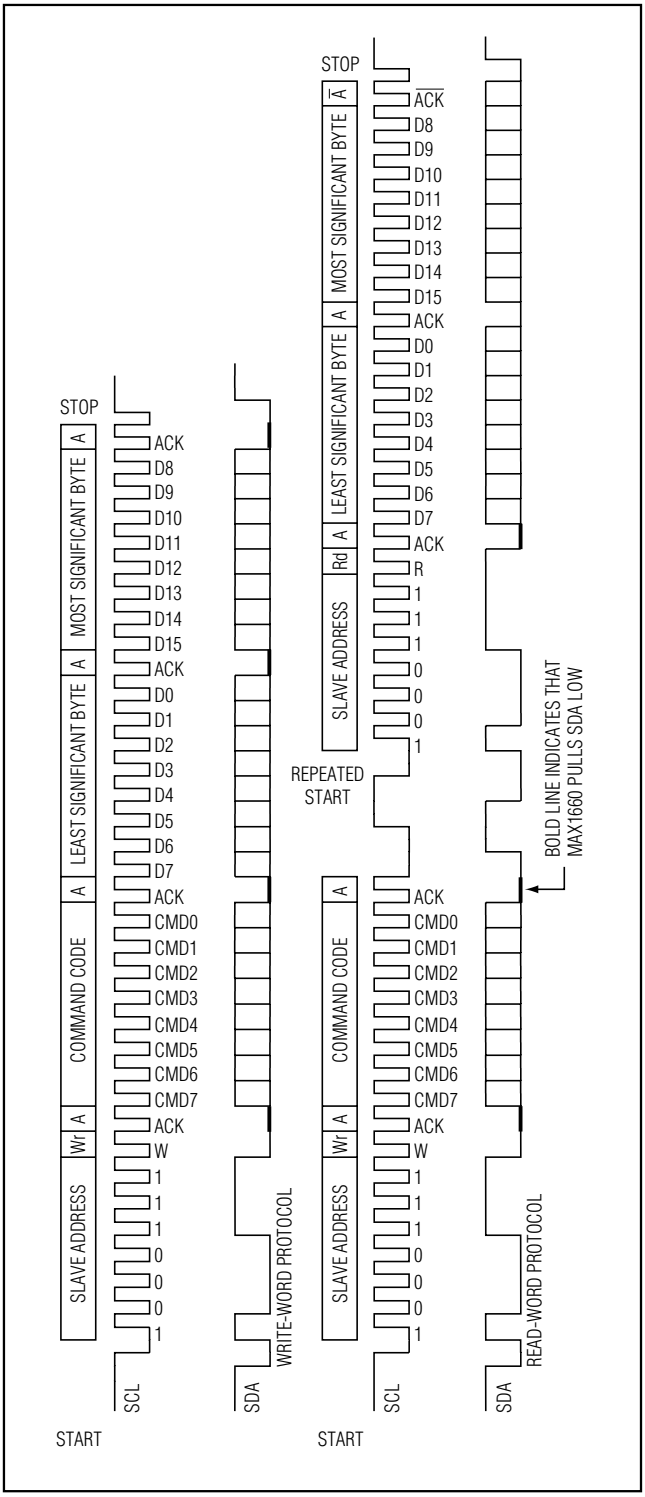

Figure 9. Write-Word and Read-Word Examples

Table 5. ReadStatus() Bit Functions

BIT NAME	BIT POSITION	POWER-ON RESET STATE	DESCRIPTION
—	15	1	Unused. Always returns 1.
—	14	1	Unused. Always returns 1.
—	13	1	Unused. Always returns 1.
—	12	1	Unused. Always returns 1.
—	11	1	Unused. Always returns 1.
—	10	1	Unused. Always returns 1.
—	9	1	Unused. Always returns 1.
—	8	1	Unused. Always returns 1.
ODSTATUS	7	0	Overcurrent-Interrupt Status. This bit sets when an overcurrent condition occurs in the discharging direction. This bit clears in soft-shutdown, following a power-on reset, or when the configuration word's CLRINT bit is set.
OCSTATUS	6	0	Overcurrent-Interrupt Status. This bit sets when an overcurrent condition occurs in the charging direction. This bit clears in soft-shutdown, following a power-on reset, or when the configuration word's CLRINT bit is set.
COMPSTATUS	5	0	COMPINT-Interrupt Status. This bit sets upon generation of the COMPINT interrupt. This bit clears in soft shutdown, on a power-on reset, or when the configuration word's CLRINT bit is set.
COUNTSTATUS	4	—	SETCOUNT Status Indicator. This bit sets when the configuration word's SETCOUNT bit is set. This bit clears when SETCOUNT clears.
SHDNSTATUS	3	0	Soft-Shutdown Status Indicator. Returns 1 when the device is in soft-shutdown mode; returns zero when it is not in soft-shutdown mode.
CHARGESTATUS	2	0	Charge-Status Indicator. This bit sets upon detection of charging current. The bit clears upon detection of discharging current.
DIRCHANGE	1	0	The bit sets when the current flow changes direction. This bit clears when the configuration word's CLRINT or SOFTSHDN bit is set, or following a power-on reset. See *Direction-Change Detection Function* section.
—	0	—	Unused. Always returns 1.

WriteConfig() Command

The host configures the MAX1660 using the WriteConfig() command. Table 6 describes each of the configuration word's bits.

Applications Information

Choosing RCS

For greatest accuracy, choose R_{CS} to ensure that the product of the maximum current to be measured (I_{MAX}) and R_{CS} does not exceed 120mV. Calculate the proper sense-resistor value as follows:

$$R_{CS} = \frac{120mV}{I_{MAX}}$$

where I_{MAX} is the maximum current to be accurately measured. Use only surface-mount metal-film resistors; wire-wound resistors are too inductive to provide acceptable results. Be sure to consider power dissipation when choosing the current-sense resistor to avoid resistor self-heating.

Setting the Overcurrent Threshold

Set the current at which the voltage on CS exceeds the voltage on OCI with a voltage-divider placed between REF and GND (Figure 10a). To set the overcharge threshold, choose R5 in the 1MΩ range and calculate R6 from:

$$R6 = \frac{R5}{\left(\frac{V_{REF}}{I_{CHG,MAX}R_{CS}} - 1\right)}$$

where V_{REF} = 2.00V, $I_{CHG,MAX}$ is the maximum allowable charging current, and R_{CS} is the current-sense resistor value.

Table 6. WriteConfig() Bit Functions

BIT NAME	BIT POSITION	POWER-ON RESET STATE	DESCRIPTION
—	15	—	Unused
—	14	—	Unused
—	13	—	Unused
—	12	—	Unused
—	11	—	Unused
DIRINTENABLE	10	0	Direction-Change Interrupt Enable. Set this bit to enable direction-change interrupt generation. Clear this bit to disable this function. See the *Direction-Change Detection Function* section.
SOFTSHDN	9	0	Soft-Shutdown Enable. Set this bit to enable soft shutdown. Clear this bit to resume normal operation. See the *Shutdown Modes* section.
CLRCOUNTER	8	—	Clear Counter. Write 1 to clear both CHGCOUNT and DISCOUNT.
CLRINT	7	—	Clear Interrupts. Write 1 to clear ODSTATUS, OCSTATUS, COMPSTATUS, and DIRCHANGE.
SETCOUNT	6	0	Counter Selection. Selects which counter is multiplexed to COUNT. Set this bit to select the charge counter. Clear this bit to select the discharge counter. See the *Charge and Discharge Counters* section.
OFFSETMEAS	5	0	Offset-Measurement Enable. Set this bit to disconnect CS from the external circuitry and internally short it to AGND. Clear this bit to reconnect CS to the external circuitry and resume normal operation. See the *Internal Offset Measurement* section.
COMPENABLE	4	0	the Compare-Interrupt Enable. Set this bit to enable the digital compare function. Clear this bit to disable this function. See the *Digital Compare Function* section.
ODHI	3	0	First of 2 bits controlling the ODO output state. See the *Overcurrent Detection* section.
ODLO	2	0	Second of 2 bits controlling the ODO output state. To ensure proper overcurrent protection, ODLO should always remain cleared. See the *Overcurrent Detection* section.
OCHI	1	0	First of 2 bits controlling OCO output state. See the *Overcurrent Detection* section.
OCLO	0	0	Second of 2 bits controlling OCO output state. To ensure proper overcurrent protection, OCLO should always remain cleared. See the *Overcurrent Detection* section.

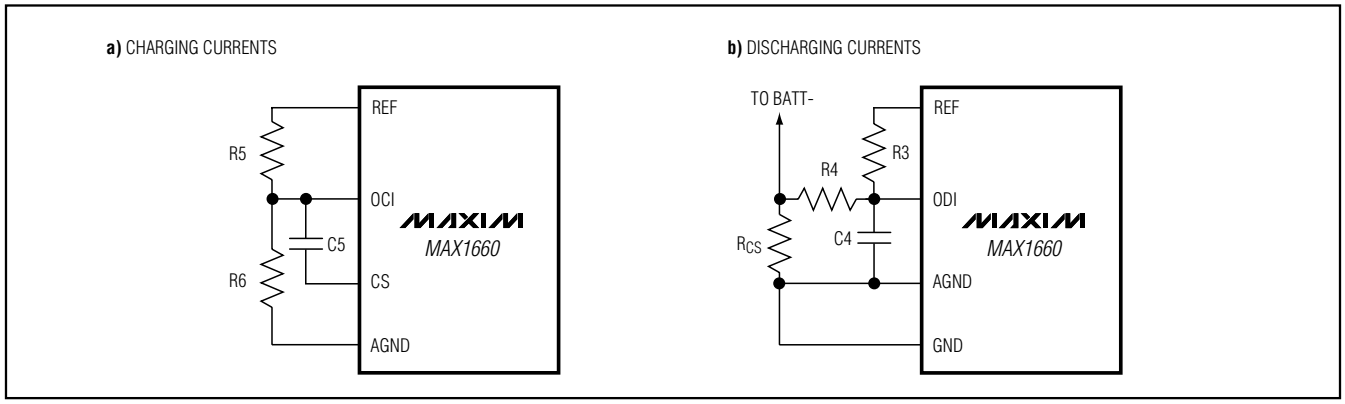

Figure 10. Overcurrent-Detection Networks

Set the current at which the ODI voltage falls below AGND with a voltage divider placed between REF and CS (Figure 10b). To set the overdischarge threshold, choose R3 in the 1MΩ range, then calculate R4 from:

$$R4 = R3 \frac{I_{DISCHG,MAX} R_{CS}}{V_{REF}}$$

where V_{REF} = 2.00V, $I_{DISCHG,MAX}$ is the maximum allowable discharging current, and R_{CS} is the current-sense resistor value.

Lowpass filter the ODI and OCI inputs with C4 and C5 (Figure 10) to prevent short current pulses from tripping the overcurrent thresholds. Use the smallest capacitances that provide the desired filtering; large capacitances slow the MAX1660's response to overcurrent conditions.

Internal Offset Measurement

Although the MAX1660 has extremely low input offset error, some low-current, high-precision applications may require accounting for this offset. Set the configuration word's OFFSETMEAS bit to disconnect the Coulomb-counter input from the external circuitry and internally short it to AGND. Subtract the resulting offset current from succeeding measurements to correct for the internal offset.

Clear OFFSETMEAS to resume normal operation. Note that since the Coulomb-counting circuitry is disconnected from the current-sense resistor during this measurement, currents that flow through the sense resistor when OFFSETMEAS is set do not increment the counters. Ensure that the command to measure the internal offset contains a low byte of 0xA (ODHI = OCHI = 1, ODLO = OCLO = 0) to force the FETs off and disconnect the load. Although the MAX1660 cannot perform its Coulomb-counting function while in offset-measurement mode, the overcurrent comparators are still active.

Improving Measurement Accuracy

Filtering the Input

Place a 100Ω resistor (R2) between R_{CS} and the CS pin, and bypass CS to AGND with a 0.1µF capacitor (C3), as shown in Figure 11. To minimize leakage errors due to finite trace-to-trace resistance, place both filter components, as well as C5, as close to the CS pin as possible.

Minimizing SMBus Activity

Although proper layout minimizes coupling from the digital data lines to the high-resolution analog interface, the MAX1660's analog interface may still detect switching noise in low-current, high-precision applications. In such applications, it may be advantageous to use the MAX1660's digital compare function to limit activity on the digital data lines during the measurement. By removing the requirement that the host poll the MAX1660 to determine when a counter has reached the desired value, the MAX1660 requires no digital switching while it accumulates sensitive data. See *Digital Compare Function* section.

Exiting Hard-Shutdown Mode

In most applications, hard-shutdown mode is used only when the battery pack has become fully discharged, at which point the pack's load current must be minimized to prevent cell overdischarge. When the MAX1660's host is powered from VL, which turns off in hard-shutdown mode, the host is unable to signal the MAX1660 to exit hard-shutdown mode. Figure 8's circuit demonstrates a simple topology that handles this situation.

During normal operation, the external MOSFETs M1 and M2 conduct so that $V_{\overline{SHDN}}$ is pulled up to V_{BATT}. If M1 is forced off, however, the voltage at $\overline{SHDN}$ falls toward ground. To ensure that the signal at $\overline{SHDN}$ is a logic high, one of the host's GPIO lines is programmed high at all times and is connected to $\overline{SHDN}$ through diode D1. This diode protects the GPIO pin from voltages at PACK+ that exceed the VL voltage. To command the MAX1660 to enter hard-shutdown mode, the host simply turns MOSFET M1 off and drives the GPIO line low, allowing the MAX1660's $\overline{SHDN}$ to fall. Once in hard-shutdown mode, the MAX1660 cannot wake up until a valid supply voltage is applied to PACK+ (i.e., when the battery is connected to a charger), pulling $\overline{SHDN}$ high through R11.

Layout Considerations

Use care during board layout to obtain the MAX1660's full precision over a wide range of input currents. Proper board layout minimizes the noise coupled to the analog sections from both high-current traces and digital switching. Use a star ground configuration and route the SCL and SDA lines away from CS and AGND. Lowpass filter the Coulomb-counter input by placing a 100Ω resistor between R_{CS} and CS, and bypass CS to AGND with a 0.1µF ceramic capacitor. To reduce leakage errors due to finite trace-to-trace resistance, place both filter components as close to the IC as possible. Use a Kelvin connection to obtain accurate measurements when large currents are flowing (Figure 11). Bypass REF to AGND with a 10nF ceramic capacitor placed as close to the IC as possible. Bypass VL to GND with a 0.33µF capacitor, also placed as close to the IC as possible. Refer to the MAX1660 evaluation kit layout for an example of proper board layout.

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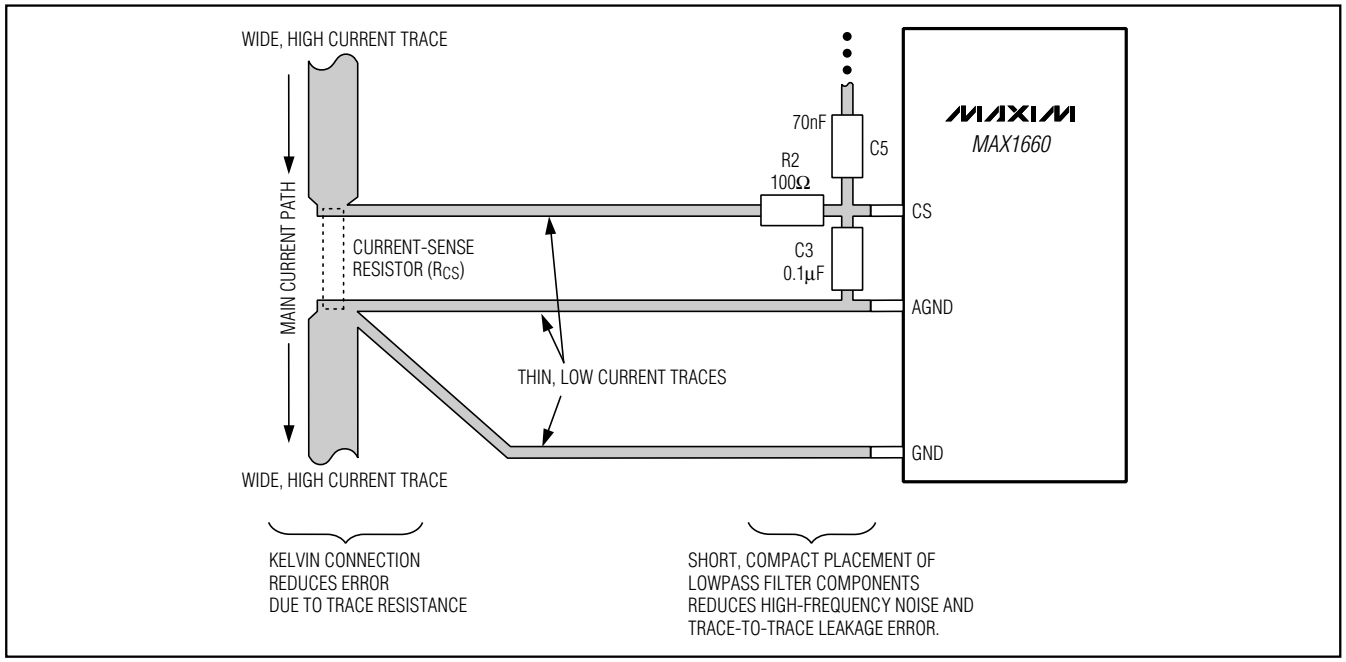
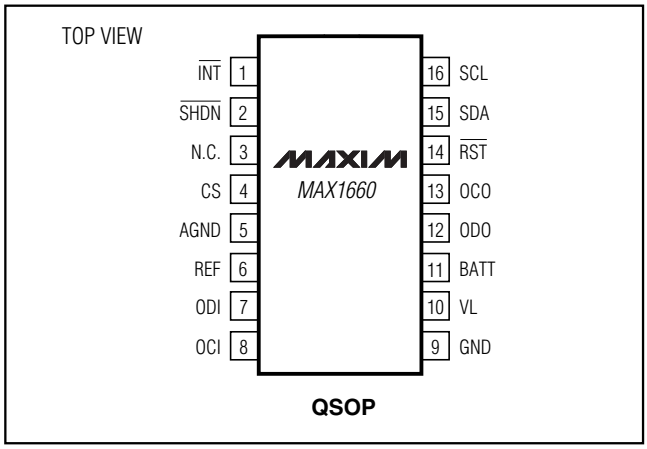


Figure 11. Proper Layout for Current-Sense Input

Pin Configuration



Chip Information

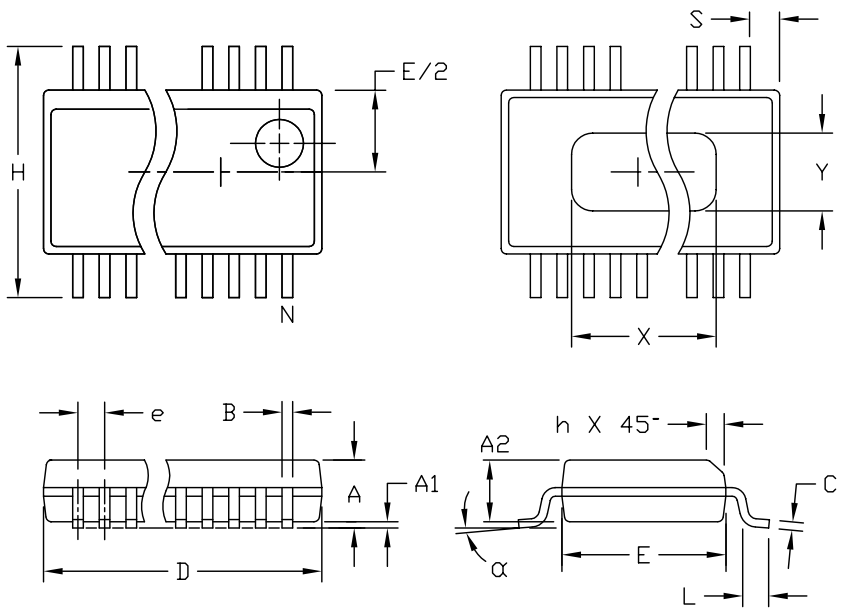
TRANSISTOR COUNT: 9078

SUBSTRATE CONNECTED TO GND

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QSOP EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	C	1/1

Revision History

Pages changed at Rev 2: 1, 2, 12, 19

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