MAX17105

8-String WLED Driver with Integrated Step-Up Regulator and SMBus/PWM Dimming Capability

General Description

The MAX17105 is a high-efficiency driver for white-light-emitting diodes (WLEDs). It is designed for large liquid-crystal displays (LCDs) that employ an array of LEDs as the light source. An internal switch-current mode step-up controller drives the LED array, which can be configured for up to 8 strings in parallel and 10 LEDs per string. Each string is terminated with ballast that achieves ±2% current regulation accuracy, ensuring even LED brightness. The MAX17105 has a wide input voltage range from 6V to 28V, and provides adjustable 0 to 30mA full-scale LED current.

The MAX17105 can internally generate a digitally adjusted pulse-width modulation (DPWM) signal for accurate WLED dimming control. The DPWM frequency is resistor programmable, while DPWM duty cycle is controlled directly from an external PWM signal or through a control word through the MAX17105's SMBus interface. This DPWM control provides a dimming range with 8-bit resolution and supports Intel display power-saving technology (DPST) to maximize battery life. The MAX17105 also has direct PWM control mode, in which the PWMI directly controls the LED current turn on/off and the SMBus interface is disabled.

The MAX17105 has multiple features to protect the controller from fault conditions. Separate feedback loops limit the output voltage under any circumstance, ensuring safe operation. Once an open string is detected, the string is disabled while other strings operate normally. The MAX17105 also features short LED detection. The shorted strings are also disabled. The controller features cycle-by-cycle current limit to provide constant operation and soft-start capability. If the MAX17105 is in current-limit condition, the step-up regulator is latched off after an internal timer expires. A thermal-shutdown circuit provides another level of protection. When the input overcurrent-limit fault, thermal shutdown, or output-voltage short condition happens, the input p-channel MOSFET is turned off and the step-up regulator output is isolated from the input supply.

The MAX17105 is available in a thermally enhanced, 24-pin, 4mm x 4mm, thin QFN package with exposed pad.

Applications

- Notebook, Subnotebook, and Tablet Computer Displays
- Handy Terminals

Features

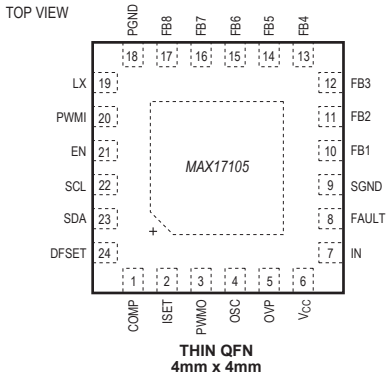
- 6V to 28V Input Supply Voltage
- Up to Eight Parallel-String Multiple Series Connected LEDs
- 500kHz-to-2MHz Adjustable Switching Frequency
- 0.15Ω Internal HV Power MOSFET (45V max)
- Low-String Feedback Voltage: 500mV at 20mA LED current
- Full-Scale LED Current Adjustable from 0mA to 30mA
- ±2% Current Regulation Accuracy Between Strings
- 100:1 Dimming Ratio at 25kHz Direct PWM Frequency
- 100Hz to 30kHz PWMI Input Range for DPWM Mode and 10kHz ±5% for SMBus Mode
- 100Hz to 5kHz Adjustable DPWM Frequency
- Full-Range Dimming with 8-Bit Resolution
- Open and Short LED Protection
- Output Overvoltage Protection
- Thermal Shutdown
- FAULT Output to Drive p-Channel MOSFET
- Small 24-Pin, 4mm x 4mm, Thin QFN Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17105ETG+	-40°C to +85°C	24 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration



Simplified Operating Circuit appears at end of data sheet.

maxim integrated™

Absolute Maximum Ratings

FAULT, IN to SGND .....-0.3V to +30V
FB_, LX to PGND.....-0.3V to +45V
PGND to SGND.....-0.3V to +0.3V
V_{CC}, EN, PWMI, SDA, SCL to SGND .....-0.3V to +6V
COMP, ISET, OSC, OVP,
PWMO, DFSET to SGND.....-0.3V to (V_{CC} + 0.3V)
LX Switch Maximum Continuous RMS Current 1.6A

Continuous Power Dissipation (T_A = +70°C)
Thin QFN (derate 20.8mW/°C above +70°C).....1667mW
(single-layer board)
Thin QFN (derate 27.8mW/°C above +70°C).....2222mW
(multilayer board)
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(Circuit of Figure 1. V_{IN} = 12V, C_{COMP} = 33nF, R_{COMP} = 1kΩ, R_{ISET} = 50kΩ, R_{OSC} = 100kΩ, R_{DFSET} = 250kΩ, PWMI = SGND, C_{PWMO} = 1µF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY						
IN Input Voltage Range (Note 1)	V_{CC} = open, EN = high		5.5		28	V
	EN = SGND, SMBus mode (Note 5)	All functions available	6.3		28	
		SMBus interface only	3.9	4.0		
IN Input Voltage UVLO Threshold (SMBus Mode Only) (Note 4)	Rising edge, hysteresis = 150mV		5.9	6.05	6.2	V
	Falling edge, hysteresis = 150mV		5.75	5.9	6.05	
IN Quiescent Current	MAX17105 is enabled at minimum brightness, in SMBus mode and no-load, V_{IN} = 28V			2.0	3.0	mA
	MAX17105 is enabled in SMBus mode and is under IN UVLO, V_{IN} = 5.5V			0.7	1.1	mA
	MAX17105 is disabled			30	60	µA
V_{CC} Output Voltage	MAX17105 is enabled, 6V < V_{IN} < 28V, 0 < I_{VCC} < 10mA		4.7	5.0	5.3	V
	MAX17105 is disabled, V_{IN} = 12V		3.7	4.6	4.95	
V_{CC} Current Limit	V_{CC} is forced to 4.5V		15	40	70	mA
V_{CC} UVLO Threshold	Rising edge, typical hysteresis = 85mV		4.00	4.3	4.45	V
STEP-UP REGULATOR						
LX On-Resistance	100mA from LX to PGND			0.15	0.3	Ω
LX Leakage Current	40V on LX, T_A = +25°C				1	µA
Operating Frequency	R_{OSC} = 50kΩ		1.7	2.0	2.3	MHz
	R_{OSC} = 100kΩ		0.9	1.0	1.1	
	R_{OSC} = 200kΩ		0.4	0.5	0.6	
Minimum On-Time	(Note 1)			50		ns
Maximum Duty Cycle	At f_{SW} = 1MHz		93	95	97	%
Minimum Off-Time				50		ns

Electrical Characteristics (continued)

(Circuit of Figure 1. V_{IN} = 12V, C_{COMP} = 33nF, R_{COMP} = 1kΩ, R_{ISET} = 50kΩ, R_{OSC} = 100kΩ, R_{DFSET} = 250kΩ, PWMI = SGND, C_{PWMO} = 1µF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LX Current Limit	Duty cycle = 75% (Note 1)	2.4	2.9	3.4	A
CONTROL INPUT					
Logic-Input High Level	SDA, SCL, PWMI, EN	2.1			V
Logic-Input Low Level	SDA, SCL, PWMI, EN			0.8	V
INPUT LEAKAGE					
PWMI Leakage Current	T_A = +25°C	-0.1		+0.1	µA
Logic Input Bias Current	T_A = +25°C, EN, SDA, SCL	-1		+1	µA
OVP Leakage Current	T_A = +25°C	-0.1		+0.1	µA
SDA Output-Low Sink Current	V_{SDA} = 0.4V	4			mA
LED CURRENT					
Full-Scale FB_ Output Current-Adjustable Range (Note 4)	PWM-only dimming mode	15		30	mA
	SMBus-enabled dimming modes	15		25	
Full-Scale FB_ Output Current	R_{ISET} = 33.3kΩ	29.1	30.0	30.9	mA
	R_{ISET} = 50.0kΩ	19.4	20.0	20.6	
	R_{ISET} = 66.6kΩ	14.45	15.0	15.55	
	V_{ISET} < 0.4V	0.2	0.3	0.4	
ISET Output Voltage		1.1	1.2	1.3	V
Current Regulation Between Strings	$I_{FB\_}$ = 30mA	-2.0		+2.0	%
	$I_{FB\_}$ = 20mA	-2.0		+2.0	
	$I_{FB\_}$ = 15mA	-2.0		+2.0	
Minimum FB_ Regulation Voltage	$I_{FB\_}$ = 30mA			770	mV
	$I_{FB\_}$ = 20mA		480		
	$I_{FB\_}$ = 15mA		450		
FB_ On-Resistance	$V_{FB\_}$ = 50mV		15	26	Ω
FB_ Leakage Current	$V_{FB\_}$ = 40V, T_A = +25°C		0.1	5	µA
FB_ On-Time		400			ns
FAULT PROTECTION					
OVP Threshold Voltage	Rising edge, hysteresis = 60mV	1.15	1.25	1.35	V
OVP Shutdown Voltage	Rising edge		1.35		V
OVP Global Fail		48		120	mV
FB_ UVLO Threshold	FB open	140	220	300	mV
FB_ Overvoltage Threshold		7.4	8	8.6	V
FB_ Check LED Source Current		0.4			mA
FB_ Check LED Time			1		ms

Electrical Characteristics (continued)

(Circuit of Figure 1. V_{IN} = 12V, C_{COMP} = 33nF, R_{COMP} = 1kΩ, R_{ISET} = 50kΩ, R_{OSC} = 100kΩ, R_{DFSET} = 250kΩ, PWMI = SGND, C_{PWMO} = 1µF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FB_ Overvoltage Fault Timer		88	128	168	µs
Thermal-Shutdown Threshold	(Note 1)		+150		°C
Overcurrent FAULT Shutdown Timer	I_{PEAK} > 2.9A at duty = 75%	72	128	168	µs
FAULT High-Level Leakage Current	V_{FAULT} = V_{IN} = 28V, T_A = +25°C			1	µA
FAULT Low-Level Clamp Voltage		V_{IN} – 5.5	V_{IN} - 5	V_{IN} – 4.5	V
FAULT Charge Current		45		65	µA
PWM FILTER					
PWM Output Impedance		20	40	60	kΩ
DPWM Oscillator Frequency	R_{DFSET} = 500kΩ		100		Hz
	R_{DFSET} = 250kΩ	190	200	210	
	R_{DFSET} = 25kΩ		2		kHz
	R_{DFSET} = 10kΩ	4.4	5.0	5.5	
DFSET Short-Detection Threshold Voltage			210	300	mV
DFSET Source Current	R_{DFSET} = 500kΩ		4.15		µA
	R_{DFSET} = 250kΩ		7.85		
	R_{DFSET} = 25kΩ		40		
	R_{DFSET} = 10kΩ		55		
PWMI Input Frequency Range	DPST/SMBus mode	9.5	10.0	10.5	kHz
	Direct-PWM mode	0.1		30.0	
PWMI Brightness Setting	SMBus mode, PWMI duty cycle = 98%	97.5	98	98.5	%
	SMBus mode, PWMI duty cycle = 50%	48	50	52	
	SMBus mode, PWMI duty cycle = 0%	0.2	0.4	0.6	
SMBus TIMING SPECIFICATION					
SMBus Frequency	f_{SMB}	10		100	kHz
Bus Free Time	t_{BUF}	4.7			µs
START Condition Hold Time from SCL	$t_{HD:STA}$	4			µs
START Condition Setup Time from SCL	$t_{SU:STA}$	4.7			µs
STOP Condition Setup Time from SCL	$t_{SU:STO}$	4			µs
SDA Hold Time from SCL	$t_{HD:DAT}$	300			ns
SDA Setup Time from SCL	$t_{SU:DAT}$	250			ns
SCL Low Period	t_{LOW}	4.7			µs
SCL High Period	t_{HIGH}	4			µs

Electrical Characteristics

(Circuit of Figure 1. V_{IN} = 12V, C_{COMP} = 33nF, R_{COMP} = 1kΩ, R_{ISET} = 50kΩ, R_{OSC} = 100kΩ, R_{DFSET} = 250kΩ, PWMI = SGND, C_{PWMO} = 1µF, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY						
IN Input Voltage Range (Note 1)	V_{CC} = open, EN = high (Note 5)		5.5		28	V
	EN = SGND, SMBus mode	All functions available	6.3		28	
		SMBus interface only	3.9	4.0		
IN Input Voltage UVLO Threshold (SMBus Mode Only) (Note 2)	Rising edge, hysteresis = 150mV		5.9		6.2	V
	Falling edge, hysteresis = 150mV		5.75		6.05	
IN Quiescent Current	MAX17105 is enabled at minimum brightness, in SMBus mode and no load, V_{IN} = 28V				3.0	mA
	MAX17105 is enabled in SMBus mode, and is under IN UVLO, V_{IN} = 5.5V				1.1	
	MAX17105 is disabled				60	µA
V_{CC} Output Voltage	MAX17105 is enabled, 6V < V_{IN} < 28V, 0 < I_{VCC} < 10mA		4.7		5.3	V
	MAX17105 is disabled, V_{IN} = 12V		3.7		4.95	
V_{CC} Current Limit	V_{CC} is forced to 4.5V		15		70	mA
V_{CC} UVLO Threshold	Rising edge, typical hysteresis = 85mV		4.00		4.45	V
STEP-UP REGULATOR						
LX On-Resistance	100mA from LX to PGND				0.3	Ω
Operating Frequency	R_{OSC} = 50kΩ		1.7		2.3	MHz
	R_{OSC} = 100kΩ		0.9		1.1	
	R_{OSC} = 200kΩ		0.45		0.6	
Maximum Duty Cycle	At f_{SW} = 1MHz		93		98	%
LX Current Limit	Duty cycle = 75%		2.4		3.4	A
CONTROL INPUT						
Logic-Input High Level	SDA, SCL, PWMI, EN		2.1			V
Logic-Input Low Level	SDA, SCL, PWMI, EN				0.8	V
SDA Output-Low Sink Current	V_{SDA} = 0.4V		4			mA
SDA, SCL Input Bias Current	T_A = +25NC		-1		+1	µA
LED CURRENT						
Full-Scale FB_ Output Current Adjustable Range (Note 3)	PWM only dimming mode		15		30	mA
	SMBus-enabled dimming modes		15		25	
Full-Scale FB_ Output Current	R_{ISET} = 33.3kΩ		28.8		31.2	mA
	R_{ISET} = 50.0kΩ		18.9		21	
	R_{ISET} = 66.6kΩ		14.25		15.75	
	V_{ISET} < 0.4V		0.2		0.4	
Current Regulation Between Strings	$I_{FB\_}$ = 30mA		-2.5		+2.5	%
	$I_{FB\_}$ = 20mA		-2.5		+2.5	
	$I_{FB\_}$ = 15mA		-2.5		+2.5	
Minimum FB_ Regulation Voltage	$I_{FB\_}$ = 30mA				770	mV
FB_ On-Resistance	$V_{FB\_}$ = 50mV				26	Ω
FB_ On-Time			400			ns

Electrical Characteristics (continued)

(Circuit of Figure 1. V_{IN} = 12V, C_{COMP} = 33nF, R_{COMP} = 1kΩ, R_{ISET} = 50kΩ, R_{OSC} = 100kΩ, R_{DFSET} = 250kΩ, PWMI = SGND, C_{PWMO} = 1µF, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FAULT PROTECTION					
OVP Threshold Voltage	Rising edge, hysteresis = 60mV	1.15		1.35	V
OVP Shutdown Voltage	Rising edge (tracks with OVP threshold voltage)	1.25		1.45	V
OVP Global Fail		48		120	mV
FB_ UVLO Threshold	FB open	140		300	mV
FB_ Overvoltage Threshold		7.4		8.6	V
FB_ Check LED Source Current		0.4			mA
FB_ Overvoltage Fault Timer		88		168	µs
Overcurrent FAULT Shutdown Timer	I_{PEAK} > 2.9A at duty = 75% (typical)	72		168	µs
FAULT High-Level Leakage Current	V_{FAULT} = V_{IN} = 28V			1	µA
FAULT Low-Level Clamp Voltage		V_{IN} – 5.5		V_{IN} – 4.5	V
FAULT Charge Current		45		65	µA
PWM FILTER					
PWM Output Impedance		20		60	kI
DPWM Oscillator Frequency	R_{DFSET} = 250kΩ	190		210	Hz
	R_{DFSET} = 10kΩ	4.4		5.5	kHz
DFSET Short-Detection Threshold Voltage				300	mV
PWMI Input Frequency Range	DPST/SMBus mode	9.5		10.5	kHz
	Direct-PWM mode	0.1		30.0	
PWMI Brightness Setting	SMBus mode, PWMI duty cycle = 98%	97.5		98.5	%
	SMBus mode, PWMI duty cycle = 50%	48		52	
	SMBus mode, PWMI duty cycle = 0%	0.2		0.6	
SMBus TIMING SPECIFICATION					
SMBus Frequency	f_{SMB}	10		100	kHz
Bus Free Time	t_{BUF}	4.7			µs
START Condition Hold Time from SCL	$t_{HD:STA}$	4			µs
START Condition Setup Time from SCL	$t_{SU:STA}$	4.7			µs
STOP Condition Setup Time from SCL	$t_{SU:STO}$	4			µs
SDA Hold Time from SCL	$t_{HD:DAT}$	300			ns
SDA Setup Time from SCL	$t_{SU:DAT}$	250			ns
SCL Low Period	t_{LOW}	4.7			µs
SCL High Period	t_{HIGH}	4			µs

Electrical Characteristics (continued)

Circuit of Figure 1. V_{IN} = 12V, C_{COMP} = 33nF, R_{COMP} = 1kΩ, R_{ISET} = 50kΩ, ROSC = 100kΩ, R_{DFSET} = 250kΩ, PWMI = SGND, C_{PWMO} = 1µF, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

Note 1: Specifications are guaranteed by design, not production tested.

Note 2: Specifications to T_A = -40°C are guaranteed by design, not production tested.

Note 3: LED full-scale current maximum value is subjected to string number, LED number per string, and LX current limit. In SMBus modes, if the total load is heavier than 8 strings with 10 WLEDs per string at 25mA LED current, upon step-up regulator input V_S removal, an OC fault may occur, resulting in SMBus status register OV_CURR and FAULT bits being set to 1 and violating SMBus specifications.

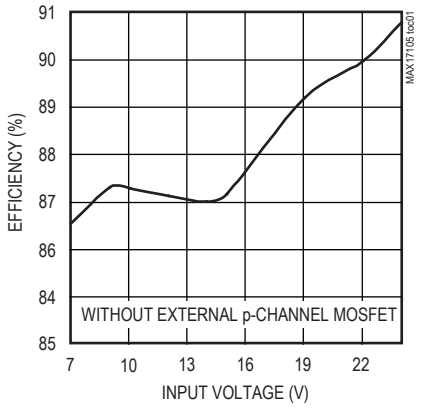
Note 4: Minimum voltage drop from V_S to IN pin, including the forward voltage drop of diode DIN1 used in Figure 1, should be no less than 0.8V. If lower forward voltage drop diode is used, upon step-up regulator input VS removal, an OC fault may occur, resulting in SMBus status register OV_CURR and FAULT bits being set to 1 and violating SMBus specifications.

Note 5: Dimming modes **not** to be done after the driver starts up or on-the-fly.

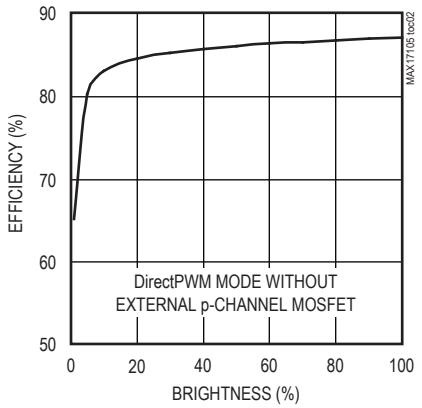
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

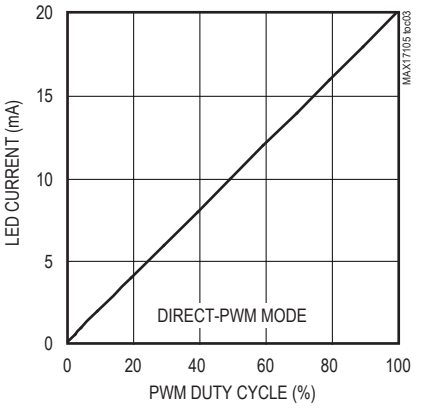
BOOST CONVERTER EFFICIENCY vs. INPUT VOLTAGE (V_S) (V_{OUT} = 32V/I_{OUT} = 160mA, BRIGHTNESS = 100%



BOOST CONVERTER EFFICIENCY vs. BRIGHTNESS (V_S = 12V, V_{OUT} = 32V/I_{OUT} = 160mA AT 100%



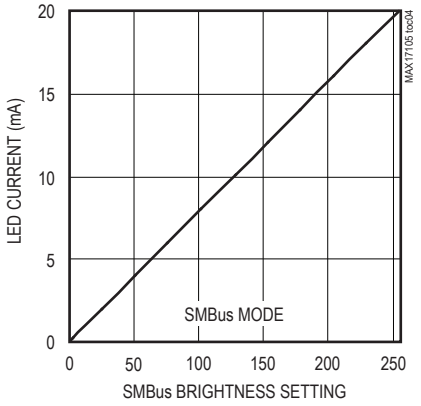
LED CURRENT vs. BRIGHTNESS SETTING



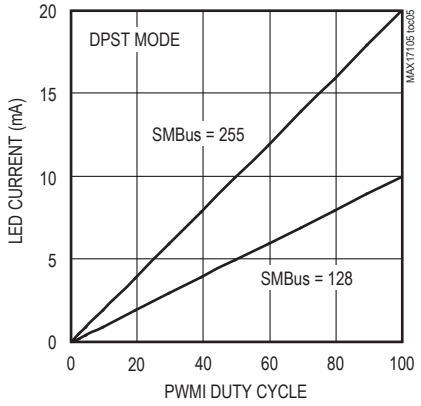
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

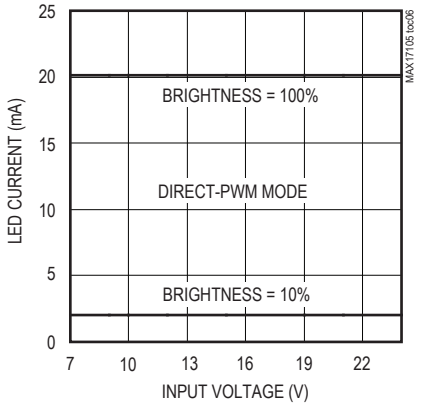
LED CURRENT vs. SMBus BRIGHTNESS SETTING



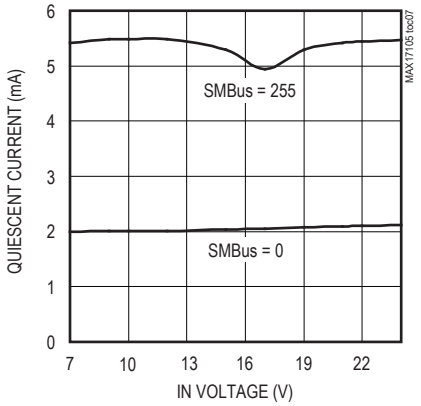
LED CURRENT vs. PWMI DUTY CYCLE



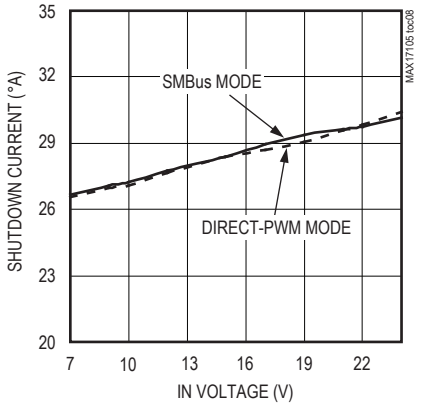
LED CURRENT vs. INPUT VOLTAGE



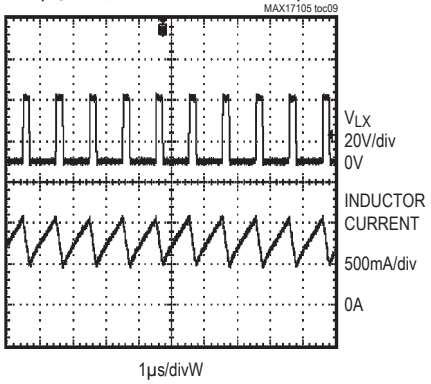
IN QUIESCENT CURRENT vs. IN VOLTAGE



IN SHUTDOWN CURRENT vs. IN VOLTAGE



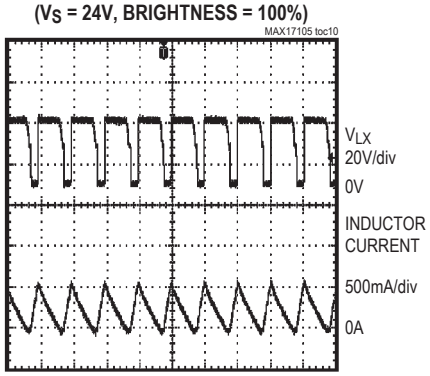
SWITCHING WAVEFORMS (V_S = 7V, BRIGHTNESS = 100%)



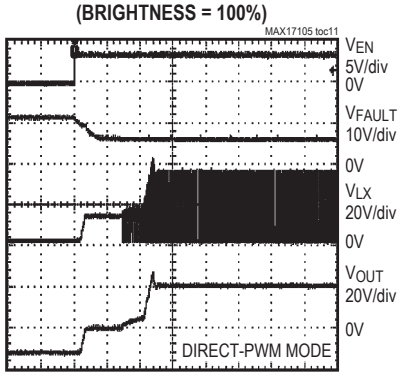
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

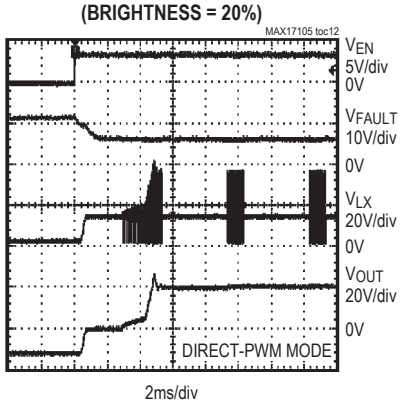
SWITCHING WAVEFORMS (V_S = 24V, BRIGHTNESS = 100%)



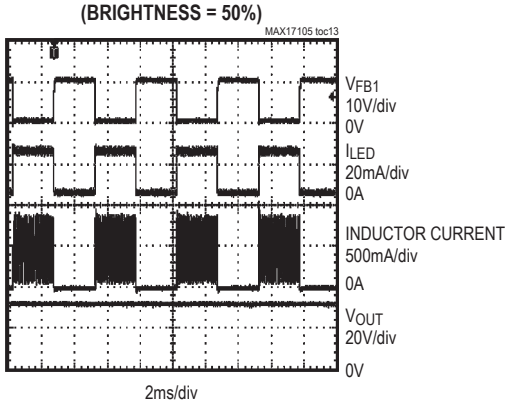
STARTUP WAVEFORMS (BRIGHTNESS = 100%)



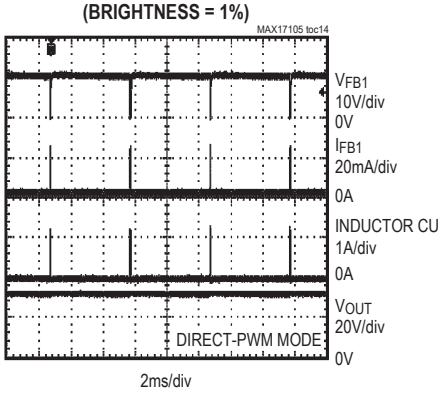
STARTUP WAVEFORMS (BRIGHTNESS = 20%)



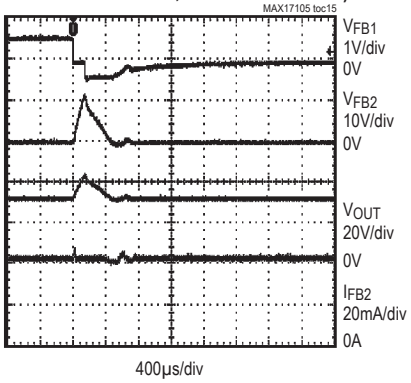
LED CURRENT WAVEFORMS (BRIGHTNESS = 50%)



LED CURRENT WAVEFORMS (BRIGHTNESS = 1%)



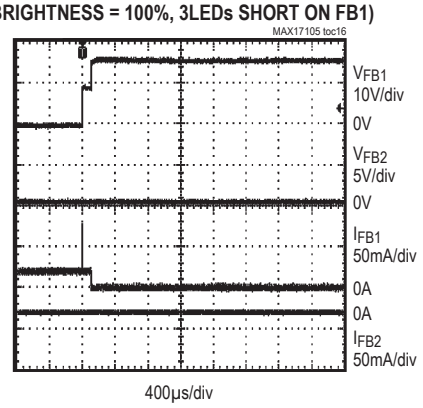
LED-OPEN FAULT PROTECTION (BRIGHTNESS = 100%, LED OPEN ON FB1)



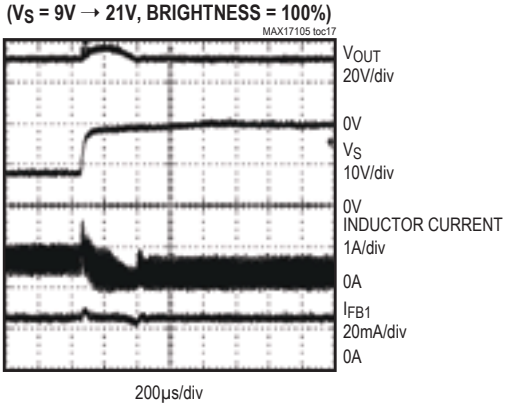
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

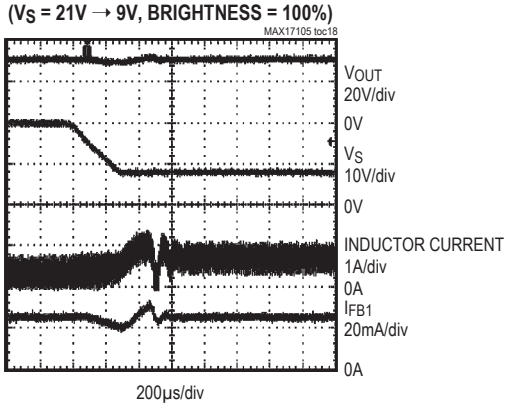
LED-SHORT FAULT PROTECTION (BRIGHTNESS = 100%, 3LEDs SHORT ON FB1)



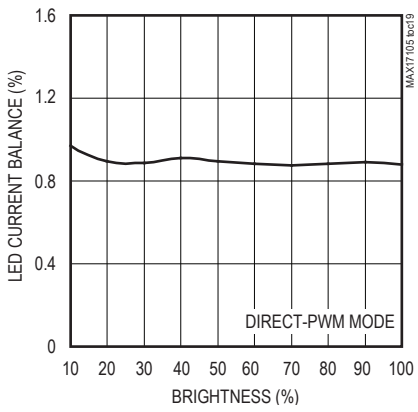
LINE-TRANSIENT RESPONSE (V_S = 9V → 21V, BRIGHTNESS = 100%)



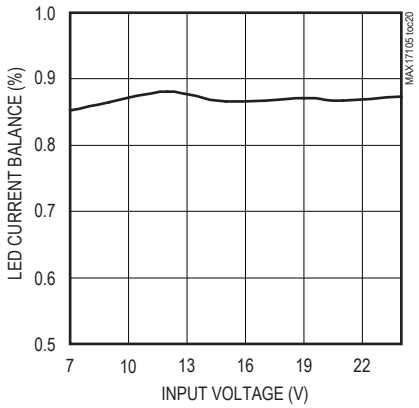
LINE-TRANSIENT RESPONSE (V_S = 21V → 9V, BRIGHTNESS = 100%)



LED CURRENT BALANCE vs. BRIGHTNESS



LED CURRENT BALANCE vs. INPUT VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	COMP	Step-Up Regulator Compensation Pin. Connect a 0.033µF ceramic capacitor and 1kΩ resistor from COMP to SGND and an additional 220pF capacitor from COMP to SGND. When the MAX17105 shuts down, COMP is discharged to 0V through an internal 20kΩ resistor.
2	ISET	Full-Scale LED Current Adjustment Pin. The resistance from ISET to SGND controls the full-scale current in each LED string: $I_{LED\_MAX} = 20mA \times 50k\Omega / R_{ISET}$ The acceptable resistance range is 33.3kΩ < R_{ISET} < open, which corresponds to full-scale LED current of 30mA > I_{LED_MAX} > 0mA. Connecting ISET to SGND sets the test mode for 0.3mA (typ) full-scale LED current.
3	PWMO	Filtered PWM Signal Output. Connect a capacitor between PWMO and SGND. The capacitor forms a lowpass filter with an internal 40kΩ (typ) resistor to filter the PWM signal into an analog signal whose level represents the duty cycle information of the input PWM signal.
4	OSC	Oscillator Frequency Adjustment Pin. The resistance from OSC to SGND sets the step-up regulator's oscillator frequency: $f_{SW} = 1MHz \times 100k\Omega / R_{OSC}$ The acceptable resistance range is 50kΩ < R_{OSC} < 200kΩ, which corresponds to the switching frequency of 2MHz > f_{SW} > 500kHz.
5	OVP	Overvoltage Sense. Connect OVP to the center tap of a resistive voltage-divider from the output of the step-up regulator to ground.
6	VCC	5V Linear-Regulator Output. VCC provides power to the MAX17105. Bypass VCC to SGND with a ceramic capacitor of 1µF or greater.
7	IN	Power-Supply Input. VIN biases the internal 5V linear regulator that powers the device. Bypass IN to SGND directly at the pin with a 0.1µF ceramic capacitor or greater.
8	FAULT	External p-Channel MOSFET Gate Drive-Output. External pullup resistor is connected between FAULT and IN when p-channel MOSFET is used. If the p-channel MOSFET is not used, leave FAULT unconnected.
9	SGND	Analog Ground
10	FB1	LED String 1 Cathode Connection. FB1 is the open-drain output of an internal regulator, which controls current through FB1. FB1 can sink up to 30mA. If unused, connect FB1 to SGND.
11	FB2	LED String 2 Cathode Connection. FB2 is the open-drain output of an internal regulator, which controls current through FB2. FB2 can sink up to 30mA. If unused, connect FB2 to SGND.
12	FB3	LED String 3 Cathode Connection. FB3 is the open-drain output of an internal regulator, which controls current through FB3. FB3 can sink up to 30mA. If unused, connect FB3 to SGND.
13	FB4	LED String 4 Cathode Connection. FB4 is the open-drain output of an internal regulator, which controls current through FB4. FB4 can sink up to 30mA. If unused, connect FB4 to SGND.
14	FB5	LED String 5 Cathode Connection. FB5 is the open-drain output of an internal regulator, which controls current through FB5. FB5 can sink up to 30mA. If unused, connect FB5 to SGND.
15	FB6	LED String 6 Cathode Connection. FB6 is the open-drain output of an internal regulator, which controls current through FB6. FB6 can sink up to 30mA. If unused, connect FB6 to SGND.
16	FB7	LED String 7 Cathode Connection. FB7 is the open-drain output of an internal regulator, which controls current through FB7. FB7 can sink up to 30mA. If unused, connect FB7 to SGND.
17	FB8	LED String 8 Cathode Connection. FB8 is the open-drain output of an internal regulator, which controls current through FB8. FB8 can sink up to 30mA. If unused, connect FB8 to SGND.

Pin Description (continued)

PIN	NAME	FUNCTION
18	PGND	Step-Up Regulator Power Ground
19	LX	Step-Up Regulator Switching Node. Drain of the internal n-channel MOSFET between LX and PGND. Connect the inductor and catch diode here and minimize trace area for lowest EMI.
20	PWMI	PWM Signal Input. This PWM signal is used for brightness control in direct-PWM mode or DPST mode of SMBus mode. In direct-PWM mode, the DPWM duty cycle is equal to the input PWM duty cycle. In DPST mode, the DPWM duty cycle is the input PWM duty cycle multiplied by the SMBus brightness command. PWMI directly controls the LED current source on or off in direct-PWM mode.
21	EN	Direct-PWM Mode Enable Pin. When direct-PWM mode is selected through the DFSET pin, the MAX17105 can start up with direct-PWM mode by EN = high.
22	SCL	SMBus Serial Clock Input
23	SDA	SMBus Serial Data Input
24	DFSET	DPWM Frequency Adjustment Pin. Connect a resistor from DFSET to SGND to set the internal DPWM frequency in SMBus mode. In direct-PWM mode, DFSET pin is connected to SGND: $f_{DPWM} = 200Hz \times 250k\Omega / R_{DFSET}$ The acceptable resistance range is $10k\Omega < R_{DFSET} < 500k\Omega$, which corresponds to the DPWM frequency of $5kHz > f_{DPWM} > 100Hz$.
—	EP	Exposed Backside Pad. Solder to the circuit board ground plane with sufficient copper connection to ensure low thermal resistance. See the *PCB Layout Guidelines* section.

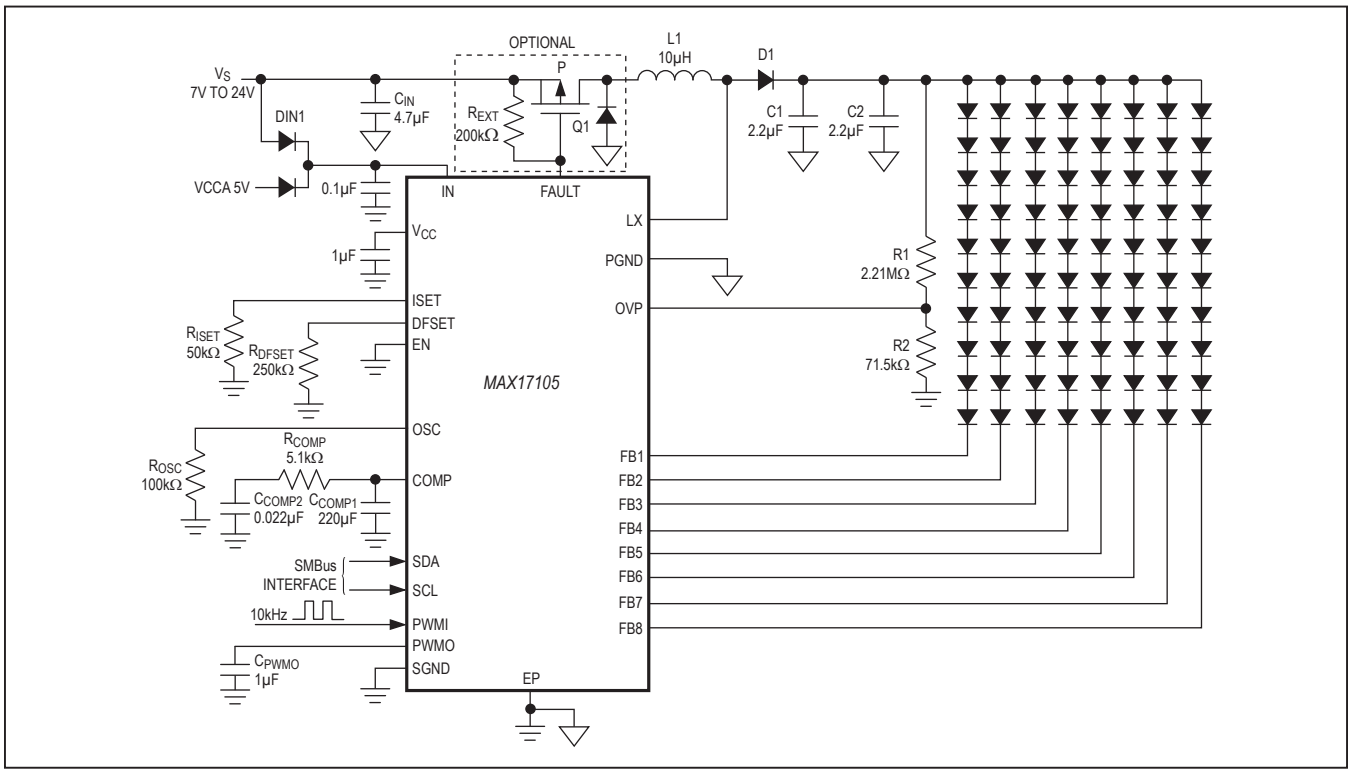


Figure 1. Typical Operating Circuit

Table 1. Component List

DESIGNATION	DESCRIPTION
White LED	Nichia NSSW008C 3.2V (typ), 3.5V (max) at 20mA
L1	10µH, 1.5A, H = 1.2mm TDK VLP6812T-100M1R5
Q1 (Optional)	30V, 65mΩ p-channel MOSFET Si3481DV FDC658AP
C_{IN}	4.7µF ±10%, 25V X5R ceramic capacitor (1206) Murata GRM319R61E475KA12D
C1, C2	2.2µF ±20%, 50V X7R ceramic capacitors (1206) Murata GRM31CR71H225K
D1	2A, 40V Schottky diode (M-flat) Toshiba CMS11

Table 2. Component Suppliers

SUPPLIER	PHONE	WEBSITE
Fairchild Semiconductor	888-522-5372	www.fairchildsemi.com
Murata	770-436-1300	www.murata-northamerica.com
Nichia Corp.	248-352-6575	www.nichia.com
TDK Corp.	847-803-6100	www.component.tdk.com
Toshiba America Electronic Components, Inc.	949-623-2900	www.toshiba.com/taec
Vishay	402-563-6866	www.vishay.com

Detailed Description

The MAX17105 typical operating circuit is shown in Figure 1. Table 1 lists some recommended components, and Table 2 lists the contact information of component suppliers.

The MAX17105 is a high-efficiency driver for arrays of white LEDs. It contains a fixed-frequency, current-mode PWM step-up controller, a 5V linear regulator, dimming control circuit, SMBus interface, internal power MOSFET, eight regulated current sources, and an external p-channel MOSFET drive circuit. Figure 2 shows the MAX17105 functional diagram. When enabled, the step-up controller boosts the output voltage to provide sufficient headroom for the current sources to regulate their respective string currents. The MAX17105 features a resistor-adjustable switching frequency (500kHz to 2MHz), which allows trade-offs between external component size and operating efficiency.

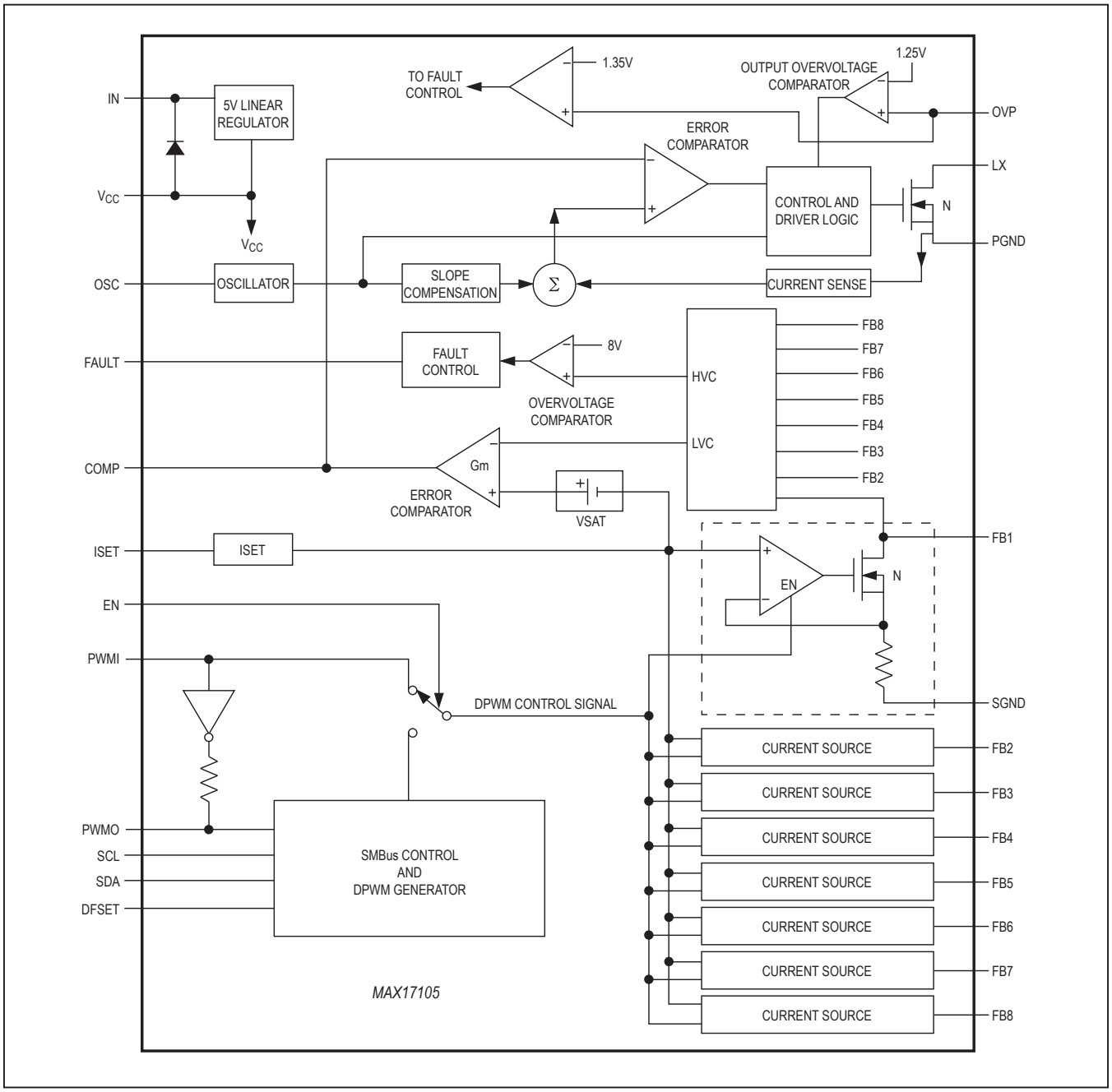


Figure 2. Functional Diagram

WLED brightness is controlled by turning the WLEDs on and off with a DPWM signal. The DPWM frequency can be accurately adjusted with a resistor or directly controlled by the PWMI signal. The brightness of the LEDs is proportional to the duty cycle of the DPWM signal, which is controlled externally through either a PWM or 2-wire SMBus-compatible interface, or both. When both interfaces are used at the same time, the product of the PWM duty cycle and SMBus command value is used for the dimming control. This DPWM control provides a dimming range with 8-bit resolution.

The MAX17105 has multiple features to protect the controller from fault conditions. Separate feedback loops limit the output voltage in all circumstances. The MAX17105 checks each FB_ voltage during the operation. If one or more strings are open, the corresponding FB_ voltages are pulled below 220mV (typ), and an open-circuit fault is detected. As a result, the respective current sources are disabled. When one or more LEDs are shorted and the FB_ voltage exceeds 8V, a short fault is detected and the respective current source is disabled. In either LED open or short conditions, the fault strings are disabled while other strings can still operate normally. The controller features cycle-by-cycle current limit to provide consistent operation and soft-start protection. In a current-limit condition, the controller shuts down after a 128µs overcurrent fault timer expires. A thermal-shutdown circuit provides yet another level of protection.

The MAX17105 includes a 5V linear regulator that provides the internal bias and gate driver for the step-up controller.

Fixed-Frequency Step-Up Controller

The MAX17105's fixed-frequency, current mode, step-up controller automatically chooses the lowest active FB_ voltage to regulate the feedback voltage. Specifically, the difference between the lowest FB_ voltage and the current source control signal plus an offset (VSAT) is integrated at the COMP output. The resulting error signal is compared to the external switch current plus slope compensation to determine the switch on-time. As the load changes, the error amplifier sources or sinks current to the COMP output to deliver the required peak inductor current. The slope-compensation signal is added to the current-sense signal in order to improve stability at high duty cycles.

Internal 5V Linear Regulator and UVLO

The MAX17105 includes an internal low-dropout (LDO) linear regulator (V_{CC}). When V_{IN} is higher than 5.5V, this linear regulator generates a 5V supply to power the internal PWM controller, control logic, and MOSFET driver. The V_{CC} voltage drops to 4.5V in standby. If V_{IN} is less than or equal to 5.5V, V_{CC} and IN can be connected together and powered from an external 5V supply. There is a body diode from V_{CC} to IN, so V_{IN} must be greater than V_{CC}. (See Figure 2.)

The MAX17105 includes power-on reset (POR) and undervoltage lockout (UVLO) features. POR resets the fault latch and sets all the SMBus resisters to their POR values. POR occurs when V_{CC} rises above 2.8V (typ). The controller is disabled until V_{CC} exceeds the UVLO threshold of 4.3V (typ). The hysteresis on V_{CC} UVLO is approximately 85mV.

In standby mode, the internal LDO is low-power mode with 60µA (max) input current and regulated at 4.5V (typ). When EN is high in direct-PWM mode or an ENABLE command through the SMBus interface, the internal LDO is enabled and regulated at 5.0V (typ). In addition to V_{CC} UVLO, the MAX17105 has also implemented an IN UVLO function. This IN UVLO function is not activated in direct-PWM mode. However, when the controller is enabled with SMBus, the IN UVLO feature is enabled. If the IN voltage is below its UVLO threshold, the step-up converter is shut off.

The V_{CC} pin should be bypassed to SGND with a minimum 1µF ceramic capacitor.

Startup

The MAX17105 has two operating modes: direct-PWM mode and SMBus mode. The two modes are identified by the DFSET pin. At the first enable signal, either EN = high or an SMBus ENABLE command, the DFSET pin sources a current to check whether the DFSET pin is connected to SGND. When the DFSET voltage is lower than 210mV (typ), the MAX17105 is set for direct-PWM mode. Otherwise, the MAX17105 is set for SMBus mode. Once the mode is set, the mode is not cleared until the VCC is lower than the POR voltage. When the MAX17105 is set for SMBus mode, the EN pin signal is ignored and the MAX17105 is woken by the SMBus ENABLE command. When the MAX17105 is set for direct-PWM mode, the SMBus command is ignored and the MAX17105is woken by the EN signal. Table 3 summarizes the operating mode.

Table 3. Operating Mode

	EN	DFSET	SCL, SDA
Direct PWM (Standby)	Low	SGND	X
Direct PWM (Startup)	High	SGND	X
SMBus (Standby)	X	R_{DFSET}	CLOCK
SMBus (Startup)	X	R_{DFSET}	ENABLE Command

X = Don't Care

At startup, there are three phases. The first phase is p-channel MOSFET soft-start time, the second is check LED time (1ms), and the last phase is boost soft-start time (4ms). In the first phase, FAULT sink current is increased from 0µA to 50µA to avoid high inrush current caused by the p-channel MOSFET turn-on. In check LED time, the MAX17105 performs a diagnostic test of the LED array. In the test phase, all FB_ are pulled up by 0.8mA (typ, 0.4mA min) current source during 1ms (typ). If some FB_ voltage is lower than 1.2V (max), the string is considered to be unused. Therefore, when a string is not in use, it should be connected to SGND. All other strings with FB_ higher than 1.2V (max) are detected as in use. After the LED string diagnostic phases are finished, the step-up regulator starts. The total startup time is less than 10ms. Figure 3 shows the sequence.

Standby and FAULT Shutdown

The MAX17105 can be placed into standby by EN = low in direct-PWM mode or clearing bit 0 of the device control register (0x01) in SMBus mode. When a critical failure is detected, the IC enters fault shutdown mode. In standby or fault shutdown mode, all functions of the IC are turned off, including the 5V linear regulator. Only a crude linear regulator remains on providing a 4.5V (typ) output voltage to V_{CC}, with 1µA current sourcing capability. The Fault/Status register is not reset in fault shutdown. When bit 0 of the device control register (0x01) is set to 1 in SMBus mode or cycling the EN pin, the MAX17105 exits fault shutdown mode and starts. The Fault/Status register is reset at startup.

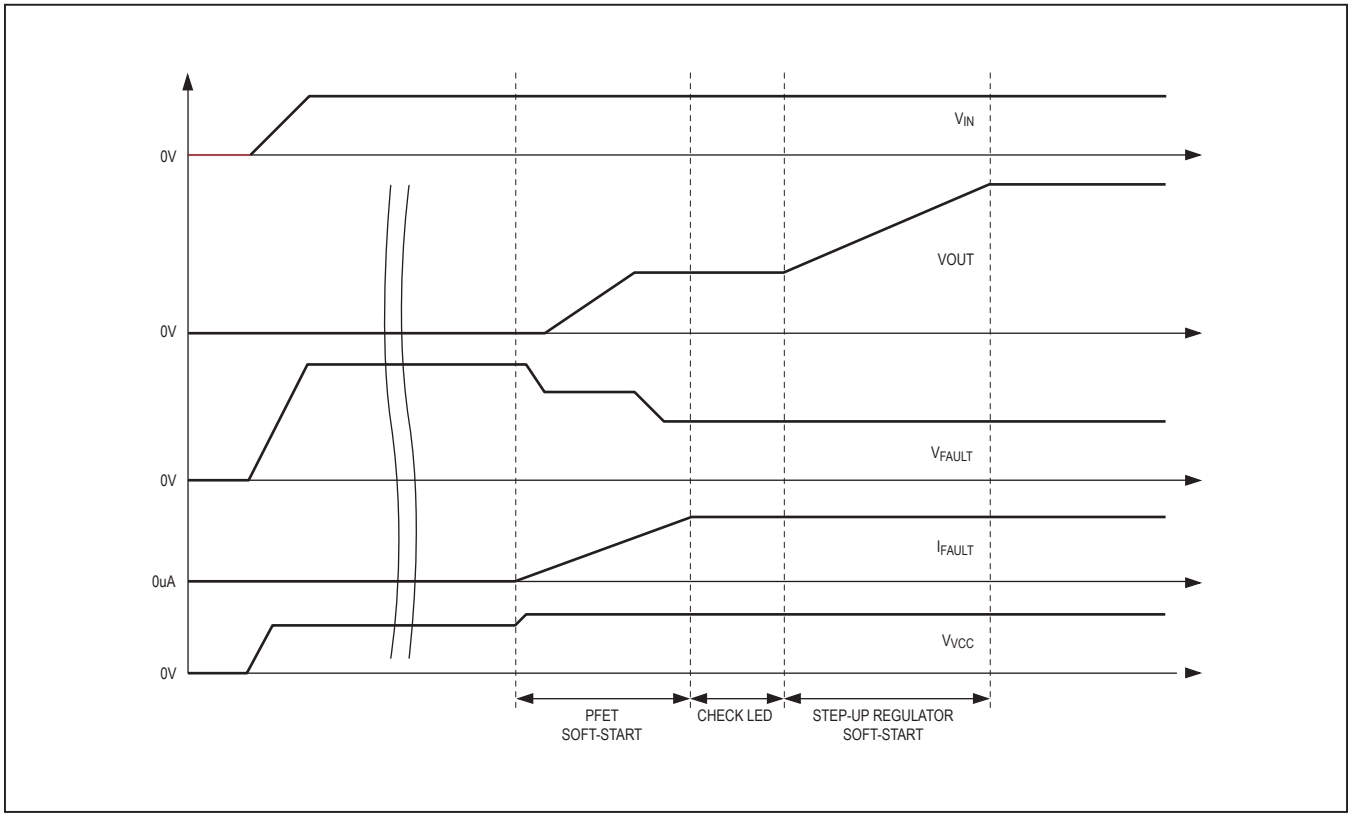


Figure 3. Startup Timing Sequence

In standby or fault shutdown, the FAULT pin is pulled up to IN with an internal resistor of 1MΩ (typ), and the p-channel MOSFET is turned off. An external resistor could be used as well (R_{EXT} > 200kΩ).

Frequency Selection

The step-up regulator switching frequency can be adjusted through the external resistor-connected OSC pin. The switching frequency adjustable range is 500kHz to 2MHz. High-frequency (2MHz) operation optimizes the regulator for the smallest component size, at the expense of efficiency due to increased switching losses. Low-frequency (500kHz) operation offers the best overall efficiency, but requires larger components and PCB area. The maximum step-up regulator duty is limited by the 50ns (typ) minimum on-time.

Overvoltage Protection

To protect the step-up regulator when the load is open, or the output voltage becomes excessive for any reason, the MAX17105 features a dedicated overvoltage feedback input (OVP). The OVP pin is connected to the center tap of a resistive voltage-divider from the high-voltage output. The OVP pin has two levels of threshold. When the OVP pin voltage, V_{OVP}, exceeds 1.25V (typ), a comparator turns off the internal power MOSFET and prevents excessive voltage from damage. This step-up regulator switch is reenabled after the V_{OVP} drops 60mV (typ) hysteresis below the protection threshold. This overvoltage-protection feature ensures the step-up regulator fail-safe operation when the LED strings are disconnected from the output. When the OVP pin voltage exceeds 1.35V (typ), the IC is in fault shutdown.

LED Current Sources

Maintaining uniform LED brightness and dimming capability are critical for backlight applications. The MAX17105 is equipped with a bank of eight matched current sources. These specialized current sources are accurate to within ±2%, and can be switched on- and off-PWM frequencies of up to 30kHz in direct-PWM mode and 5kHz in SMBus mode. All LED full-scale currents are identical and are set through the ISET pin (0mA < I_{LED} < 30mA). The LED current source has high-speed capability and allows 400ns minimum on-time within 400ns rise and fall time.

The minimum voltage drop across each current source is 500mV (max) when the LED current is 20mA. The low voltage drop helps reduce dissipation while maintaining sufficient compliance to control the LED current within the required tolerances.

The LED current sources can be disabled by connecting the respective FB_ pin to SGND at startup. When the IC is enabled, the controller scans settings for all FB_ pins. If a FB_ pin is not connected to SGND, an internal circuit pulls this pin high, and the controller enables the corresponding current source to regulate the string current. If the FB_ pin is connected to SGND, the controller disables the corresponding current regulator. The current regulator cannot be disabled by connecting the respective FB_ pin to SGND after the IC is enabled.

All FB_ pins in use are combined to extract a lowest FB_ voltage (LVC) (see Figure 2). LVC is fed into the step-up regulator's error amplifier and is used to set the output voltage.

Current Source Fault Protection

LED fault open/short is detected after startup. When one or more strings fail after startup, the corresponding current source is disabled. The remaining LED strings are still operated normally. When a fault is detected, bit 4 or/and bit 5 of the Fault/Status resister are set in SMBus mode. (See the Fault Status Register description in the *Dimming Control Register Descriptions* section.)

LED Short and String Mismatch Protection

The MAX17105 can tolerate slight mismatch between LED strings. When severe mismatches or WLED shorts occur, the FB_ voltages are uneven because of mismatched voltage drops across strings. At each LED turn-on, the FB_ voltage is brought down to the regulation voltage quickly. When FB_ voltage is higher than 8V (typ) after the LED turns on, the LED short is detected. When the LED short condition is continued for 2ms, the strings are disabled. The remaining LED strings can still operate normally. If only one string is used, the output voltage decreases and regulates the needed current during the operation of LED short. The LED short protection is not triggered since FB_ voltage is never higher than the threshold. The LED short protection is disabled during the soft-start phase of the step-up regulator.

Open-Current Source Protection

The MAX17105 step-up regulator output voltage is regulated according to the minimum FB_ voltages on all of the strings in use. If one or more strings are open, the respective FB_ pins are pulled to ground. For any FB_ lower than 220mV, the corresponding current source is disabled. The remaining LED strings can still operate normally. If all strings in use are open, the MAX17105 shuts the step-up regulator down.

Dimming Control

The MAX17105 has two dimming modes that are selected by the DFSET pin as shown in Table 3. The LED on/off DPWM frequency is generated by the internal oscillator for SMBus mode, while LED is directly on/off by the PWMI pin in direct-PWM mode. The DPWM frequency is adjustable through an external setting resistor and has 3% accuracy over the 200Hz to 2kHz range. In SMBus mode, the duty cycle of this DPWM signal can be controlled externally through two interfaces: PWM and SMBus. The ISET pin sets the amplitude of the current sources for each LED string (Figure 2). The internal DPWM signal directly controls the duty cycle of these current sources. The resulting current is chopped and synchronized to the DPWM signal. When filtered by the slow response time of the human eye, the overall brightness is modulated in a consistent flicker-free manner.

Full-Scale LED and Low-Level LED Current

The full-scale LED current IISET is determined by the resistors connected from ISET to SGND:

$$I_{LED\_MAX} = \frac{20mA \times 50k\Omega}{R_{ISET}}$$

The acceptable resistance range is 33.3kΩ < R_{ISET} < open, which corresponds to full-scale LED current of 30mA > I_{LED_MAX} > 0mA. Connect ISET to SGND sets the test mode for 0.3mA (typ) full-scale LED current.

DPWM Frequency Setting

The MAX17105 uses an internal DPWM signal to perform dimming control while operating at SMBus mode. The DPWM frequency is specified by an external resistor connected from the DFSET pin to SGND:

$$f_{DPWM} = \frac{200Hz \times 250k\Omega}{R_{DFSET}}$$

The adjustable range for the DFSET resistor, R_{DFSET}, is from 10kΩ to 500kΩ, corresponding to the DPWM frequency of 5kHz > f_{DPWM} > 100Hz.

Dimming Control Interfaces for SMBus Mode

The MAX17105's dimming control circuit consists of two interfaces: PWM and SMBus. The block diagram of these two input interfaces is shown in Figure 4. The dimming can be performed in three modes: PWM, SMBus, or DPST. In PWM mode, the brightness is adjusted by the PWM signal applied to the PWMI pin. In SMBus mode, the brightness is adjusted by an I²C command from an uplink processor through a 2-wire SMBus. In DPST mode, the brightness is adjusted by the product of the PWM duty cycle and SMBus command value. This DPWM control provides a dimming range with 8-bit resolution down to 0% and supports Intel DPST to maximize battery life.

The SMBus interface can be used to adjust the dimming, as well as shut down the MAX17105. Before the MAX17105 receives a turn-on command from the SMBus, it automatically remains off. In this low-power state, most of the control circuits are turned off, and only part of the LDO is active to provide a loosely regulated output of approximately 4.5V on the V_{CC} pin to power the SMBus interface.

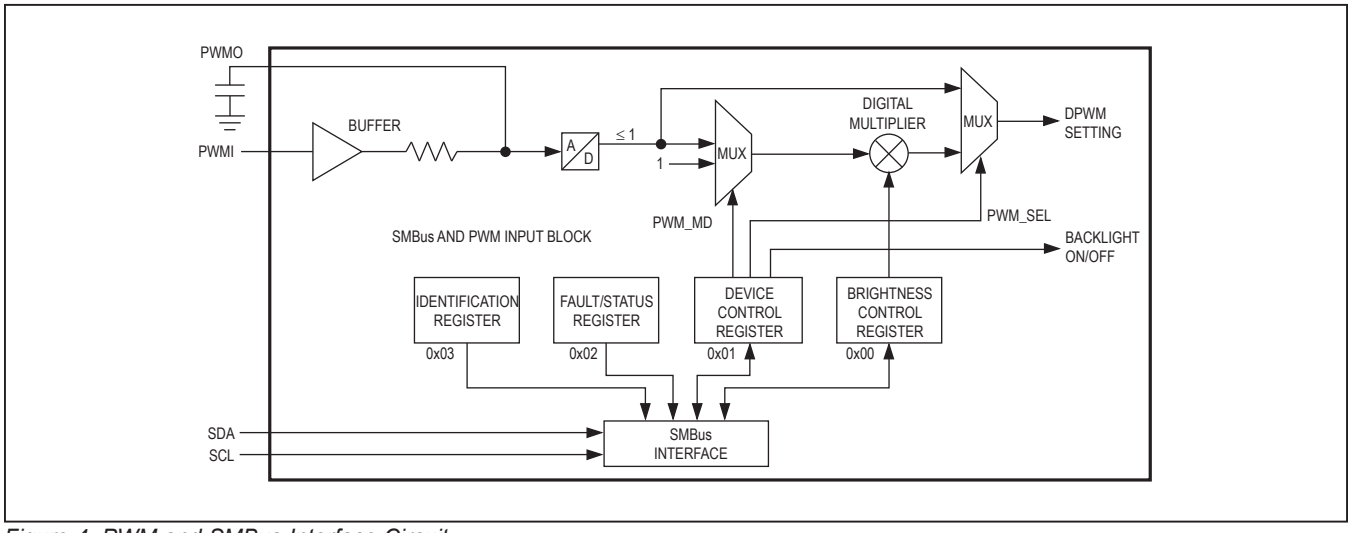


Figure 4. PWM and SMBus Interface Circuit

Dimming Control Register Descriptions

The MAX17105 includes four registers to monitor and control brightness, fault status, driver ID, and operating mode.

Brightness Control Register: Address is 0x00. This register is both readable and writeable for all 8 bits, and for BRT0, and BRT7, which are used to control the LED brightness level. In SMBus dimming mode, an SMBus write byte cycle to register 0x00 sets the output brightness level. The SMBus setting of 0xFF for this register sets the backlight controller to the maximum brightness output, and 0x00 sets 0.4% backlight brightness. The default value for register 0x00 is 0xFF. A write byte cycle to register 0x00 has no effect when the backlight controller is in PWM mode. The SMBus read byte cycle to register 0x00 returns the current brightness level regardless of the dimming mode.

REGISTER 0x00		BRIGHTNESS CONTROL REGISTER			DEFAULT VALUE 0xFF		
BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

Bit Field Definitions:

BIT FIELD	DEFINITION	DESCRIPTION
Bit [7:0]	BRT [7:0]	8-bit brightness setting, adjusting brightness levels in 256 steps, default value is 0xFF.

Device Control Register: Address is 0x01. This register is both readable and writeable for Bit 0 to Bit 2. Bit 0, also named BL_CTL, is used as on/off control for the output LEDs. Bit 1 and Bit 2, named PWM_SEL and PWM_MD respec tively, control the operating mode of the backlight controller. Bit 3 to Bit 7 are reserved bits. All reserved bits, return 0 when read, and are ignored by the controller when written. A value of 1 written to BL_CTL turns on the backlight in 10ms or less after the write cycle completes. A value of 0 written to BL_CTL immediately turns off the backlight.

REGISTER 0x01		DEVICE CONTROL REGISTER			DEFAULT VALUE 0X00		
Reserved	Reserved	Reserved	Reserved	Reserved	PWM_MD	PWM_SEL	BL_CTL
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

Bit Field Definitions:

BIT FIELD	DEFINITION	DESCRIPTION
Bit 2	PWM_MD	PWM mode select (1 = absolute brightness, 0 = % change) default = 0
Bit 1	PWM_SEL	Brightness MUX select (1 = PWMI pin, 0 = SMBus value) default = 0
Bit 0	BL_CTL	BL on/off (1 = On, 0 = Off) default = 0

The MAX17105 uses two multiplexers internally to direct the dimming signal processing (Figure 4). These two multiplexers are controlled by 2 bits of the device control register, PWM_SEL and PWM_MD, respectively. The PWM_SEL bit selects either the SMBus or the PWMI input to control the brightness. The PWM_MD bit selects the mode in which the PWMI input is to be interpreted. Table 4 provides a complete setting of the three dimming modes.

Table 4. Operating Modes Selected by Device Control Register Bits 1 and 2

PWM_MD	PWM_SEL	MODE	DPWM DUTY-CYCLE SETTING
X	1	PWM mode	PWMI input duty cycle
1	0	SMBus mode	SMBus command
0	0	DPST mode	Product of PWMI input duty cycle and SMBus command

X = Don't Care

In PWM mode, the output LED brightness is solely controlled by the percentage duty cycle of the input signal to PWMI. In SMBus mode, the input of PWMI has no effect on the dimming control, and only the SMBus command to the brightness control register adjusts the output brightness. In DPST mode, the overall brightness level is the normalized product of the SMBus command setting and PWM input duty cycle. The PWM signal starts from 100% when operating in DPST mode. The default value for register 0x01 is 0x00.

Fault/Status Register: Address is 0x02. This register has 6 status bits that allow monitoring the backlight controller's operating state. Bit 6 and Bit 7 are reserved bits, and Bit 3 is the status indicator or backlight. The other 5 bits are fault indicators. Bit 0 is a logical OR of all fault codes to simplify error detection (GLOBAL FAIL, OVCURR FAIL, 1CH SHORT/OPEN, 2 CH SHORT/OPEN, THRM_SHDN). All the bits in this register are read only. The reserved bits return a 0 when read.

REGISTER 0x02		FAULT/STATUS REGISTER			DEFAULT VALUE 0X00		
Reserved	Reserved	2_CH_SD	1_CH_SD	BL_STAT	OVCURR	THRM_SHDN	FAULT
Bit 7 (R)	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

Bit Field Definitions:

BIT FIELD	DEFINITION	DESCRIPTION
Bit 5	2_CH_SD	Two or more LED output channels are shut down (1 = shutdown, 0 = okay)
Bit 4	1_CH_SD	One LED output channel is shut down (1 = shutdown, 0 = okay)
Bit 3	BL_STAT	Backlight status (1 = BL on, 0 = BL off)
Bit 2	OV_CURR	Input overcurrent (1 = overcurrent condition, 0 = current okay)
Bit 1	THRM_SHDN	Thermal shutdown (1 = thermal fault, 0 = thermal okay)
Bit 0	FAULT	Fault occurred (logic OR of all the fault conditions)

Identification Register: Address is 0x03. The ID register contains two bit fields to denote the manufacturer and the silicon revision of the controller IC. The bit field widths were chosen to allow up to 32 vendors with up to eight silicon revisions each. This register is read only.

REGISTER 0x03		ID REGISTER			DEFAULT VALUE 0X80		
LED Panel	MFG3	MFG2	MFG1	MFG0	REV2	REV1	REV0
Bit 7 = 1	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

Bit Field Definitions:

BIT FIELD	DEFINITION	DESCRIPTION
Bit 7	LED Panel	Display panel using LED backlight, Bit 7 = 1
Bit [6:3]	MFG[3:0]	Manufacturer ID, see Table 5, default = 0
Bit [2:0]	REV[2:0]	Silicon rev (revs 0 to 7 allowed for silicon spins), default = 0

The list of ID values for vendors is shown below, based on the current backlight controller vendor list and is not sorted in any particular order.

Table 5. Vendor IDs

ID	VENDOR
0	Maxim
1	Micro Semi
2	MPS
3	O2 Micro
4	TI

ID	VENDOR
5	ST
6	Analog Devices
7-14	Reserved
15	Vendor ID register not implemented

Thermal Shutdown

The MAX17105 includes a thermal-protection circuit. When the local IC temperature exceeds +150°C (typ), the controller and current sources shut down and do not restart until the next enable signal is sent.

Design Procedure

All MAX17105 designs should be prototyped and tested prior to production.

External component value choice is primarily dictated by the output voltage and the maximum load current, as well as maximum and minimum input voltages. Begin by selecting an inductor value. Once the inductor is known, choose the diode and capacitors.

Step-Up Converter Current Calculation

To ensure stable operation, the MAX17105 includes slope compensation, which sets the minimum inductor value. In continuous-conduction mode (CCM), the minimum inductor value is calculated with the following equation:

$$L_{CCM(MIN)} = \frac{\left(V_{OUT(MAX)} + V_{DIODE} - 2 \times V_{S(MIN)}\right) \times R_S}{2 \times 25.5mV \times f_{SW(MIN)}}$$

where 25.5mV is a scale factor from the slope compensation, $L_{CCM(MIN)}$ is the minimum inductor value for stable operation in CCM, and R_S =13.7mΩ (typ) is the equivalent sensing-scale factor from the controller's internal current-sense circuit.

The controller can also operate in discontinuous-conduction mode (DCM). In this mode, the inductor value can be lower, but the peak inductor current is higher than in CCM. In DCM, the maximum inductor value is calculated with the following equation:

$$L_{DCM(MAX)} = \left(1 - \frac{V_{S(MIN)}}{V_{OUT(MAX)} + V_{DIODE}}\right) \times \frac{V_{S(MIN)}^2 \times \eta}{2 \times f_{SW(MAX)} \times V_{OUT(MAX)} \times I_{OUT(MAX)}}$$

where $L_{DCM(MAX)}$ is the maximum inductor value for DCM, η is the nominal regulator efficiency (85%), and $I_{OUT(MAX)}$ is the maximum output current.

The output current capability of the step-up regulator is a function of current limit, input voltage, operating frequency, and inductor value. Because the slope compensation is used to stabilize the feedback loop, the inductor current limit depends on the duty cycle, and is determined with the following equation:

$$I_{LIM} = 2A + \frac{25.5mV \times (0.75 - D)}{R_S}$$

where 25.5mV is the scale factor from the slope compensation, 2A is the current limit specified at 75% duty cycle, and D is the duty cycle.

The output current capability depends on the current- limit value and operating mode. The maximum output current in CCM is governed by the following equation:

$$I_{OUT\_CCM(MAX)} = \left(I_{LIM} - \frac{0.5 \times D \times V_S}{f_{SW} \times L}\right) \times \frac{V_S}{V_{OUT}} \times \eta$$

where I_{LIM} is the current limit calculated above, η is the nominal regulator efficiency (85%), and D is the duty cycle. The corresponding duty cycle for this current is:

$$D = \frac{V_{OUT} - V_S + V_{DIODE}}{V_{OUT} - I_{LIM} \times R_{ON} + V_{DIODE}}$$

where V_{DIODE} is the forward voltage of the rectifier diode and R_{ON} is the internal MOSFET's on-resistance (0.15Ω (typ)).

The maximum output current in DCM is governed by the following equation:

$$I_{OUT\_DCM(MAX)} = \frac{L \times I_{LIM}^2 \times f_{SW} \times \eta \times (V_{OUT} + V_{DIODE})}{2 \times V_{OUT} \times (V_{OUT} + V_{DIODE} - V_S)}$$

Inductor Selection

The inductance, peak current rating, series resistance, and physical size should all be considered when selecting an inductor. These factors affect the converter's operating mode, efficiency, maximum output load capability, transient-response time, output voltage ripple, and cost.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance minimizes the current ripple, and therefore reduces the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increases physical size and I^2R copper losses. Low inductor values decrease the physical size but increase the current ripple and peak current. Finding the best inductor involves the compromises among circuit efficiency, inductor size, and cost.

In choosing an inductor, the first step is to determine the operating mode: continuous-conduction mode (CCM) or discontinuous-conduction mode (DCM). The MAX17105 has a fixed internal slope compensation, which requires minimum inductor value. When CCM mode is chosen, the ripple current and the peak current of the inductor can be minimized. If a small-size inductor is required, DCM mode can be chosen. In DCM mode, the inductor value and size can be minimized, but the inductor ripple current and peak current are higher than those in CCM. The controller can be stable, independent of the internal slope-compensation mode, but there is a maximum inductor value requirement to ensure the DCM operating mode.

The equations used here include a constant LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The controller operates in DCM mode when LIR is higher than 2.0, and it works in CCM mode when LIR is lower than 2.0. The best trade-off between inductor size and converter efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripples can be accepted to reduce the number of required turns and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can reduce losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, LIR higher than 2.0 can be chosen for DCM operating mode.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions. The detail design procedure for CCM can be described as:

Calculate the approximate inductor value using the typical input voltage (V_S), the maximum output current ($I_{OUT(MAX)}$), the expected efficiency (ηTYP) taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{S(MIN)}}{V_{OUT}}\right)^2 \left(\frac{V_{OUT} - V_{S(MIN)}}{I_{OUT(MAX)} \times f_{SW}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

The MAX17105 has a minimum inductor value limitation for stable operation in CCM mode at low input voltage, because of the internal fixed slope compensation. The minimum inductor value for stability is calculated with the following equation:

$$L_{CCM(MIN)} = \frac{\left(V_{OUT(MAX)} + V_{DIODE} - 2 \times V_{S(MIN)}\right) \times R_S}{2 \times 25.5mV \times f_{SW(MIN)}}$$

where 25.5mV is a scale factor from slope compensation, and R_S is the equivalent current-sensing scale factor (13.7mΩ typ).

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{S(MIN)}$, using conservation of energy and the expected efficiency at that operating point (ηMIN) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{OUT(MAX)} \times V_{OUT}}{V_{S(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{S(MIN)} \times \left(V_{OUT(MAX)} - V_{S(MIN)}\right)}{L \times V_{OUT(MAX)} \times f_{SW}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

When the DCM operating mode is chosen to minimize the inductor value, the calculations are different from those above in CCM mode. The maximum inductor value for DCM mode is calculated with the following equation:

$$L_{DCM(MAX)} = \left(1 - \frac{V_{S(MIN)}}{V_{OUT(MAX)} + V_{DIODE}}\right) \times \frac{V_{S(MIN)}^2 \times \eta}{2 \times f_{SW(MAX)} \times V_{OUT(MAX)} \times I_{OUT(MAX)}}$$

The peak inductor current in DCM is calculated with the following equation:

$$I_{PEAK} = \sqrt{\frac{I_{OUT(MAX)} \times 2 \times V_{OUT(MAX)} \times (V_{OUT(MAX)} + V_{DIODE} - V_{S(MIN)})}{L \times f_{SW(MIN)} \times \eta \times (V_{OUT(MAX)} + V_{DIODE})}}$$

The inductor's saturation current rating should exceed IPEAK, and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the circuit with eight 10-LED strings and 20mA LED full-scale current, the maximum load current ($I_{OUT(MAX)}$) is 160mA with a 32V output and a minimal input voltage of 7V.

Choosing a CCM operating mode with LIR = 0.7 at 1MHz and an estimating efficiency of 85% at this operating point:

$$L = \left(\frac{7V}{32V}\right)^2 \left(\frac{32V - 7V}{160mA \times 1MHz}\right)\left(\frac{0.85}{0.7}\right) = 9.08\mu H$$

In CCM, the inductor has to be higher than $L_{CCM(MIN)}$:

$$L_{CCM(MIN)} = \frac{(32V + 0.4V - 2 \times 7V) \times 13.7m\Omega}{2 \times 25.5mV \times 0.9MHz} = 5.5\mu H$$

10µH inductor is chosen, which is higher the minimum L that guarantees stability in CCM.

The peak inductor current at minimum input voltage is calculated as follows:

$$I_{PEAK} = \frac{160mA \times 32V}{7V \times 0.85} + \frac{7V \times (32V - 7V)}{2 \times 10\mu H \times 32V \times 0.9MHz} = 1.16A$$

Alternatively, choosing a DCM operating mode will lower inductance and estimate efficiency of 85% at this operating point. Since DCM will have higher peak inductor current at lower input, it will cause current limit when the parameters are not chosen properly. Consider the case with six 10-LED strings and 20mA LED full-scale current to prevent excessive switch current from causing current limit:

$$L_{DCM(MAX)} = \left(1 - \frac{7V}{32V + 0.4V}\right) \times \frac{(7V)^2 \times 0.85}{2 \times 1.1MHz \times 32V \times 120mA} = 3.9\mu H$$

3.3µH inductor is chosen. The peak inductor current at minimum input voltage is calculated as follows:

$$I_{PEAK} = \sqrt{\frac{120mA \times 2 \times 32V \times (32V + 0.4V - 7V)}{3.3\mu H \times 1.1MHz \times 0.85 \times (32V + 0.4V)}} = 1.40A$$

Output Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging on the output capacitor, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{OUT(MAX)}}{C_{OUT}}\left(\frac{V_{OUT(MAX)} - V_{S(MIN)}}{V_{OUT(MAX)} \times f_{SW}}\right)$$

and:

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section).

The output voltage ripple should be low enough for the FB_ current source regulation. The ripple voltage should be less than $200mV_{P-P}$. For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Rectifier Diode Selection

The MAX17105's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. The diode should be rated to handle the output voltage and the peak switch current. Make sure that the diode's peak current rating is at least IPEAK calculated in the *Inductor Selection* section and that its breakdown voltage exceeds the output voltage.

Overvoltage-Protection Determination

The overvoltage-protection circuit should ensure the circuit safe operation; therefore, the controller should limit the output voltage within the ratings of all MOSFET, diode, and output capacitor components, while providing sufficient output voltage for LED current regulation. The OVP pin is connected to the center tap of a resistive voltage-divider (R1 and R2 in Figure 1) from the high-voltage output. When the controller detects the OVP pin voltage reaching the threshold VOVP_TH, typically 1.25V, overvoltage protection is activated. Hence, the step-up converter output overvoltage protection point is:

$$V_{OUT(OVP)} = V_{OVP\_TH} \times (1 + \frac{R1}{R2})$$

In Figure 1, the output OVP voltage is set to:

$$V_{OUT(OVP)} = 1.25V \times (1 + \frac{2.21M\Omega}{71.5k\Omega}) = 39.89V$$

Input Capacitor Selection

The input capacitor (C_{IN}) filters the current peaks drawn from the input supply and reduces noise injection into the IC. A 4.7µF ceramic capacitor is used in the typical operating circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. In some applications, C_{IN} can be reduced below the values used in the typical operating circuit. Ensure a low noise supply at IN by using adequate C_{IN}. Alternatively, greater voltage variation can be tolerated on C_{IN} if IN is decoupled from C_{IN} using an RC lowpass filter.

LED Selection and Bias

The series/parallel configuration of the LED load and the full-scale bias current have a significant effect on regulator performance. LED characteristics vary significantly from manufacturer to manufacturer. Consult the respective LED data sheets to determine the range of output voltages for a given brightness and LED current. In general, brightness increases as a function of bias current. This suggests that the number of LEDs could be decreased if higher bias current is chosen; however, high current increases LED temperature and reduces operating life. Improvements in LED technology are resulting in devices with lower forward voltage while increasing the bias current and light output.

LED manufacturers specify LED color at a given LED current. With lower LED current, the color of the emitted light tends to shift toward the blue range of the spectrum. A blue bias is often acceptable for business applications but not for high-image-quality applications such as DVD players. Direct-PWM dimming is a viable solution for reducing power dissipation while maintaining LED color integrity. Careful attention should be paid to switching noise to avoid other display quality problems.

Using fewer LEDs in a string improves step-up converter efficiency, and lowers breakdown voltage requirements of the external MOSFET and diode. The minimum number of LEDs in series should always be greater than the maximum input voltage. If the diode voltage drop is lower than maximum input voltage, the voltage drop across the current-sense inputs (FB_) increases and causes excess heating in the IC. Between 8 and 12 LEDs in series are ideal for input voltages up to 20V.

Applications Information

LED $V_{FB\_}$ Variation

The forward voltage of each white LED may vary up to 25% from part to part, and the accumulated voltage difference in each string equates to additional power loss within the IC. For the best efficiency, the voltage difference between strings should be minimized. The difference between lowest voltage string and highest voltage string should be less than 8V (typ). Otherwise, the internal LED short-protection circuit disables the high FB string.

FB_ Pin Maximum Voltage

The current through each FB_ pin is controlled only during the step-up converter's on-time. During the converter's off-time, the current sources are turned off. The output voltage does not discharge and stays high. The MAX17105 disables the FB current source from which the string is shorted. In this case, the step-up converter's output voltage is always applied to the disabled FB_ pin. FB_ pin can withstand 45V.

PCB Layout Guidelines

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

1) Minimize the area of the high-current switching loop of rectifier diode, internal MOSFET, and output capacitor to avoid excessive switching noise.
2) Connect high-current input and output components with short and wide connections. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the internal MOSFET, then to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the rectifier diode, and to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Avoid using vias in the high-current paths. If vias are unavoidable, use multiple vias in parallel to reduce resistance and inductance.

3) Create a ground island (PGND) consisting of the input and output capacitor ground and negative terminal of the current-sense resistor. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes. Create an analog ground island (AGND) consisting of the overvoltage-detection divider ground connection, the ISET and DFSET resistor connections, the COMP resistor and capacitor connections, and the device's exposed backside pad. Connect the AGND and PGND islands by connecting the SGND pins directly to the exposed backside pad. Make no other connections between these separate ground planes.

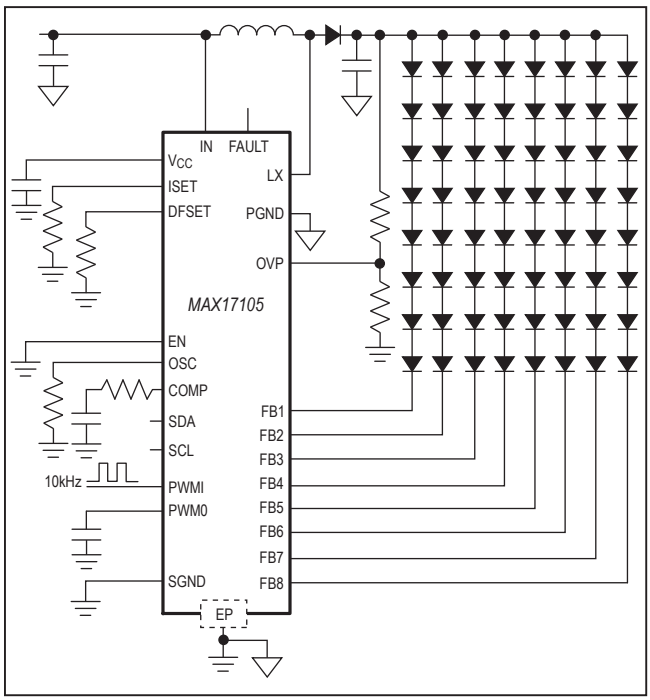
4) Place the overvoltage-detection divider resistors as close to the OVP pin as possible. The divider's center trace should be kept short. Placing the resistors far away causes the sensing trace to become antennas that can pick up switching noise. Avoid running the sensing traces near LX.

5) Place the IN pin bypass capacitor as close to the device as possible. The ground connection of the IN bypass capacitor should be connected directly to SGND pins with a wide trace.

6) Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from the feedback node and ground. If possible, avoid running the LX node from one side of the PCB to the other. Use DC traces as a shield if necessary.

Refer to the MAX17105 evaluation kit for an example of proper board layout.

Simplified Operating Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2444+4	21-0139	90-0022

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/09	Initial release	—
1	12/09	Updated *Electrical Characteristics*, *Typical Operating Characteristics* graphs 1 and 2, and COMP pin function with specifications for final production version	2–7, 11
2	9/14	Removed automotive reference from *Applications*	1

