19-4709; Rev 0; 8/09

EVALUATION KIT AVAILABLE

Low-Cost, Multiple-Output Power Supply for LCD TVs

General Description

The MAX17113 multiple-output power-supply controller generates all the supply rails for thin-film transistor (TFT) liquid-crystal display (LCD) panels in TVs and monitors operating from a regulated 12V input. It includes a step-down and a step-up regulator, a positive and a negative charge pump, a Dual Mode™ logic-controlled high-voltage switch control block, and an adjustable-timing power-good output. The MAX17113 can operate from 8V to 16.5V input voltages and is optimized for LCD TV panel and LCD monitor applications running directly from 12V supplies.

The step-up and step-down regulators feature internal power MOSFETs and high-frequency operation allowing the use of small inductors and capacitors, resulting in a compact solution. Both switching regulators use fixed-frequency current-mode control architectures, providing fast load-transient response and easy compensation. A current-limit function for internal switches and output-fault shutdown protect the step-up and step-down power supplies against fault conditions. The MAX17113 provides soft-start functions to limit inrush current during startup. The MAX17113 provides adjustable power-up timing.

The positive and negative charge-pump regulators provide TFT gate-driver supply voltages. Both output voltages can be adjusted with external resistive voltage-dividers. The switch control block allows the manipulation of the positive TFT gate-driver voltage.

A series p-channel MOSFET is integrated to sequence power to AV_{DD} after the MAX17113 has proceeded through normal startup, and provides True Shutdown™.

The MAX17113 is available in a small (5mm x 5mm), low-profile (0.8mm), 40-pin thin QFN package and operates over a -40°C to +85°C temperature range.

Applications

LCD TV Panels

LCD Monitor Panels

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17113ETL+	-40°C to +85°C	40 Thin QFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

***EP = Exposed pad.*

Simplified Operating Circuit appears at end of data sheet.

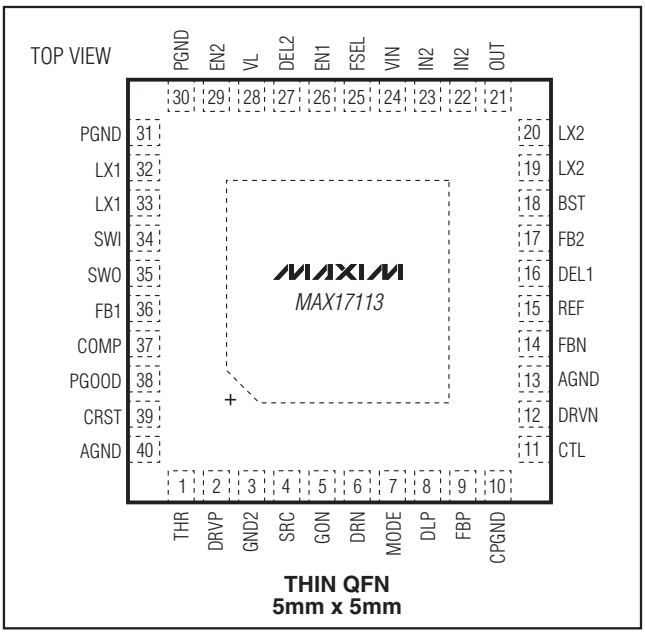
Dual Mode is a trademark of Maxim Integrated Products, Inc.

True Shutdown is a trademark of Maxim Integrated Products, Inc.

Features

- **Optimized for 10.8V to 13.2V Input Supply**
- **8V to 16.5V Input Supply Range**
- **Selectable Frequency (450kHz/600kHz)**
- **Current-Mode Step-Up Regulator**
  - **Built-In 24V, 3.3A, 80mΩ n-Channel MOSFET**
  - **High-Accuracy Output Voltage (1%)**
  - **True Shutdown**
  - **Fast Load-Transient Response**
  - **High Efficiency**
  - **10ms Internal Soft-Start**
- **Current-Mode Step-Down Regulator**
  - **Built-In 24V, 3A, 100mΩ n-Channel MOSFET**
  - **Fast Load-Transient Response**
  - **Adjustable Output Voltage Down to 1.5V**
  - **Skip Mode at Light Load (EN2 = AGND)**
  - **High Efficiency**
  - **3ms Internal Soft-Start**
- **Adjustable Positive and Negative Charge-Pump Regulators**
- **Soft-Start and Timer-Delay Fault Latch for All Outputs**
- **Logic-Controlled High-Voltage Integrated Switches with Adjustable Delay**
- **120mΩ p-Channel FET for AV_{DD} Sequencing**
- **Input Undervoltage Lockout and Thermal-Overload Protection**
- **40-Pin, 5mm x 5mm Thin QFN Package**

Pin Configuration



THIN QFN
5mm x 5mm

Low-Cost, Multiple-Output Power Supply for LCD TVs

ABSOLUTE MAXIMUM RATINGS

VIN, IN2, EN1, EN2, FSEL to AGND .....-0.3V to +24V
CPGND, GND2, PGND to AGND .....±0.3V
MODE, DLP, CTL, THR, DEL1, DEL2, VL, PGOOD to AGND .....-0.3V to +7.5V
REF, FBP, FBN, FB1, FB2, COMP, OUT, CRST to AGND .....-0.3V to (V_{VL} + 0.3V)
LX1, SWI, SWO to AGND .....-0.3V to +24V
SWI to SWO .....-0.3V to +24V
DRVN to AGND .....-0.3V to (V_{IN2} + 0.3V)
DRVP to AGND .....-0.3V to (V_{SWO} + 0.3V)
LX2 to GND2 .....-0.3V to (V_{IN2} + 0.3V)
BST to VL .....-0.3V to +24V
SRC to AGND .....-0.3V to +48V
GON, DRN to AGND .....-0.3V to (V_{SRC} + 0.3V)
SRC to DRN .....-0.3V to +40V
DRN to AGND .....-0.3V to +40V
GON to DRN .....-0.3V to +48V
REF Short Circuit to AGND .....Continuous
RMS LX1 Current (total for both pins) 3.2A
RMS PGND Current (total for both pins) 3.2A
RMS IN2 Current (total for both pins) 3.2A
RMS LX2 Current (total for both pins) 3.2A
RMS GND2, CPGND Current 0.8A
RMS SWI Current 2.4A
RMS SWO Current 2.4A
RMS DRVN, DRVP Current 0.8A
RMS VL Current 50mA
Continuous Power Dissipation (T_A = +70°C) 40-Pin Thin QFN (derate 35.7mW/°C above +70°C) 2857.1mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+160°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{VIN} = V_{IN2} = 12V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
VIN, IN2 Input Voltage Range		8.5		16.5	V
VIN + IN2 Quiescent Current	Only LX2 switching (V_{FB1} = V_{FBP} = 1.5V, V_{FBN} = 0V); EN1 = EN2 = VL, V_{FSEL}= 0V		10		mA
VIN + IN2 Standby Current	LX2 not switching (V_{FB1} = V_{FB2} = V_{FBP} = 1.5V, V_{FBN} = 0V); EN1 = EN2 = VL, V_{FSEL}= 0V		3		mA
VIN + IN2 Shutdown Current	EN1 = EN2 = AGND (shutdown)		300	600	µA
SWO Shutdown Current	EN1 = EN2 = AGND (shutdown)		0.25	2	µA
SMPS Operating Frequency	FSEL = VIN	510	600	690	kHz
	FSEL = AGND	390	450	510	
Phase Difference Between Step-Down/Positive and Step-Up/Negative Regulators			180		Degrees
VIN Undervoltage Lockout Threshold	VIN rising edge, 100mV typical hysteresis	6.0	7.0	8.3	V
VL REGULATOR					
VL Output Voltage	I_{VL} = 25mA, V_{FB1} = V_{FB2} = V_{FBP} = 1.1V, V_{FBN} = 0.4V (all regulators switching)	4.9	5.0	5.15	V
VL Undervoltage Lockout Threshold	VL rising edge, 100mV typical hysteresis	3.6	4.0	4.5	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{VIN} = V_{IN2} = 12V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE						
REF Output Voltage	No external load		1.235	1.250	1.265	V
REF Load Regulation	0 < I_{LOAD} < 50µA				10	mV
REF Sink Current	In regulation		10			µA
REF Undervoltage-Lockout Threshold	Rising edge; 25mV typical hysteresis			1.0	1.2	V
STEP-DOWN REGULATOR						
OUT Voltage in Fixed Mode	FB2 = AGND, no load (Note 1)	0°C < T_A < +85°C	3.25	3.30	3.35	V
		T_A = +25°C	3.267		3.333	
FB2 Voltage in Adjustable Mode	V_{OUT} = 2.5V, no load (Note 1)	0°C < T_A < +85°C	1.23	1.25	1.27	V
		T_A = +25°C	1.2375		1.2625	
FB2 Adjustable-Mode Threshold Voltage	Dual-mode comparator		0.10	0.15	0.20	V
Output-Voltage Adjust Range	Step-down output		1.5		5.0	V
FB2 Fault Trip Level	Falling edge		0.94	1.00	1.06	V
FB2 Input Bias Current	V_{FB2} = 1.5V, T_A = +25°C		50	125	200	nA
DC Load Regulation	0.4A < I_{LOAD} < 2A			0.5		%
DC Line Regulation	No load, 10.8V < V_{IN2} < 13.2V			0.05		%/V
LX2-to-IN2 nMOS Switch On-Resistance				100	200	mΩ
LX2-to-CPGND nMOS Switch On-Resistance			7	12	25	Ω
BST-to-VL pMOS Switch On-Resistance			7	12	25	Ω
Low-Frequency Operation OUT Threshold	Step-down only			0.8		V
Low-Frequency Operation Switching Frequency	FSEL = VIN			100		kHz
	FSEL = AGND			75		
LX2 Positive Current Limit			2.50	3	3.50	A
Soft-Start Period				3.3		ms
Soft-Start Step Size				V_{REF}/128		V
Maximum Duty Factor			65	75	90	%
POWER-GOOD						
FB2 Power-Good Threshold	FB2 rising		0.94	1.00	1.06	V
FB2 Threshold Hysteresis				12		mV
PGOOD Output Low Voltage	I_{PGOOD} = 1mA			0.1	0.3	V
PGOOD Leakage Current	V_{PGOOD} = 3V, T_A = +25°C				1	µA
CRST Charge Current	V_{CRST} = 1V		0.8	1.0	1.2	µA
CRST Voltage Threshold			1.2	1.25	1.3	V
CRST Pulldown Resistance	V_{CRST} = 1V			150	300	Ω

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{VIN} = V_{IN2} = 12V$, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
STEP-UP REGULATOR						
Output-Voltage Range			V_{VIN}		18	V
Minimum t_{ON}				70	100	ns
FB1 Regulation Voltage	FB1 = COMP, C_{COMP} = 1mF	T_A = +25°C	1.2375	1.250	1.2625	V
		0°C < T_A < +85°C	1.225		1.275	
FB1 Fault Threshold	FB rising, hysteresis = 12mV		0.96	1.0	1.06	V
FB1 UVLO Threshold			0.05	0.125	0.2	V
FB1 Load Regulation	0A < I_{LOAD} < full			0.5		%
FB1 Line Regulation	10.8V < V_{IN} < 13.2V			0.08	0.15	%/V
FB1 Input Bias Current	V_{FB1} = 1.25V		20	125	300	nA
FB1 Transconductance	ΔI = ±2.5µA at COMP, FB1 = COMP		125	320	600	µS
FB1 Voltage Gain	FB1 to COMP			1400		V/V
LX1 Leakage Current	V_{FB1} = 1.5V, V_{LX1} = 20V			10	25	µA
LX1 Current Limit	V_{FB1} = 1.1V, duty cycle = 25%		2.8	3.3	3.8	A
Current-Sense Transresistance			0.1	0.2	0.30	V/A
LX1 On-Resistance				80	200	mΩ
Soft-Start Period				10		ms
Soft-Start Step Size				I_{LIM}/128		A
POSITIVE AND NEGATIVE CHARGE-PUMP REGULATORS						
FBP Regulation Voltage	0°C < T_A < +85°C		1.23	1.25	1.27	V
	T_A = +25°C		1.2375		1.2625	
FBP Line-Regulation Error	11V < V_{SUP} < 16V, not in dropout			0.01	0.2	%/V
FBP Input Bias Current	V_{FBP} = 1.5V, T_A = +25°C		-50		+50	nA
DRVP p-Channel MOSFET On-Resistance				2.0	4.0	Ω
DRVP n-Channel MOSFET On-Resistance				0.8	1.5	Ω
FBP Fault Trip Level	Falling edge		0.96	1.02	1.08	V
Positive Charge-Pump Soft-Start Period				3.3		ms
Positive Charge-Pump Soft-Start Step Size				V_{REF}/128		V
FBN Regulation Voltage	$V_{REF} - V_{FBN}$	0°C < T_A < +85°C	0.985	1.000	1.015	V
		T_A = +25°C	0.99	1.00	1.01	
FBN Input Bias Current	V_{FBN} = 250mV, T_A = +25°C		-50		+50	nA
FBN Line Regulation Error	11V < V_{SUP} < 16V, not in dropout			0.01	0.2	%/V
DRVN p-Channel On-Resistance				2.0	4.0	Ω
DRVN n-Channel On-Resistance				0.8	1.5	Ω
FBN Fault Trip Level	Rising edge		450	500	550	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{VIN} = V_{IN2} = 12V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Negative Charge-Pump Soft-Start Period			2		ms
Negative Charge-Pump Soft-Start Step Size			(V_{REF} - V_{FBN}/128		V
AV_{DD} SWITCH					
SWI Supply Range		8.0		18.5	V
SWI Overvoltage Fault Threshold	SWI rising edge, 300mV typical hysteresis (Note 2)	18.50	19.2	19.90	V
SWI-SWO Switch Resistance			120	250	mΩ
HIGH-VOLTAGE SWITCH ARRAY					
SRC Supply Range				44	V
SRC Supply Current			250	500	µA
GON-to-SRC Switch On-Resistance	V_{DLP} = 2V, CTL = VL		10	20	Ω
GON-to-SRC Switch Saturation Current	(V_{SRC} - V_{GON}) > 5V	180	390		mA
GON-to-DRN Switch On-Resistance	V_{DLP} = 2V, CTL = AGND		25	50	Ω
GON-to-DRN Switch Saturation Current	(V_{GON} - V_{DRN}) > 5V	40	180		mA
GON-to-GND Switch On-Resistance	DLP = AGND, V_{GON} = 5V		5	10	kΩ
CTL Input Low Voltage				0.6	V
CTL Input High Voltage		1.6			V
CTL Input Current	CTL = AGND or VL, T_A = +25°C	-1		+1	µA
CTL-to-GON Rising Propagation Delay	1kΩ from DRN to GND, CTL = AGND to VL step, no load on GON, measured from V_{CTL} = 2V to GON = 20%		100		ns
CTL-to-GON Falling Propagation Delay	1kΩ from DRN to GND, CTL = VL to AGND step, no load on GON, measured from V_{CTL} = 0.6V to GON = 80%		200		ns
MODE Switch On-Resistance			1200		Ω
Mode 1 Voltage Threshold	V_{MODE} rising		3.8	4.1	V
MODE Capacitor Charge Current (Mode 2)	V_{MODE} = 1V	40	50	65	µA
MODE Voltage Threshold for Enabling DRN Switch Control in Mode 2	GON connects to DRN	1.15	1.25	1.35	V
MODE Current-Source Stop Voltage Threshold	MODE rising	2		3	V
THR-to-GON Voltage Gain		9.4	10.0	10.6	V/V
SEQUENCE CONTROL					
EN1, EN2 Input Low Voltage				0.6	V
EN1, EN2 Input High Voltage		1.6			V
EN1, EN2 Pulldown Resistance			1		MΩ
DEL1, DEL2, DLP Charge Current	V_{DEL1} = V_{DEL2} = V_{DLP} = 1V	7	8	9	µA
DEL1, DEL2, DLP Turn-On Threshold		1.2	1.25	1.32	kV
DEL1, DEL2, DLP Discharge Switch On-Resistance	EN1 = AGND or fault tripped		10		Ω
FBN Discharge Switch On-Resistance	EN2 = AGND or fault tripped		3		kΩ

Low-Cost, Multiple-Output Power Supply for LCD TVs

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{VIN} = V_{IN2} = 12V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FAULT DETECTION					
Duration to Trigger Fault		45	55	65	ms
Duration to Restart After Fault			240		ms
Number of Restart Attempts Before Shutdown			3		Times
Thermal-Shutdown Threshold	15°C typical hysteresis		+160		°C
SWITCHING FREQUENCY SELECTION					
FSEL Input Low Voltage	450kHz			0.6	V
FSEL Input High Voltage	600kHz	1.6			V
FSEL Pulldown Resistance			1		MΩ

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{VIN} = V_{IN2} = 12V, **T_A = -40°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
VIN + IN2 Input-Voltage Range		8.5		16.5	V
VIN + IN2 Shutdown Current	EN1 = EN2 = AGND (shutdown)			600	µA
SWO Shutdown Current	EN1 = EN2 = AGND (shutdown)			2	µA
SMPS Operating Frequency	FSEL = VIN	510		690	kHz
	FSEL = AGND	390		510	
VIN Undervoltage-Lockout Threshold	VIN rising edge, 100mV typical hysteresis	5.75		7.25	V
VL REGULATOR					
VL Output Voltage	I_{VL} = 25mA, V_{FB1} = V_{FB2} = V_{FBP} = 1.1V, V_{FBN} = 0.4V (all regulators switching)	4.9		5.15	V
VL Undervoltage-Lockout Threshold	VL rising edge, 100mV typical hysteresis	3.6		4.5	V
REFERENCE					
REF Output Voltage	No external load	1.235		1.265	V
REF Load Regulation	0 < I_{LOAD} < 50µA			10	mV
REF Undervoltage-Lockout Threshold	Rising edge; 25mV typical hysteresis			1.2	V
STEP-DOWN REGULATOR					
OUT Voltage in Fixed Mode	FB2 = GND, no load (Note 1)	3.25		3.35	V
FB2 Voltage in Adjustable Mode	V_{OUT} = 2.5V, no load (Note 1)	1.23		1.27	V
FB2 Adjustable-Mode Threshold Voltage	Dual-mode comparator	0.10		0.20	V
Output-Voltage Adjust Range	Step-down output	1.5		5.0	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{VIN} = V_{IN2} = 12V, **T_A = -40°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LX2-to-IN2 nMOS Switch On-Resistance				200	mΩ
LX2-to-CPGND nMOS Switch On-Resistance		7		25	Ω
BST-to-VL pMOS Switch On-Resistance		7		25	Ω
LX2 Positive Current Limit		2.50		3.50	A
Maximum Duty Factor		65		90	%
FB2 Power-Good Threshold	FB2 rising	0.94		1.06	V
PGOOD Output Low Voltage	I_{PGOOD} = 1mA			0.3	V
CRST Charge Current	V_{CRST} = 1V	0.8		1.2	µA
CRST Voltage Threshold		1.2		1.3	V
CRST Pulldown Resistance	V_{CRST} = 1V			300	Ω
STEP-UP REGULATOR					
Output-Voltage Range		V_{VIN}		18	V
Oscillator Maximum Duty Cycle		65		90	%
FB1 Regulation Voltage	FB1 = COMP, C_{COMP} = 1nF	1.225		1.275	V
LX1 Current Limit	V_{FB1} = 1.1V, duty cycle = 25%	3.2		4.2	A
Current-Sense Transresistance		0.10		0.30	V/A
LX1 On-Resistance				200	mΩ
POSITIVE AND NEGATIVE CHARGE-PUMP REGULATORS					
FBP Regulation Voltage		1.23		1.27	V
DRVP p-Channel MOSFET On-Resistance				4	Ω
DRVP n-Channel MOSFET On-Resistance				1.5	Ω
FBN Regulation Voltage	V_{REF} - V_{FBN}	0.985		1.015	V
DRVN p-Channel On-Resistance				3	Ω
DRVN n-Channel On-Resistance				1.5	Ω
AVDD SWITCH					
SWI Supply Range		8.0		18.5	V
SWI Overvoltage Fault Threshold	V_{SWI} = rising, 300mV typical hysteresis (Note 3)	18.5		19.9	V
SWI-SWO Switch Resistance				360	mΩ
HIGH-VOLTAGE SWITCH ARRAY					
SRC Supply Range				44	V
GON-to-SRC Switch On-Resistance	V_{DLP} = 2V, CTL = VL			20	Ω
GON-to-DRN Switch On-Resistance	V_{DLP} = 2V, CTL = AGND			50	Ω
GON-to-GND Switch On-Resistance	DLP = AGND, V_{GON} = 5V	2.5		10	kΩ
CTL Input Low Voltage				0.6	V
CTL Input High Voltage		1.6			V
Mode 1 Voltage Threshold	V_{MODE} rising edge			4.1	V

Low-Cost, Multiple-Output Power Supply for LCD TVs

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{VIN} = V_{IN2} = 12V$, **T_A = -40°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MODE Voltage Threshold for Enabling DRN Switch Control in Mode 2	GON connects to DRN	1.15		1.35	V
MODE Current-Source Stop Voltage Threshold	MODE rising	2		3	V
THR-to-GON Voltage Gain		9.4		10.6	V/V
SEQUENCE CONTROL					
EN1, EN2 Input Low Voltage				0.6	V
EN1, EN2 Input High Voltage		1.6			V
SWITCHING FREQUENCY SELECTION					
FSEL Input Low Voltage	600kHz			0.6	V
FSEL Input High Voltage	1.2MHz	1.6			V

Note 1: When the inductor is in continuous conduction (EN2 = VL or heavy load), the output voltage has a DC regulation level lower than the error comparator threshold by 50% of the output-voltage ripple. In discontinuous conduction (EN2 = GND with light load), the output voltage has a DC regulation level higher than the error comparator threshold by 50% of the output-voltage ripple.

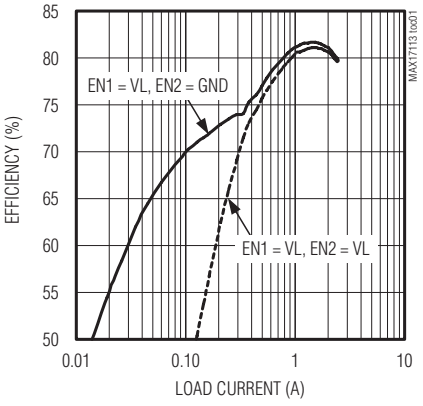
Note 2: Disables boost switching if either SUP, SWI, or OVIN exceeds the threshold. Switching resumes when no threshold is exceeded.

Note 3: Specifications to T_A = -40°C are guaranteed by design, not production tested.

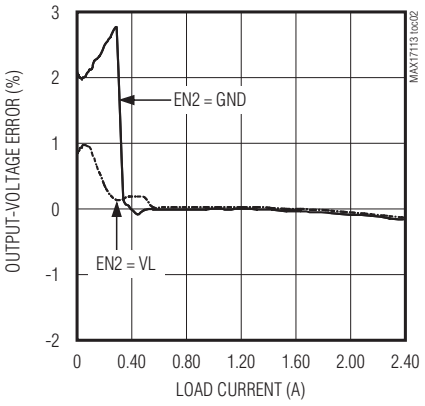
Typical Operating Characteristics

(Circuit of Figure 1. $V_{IN} = V_{INL} = V_{SUPP} = 12V$, $AV_{DD} = 16V$, $V_{GON} = 34.5V$, $V_{GOFF} = -6V$, $V_{OUT1} = 3.3V$, T_A = +25°C, unless otherwise noted.)

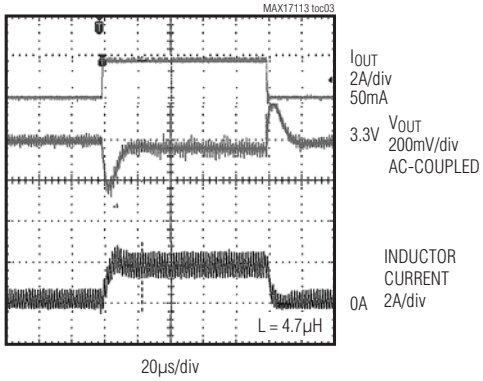
STEP-DOWN REGULATOR EFFICIENCY vs. LOAD CURRENT



STEP-DOWN REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



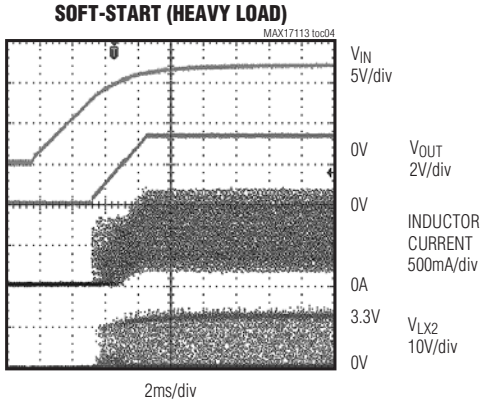
STEP-DOWN REGULATOR LOAD-TRANSIENT RESPONSE



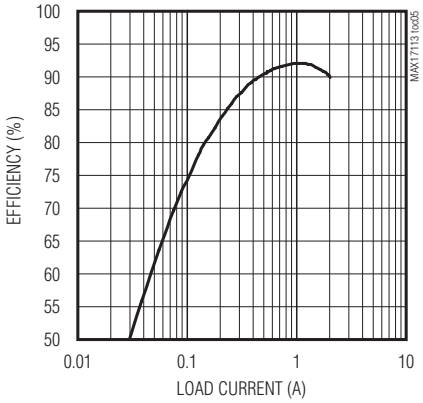
Typical Operating Characteristics (continued)

(Circuit of Figure 1. V_{IN} = V_{INL} = V_{SUPP} = 12V, AV_{DD} = 16V, V_{GON} = 34.5V, V_{GOFF} = -6V, V_{OUT1} = 3.3V, T_A = +25°C, unless otherwise noted.)

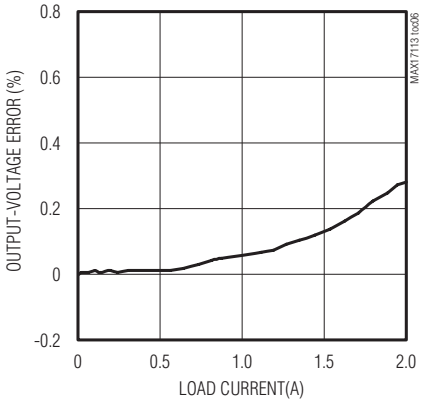
STEP-DOWN REGULATOR SOFT-START (HEAVY LOAD)



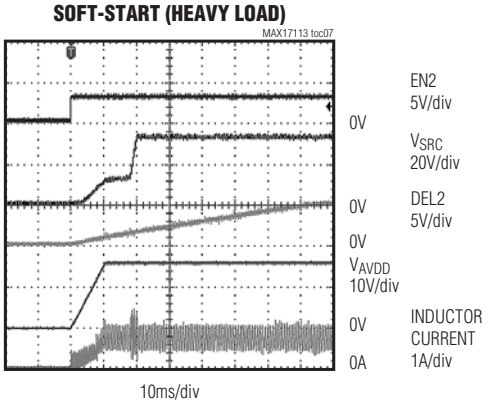
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT



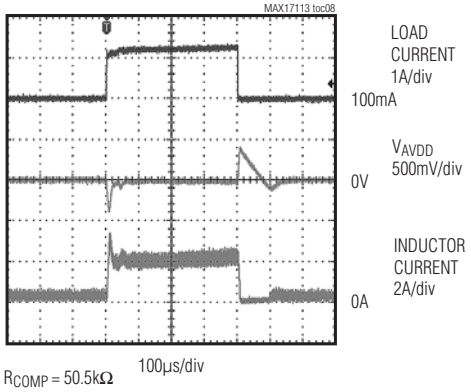
STEP-UP REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



STEP-DOWN REGULATOR SOFT-START (HEAVY LOAD)

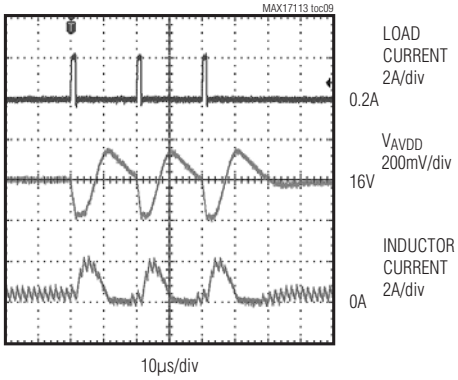


STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE



R_{COMP} = 50.5kΩ
C_{COMP} = 330pF

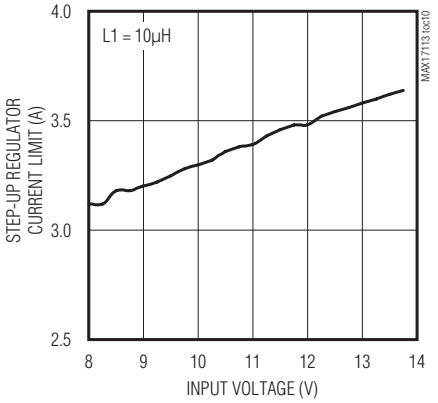
STEP-UP REGULATOR PULSED LOAD-TRANSIENT RESPONSE



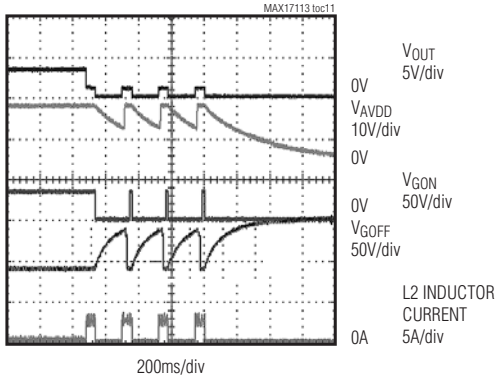
Typical Operating Characteristics (continued)

(Circuit of Figure 1. V_{IN} = V_{INL} = V_{SUPP} = 12V, AV_{DD} = 16V, V_{GON} = 34.5V, V_{GOFF} = -6V, V_{OUT1} = 3.3V, T_A = +25°C, unless otherwise noted.)

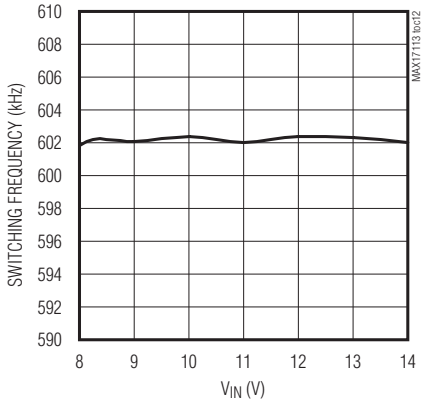
STEP-UP REGULATOR CURRENT LIMIT vs. INPUT VOLTAGE



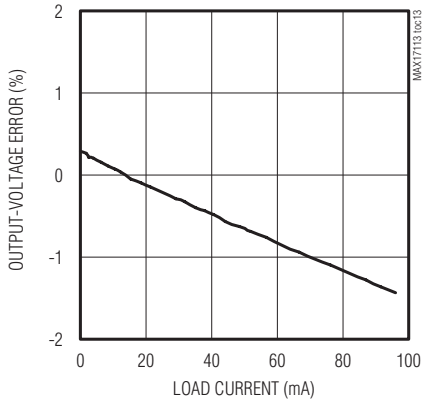
TIME-DELAY LATCH RESPONSE TO OVERLOAD



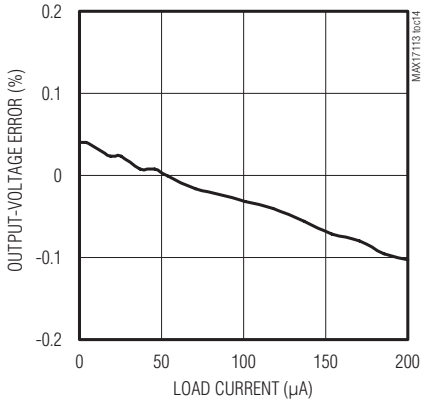
SWITCHING FREQUENCY vs. INPUT VOLTAGE



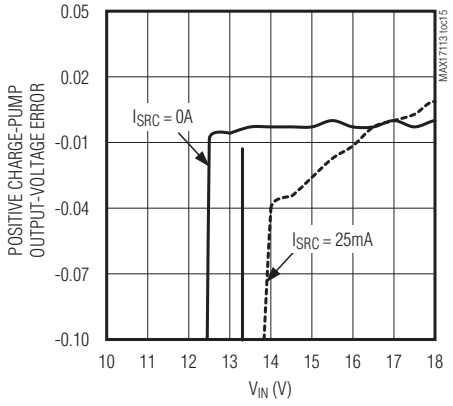
VL LOAD REGULATION



NORMALIZED REFERENCE VOLTAGE LOAD REGULATION



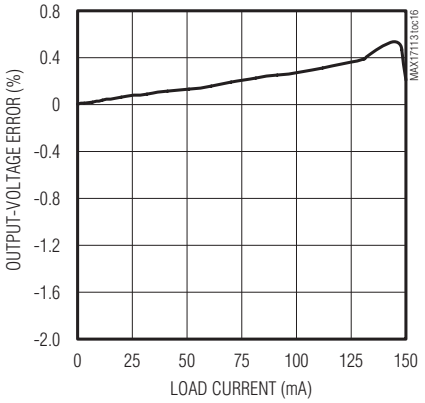
POSITIVE CHARGE-PUMP REGULATOR NORMALIZED LINE REGULATION



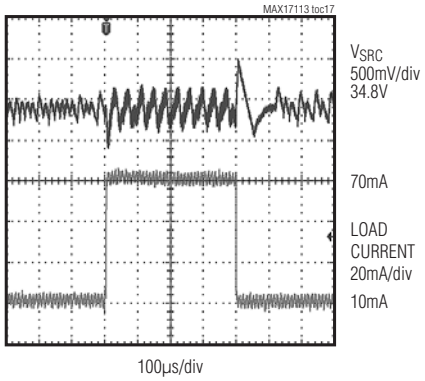
Typical Operating Characteristics (continued)

(Circuit of Figure 1. V_{IN} = V_{INL} = V_{SUPP} = 12V, AV_{DD} = 16V, V_{GON} = 34.5V, V_{GOFF} = -6V, V_{OUT1} = 3.3V, T_A = +25°C, unless otherwise noted.)

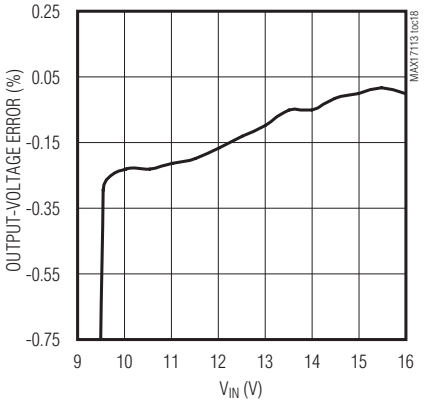
POSITIVE CHARGE-PUMP REGULATOR NORMALIZED LOAD REGULATION



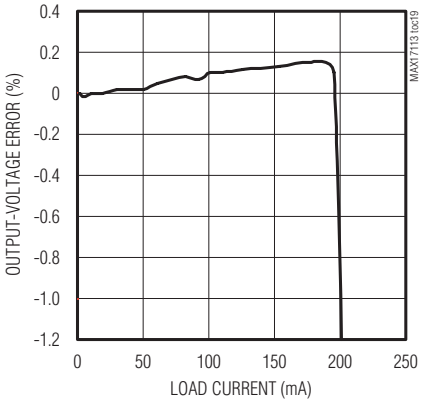
POSITIVE CHARGE-PUMP REGULATOR LOAD-TRANSIENT RESPONSE



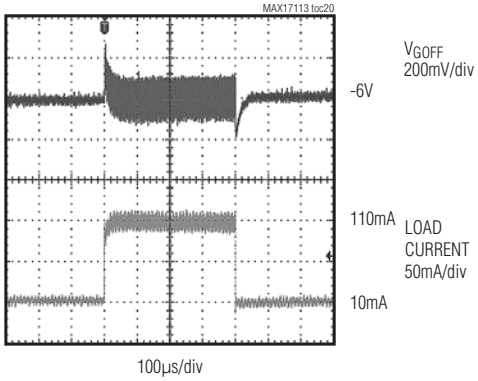
NEGATIVE CHARGE-PUMP REGULATOR NORMALIZED LINE REGULATION



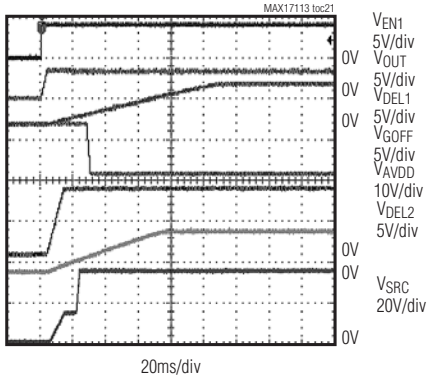
NEGATIVE CHARGE-PUMP REGULATOR NORMALIZED LOAD REGULATION



NEGATIVE CHARGE-PUMP REGULATOR LOAD-TRANSIENT RESPONSE



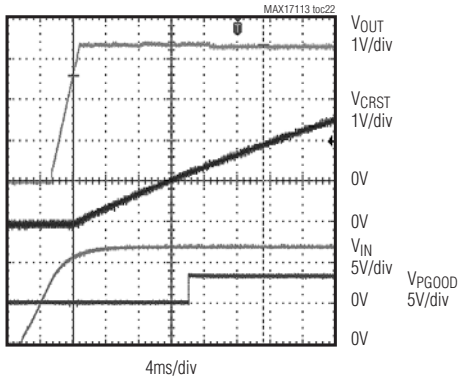
POWER-UP SEQUENCE



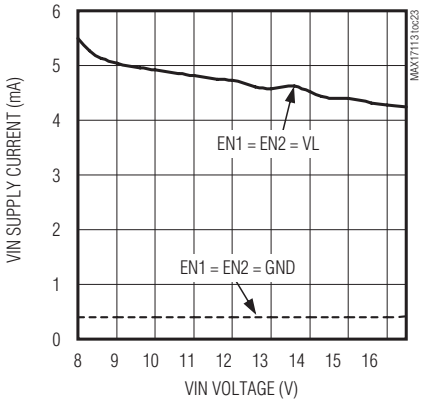
Typical Operating Characteristics (continued)

(Circuit of Figure 1. V_{IN} = V_{INL} = V_{SUPP} = 12V, AV_{DD} = 16V, V_{GON} = 34.5V, V_{GOFF} = -6V, V_{OUT1} = 3.3V, T_A = +25°C, unless otherwise noted.)

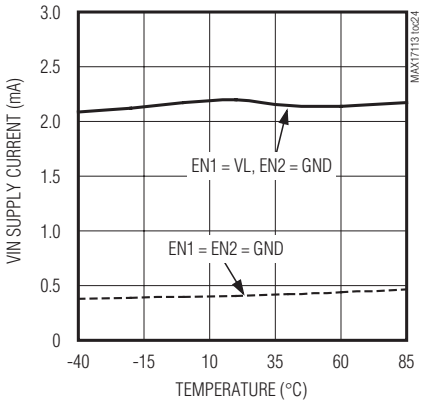
POWER-GOOD FUNCTION



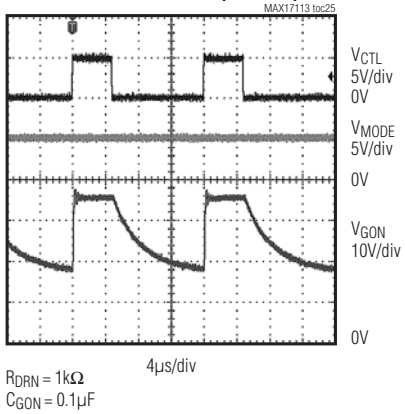
VIN SUPPLY CURRENT vs. VIN VOLTAGE



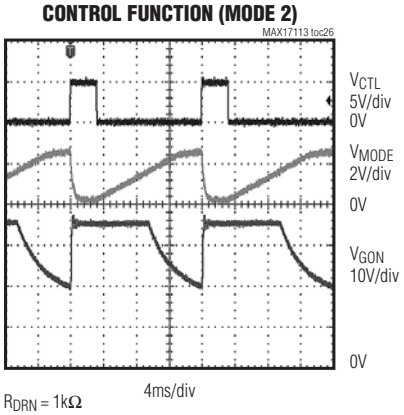
VIN SUPPLY CURRENT vs. TEMPERATURE



HIGH-VOLTAGE SWITCH CONTROL FUNCTION (MODE 1)



HIGH-VOLTAGE SWITCH CONTROL FUNCTION (MODE 2)



Pin Description

PIN	NAME	FUNCTION
1	THR	GON Low-Level Regulation Set-Point Input. Connects THR to the center of a resistive voltage-divider between AVDD and GND to set the V_{GON} falling regulation level. The actual level is $10 \times V_{THR}$. See the *High-Voltage Switch Control* section for details.
2	DRVP	Positive Charge-Pump Driver Output. Connects DRVP to the positive charge-pump flying capacitor(s).
3	GND2	Internal Buck LSS Power Ground
4	SRC	Switch Input. Source of the internal high-voltage p-channel MOSFET between SRC and GON.
5	GON	Internal High-Voltage MOSFET Switch Common Terminal. GON is the output of the high-voltage switch-control block.
6	DRN	Switch Input. Drain of the internal high-voltage p-channel MOSFET connected to GON.
7	MODE	High-Voltage Switch-Control Block Mode Selection Input and Timing-Adjustment Input. See the *High-Voltage Switch Control* section for details. MODE is high impedance when it is connected to VL. MODE is internally pulled to GND by a 10Ω resistor for 0.1µs (typ) when the high-voltage switch-control block is enabled.
8	DLP	GON Output Enable. See the *High-Voltage Switch Control* section for details.
9	FBP	Positive Charge-Pump Regulator Feedback Input. Connects FBP to the center of a resistive voltage-divider between the positive charge-pump regulator output and AGND to set the positive charge-pump regulator output voltage. Place the resistive voltage-divider within 5mm of FBP.
10	CPGND	Charge Pump and Internal Step-Down Regulator Pulldown Switch Power Ground
11	CTL	High-Voltage Switch-Control Block Timing Control Input. See the *High-Voltage Switch Control* section
12	DRVN	Negative Charge-Pump Driver Output. Connects DRVN to the negative charge-pump flying capacitor(s).
13, 40	AGND	Analog Ground
14	FBN	Negative Charge-Pump Regulator Feedback Input. Connects FBN to the center of a resistive voltage-divider between the negative output and REF to set the negative charge-pump regulator output voltage. Place the resistive voltage-divider within 5mm of FBN.
15	REF	Reference Output. Connects a 0.22µF capacitor from REF to AGND. All power outputs are disabled until REF exceeds its UVLO threshold. REF is active whenever V_{IN} is above its UVLO threshold.
16	DEL1	Negative Charge-Pump Delay Input. Connects a capacitor from DEL1 and AGND to set the delay time between the step-down output and the negative output. An 8µA current source charges C_{DEL1}. DEL1 is internally pulled to AGND through 10Ω resistance when EN1 is low or VL is below its UVLO threshold.
17	FB2	Step-Down Regulator Feedback Input. Connects FB2 to GND to select the step-down converter's 3.3V fixed mode. For adjustable mode, connect FB2 to the center of a resistive voltage-divider between the step-down regulator output and GND to set the step-down regulator output voltage. Place the resistive voltage-divider within 5mm of FB2.
18	BST	Step-Down Regulator Bootstrap Capacitor Connection for High-Side Gate Driver. Connects a 0.1µF ceramic capacitor from BST to LX2.
19, 20	LX2	Step-Down Regulator Switching Node. LX2 is the source of the internal n-channel MOSFET connected between IN2 and LX2. Connect the inductor and Schottky catch diode to both LX2 pins to minimize the trace area for low EMI.
21	OUT	Step-Down Regulator Output-Voltage Sense Input. Connects OUT to the step-down regulator output.
22, 23	IN2	Step-Down Regulator Power Input. Drain of the internal n-channel MOSFET connected between IN2 and LX2.
24	VIN	Input of the Internal 5V Linear Regulator and the Startup Circuitry. Bypass VIN to AGND with 0.22µF close to the IC.

Pin Description (continued)

PIN	NAME	FUNCTION
25	FSEL	Frequency Select Pin. Connect FSEL to AGND for 450kHz operation. Connect to VL or VIN for 600kHz operation.
26	EN1	Step-Down and Negative Charge-Pump Regulator Enable Input. Input high also enables DLY1 pullup current.
27	DEL2	Step-Up Regulator and Positive Charge-Pump Delay Input. Connects a capacitor from DEL2 and AGND to set the delay time between EN2 and the startup of these regulators, or between the step-down startup and the startup of these regulators if EN1 is high before the step-down starts. An 8µA current source charges C_{DEL2}. DEL2 is internally pulled to AGND through 10Ω resistance when EN1 or EN2 is low or when VL is below its UVLO threshold.
28	VL	5V Internal Linear Regulator Output. Bypass VL to AGND with 1µF minimum. Provides power for the internal MOSFET driving circuit, the PWM controllers, charge-pump regulators, logic, and reference and other analog circuitry. Provides 25mA load current when all switching regulators are enabled. VL is active whenever V_{IN} is above its UVLO threshold.
29	EN2	Step-Up and Positive Charge-Pump Regulator Enable Input. Input high also enables DLY2 pullup current. EN2 is inactive when EN1 is low.
30, 31	PGND	Step-Up Regulator Power Ground. Source of the internal power n-channel MOSFET.
32, 33	LX1	Step-Up Regulator Power MOSFET n-Channel Drain and Switching Node. Connects the inductor and Schottky catch diode to both LX1 pins and minimize the trace area for the lowest EMI.
34	SWI	Step-Up Regulator Internal PMOS Pass Switch Source Input. Connects to the anode of the step-up regulator Schottky catch diode.
35	SWO	Step-Up Regulator Internal pMOS Pass Switch Drain Output
36	FB1	Boost Regulator Feedback Input. Connects FB1 to the center of a resistive voltage-divider between the boost regulator output and AGND to set the boost regulator output voltage. Place the resistive voltage-divider within 5mm of FB1.
37	COMP	Compensation Pin for the Step-Up Error Amplifier. Connects a series resistor and capacitor from COMP to AGND.
38	PGOOD	Open-Drain Power-Good Output. Monitors the step-down output voltage.
39	CRST	Power-Good Reset Timing Pin. Connects a capacitor from CRST to AGND to set the step-down output-rising PGOOD delay.
—	EP	Exposed Pad = AGND

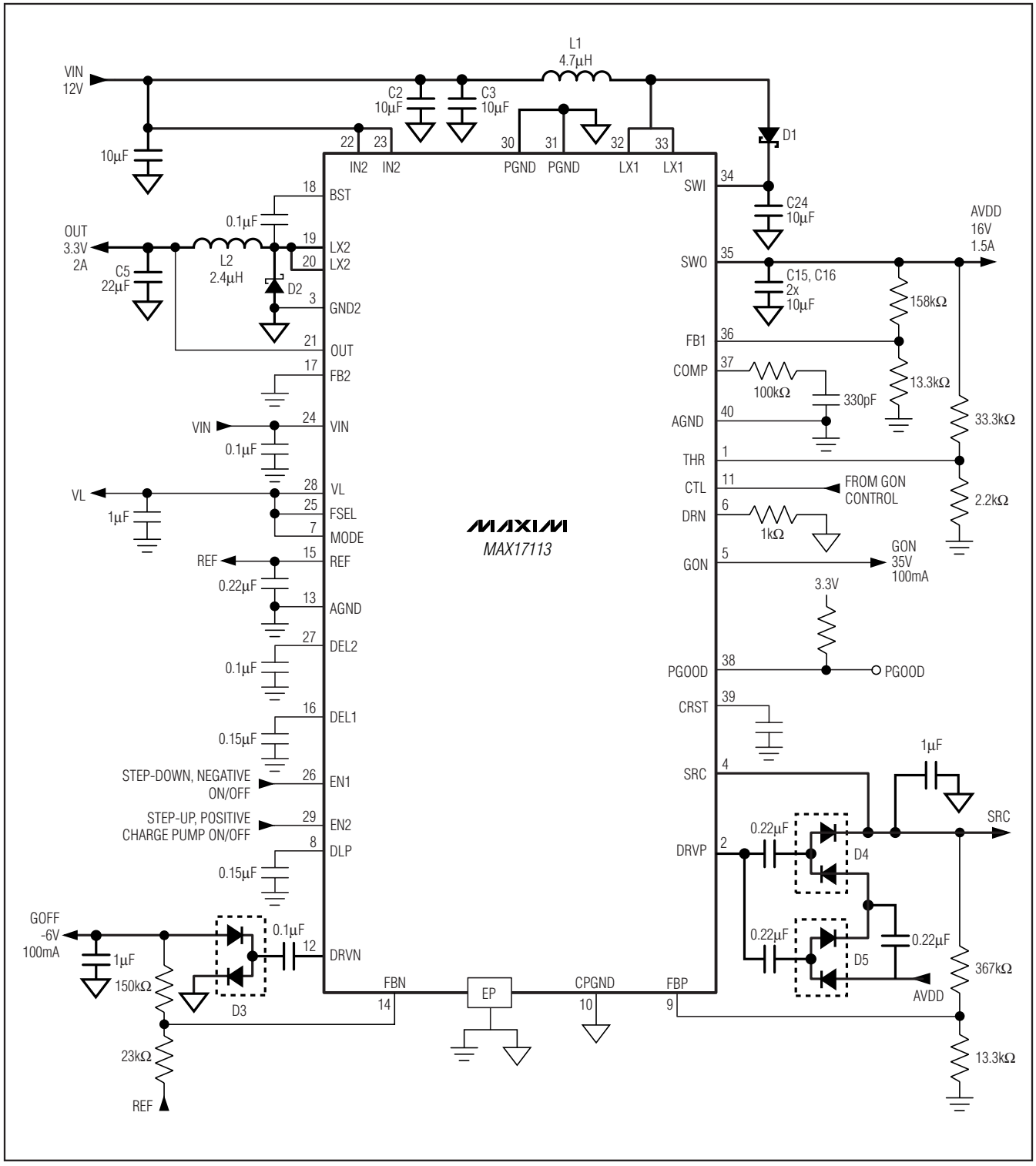


Figure 1. Typical Operating Circuit

Low-Cost, Multiple-Output Power Supply for LCD TVs

Typical Operating Circuit

The typical operating circuit (Figure 1) of the MAX17113 is a complete power-supply system for TFT LCD panels in monitors and TVs. The circuit generates a +3.3V logic supply, a +16V source driver supply, a +34.5V positive gate driver supply, and a -6V negative gate driver supply from a 12V ±10% input supply. Table 1 lists some selected components and Table 2 lists the contact information for component suppliers.

Table 1. Component List

DESIGNATION	DESCRIPTION
C1, C2, C3	10µF ±20%, 16V X5R ceramic capacitors (1206) Taiyo Yuden EMK325BJ106MD TDK C3225X7R1C106M
C5	22µF ±10%, 6.3V X5R ceramic capacitor (1206) Taiyo Yuden JMK316BJ226KL Murata GRM31CR60J226M
C15, C16, C24	10µF ±20%, 25V X5R ceramic capacitors (1210) TDK C3225X5R1E106M
D1, D2	3A, 30V Schottky diodes (M-Flat) Toshiba CMS02 (TE12L,Q) Central Semiconductor
D3, D4, D5	200mA, 100V dual ultra-fast diodes (SOT23) Fairchild MMBD4148SE (top mark D4) Central Semiconductor CMPD1001S lead free (top mark L21)
L1	Low-profile 4.7µH, 3.5A inductor (2mm height) TOKO FDV0620-4R7M
L2	Low-profile 2.4µH, 2.6A inductor (1.8mm height) TOKO 1124BS-2R4M (2.4µH) Würth 744052002 (2.5µH)

Detailed Description

The MAX17113 is a multiple-output power supply designed primarily for TFT LCD panels used in monitors and TVs. It contains a step-down switching regulator to generate the logic supply rail, a step-up switching regulator to generate the source driver supply, and two charge-pump regulators to generate the gate driver supplies. Each regulator features adjustable output voltage, digital soft-start, and timer-delayed fault protection. Both the step-down and step-up regulators use a fixed-frequency current-mode control architecture. The two switching regulators are 180° out-of-phase to minimize the input ripple. The internal oscillator offers two pin-selectable frequency options (450kHz/600kHz), allowing users to optimize their designs based on the specific application requirements. In addition, the MAX17113 features a high-voltage switch-control block, a PGOOD logic block, an internal 5V linear regulator, a 1.25V reference output, well-defined power-up and power-down sequences, and thermal-overload protection. Figure 2 shows the MAX17113 functional diagram.

Step-Down Regulator

The step-down regulator consists of an internal n-channel MOSFET with gate driver, a lossless current-sense network, a current-limit comparator, and a PWM controller block. The external power stage consists of a Schottky diode rectifier, an inductor, and output capacitors. The output voltage is regulated by changing the duty cycle of the n-channel MOSFET. A bootstrap circuit that uses a 0.1µF flying capacitor between LX2 and BST provides the supply voltage for the high-side gate driver. Although the MAX17113 also includes a 10Ω (typ) low-side MOSFET, this switch is used to charge the bootstrap capacitor during startup and maintains fixed-frequency operation at light load and cannot be used as a synchronous rectifier. An external Schottky diode (D2 in Figure 1) is always required.

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Fairchild Semiconductor	408-822-2000	408-822-2102	www.fairchildsemi.com
Sumida Corp.	847-545-6700	847-545-6720	www.sumida.com
TDK Corp.	847-803-6100	847-390-4405	www.component.tdk.com
Toshiba America Electronic Components, Inc.	949-455-2000	949-859-3963	www.toshiba.com/taec

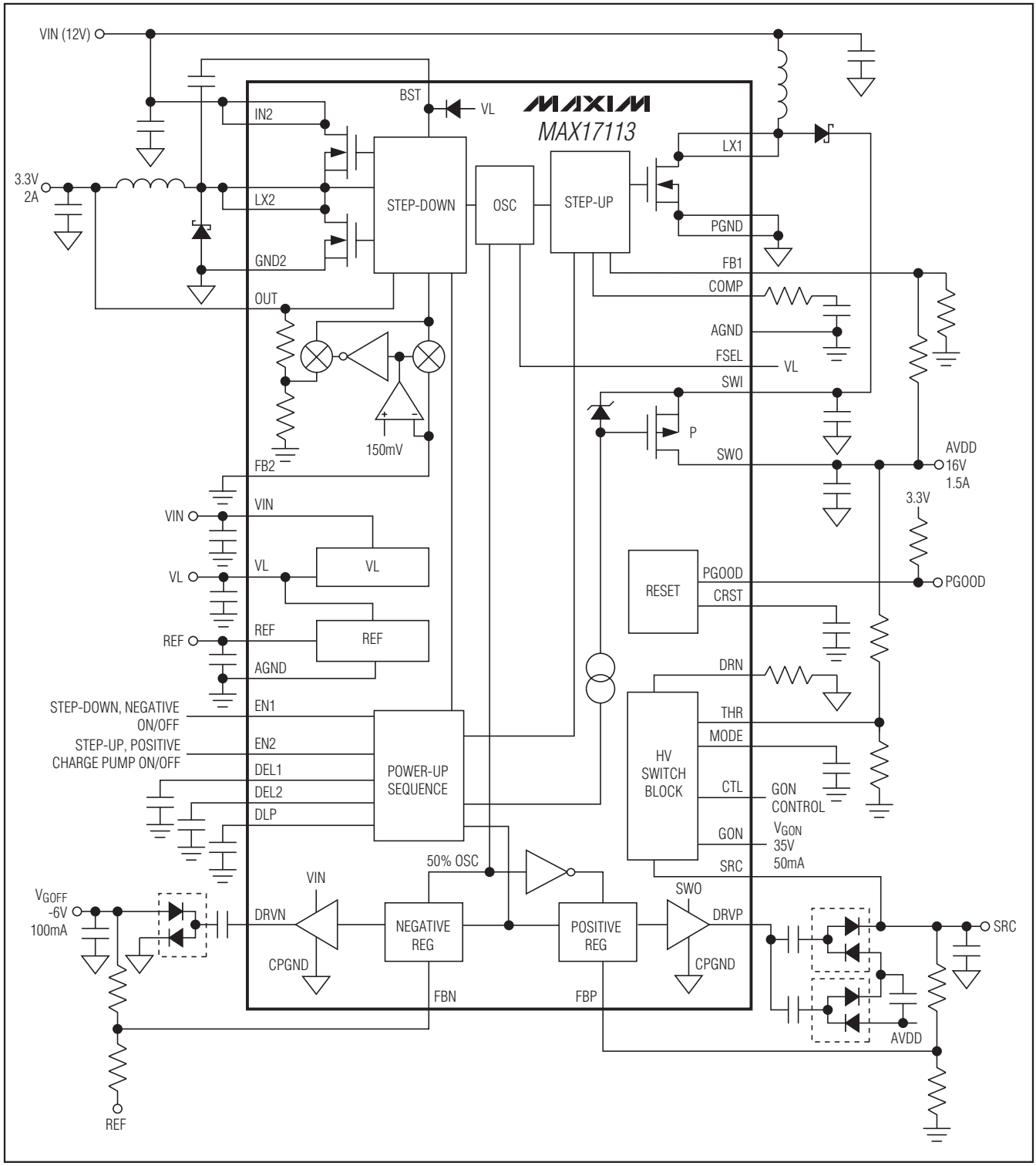


Figure 2. Functional Diagram

Low-Cost, Multiple-Output Power Supply for LCD TVs

PWM Controller Block

The heart of the PWM control block is a multi-input, open-loop comparator that sums three signals: the output-voltage signal with respect to the reference voltage, the current-sense signal, and the slope compensation. The PWM controller is a direct-summing type, lacking a traditional error amplifier and the phase shift associated with it. This direct-summing configuration approaches ideal cycle-by-cycle control over the output voltage.

When EN1 and EN2 are high, the controller always operates in fixed-frequency PWM mode. Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch until the PWM comparator changes state.

When EN1 is high and EN2 is low, the controller operates in skip mode. The skip mode dramatically improves light-load efficiency by reducing the effective frequency, which reduces switching losses. It keeps the peak inductor current at about 0.9A (typ) in an active cycle, allowing subsequent cycles to be skipped. Skip mode transitions seamlessly to fixed-frequency PWM operation as load current increases.

Current Limiting and Lossless Current Sensing

The current-limit circuit turns off the high-side MOSFET switch whenever the voltage across the high-side MOSFET exceeds an internal threshold. The actual current limit is 3A (typ).

For current-mode control, an internal lossless sense network derives a current-sense signal from the inductor DCR. The time constant of the current-sense network is not required to match the time constant of the inductor and has been chosen to provide sufficient current ramp signal for stable operation at both operating frequencies. The current-sense signal is AC-coupled into the PWM comparator, eliminating most DC output-voltage variation with load current.

Low-Frequency Operation

The step-down regulator of the MAX17113 enters into low-frequency operating mode if the voltage on OUT is below 0.8V. In the low-frequency mode, the switching frequency of the step-down regulator is 1/6 the oscillator frequency. This feature prevents potentially uncontrolled inductor current if OUT is overloaded or shorted to ground.

Dual-Mode Feedback

The step-down regulator of the MAX17113 supports both fixed and adjustable output voltages. Connect FB2 to AGND to enable the 3.3V fixed output voltage. Connect a resistive voltage-divider between OUT and AGND with the center tap connected to FB2 to adjust the output voltage. Choose RB (resistance from FB2 to AGND) to be between 5kΩ and 50kΩ, and solve for RA (resistance from OUT1 to FB1) using the equation:

$$RA = RB \times \left(\frac{V_{OUT}}{V_{FB2}} - 1 \right)$$

where V_{FB2} = 1.25V, and V_{OUT} can vary from 1.25V to 5V.

Because of FB2's (pin 17) close proximity to the noisy BST (pin 18), a noise filter is required for FB2 adjustable-mode operation. Place a 100pF capacitor from FB2 to AGND to prevent unstable operation. No filter is required for 3.3V fixed-mode operation.

Soft-Start

The step-down regulator includes a 7-bit soft-start DAC that steps its internal reference voltage from 0 to 1.25V in 128 steps. The soft-start period is 3ms (typ) and FB2 fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup (see the Step-Down Regulator Soft-Start (Heavy Load) waveforms in the *Typical Operating Characteristics*).

Step-Up Regulator

The step-up regulator employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast-transient response to pulsed loads typical of TFT LCD panel source drivers. The integrated MOSFET and the built-in digital soft-start function reduce the number of external components required while controlling inrush currents. The output voltage can be set from V_{IN} to 20V with an external resistive voltage-divider. The regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{AVDD} - V_{IN}}{V_{AVDD}}$$

where V_{AVDD} is the output voltage of the step-up regulator.

PWM Controller Block

An error amplifier compares the signal at FB1 to 1.25V and changes the COMP output. The voltage at COMP sets the peak inductor current. As the load varies, the error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope compensation signal is summed with the current-sense signal.

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceed the COMP voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the diode (D1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

Step-Up Regulator Internal p-Channel MOSFET Pass Switch

The MAX17113 includes an integrated 130mΩ high-voltage p-channel MOSFET to allow true shutdown of the step-up converter output (AVDD). This switch is typically connected in series between the step-up regulator's Schottky catch diode and its output capacitors. In addition to allowing step-up output to discharge completely when disabled, this switch also controls the startup inrush current into the step-up regulator's output capacitors.

Soft-Start

The step-up regulator includes a 7-bit soft-start DAC that steps its internal reference voltage from 0 to 1.25V in 128 steps. This DAC also controls linearly the gate of the pMOS switch, which is in between SWI and SWO, and the output AVDD goes up smoothly, and when the AVDD reaches the input voltage, the step-up regulator takes over seamlessly and the output-voltage AVDD reaches its regulation point. The soft-start period is 10ms (typ) and FB1 fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup.

Positive Charge-Pump Regulator

The positive charge-pump regulator is typically used to generate the positive supply rail for the TFT LCD gate driver ICs. The output voltage is set with an external resistive voltage-divider from its output to GND with the midpoint connected to FBP. The number of charge-pump stages and the setting of the feedback divider determine the output voltage of the positive charge-pump regulator. The charge pump includes a high-side p-channel MOSFET (P1) and a low-side n-channel MOSFET (N1) to control the power transfer as shown in Figure 3.

During the first half-cycle, N1 turns on and charges flying capacitors C20 and C21 (Figure 3). During the second half cycle, N1 turns off and P1 turns on, level shifting C20 and C21 by V_{AVDD} volts. If the voltage across C23 plus a diode drop (V_{OUT} + V_D) is smaller than the level-shifted flying capacitor voltage (V_{C20} + V_{AVDD}), charge flows from C20 to C23 until the diode (D5) turns off. The amount of charge transferred to the output is determined by the error amplifier that controls N1's on-resistance.

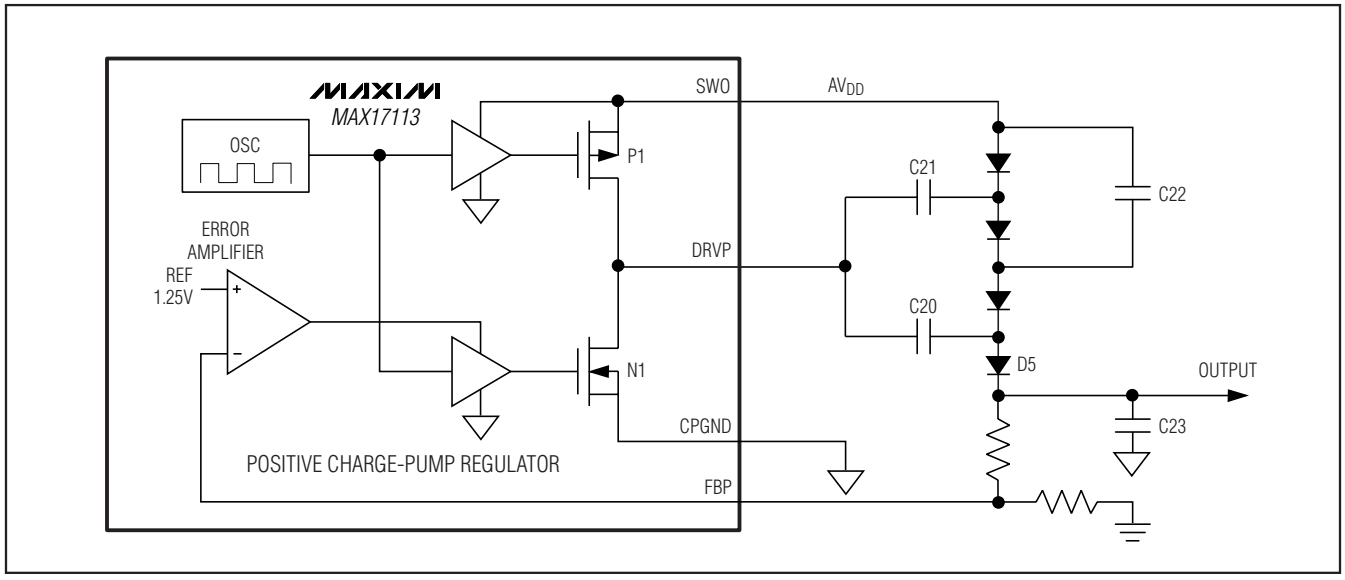


Figure 3. Positive Charge-Pump Regulator Block Diagram

Low-Cost, Multiple-Output Power Supply for LCD TVs

The positive charge-pump regulator's startup can be delayed by connecting an external capacitor from DEL2 to AGND. An internal constant-current source begins charging the DEL2 capacitor when EN2 is logic-high, and the step-down regulator reaches regulation. When the DEL2 voltage exceeds V_{REF}, the positive charge-pump regulator is enabled. Each time it is enabled, the positive charge-pump regulator goes through a soft-start routine by ramping up its internal reference voltage from 0 to 1.25V in 128 steps. The soft-start period is 3ms (typ) and FBP fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup.

Negative Charge-Pump Regulator

The negative charge-pump regulator is typically used to generate the negative supply rail for the TFT LCD gate driver ICs. The output voltage is set with an external resistive voltage-divider from its output to REF with the midpoint connected to FBN. The number of charge-pump stages and the setting of the feedback divider determine the output of the negative charge-pump regulator. The charge-pump controller includes a high-side p-channel MOSFET (P2) and a low-side n-channel MOSFET (N2) to control the power transfer as shown in Figure 4.

During the first half cycle, P2 turns on, and flying capacitor C13 charges to VIN minus a diode drop (Figure 4). During the second half cycle, P2 turns off, and N2 turns on, level shifting C13. This connects C13 in parallel with reservoir capacitor C12. If the voltage across C12 minus a diode drop is greater than the voltage across C13, charge flows from C12 to C13 until the diode (D3) turns off. The amount of charge transferred from the output is determined by the error amplifier, which controls N2's on-resistance.

The negative charge-pump regulator is enabled when EN1 is logic-high and the step-down regulator reaches regulation. Each time it is enabled, the negative charge-pump regulator goes through a soft-start routine by ramping down its internal reference voltage from 1.25V to 250mV in 102 steps. The soft-start period is 3ms (typ) and FBN fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup.

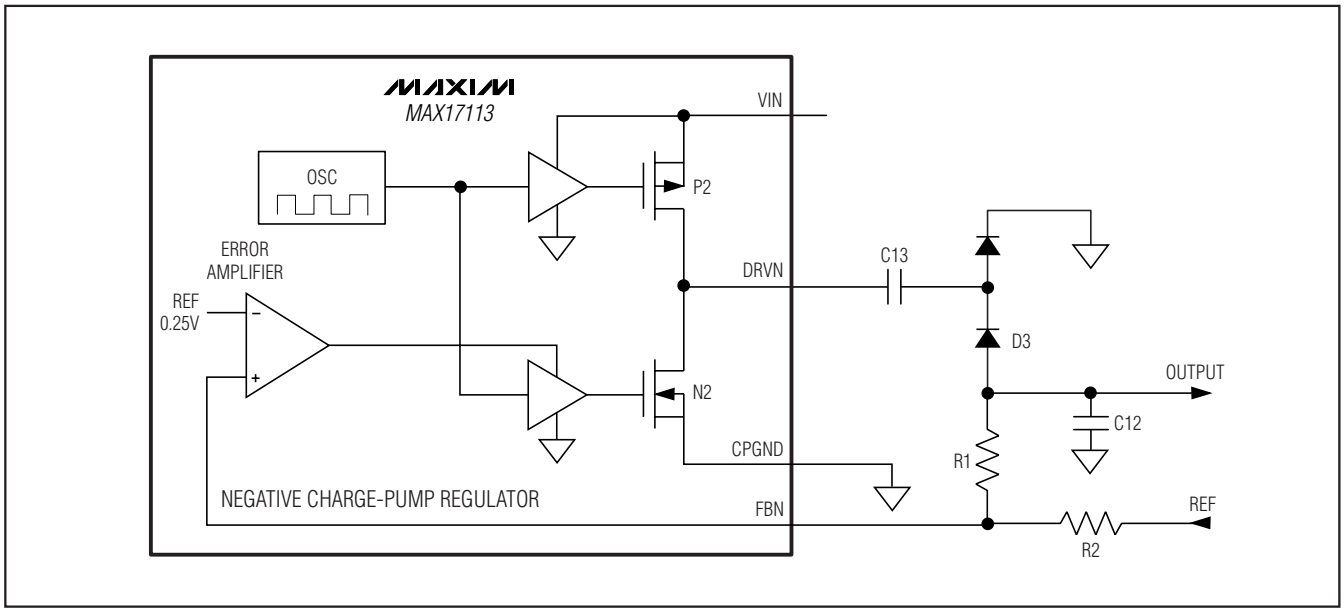


Figure 4. Negative Charge-Pump Regulator Block Diagram

High-Voltage Switch Control

The MAX17113's high-voltage switch control block (Figure 5) consists of two high-voltage p-channel MOSFETs: Q1, between SRC and GON and Q2, between GON and DRN. The switch control block is enabled when V_{DLP} exceeds V_{REF}. Q1 and Q2 are controlled by CTL and MODE. There are two different modes of operation (see the *Typical Operating Characteristics*).

Select the first mode by connecting MODE to VL. When CTL is logic-high, Q1 turns on and Q2 turns off, connecting GON to SRC. When CTL is logic-low, Q1 turns off and Q2 turns on, connecting GON to DRN. GON can then be discharged through a resistor connected between DRN and GND or AV_{DD}. Q2 turns off and stops discharging GON when V_{GON} reaches 10 times the voltage on THR.

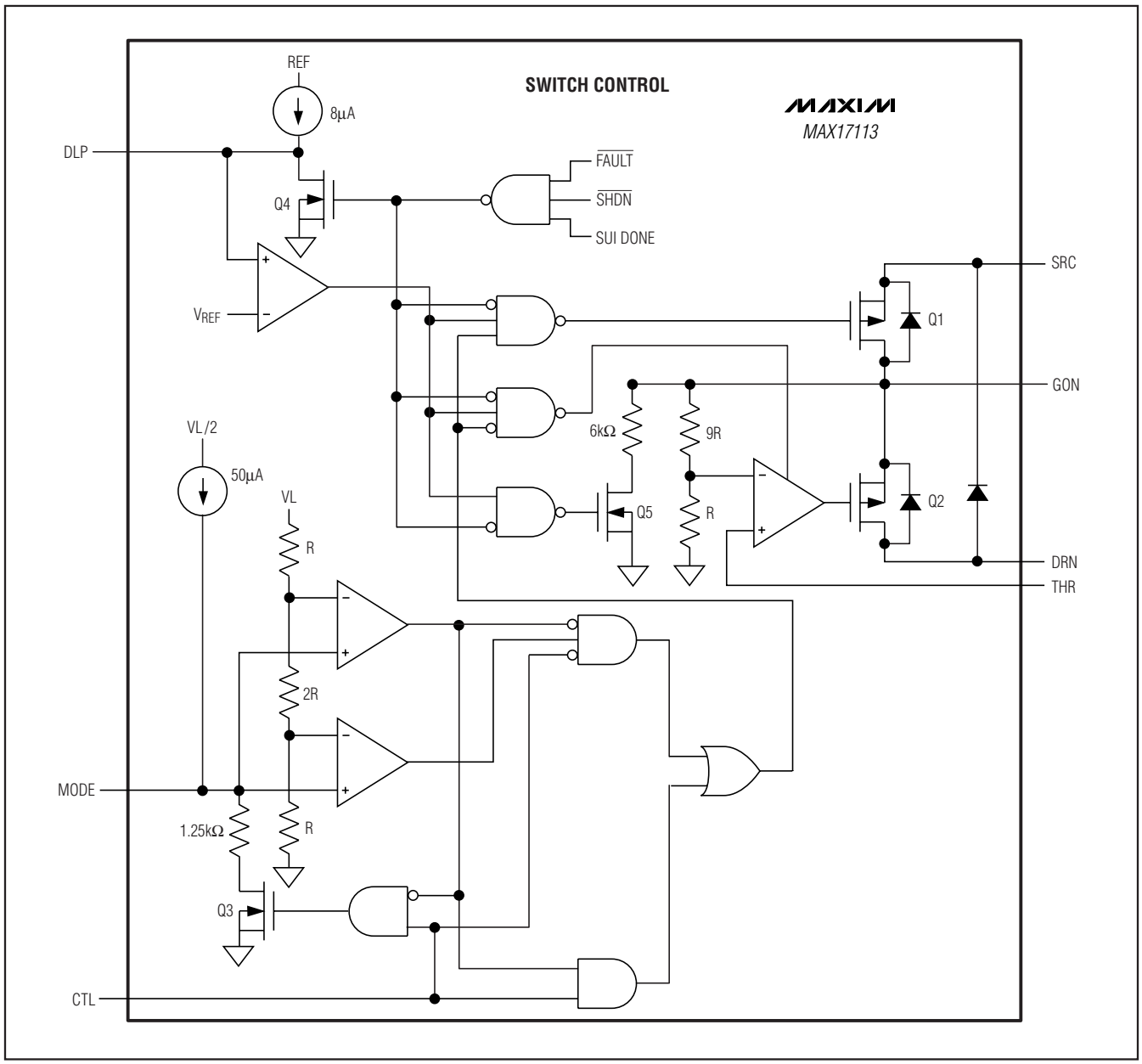


Figure 5. Switch Control

Low-Cost, Multiple-Output Power Supply for LCD TVs

When V_{MODE} is less than 0.8 x V_{VL}, the switch control block works in the second mode. The rising edge of V_{CTL} turns on Q1 and turns off Q2, connecting GON to SRC. An internal n-channel MOSFET, Q3, between MODE and AGND is also turned on to discharge an external capacitor between MODE and AGND. The falling edge of V_{CTL} turns off Q3, and an internal 50µA current source starts charging the MODE capacitor. Once V_{MODE} exceeds $V_{VL/4}$, the switch control block turns off Q1 and turns on Q2, connecting GON to DRN. GON can then be discharged through a resisor connected between DRN and PGND or AVDD. Q2 turns off and stops discharging GON when V_{GON} reaches 10 times the voltage on THR.

The switch control block is disabled and DLP is held low when EN1 or EN2 is low or the IC is in a fault state.

Linear Regulator (VL)

The MAX17113 includes an internal linear regulator. VIN is the input of the linear regulator. The input voltage range is between 8V and 16.5V. The output voltage is set to 5V. The regulator powers the internal MOSFET drivers, PWM controllers, charge-pump regulators, and logic circuitry. The total external load capability is 25mA. Bypass VL to AGND with a minimum 1µF ceramic capacitor.

Reference Voltage (REF)

The reference output is nominally 1.25V, and can source at least 50µA (see the *Typical Operating Characteristics*). VL is the input of the internal reference block. Bypass REF with a 0.22µF ceramic capacitor connected between REF and AGND.

Frequency Selection (FSEL)

The step-down regulator and step-up regulator use the same internal oscillator. The FSEL input selects the switching frequency. Table 3 shows the switching frequency based on the FSEL connection. High-frequency (600kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. Low-frequency (450kHz) operation offers the best overall efficiency at the expense of component size and board space.

Table 3. Frequency Selection

FSEL	SWITCHING FREQUENCY (kHz)
VIN	600
AGND	450

Power-Up Sequence

The step-down regulator starts up when the MAX17113's internal reference voltage (REF) is above its undervoltage lockout (UVLO) threshold and EN1 is logic-high. Once the step-down regulator reaches regulation, the FB2 fault-detection circuit and the negative charge-pump delay block are enabled. An 8µA current source at DEL1 charges C_{DEL1} linearly. The negative charge-pump regulator soft-starts when V_{DEL1} reaches V_{REF}. FBN fault detection is enabled once the negative charge-pump soft-start is done. See Figure 6.

The step-up regulator, p-channel MOSFET pass switch, and positive charge-pump startup sequence begin when the step-down regulator reaches regulation and EN2 is logic-high. An 8µA current source at DEL2 charges C_{DEL2} linearly and the positive charge pump is enabled when V_{DEL2} reaches V_{REF}. When the positive charge pump is in regulation, an 8µA current source charges C_{DLP} linearly and when V_{DLP} reaches V_{REF}, the high-voltage switch is enabled and GON can be controlled by CTL.

The FB1 fault-detection circuit is enabled after the step-up regulator reaches regulation, and similarly the FBP fault-detection circuit is enabled after the positive charge pump reaches regulation. For nondelayed startups, capacitors can be omitted from DEL1, DEL2, and DLP. When their current sources pull the pins above their thresholds, the associated outputs start.

Power-Down Control

The MAX17113 disables the step-up regulator, positive-charge-pump regulator input switch control block, delay block, and high-voltage switch control block when EN2 is logic-low, or when the fault latch is set. The step-down regulator and negative charge-pump regulator are disabled only when EN1 is logic-low or when the fault latch is set.

Fault Protection

During steady-state operation, if any output of the four regulators (step-down regulator, step-up regulator, positive charge-pump regulator, and negative charge-pump regulator) does not exceed its respective fault-detection threshold, the MAX17113 activates an internal fault timer. If any condition or the combination of conditions indicates a continuous fault for the fault timer duration (50ms, typ), the MAX17113 triggers a non-latching output undervoltage fault. After triggering, the MAX17113 turns off for 160ms (typ) and then restarts according to the EN1 and EN2 logic states. If, after restarting, another 50ms fault timeout occurs, the MAX17113 shuts down for 160ms again, and then restarts. The restart sequence is repeated 3 times and after the 50ms fault timeout, the MAX17113 shuts down and latches off. Once the fault condition is removed, toggle either EN1 or EN2, or cycle the input voltage to clear the fault latch and restart the supplies.

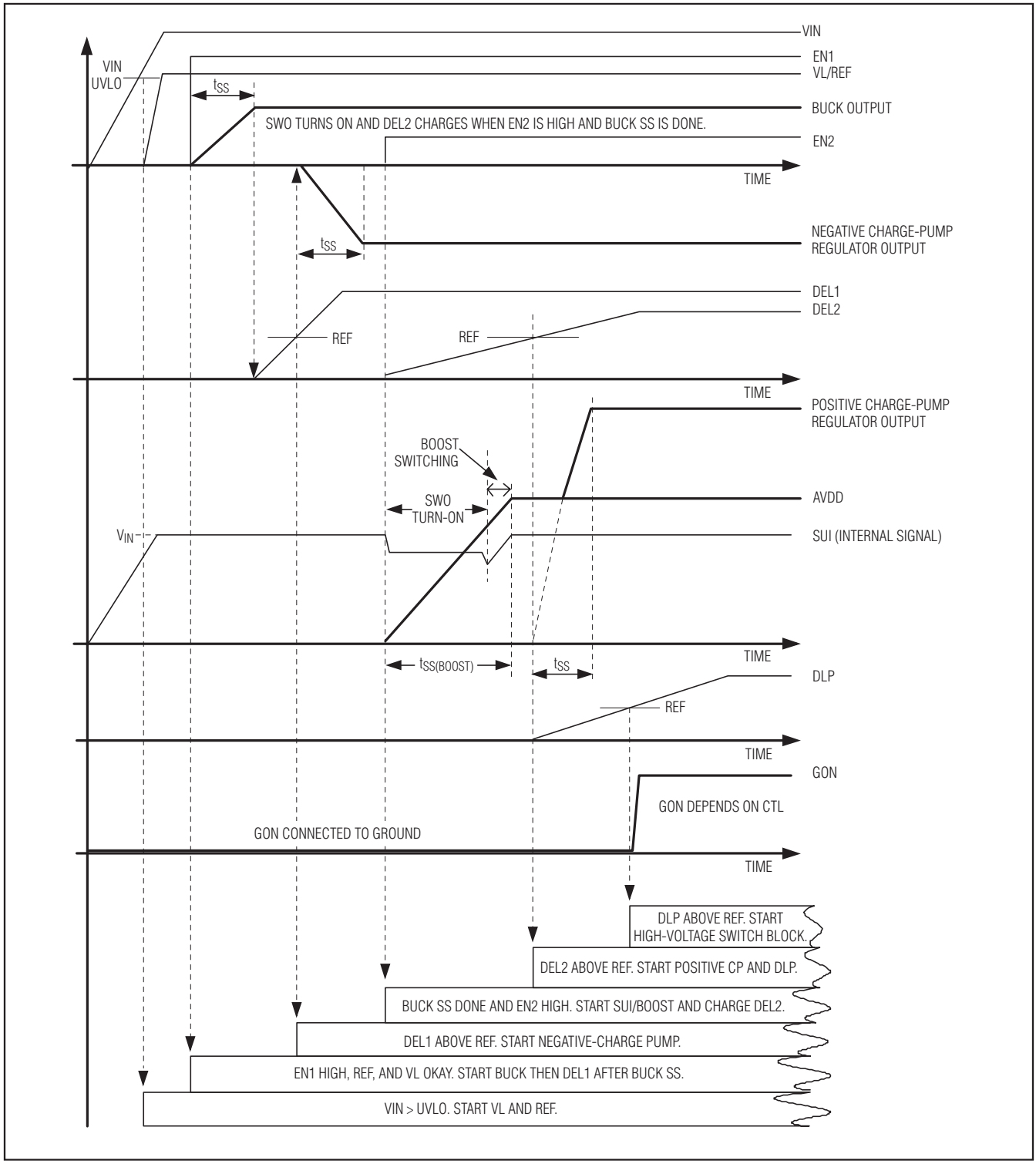


Figure 6. Startup Sequence

Low-Cost, Multiple-Output Power Supply for LCD TVs

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the MAX17113. When the junction temperature exceeds T_J = +160°C, a thermal sensor immediately activates the fault protection that shuts down all the outputs except the reference and latches off, allowing the device to cool down. Once the device cools down by at least approximately 15°C, cycle the input voltage to clear the fault latch and restart the MAX17113.

The thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Design Procedure

Step-Down Regulator

Inductor Selection

Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant, LIR, which is the ratio of peak-to-peak inductor ripple current to DC load current. A higher LIR value allows smaller inductance, but results in higher losses and higher ripple. A good compromise between size and losses is typically found at about 20% to 50% ripple-current to load-current ratio (LIR):

$$L_{OUT} = \frac{V_{OUT} \times (V_{IN2} - V_{OUT})}{V_{IN2} \times f_{SW} \times I_{OUT(MAX)} \times LIR}$$

where $I_{OUT(MAX)}$ is the maximum DC load current, and the switching frequency f_{SW} is 600kHz when FSEL is connected to VL or 450kHz when FSEL is connected to AGND. The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, but they also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values increase efficiency, but at some point resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels.

The inductor's saturation current must exceed the peak inductor current. The peak current can be calculated by:

$$I_{OUT\_RIPPLE} = \frac{V_{OUT} \times (V_{IN2} - V_{OUT})}{f_{SW} \times L_{OUT} \times V_{IN2}}$$

$$I_{OUT\_PEAK} = I_{OUT(MAX)} + \frac{I_{OUT\_RIPPLE}}{2}$$

The inductor's DC resistance should be low for good efficiency. Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice. Shielded-core geometries help keep noise, EMI, and switching waveform jitter low.

Considering the typical operating circuit in Figure 1, the maximum load current ($I_{OUT(MAX)}$) is 2A with a 3.3V output and a typical 12V input voltage. Choosing an LIR of 0.4 at this operating point:

$$L_{OUT} = \frac{3.3V \times (12V - 3.3V)}{12V \times 600kHz \times 2A \times 0.4} \approx 5.0\mu H$$

At that operating point, the ripple current and the peak current are:

$$I_{OUT\_RIPPLE} = \frac{3.3V \times (12V - 3.3V)}{600kHz \times 5.0\mu H \times 12} \approx 0.8A$$

$$I_{OUT\_PEAK} = 2A + \frac{0.8A}{2} = 2.4A$$

Input Capacitors

The input filter capacitors reduce peak currents drawn from the power source and reduce noise and voltage ripple on the input caused by the regulator's switching. They are usually selected according to input ripple current requirements and voltage rating, rather than capacitance value. The input voltage and load current determine the RMS input ripple current (I_{RMS}):

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} \times (V_{IN2} - V_{OUT})}}{V_{IN2}}$$

The worst case is I_{RMS} = 0.5 x I_{OUT}, which occurs at V_{IN2} = 2 x V_{OUT}.

For most applications, ceramic capacitors are used because of their high ripple current and surge current capabilities. For optimal circuit long-term reliability, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current corresponding to the maximum load current.

Output Capacitor Selection

Since the MAX17113's step-down regulator is internally compensated, it is stable with any reasonable amount of output capacitance. However, the actual capacitance and equivalent series resistance (ESR) affect the regulator's output ripple voltage and transient response. The rest of this section deals with how to determine the output capacitance and ESR needs according to the ripple-voltage and load-transient requirements.

The output-voltage ripple has two components: variations in the charge stored in the output capacitor, and the voltage drop across the capacitor's ESR caused by the current into and out of the capacitor:

$$V_{OUT\_RIPPLE} = V_{OUT\_RIPPLE(ESR)} + V_{OUT\_RIPPLE(C)}$$

$$V_{OUT\_RIPPLE(ESR)} = I_{OUT\_RIPPLE} \times R_{ESR\_OUT}$$

$$V_{OUT\_RIPPLE(C)} = \frac{I_{OUT\_RIPPLE}}{8 \times C_{OUT} \times f_{SW}}$$

where I_{OUT_RIPPLE} is defined in the *Inductor Selection* of the *Step-Down Regulator* section, C_{OUT} is the output capacitance, and R_{ESR_OUT} is the ESR of the output capacitor C_{OUT}. In Figure 1's circuit, the inductor ripple current is 0.8A. If the voltage-ripple requirement of Figure 1's circuit is ±1% of the 3.3V output, then the total peak-to-peak ripple voltage should be less than 66mV. Assuming that the ESR ripple and the capacitive ripple each should be less than 50% of the total peak-to-peak ripple, then the ESR should be less than 43mΩ and the output capacitance should be more than 5µF to meet the total ripple requirement. A 22µF capacitor with ESR (including PCB trace resistance) of 10mΩ is selected for the standard application circuit in Figure 1, which easily meets the voltage-ripple requirement.

The step-down regulator's output capacitor and ESR can also affect the voltage undershoot and overshoot when the load steps up and down abruptly. The step-down regulator's transient response is typically dominated by its loop response and the time constant of its internal integrator. However, excessive inductance or insufficient output capacitance can degrade the natural transient response. Calculating the ideal transient response of the inductor and capacitor, which assumes an ideal response from the regulator, can ensure that these components do not degrade the IC's natural response.

The ideal undershoot and overshoot have two components: the voltage steps caused by ESR, and the voltage sag and soar due to the finite capacitance and the inductor current slew rate. Use the following formulas to check if the ESR is low enough and the output capacitance is large enough to prevent excessive soar and sag.

The amplitude of the ESR step is a function of the load step and the ESR of the output capacitor:

$$V_{OUT\_ESR\_STEP} = \Delta I_{OUT} \times R_{ESR\_OUT}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle:

$$V_{OUT\_SAG} = \frac{L_{OUT} \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times \left(V_{IN(MIN)} \times D_{MAX} - V_{OUT}\right)}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value, and the output voltage:

$$V_{OUT\_SOAR} = \frac{L_{OUT} \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Keeping the full-load overshoot and undershoot less than 3% ensures that the step-down regulator's natural integrator response dominates. Given the component values in the circuit of Figure 1 and assuming a full 1.5A step load transient, the voltage step due to capacitor ESR is negligible. The voltage sag and soar are 76mV and 73mV, or a little over 1% and 2%, respectively.

Rectifier Diode

The MAX17113's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 2A Schottky diode works well in the MAX17113's step-down regulator.

Step-Up Regulator

Inductor Selection

The inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient response time, and output-voltage ripple. Physical size and cost are also important factors to be considered.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple, and therefore, reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire that increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size, but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise among circuit efficiency, inductor size, and cost.

The equations used here include a constant, LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full-load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.2 and 0.5. However, depending on the AC

characteristics of the inductor core material and ratio of inductor resistance to other power path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for smaller LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

Calculate the approximate inductor value using the typical input voltage (V_{VIN}), the maximum output current ($I_{AVDD(MAX)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate of LIR based on the above discussion:

$$L_{AVDD} = \left(\frac{V_{VIN}}{V_{AVDD}}\right)^2 \left(\frac{V_{AVDD} - V_{VIN}}{I_{AVDD(MAX)} \times f_{SW}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{VIN(MIN)}$ using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{VIN(DC,MAX)} = \frac{I_{AVDD(MAX)} \times V_{AVDD}}{V_{VIN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{AVDD\_RIPPLE} = \frac{V_{VIN(MIN)} \times \left(V_{AVDD} - V_{VIN(MIN)}\right)}{L_{AVDD} \times V_{AVDD} \times f_{SW}}$$

$$I_{AVDD\_PEAK} = I_{VIN(DC,MAX)} + \frac{I_{AVDD\_RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX17113's LX1 current limit should exceed I_{AVDD_PEAK} and the inductor's DC current rating should exceed $I_{VIN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.05Ω series resistance.

Considering the typical operating circuit in Figure 1, the maximum load current ($I_{AVDD(MAX)}$) is 1.0A with a 16V output and a typical 12V input voltage. Choosing an LIR of 0.6 and estimating efficiency of 90% at this operating point:

$$L_{AVDD} = \left(\frac{12V}{16V}\right)^2 \left(\frac{16V - 12V}{1A \times 600kHz}\right)\left(\frac{0.90}{0.6}\right) \approx 5.6\mu H$$

Using the circuit's minimum input voltage (10.8V) and estimating efficiency of 90% at that operating point:

$$I_{VIN(DC,MAX)} = \frac{1.0A \times 16V}{10.8V \times 0.9} \approx 1.64A$$

Choosing a 4.7µH inductor, the ripple current and the peak current are:

$$I_{RIPPLE} = \frac{10.8V \times (16V - 10.8V)}{4.7\mu H \times 16V \times 600kHz} \approx 1.2A$$

$$I_{PEAK} = 1.64A + \frac{1.2A}{2} \approx 2.24A$$

Output Capacitor Selection

The total output-voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's ESR:

$$V_{AVDD\_RIPPLE} = V_{AVDD\_RIPPLE(C)} + V_{AVDD\_RIPPLE(ESR)}$$

$$V_{AVDD\_RIPPLE(C)} \approx \frac{I_{AVDD}}{C_{AVDD}}\left(\frac{V_{AVDD} - V_{VIN}}{V_{AVDD} f_{SW}}\right)$$

and:

$$V_{AVDD\_RIPPLE(ESR)} \approx I_{AVDD\_PEAK} R_{ESR\_AVDD}$$

where I_{AVDD_PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output-voltage ripple is typically dominated by $V_{AVDD\_RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered. Note that all ceramic capacitors typically have large temperature coefficient and bias voltage coefficients. The actual capacitor value in circuit is typically significantly less than the stated value.

Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the input supply and reduces noise injection into the IC. Two 10µF ceramic capacitors are used in the typical operating circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance

since the step-up regulator often runs directly from the output of another regulated supply. Typically, the input capacitance can be reduced below the values used in the typical operating circuit.

Rectifier Diode

The MAX17113's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 2A Schottky diode complements the internal MOSFET well.

Output-Voltage Selection

The output voltage of the step-up regulator can be adjusted by connecting a resistive voltage-divider from the output (V_{AVDD}) to AGND with the center tap connected to FB1 (see Figure 1). Select R4 in the 10kΩ to 50kΩ range. Calculate R3 with the following equation:

$$R3 = R4 \times \left(\frac{V_{AVDD}}{V_{FB1}} - 1 \right)$$

where V_{FB1}, the step-up regulator's feedback set point, is 1.25V. Place R4 and R3 close to the IC.

Loop Compensation

Choose R_{COMP} (R5 in Figure 1) to set the high-frequency integrator gain for fast transient response. Choose C_{COMP} (C17 in Figure 1) to set the integrator zero to maintain loop stability.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{125 \times V_{VIN} \times V_{AVDD} \times C_{AVDD}}{L_{AVDD} \times I_{AVDD(MAX)}}$$

$$C_{COMP} \approx \frac{V_{AVDD} \times C_{AVDD}}{1250 \times I_{AVDD(MAX)} \times R_{COMP}}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient response waveforms.

Charge-Pump Regulators

Selecting the Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meet the output requirement.

The number of positive charge-pump stages is given by:

$$n_{POS} = \frac{V_{GON} + V_{DROPOUT} - V_{AVDD}}{V_{SWO} - 2 \times V_D}$$

where n_{POS} is the number of positive charge-pump stages, V_{GON} is the output of the positive charge-pump regulator, V_{SWO} is the supply voltage of the positive charge-pump regulators, V_D is the forward voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the regulator. Use $V_{DROPOUT}$ = 300mV.

The number of negative charge-pump stages is given by:

$$n_{NEG} = \frac{-V_{GOFF} + V_{DROPOUT}}{V_{VIN} - 2 \times V_D}$$

where n_{NEG} is the number of negative charge-pump stages and V_{GOFF} is the output of the negative charge-pump regulator.

The above equations are derived based on the assumption that the first stage of the positive charge pump is connected to V_{AVDD} and the first stage of the negative charge pump is connected to ground. Sometimes fractional stages are more desirable for better efficiency. This can be done by connecting the first stage to V_{OUT} or another available supply. If the first charge-pump stage is powered from V_{OUT}, then the above equations become:

$$n_{POS} = \frac{V_{GON} + V_{DROPOUT} - V_{OUT}}{V_{SWO} - 2 \times V_D}$$

$$n_{NEG} = \frac{-V_{GOFF} + V_{DROPOUT} + V_{OUT}}{V_{VIN} - 2 \times V_D}$$

Flying Capacitors

Increasing the capacitance of the flying capacitors (connected to DRVN and DRVP) value lowers the effective source impedance and increases the output-current capability. Increasing the capacitance indefinitely has a negligible effect on output-current capability because the internal switch resistance and the diode impedance place a lower limit on the source impedance. A 0.1µF ceramic capacitor works well in most low-current applications. The flying capacitor's voltage rating must exceed the following:

$$V_{CX} > n \times V_{SWO}$$

where n is the stage number in which the flying capacitor appears.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. With ceramic capacitors, the output-voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{OUT\_CP} \geq \frac{I_{LOAD\_CP}}{2 f_{OSC} V_{RIPPLE\_CP}}$$

Low-Cost, Multiple-Output Power Supply for LCD TVs

where C_{OUT_CP} is the output capacitor of the charge pump, I_{LOAD_CP} is the load current of the charge pump, and V_{RIPPLE_CP} is the peak-to-peak value of the output ripple.

Output-Voltage Selection

Adjust the positive charge-pump regulator's output voltage by connecting a resistive voltage-divider from the SRC output to AGND with the center tap connected to FBP (Figure 1). Select the lower resistor of divider R17 in the 10kΩ to 30kΩ range. Calculate the upper resistor, R16, with the following equation:

$$R17 = R16 \times \left(\frac{V_{GON}}{V_{FBP}} - 1 \right)$$

where V_{FBP} = 1.25V (typ).

Adjust the negative charge-pump regulator's output voltage by connecting a resistive voltage-divider from V_{GOFF} to REF with the center tap connected to FBN (Figure 1). Select R2 in the 20kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2 \times \frac{V_{FBN} - V_{GOFF}}{V_{REF} - V_{FBN}}$$

where V_{FBN} = 250mV, V_{REF} = 1.25V. Note that REF can only source up to 50µA, using a resistor less than 20kΩ for R1 results in higher bias current than REF can supply.

PCB Layout and Grounding

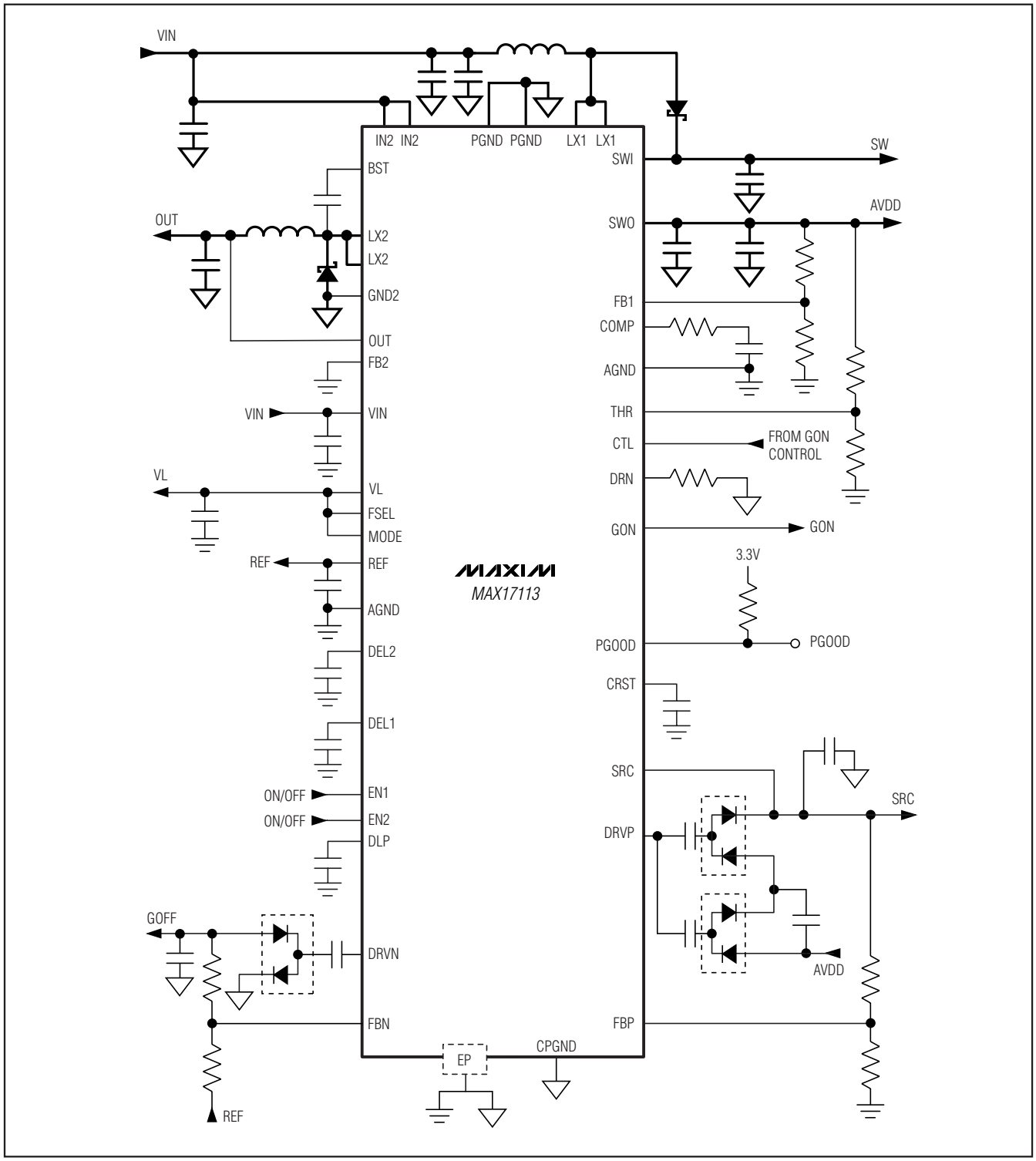
Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Minimize the area of respective high-current loops by placing each DC-DC converter's inductor, diode, and output capacitors near its input capacitors and its LX_ and GND_ pins. For the step-down regulator, the high-current input loop goes from the positive terminal of the input capacitor to the IC's IN pin, out of LX2, to the inductor, to the positive terminals of the output capacitors, reconnecting the output capacitor and input capacitor ground terminals. The high-current output loop is from the inductor to the positive terminals of the output capacitors, to the negative terminals of the output capacitors, and to the Schottky diode (D2). For the step-up regulator, the high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX1 pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.

  Create a power ground island for the step-down regulator, consisting of the input and output capacitor grounds and the diode ground. Connect all these together with short, wide traces or a small ground plane. Similarly, create a power ground island (PGND) for the step-up regulator, consisting of the input and output capacitor grounds and the PGND pin. Create a power ground island (CPGND) for the positive and negative charge pumps, consisting of the output (SRC, V_{GOFF}) capacitor grounds, and negative charge-pump diode ground. Connect CPGND ground plane to PGND together with wide traces. Maximizing the width of the power ground traces improves efficiency and reduces output-voltage ripple and noise spikes.
- Create an analog ground plane (AGND) consisting of the AGND pin, all the feedback divider ground connections, the COMP and DEL capacitor ground connections, and the device's exposed backside pad. Connect PGND and AGND islands by connecting the two ground pins directly to the exposed backside pad. Make no other connections between the PGND and AGND ground planes.
- Place all feedback voltage-divider resistors as close as possible to their respective feedback pins. The divider's center trace should be kept short. Placing the resistors far away causes their FB traces to become antennas that can pick up switching noise. Care should be taken to avoid running any feedback trace near LX1, LX2, DRVP, or DRVN.
- Place VIN pin, VL pin, and REF pin bypass capacitors as close as possible to the device. The ground connection of the VL bypass capacitor should be connected directly to the AGND pin with a wide trace.
- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
- Minimize the size of the LX1 and LX2 nodes while keeping them wide and short. Keep the LX1 and LX2 nodes away from feedback nodes (FB1, FB2, FBP, and FBN) and analog ground. Use DC traces as a shield, if necessary.

Refer to the MAX17113 evaluation kit for an example of proper board layout.

Simplified Operating Circuit



Low-Cost, Multiple-Output Power Supply for LCD TVs

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
40 TQFN-EP	T4055+1	**21-0140**