Data Sheet

MAX17793

3V to 80V, 3A, High-Efficiency, Synchronous Step-Down DC-DC Converter

FEATURES

- Reduces solution size and Cost
  - No Schottky–Synchronous Operation
  - Internal Compensation Components
  - All-Ceramic Capacitors, Compact Layout
  - Adjustable Output Range from 0.6V to 90% of V_{IN}
  - 300kHz to 1.5MHz Adjustable Frequency with External Clock Synchronization
  - EMI with symmetrical IN pins
  - 4mm x 4mm 18L-FC2QFN
- Reduces Power Dissipation
  - Peak Efficiency of 91% (V_{IN} = 48V and V_{OUT} = 5V)
  - Enhanced Light-load Efficiency with Switching Frequency Modulation (SFM) Mode
  - External Bias Input for Improved Efficiency
- Die Temperature Monitoring
- Operates Reliably in Adverse Industrial Environments
  - Built-in Hiccup-Mode Overload Protection
  - Programmable Soft-Start
  - Built-in Output-Voltage Monitoring with $\overline{\text{RESET}}$/TJ pin
  - Programmable EN/UVLO Threshold
  - Complies with CISPR32 (EN55032) Class B Conducted and Radiated Emissions
  - High Industrial -40°C to +125°C Ambient Operating Temperature Range/-40°C to +150°C Junction Temperature range

GENERAL DESCRIPTION

The MAX17793 is a high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operating over an input voltage range of 3V to 80V. The device can deliver up to 3A current and generate output voltages ranging from 0.6V up to 90% of V_{IN}.

The device features a MODE/SYNC pin that can be used to program the device in forced pulse-width modulation (PWM) or switching frequency modulation (SFM) modes of operation and to synchronize the internal clock to an external clock. The device offers an enable/ input undervoltage lockout (EN/UVLO) pin to program the desired input voltage at which the converter turns on/off. The device also has a soft-start (SS) pin to reduce inrush currents during startup. In addition, the device features a $\overline{\text{RESET}}$/TJ, pin which can be used either to monitor the status of output voltage or die temperature. The die temperature monitor allows the user to directly measure the silicon die temperature instead of relying on theoretical estimation, thus enabling robust, reliable power supply design.

APPLICATIONS

- Industrial, Avionics and Heavy Equipment
- Factory and Building Automation
- Motor Control
- General Purpose Power Supply

SIMPLIFIED APPLICATION DIAGRAM

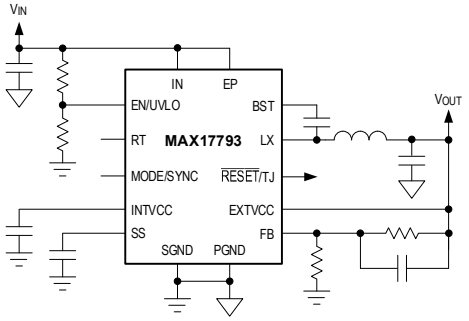

Figure 1. Typical Application Circuit

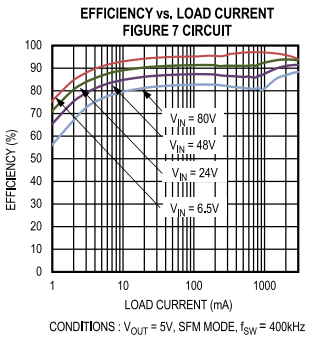

Figure 2. Efficiency vs load current

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/23	Initial Release	—
1	12/23	Updated Current limit and Switching frequency specifications in the *Electrical Characteristics* table, *Overcurrent Protection* section, and the *Typical Application Circuit*	4, 5, 20, 27

SPECIFICATIONS

Table 1. Electrical Characteristics

(V_{IN} = 24V, $V_{EN/UVLO}$ = 24V, C_{INTVCC} = 2.2µF, V_{SGND} = V_{PGND} = $V_{MODE/SYNC}$ = V_{EXTVCC} = 0V, V_{FB} = 0.64V, LX = SS = $\overline{RESET}$/TJ = R_{RT} = Open, V_{BST} to V_{LX} = 1.8V, T_A = -40°C to 125°C. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.[1])

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)						
Input Voltage Range	V_{IN}		3		80	V
Input Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V (Shutdown mode)		4.5	14	µA
No Load IN Pin Current (See *Figure 7*)	I_{IN_SFM}	MODE/SYNC = Open, V_{IN} = 48V		31		µA
	I_{IN_PWM}	$V_{MODE/SYNC}$ = 0V, V_{IN} = 48V		12.5		mA
Input UVLO	$V_{IN\_UVLO\_R}$	V_{IN} rising	2.7	2.8	2.9	V
	$V_{IN\_UVLO\_F}$	V_{IN} falling	2.45	2.55	2.65	
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.22	1.25	1.28	V
EN/UVLO Threshold	V_{ENF}	$V_{EN/UVLO}$ falling	1.12	1.15	1.18	V
EN/UVLO Input Leakage Current	I_{EN}	$V_{EN/UVLO}$ = 0V, T_A = +25°C	-100	0	+100	nA
LINEAR REGULATORS (INTVCC, EXTVCC)						
INTVCC Output Voltage Range	V_{INTVCC}	3 ≤ V_{IN} ≤ 80V, I_{INTVCC} = 1mA	1.74	1.8	1.86	V
		V_{IN}=3V, 1mA ≤ I_{INTVCC} ≤ 20mA	1.74	1.8	1.86	
		2.35 ≤ V_{EXTVCC} ≤ 24V, I_{INTVCC} = 1mA	1.74	1.8	1.86	
INTVCC Undervoltage Threshold	V_{INTVCC_UVR}	V_{INTVCC} rising	1.61	1.64	1.69	V
	V_{INTVCC_UVF}	V_{INTVCC} falling	1.545	1.58	1.625	
EXTVCC Voltage Range	V_{EXTVCC}		2.35		25.5	V
EXTVCC Switchover Threshold	V_{EXTVCC_UVR}	V_{EXTVCC} rising	2.25	2.3	2.35	V
	V_{EXTVCC_UVF}	V_{EXTVCC} falling	2.15	2.2	2.25	

(V_{IN} = 24V, $V_{EN/UVLO}$ = 24V, C_{INTVCC} = 2.2µF, V_{SGND} = V_{PGND} = $V_{MODE/SYNC}$ = V_{EXTVCC} = 0V, V_{FB} = 0.64V, LX = SS = $\overline{RESET}$/TJ = R_{RT} = Open, V_{BST} to V_{LX} = 1.8V, T_A = -40°C to 125°C. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.[1])

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
HIGH-SIDE AND LOW-SIDE MOSFETS						
High-Side nMOS On-Resistance	R_{DS-ONH}	I_{LX} = 1A, sourcing		80	150	mΩ
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 1A, sinking		40	80	mΩ
LX Leakage Current	I_{LX_LKG}	V_{IN} = 80V, V_{LX} = (V_{PGND} +1)V to (V_{IN} -1)V, T_A = +25°C, V_{EN} = 0	-5		+2	µA
SOFT-START (SS)						
Charging Current	I_{SS}	V_{SS} = 0.3V	4.6	5	5.35	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB-REG}		0.592	0.598	0.604	V
FB Input Bias Current	I_{FB}	V_{FB} = 1V, T_A = +25°C	-50		+50	nA
MODE SELECTION AND EXTERNAL CLOCK SYNCHRONIZATION (MODE/SYNC)						
MODE Threshold	V_{M-SFM}	SFM Mode	1.3			V
	V_{M-PWM}	PWM Mode			0.5	
SYNC Frequency Capture Range	f_{SYNC}	f_{SW} set by R_{RT}[2]	1.1 x f_{SW}		1.4 x f_{SW}	kHz
SYNC High Pulse Width	t_{SYNC_H}		100			ns
SYNC Low Pulse Width	t_{SYNC_L}		100			ns
SYNC Threshold	V_{IH}		1.3			V
	V_{IL}				0.5	
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$		4.5	5.3	6.1	A
Valley Current-Limit Threshold	$I_{VALLEY-LIMIT}$	SFM Mode	0	70	200	mA
		PWM Mode	-2.4	-3	-3.45	A

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PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
SWITCHING FREQUENCY (RT)						
Switching Frequency	f_{SW}	R_{RT} = 102kΩ	280	300	320	kHz
		R_{RT} = 16.9kΩ	1330	1450	1570	
		R_{RT} = Open	370	400	430	
V_{FB} Hiccup Threshold	$V_{FB-HICF}$	V_{FB} falling	0.35	0.36	0.37	V
HICCUP Timeout		See Note[3]		130		ms
Minimum On-Time	t_{ON-MIN}			80	110	ns
Minimum Off-Time	$t_{OFF-MIN}$			130	150	ns
LX Dead Time	LX_{DT}			3		ns
OUTPUT VOLTAGE MONITOR AND DIE TEMPERATURE MONITOR ($\overline{RESET}$/TJ)						
$\overline{RESET}$ Output Level Low	$V_{\overline{RESETL}}$	$I_{\overline{RESET}}$ = 10mA			0.6	V
$\overline{RESET}$ Output leakage Current	$I_{\overline{RESETLKG}}$	T_A = T_J = 25°C $V_{\overline{RESET}}$ = 5V	-50		50	nA
FB Threshold for $\overline{RESET}$ Deassertion	V_{FB-OKR}	V_{FB} Rising	93.3	95	96.7	%
FB Threshold for $\overline{RESET}$ Assertion	V_{FB-OKF}	V_{FB} Falling	90	91.7	93.3	%
$\overline{RESET}$ Delay after FB Reaches V_{FB-OKR}				2		ms
$\overline{RESET}$ /TJ Pin Voltage	V_{T25}	T_A = +25°C; $\overline{RESET}$ /TJ = 20kΩ connected to SGND	580	595	610	mV
$\overline{RESET}$/TJ Pin Voltage Variation with respect to Die Temperature	dV_{TJ}/dt	25°C to 125°C		2		mV/°C
THERMAL SHUTDOWN (TEMPERATURE)						
Thermal Shutdown Threshold		Temperature rising		165		°C

(V_{IN} = 24V, $V_{EN/UVLO}$ = 24V, C_{INTVCC} = 2.2µF, V_{SGND} = V_{PGND} = $V_{MODE/SYNC}$ = V_{EXTVCC} = 0V, V_{FB} = 0.64V, LX = SS = $\overline{RESET}$/TJ = R_{RT} = Open, V_{BST} to V_{LX} = 1.8V, T_A = -40°C to 125°C. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.[1])

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Thermal Shutdown Hysteresis				20		°C

1 Electrical specifications are production tested at T_A = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization.

2 The maximum allowable external clock frequency is 1.5MHz.

3 See the *Overcurrent Protection (OCP)/Hiccup Mode* section for more details

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
IN to PGND	-0.3V to +85V
EN/UVLO to SGND	-0.3 to (V_{IN} + 0.3V)
LX to PGND	-0.3V to (V_{IN} + 0.3V)
EXTVCC to SGND	-14V to +26.5V
BST to PGND	-0.3V to +87V
BST to LX	-0.3V to +2.2V
BST to INTVCC	-0.3V to +85V
FB, SS, INTVCC, RT to SGND	-0.3V to +2.2V
$\overline{\text{RESET}}$/TJ, MODE/SYNC, to SGND	-0.3V to +6V
PGND to SGND	-0.3V to +0.3V
LX total RMS current	5A
Output Short-circuit duration	Continuous
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 52.6mW/°C above +70°C)	4210mW
Operating Temperature Range[1]	-40°C to 125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

[1] Junction temperature greater than +125°C degrades operating lifetimes

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

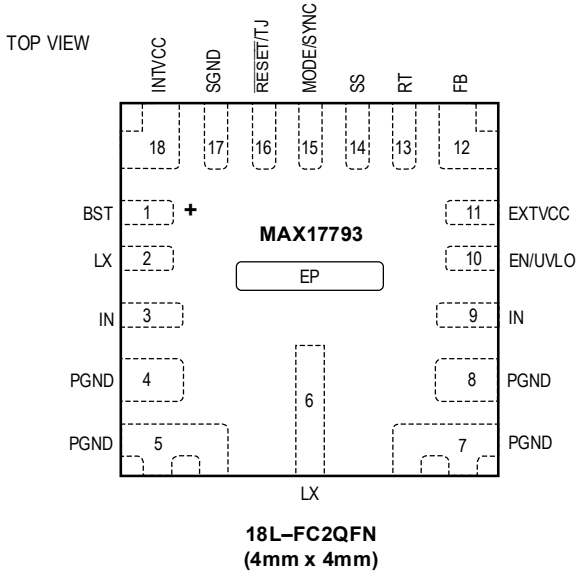


Figure 3. MAX17793 Pin Configuration

PIN DESCRIPTIONS

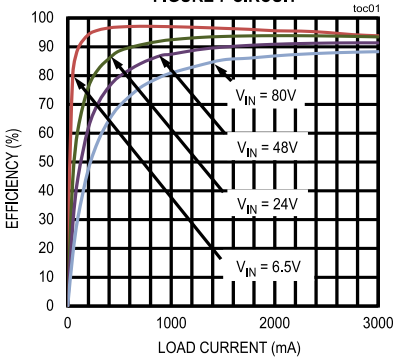
PIN	NAME	DESCRIPTION
1	BST	Boot Strap Capacitor Pin. Connect a 0.1µF ceramic capacitor between BST and LX (Pin 2).
2, 6	LX	Switching Node Pins. Connect LX (Pin 2) to the one end of the bootstrap capacitor. Connect LX (Pin 6) to the switching side of the inductor.
3, 9	IN	Power Supply Input Pins. The MAX17793 requires two 0.1µF input bypass capacitors. One 0.1µF capacitor should be placed between IN (Pin 3) and PGND (Pin 4, 5). A second 0.1µF capacitor should be placed between IN (Pin 9) and PGND (Pin 7, 8). These capacitors must be placed as close as possible to the MAX17793. The input capacitor (2 x 4.7µF or more) should be placed close to the MAX17793 across the input power traces. Connect the IN pins (3, 9) to EP using a plane. Refer to the MAX17793 evaluation board user guide for a layout example.
4, 5, 7, 8	PGND	Power Ground Pins. Connect PGND pins to the power ground plane. Refer to the MAX17793 evaluation board user guide for a layout example.
10	EN/UVLO	Enable/Undervoltage Lockout Pin. Drive the EN/UVLO pin high to enable the device. Connect to the center of the resistor-divider between IN and SGND pins to set the input voltage at which the part turns on. Pull low to disable the device.
11	EXTVCC	External Bias Input for EXT-LDO. Connect the EXTVCC pin to the converter output voltage node for output voltages ranging from 2.5V to 24V for improved efficiency.

		Connect the EXTVCC pin to the SGND pin when the EXTVCC feature is not used. See the *Linear Regulator (INTVCC and EXTVCC)* section for more details.
12	FB	Feedback Input Pin. Connect the FB pin to the center node of an external resistor divider from the output to the SGND pin to set the output voltage. See the *Adjusting Output Voltage* section for more details.
13	RT	Switching Frequency Programming Input Pin. Connect a resistor from RT to SGND pins to set the converter switching frequency between 300kHz and 1.5MHz. Leave the RT pin open for the default 400kHz frequency. See the *Setting the Switching Frequency (RT)* section for more details.
14	SS	Soft-Start Input Pin. Connect a capacitor from SS to SGND pins to set the soft-start time.
15	MODE/SYNC	Mode Selection Input/ External Clock Synchronization Input Pin. MODE/SYNC pin configures the device to operate in PWM or SFM modes of operation. Connect MODE/SYNC to SGND for constant-frequency PWM operation at all loads. Leave the MODE/SYNC pin open for SFM operation at light loads. The MODE/SYNC pin can also be used to synchronize the converter to an external clock. See the *Mode Selection and External Clock Synchronization (MODE/SYNC)* section for more details.
16	$\overline{\text{RESET}}$/TJ	Open-Drain Status Output/ Die Temperature Monitor Output Pin. This pin can be used to monitor either the status of the output voltage or the die temperature. The two functions cannot be used at the same time. Output voltage status can be monitored by connecting the $\overline{\text{RESET}}$/TJ pin to a power supply through a pull-up resistor. The $\overline{\text{RESET}}$/TJ output is driven low if FB node voltage drops below 92% of its set value. $\overline{\text{RESET}}$/TJ goes high 2ms after FB rises above 95% of its set value. Die temperature can be monitored by connecting a 20kΩ resistor from the $\overline{\text{RESET}}$/TJ pin to SGND. See the *RESET Output and Die Temperature Monitor (RESET/TJ)* section for more details.
17	SGND	Signal Ground.
18	INTVCC	1.8V Linear Regulator Output Pin. Connect a minimum of 2.2µF ceramic capacitor between INTVCC and SGND. The linear regulator does not support the external loading on the INTVCC pin.
—	EP	Exposed pad, internally connected to IN Pins (3, 9). Always connect EP to the IN pins on the PCB using a plane. Refer to the MAX17793 evaluation board user guide for a layout example.

TYPICAL PERFORMANCE CHARACTERISTICS

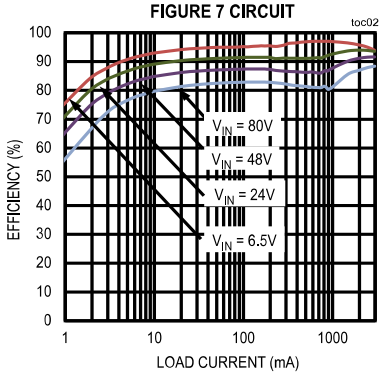
(V_{IN} = $V_{EN/UVLO}$ = 48V, C_{INTVCC} = 2.2µF, V_{SGND} = V_{PGND} = 0V, V_{EXTVCC} = V_{OUT} , C_{BST} = 0.1µF, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

EFFICIENCY vs. LOAD CURRENT
FIGURE 7 CIRCUIT



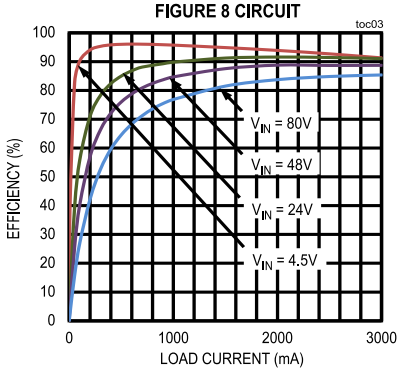
CONDITIONS: V_{OUT} = 5V, PWM MODE, f_{SW} = 400kHz

EFFICIENCY vs. LOAD CURRENT
FIGURE 7 CIRCUIT



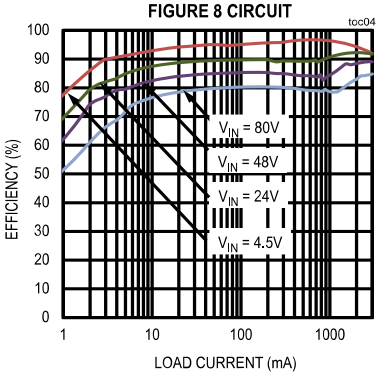
CONDITIONS: V_{OUT} = 5V, SFM MODE, f_{SW} = 400kHz

EFFICIENCY vs. LOAD CURRENT
FIGURE 8 CIRCUIT



CONDITIONS: V_{OUT} = 3.3V, PWM MODE, f_{SW} = 375kHz

EFFICIENCY vs. LOAD CURRENT
FIGURE 8 CIRCUIT



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EFFICIENCY vs. LOAD CURRENT
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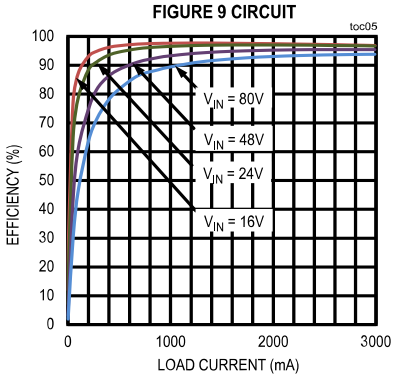
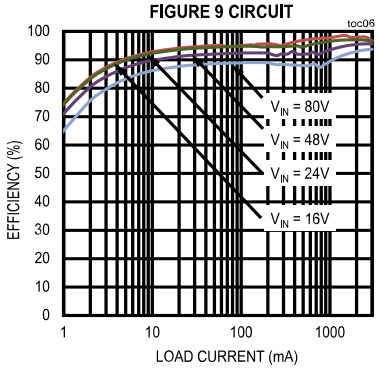


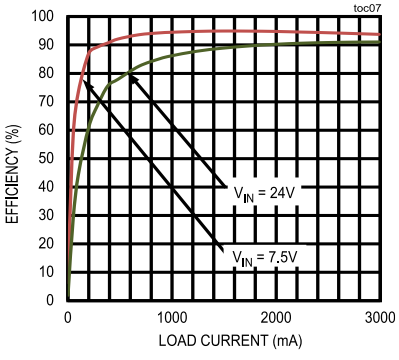
CONDITIONS: V_{OUT} = 12V, PWM MODE, f_{SW} = 400kHz

EFFICIENCY vs. LOAD CURRENT
FIGURE 9 CIRCUIT



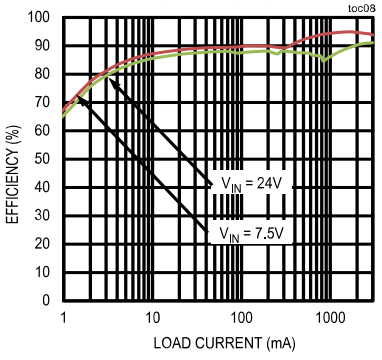
CONDITIONS: V_{OUT} = 12V, SFM MODE, f_{SW} = 400kHz

EFFICIENCY vs. LOAD CURRENT
FIGURE 10 CIRCUIT



CONDITIONS: V_{OUT} = 5V, PWM MODE, f_{SW} = 1500kHz

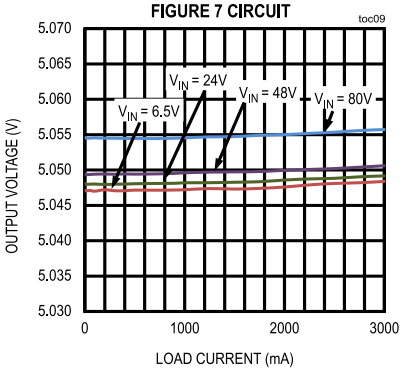
EFFICIENCY vs. LOAD CURRENT
FIGURE 10 CIRCUIT



CONDITIONS: V_{OUT} = 5V, SFM MODE, f_{SW} = 1500kHz

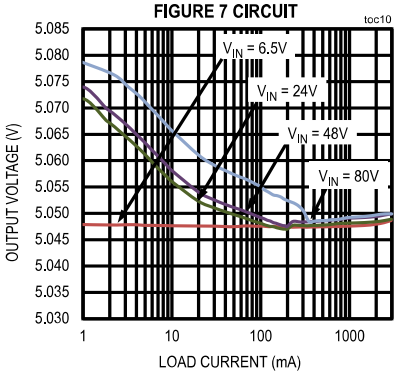
(V_{IN} = $V_{EN/UVLO}$ = 48V, C_{INTVCC} = 2.2µF, V_{SGND} = V_{PGND} = 0V, V_{EXTVCC} = V_{OUT} , C_{BST} = 0.1µF, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 7 CIRCUIT



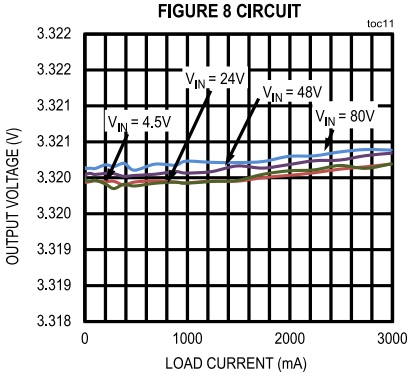
CONDITIONS: V_{OUT} = 5V, PWM MODE, f_{SW} = 400kHz

OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 7 CIRCUIT



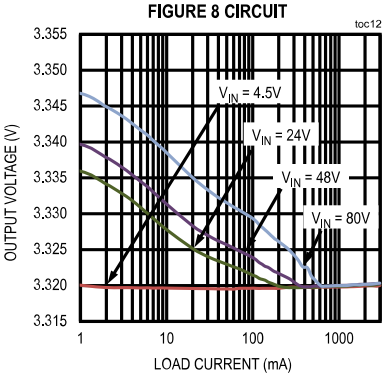
CONDITIONS : V_{OUT} = 5V, SFM MODE, f_{SW} = 400kHz

OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 8 CIRCUIT



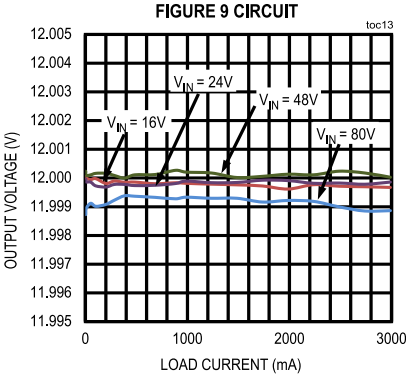
CONDITIONS: V_{OUT} = 3.3V, PWM MODE, f_{SW} = 375kHz

OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 8 CIRCUIT



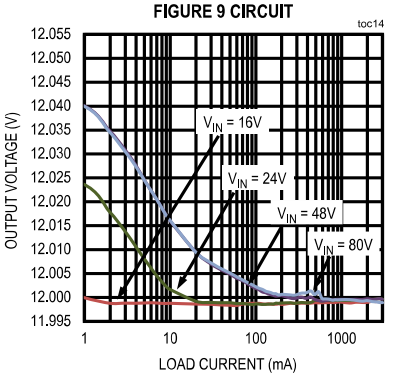
CONDITIONS: V_{OUT} = 3.3V, SFM MODE, f_{SW} = 375kHz

OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 9 CIRCUIT



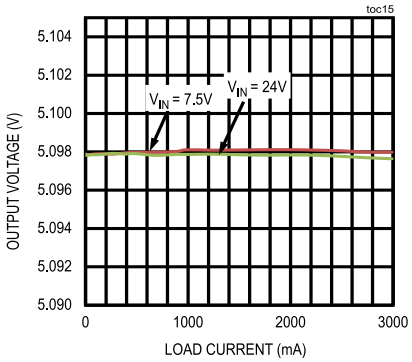
CONDITIONS: V_{OUT} = 12V, PWM MODE, f_{SW} = 400kHz

OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 9 CIRCUIT



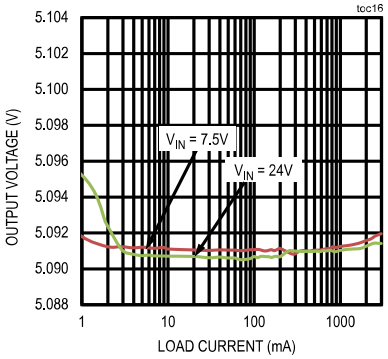
CONDITIONS: V_{OUT} = 12V, SFM MODE, f_{SW} = 400kHz

OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 10 CIRCUIT



CONDITIONS: V_{OUT} = 5V, PWM MODE, f_{SW} = 1500kHz

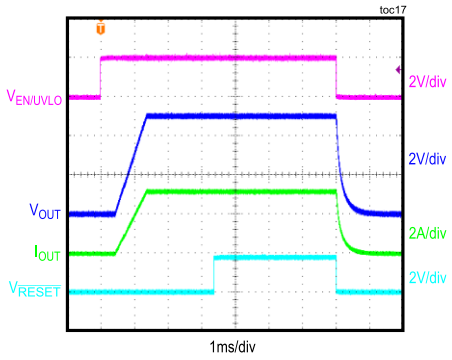
OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 10 CIRCUIT



CONDITIONS: V_{OUT} = 5V, SFM MODE, f_{SW} = 1500kHz

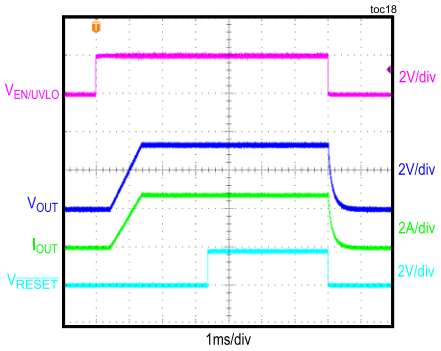
(V_{IN} = $V_{EN/UVLO}$ = 48V, C_{INTVCC} = 2.2µF, V_{SGND} = V_{PGND} = 0V, V_{EXTVCC} = V_{OUT} , C_{BST} = 0.1µF, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

STARTUP/SHUTDOWN THROUGH EN/UVLO
FIGURE 7 CIRCUIT



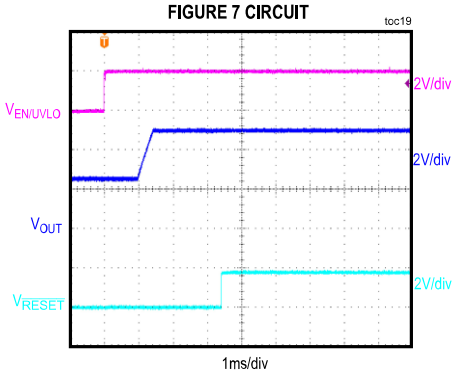
CONDITIONS: V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 3A, PWM MODE
$\overline{RESET}$/TJ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

STARTUP/SHUTDOWN THROUGH EN/UVLO
FIGURE 8 CIRCUIT



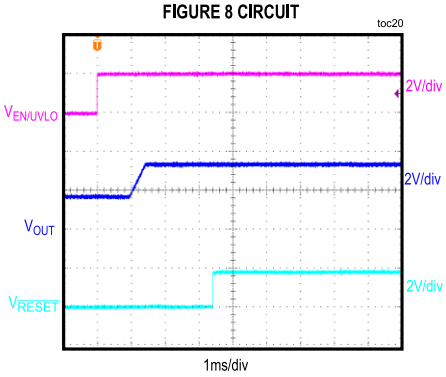
CONDITIONS: V_{IN} = 48V, V_{OUT} = 3.3V, I_{OUT} = 3A, PWM MODE
$\overline{RESET}$/TJ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

SOFT-START WITH PREBIAS
FIGURE 7 CIRCUIT



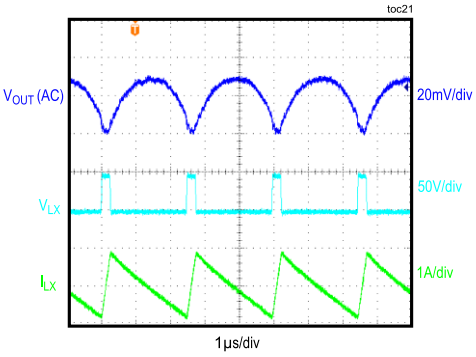
CONDITIONS: V_{IN} = 48V, V_{OUT} = 5V, NO LOAD, PWM MODE, PREBIAS = 2.5V
$\overline{RESET}$/TJ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

SOFT-START WITH PREBIAS
FIGURE 8 CIRCUIT



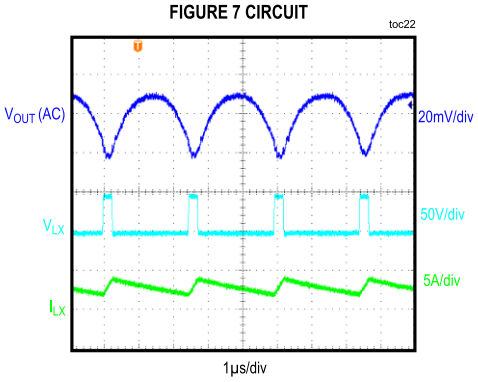
CONDITIONS: V_{IN} = 48V, V_{OUT} = 3.3V, NO LOAD, PWM MODE, PREBIAS = 1.65V
$\overline{RESET}$/TJ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

STEADY-STATE SWITCHING WAVEFORMS
FIGURE 7 CIRCUIT



CONDITIONS: V_{IN} = 48V, V_{OUT} = 5V, NO LOAD, PWM MODE

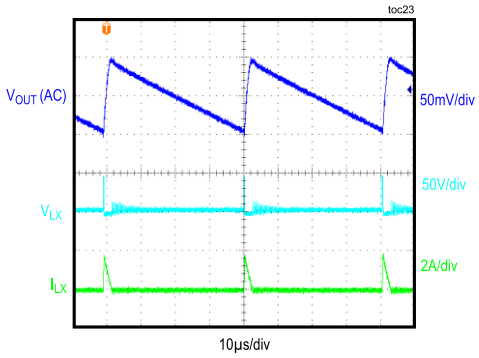
STEADY-STATE SWITCHING WAVEFORMS
FIGURE 7 CIRCUIT



CONDITIONS: V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 3A, PWM MODE

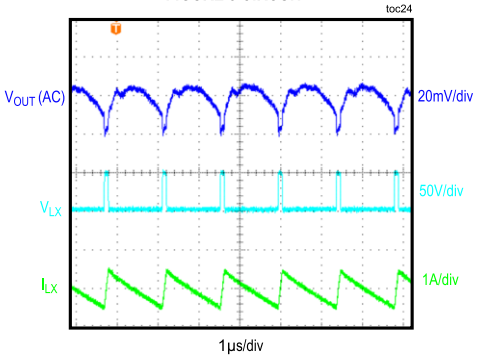
(V_{IN} = $V_{EN/UVLO}$ = 48V, C_{INTVCC} = 2.2µF, V_{SGND} = V_{PGND} = 0V, V_{EXTVCC} = V_{OUT} , C_{BST} = 0.1µF, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

STEADY-STATE SWITCHING WAVEFORMS
FIGURE 7 CIRCUIT



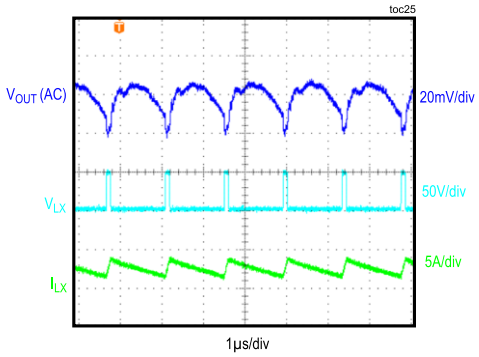
CONDITIONS: V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 0.05A, SFM MODE

STEADY-STATE SWITCHING WAVEFORMS
FIGURE 8 CIRCUIT



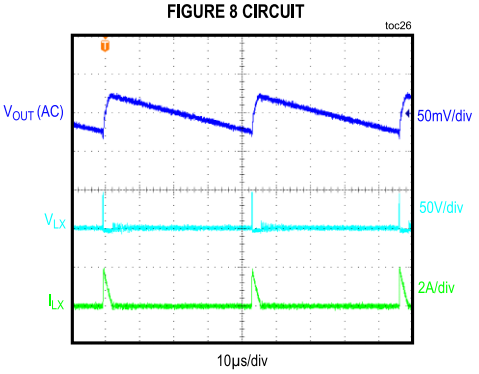
CONDITIONS: V_{IN} = 48V, V_{OUT} = 3.3V, NO LOAD, PWM MODE

STEADY-STATE SWITCHING WAVEFORMS
FIGURE 8 CIRCUIT



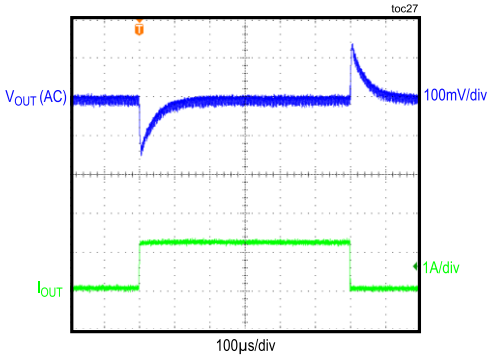
CONDITIONS: V_{IN} = 48V, V_{OUT} = 3.3V, I_{OUT} = 3A, PWM MODE

STEADY-STATE SWITCHING WAVEFORMS
FIGURE 8 CIRCUIT



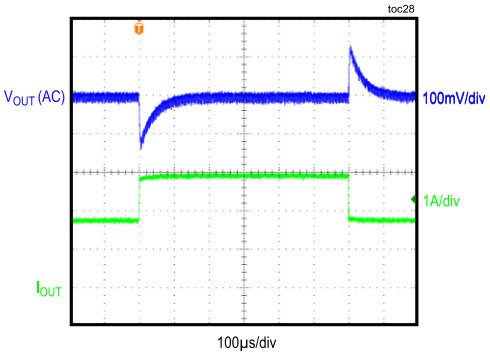
CONDITIONS: V_{IN} = 48V, V_{OUT} = 3.3V, I_{OUT} = 0.05A, SFM MODE

LOAD CURRENT STEPPED FROM 10mA TO 1.2A
FIGURE 7 CIRCUIT



CONDITIONS: V_{IN} = 48V, V_{OUT} = 5V, PWM MODE

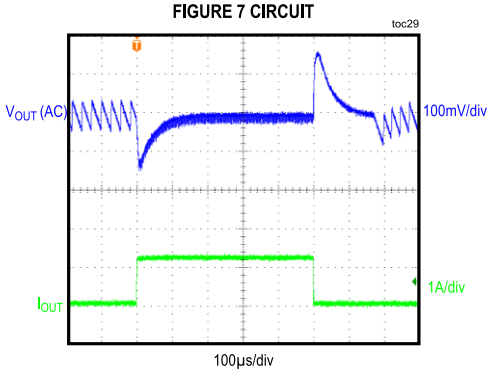
LOAD CURRENT STEPPED FROM 1.8A TO 3A
FIGURE 7 CIRCUIT



CONDITIONS: V_{IN} = 48V, V_{OUT} = 5V, PWM MODE

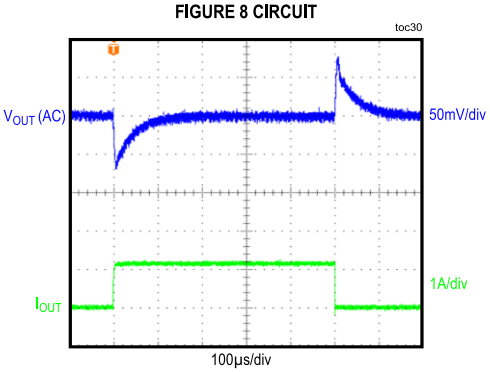
(V_{IN} = $V_{EN/UVLO}$ = 48V, C_{INTVCC} = 2.2µF, V_{SGND} = V_{PGND} = 0V, V_{EXTVCC} = V_{OUT} , C_{BST} = 0.1µF, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

LOAD CURRENT STEPPED FROM 100mA TO 1.2A
FIGURE 7 CIRCUIT



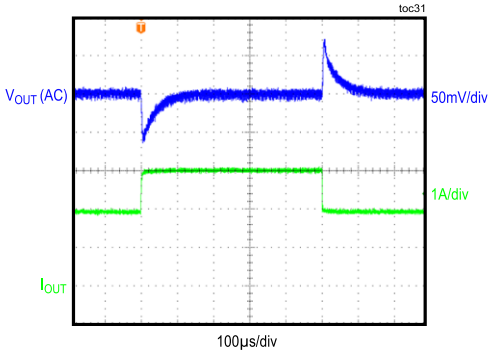
CONDITIONS: V_{IN} = 48V, V_{OUT} = 5V, SFM MODE

LOAD CURRENT STEPPED FROM 10mA TO 1.2A
FIGURE 8 CIRCUIT



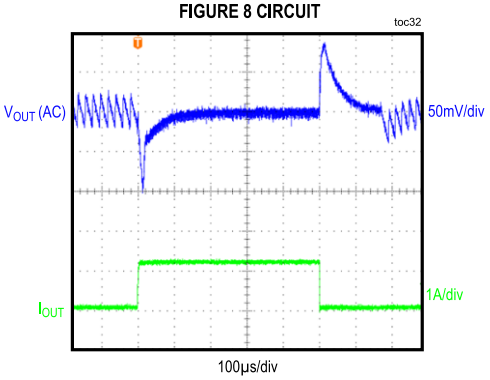
CONDITIONS: V_{IN} = 48V, V_{OUT} = 3.3V, PWM MODE

LOAD CURRENT STEPPED FROM 1.8A TO 3A
FIGURE 8 CIRCUIT



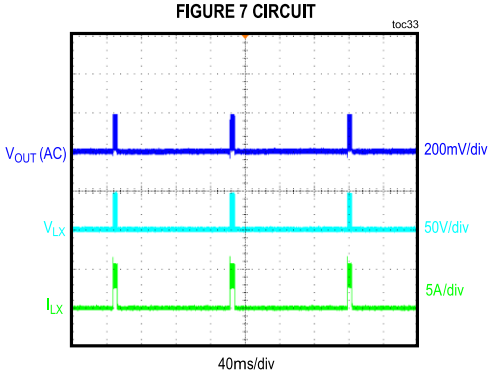
CONDITIONS: V_{IN} = 48V, V_{OUT} = 3.3V, PWM MODE

LOAD CURRENT STEPPED FROM 100mA TO 1.2A
FIGURE 8 CIRCUIT



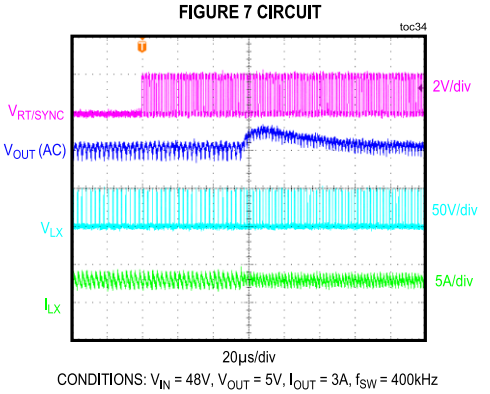
CONDITIONS: V_{IN} = 48V, V_{OUT} = 3.3V, SFM MODE

OVERLOAD PROTECTION
FIGURE 7 CIRCUIT



CONDITIONS: V_{IN} = 48V, V_{OUT} = 5V

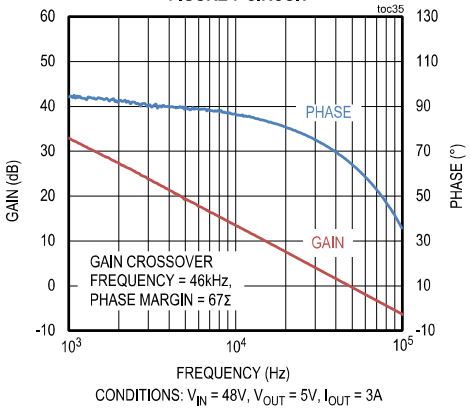
EXTERNAL CLOCK SYNCHRONIZATION
FIGURE 7 CIRCUIT



CONDITIONS: V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 3A, f_{SW} = 400kHz
EXTERNAL CLOCK FREQUENCY = 560kHz

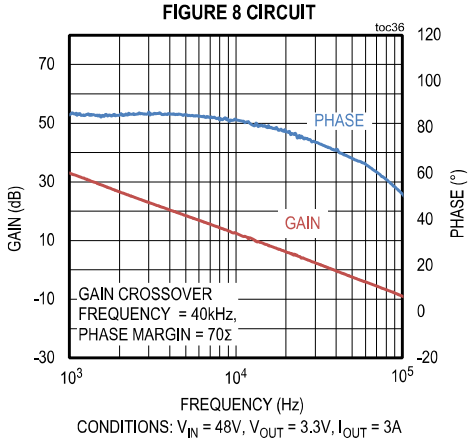
(V_{IN} = $V_{EN/UVLO}$ = 48V, C_{INTVCC} = 2.2µF, V_{SGND} = V_{PGND} = 0V, V_{EXTVCC} = V_{OUT} , C_{BST} = 0.1µF, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

BODE PLOT
FIGURE 7 CIRCUIT



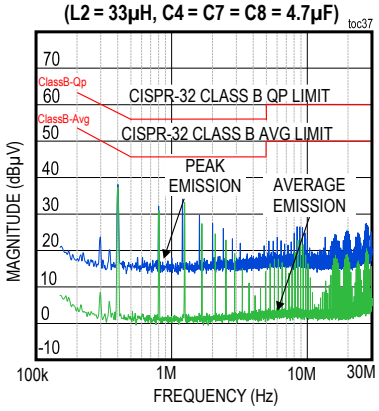
CONDITIONS: V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 3A

BODE PLOT
FIGURE 8 CIRCUIT



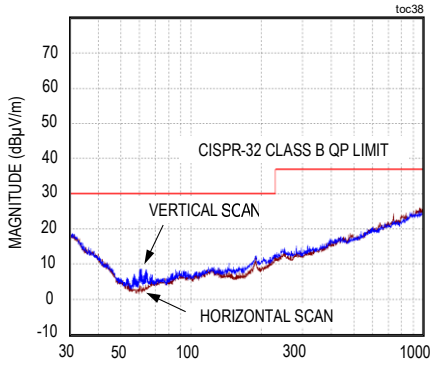
CONDITIONS: V_{IN} = 48V, V_{OUT} = 3.3V, I_{OUT} = 3A

CONDUCTED EMISSIONS PLOT
(L2 = 33µH, C4 = C7 = C8 = 4.7µF)



CONDITIONS: V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 3A
MEASURED ON MAX17793EVKITA#

RADIATED EMISSIONS PLOT



CONDITIONS : V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 3A
MEASURED ON MAX17793EVKITA#

FUNCTIONAL DIAGRAM

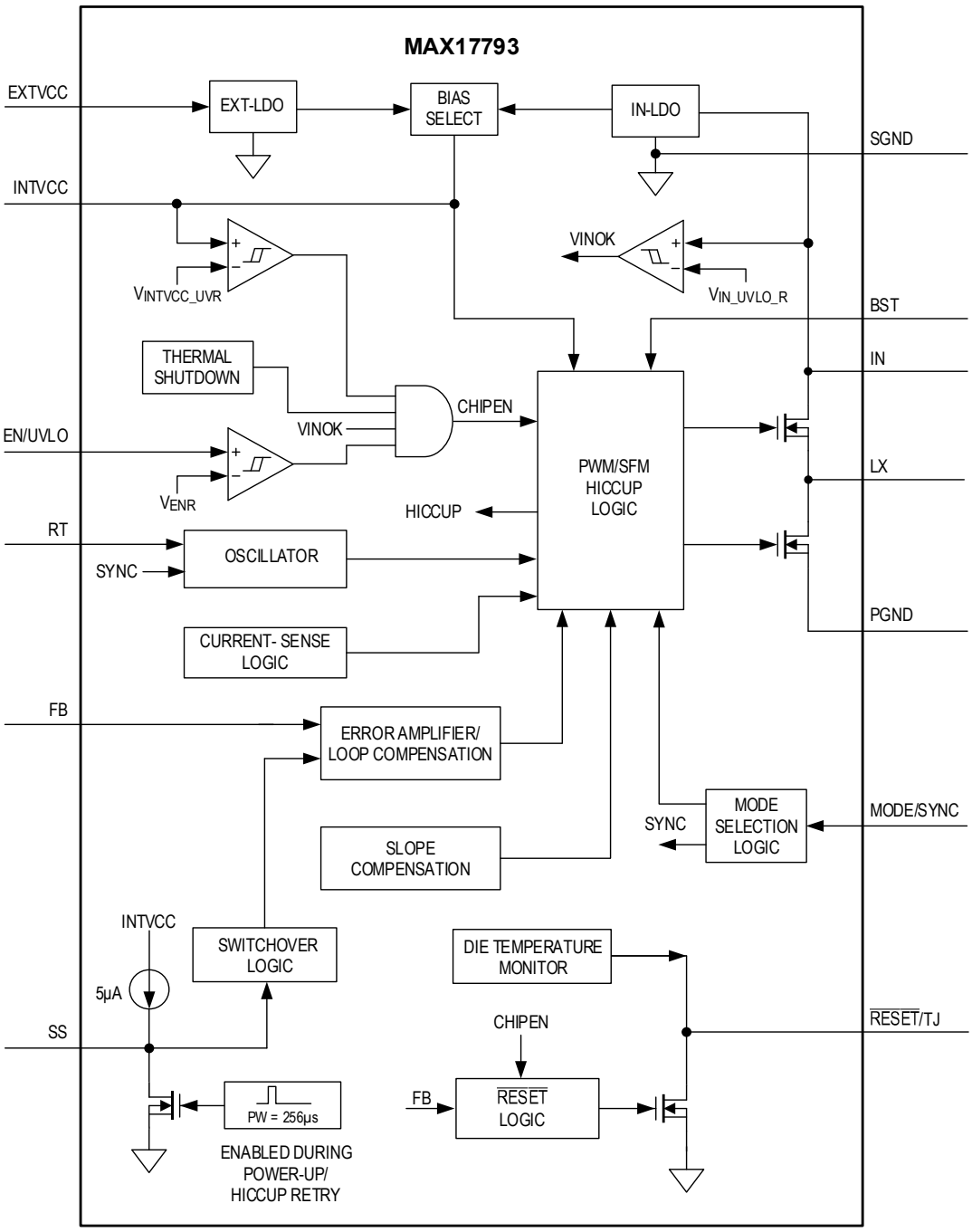


Figure 4. MAX17793 Functional diagram

DETAILED DESCRIPTION

The MAX17793 is a high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operating over an input voltage range of 3V to 80V. The device can deliver up to 3A current and generate output voltages ranging from 0.6V up to 90% of V_{IN}. Built-in compensation across the output-voltage range eliminates the need for external compensation components. The feedback-voltage regulation accuracy is ±1% over -40°C to +125°C junction temperature range.

The device features a peak-current-mode control architecture. An internal transconductance error amplifier produces an integrated error voltage at an internal node, which sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side MOSFET turns on and remains on until the appropriate or maximum duty cycle is reached or the peak current limit is detected. During the high-side MOSFET's on-time, the inductor current ramps up and stores energy in the inductor, and also provides current to the output. During the rest of the switching cycle, the high-side MOSFET turns off, and the low-side MOSFET turns on. The inductor releases the stored energy as its current ramps down and provides current to the output.

The device features a MODE/SYNC pin that can be used to program the device in forced pulse-width modulation (PWM) or switching frequency modulation (SFM) modes of operation and to synchronize the internal clock to an external clock. The device offers an enable/ input undervoltage lockout (EN/UVLO) pin to program the desired input voltage at which the converter turns on/off. The device also has a soft-start (SS) pin to reduce inrush currents during startup. In addition, the device features a $\overline{\text{RESET}}$/TJ pin, which can be used either to monitor the status of output voltage or die temperature. The die temperature monitor allows the user to directly measure the silicon die temperature instead of relying on theoretical estimation, thus enabling robust, reliable power supply design. The device offers low minimum on-time and low minimum off-time allowing the converter to operate with a wider input voltage range for a given switching frequency.

Mode Selection and External Clock Synchronization (MODE/SYNC)

The MAX17793 supports PWM and SFM modes of operation. The device enters the programmed mode of operation based on the setting of the MODE/SYNC pin. If the MODE/SYNC pin is low (< 0.5V), the device operates in a constant-frequency PWM mode at all loads. If the MODE/SYNC pin is left open (> 1.3V), the device operates in SFM mode at light loads. The device also supports on-the-fly mode change among PWM and SFM modes. When there is a state transition on the MODE/SYNC pin, the device waits for a period of 40µs (typ) and transitions into the mode based on the MODE/SYNC pin voltage at the end of 40µs (typ) period.

The MODE/SYNC pin can be used to synchronize the internal oscillator of the device to an external clock in all three modes of operation. The external clock frequency must be between 1.1 x f_{SW} and 1.4 x f_{SW}, where f_{SW} is the programmed switching frequency. When an external clock is applied to the MODE/SYNC pin, if eight or more external clock rising edges are detected in a period of 40µs (typ), the device operates in PWM mode only and the internal oscillator frequency changes to the external clock frequency at the end of the 40µs (typ) period. When the external clock is removed, the device continues to operate in PWM mode for a period of 40µs (typ) with the frequency set by RT and enters a mode based on the MODE/SYNC pin status. The external clock logic high and low pulse widths should be more than 100ns.

PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads and is useful in applications sensitive to switching frequency. However, the PWM mode of operation gives lower efficiency at light loads compared to the SFM mode of operation.

SFM Mode Operation

In SFM mode, the inductor current is discontinuous at light loads. SFM mode provides reduced frequency operation at light loads and allows the device to hibernate, enabling higher efficiency.

At light loads, the inductor peak current is forced to the SFM peak current ($I_{PK\text{-}SFM}$) by turning on the high-side MOSFET. After the inductor current reaches $I_{PK\text{-}SFM}$, the high-side MOSFET is turned off, and the low-side MOSFET is turned on.

The low-side MOSFET is turned off when the inductor current reaches zero, and the device enters a high impedance state. Consequently, the output voltage rises above the set voltage. The next switching cycle is initiated when the output voltage falls to the set voltage. As a result, the switching frequency decreases linearly as the load current reduces.

The device enters SFM mode when the inductor peak current demanded by the load is less than $I_{PK\text{-}SFM}$, and the inductor valley current reaches zero for 32 consecutive switching cycles. The device exits SFM mode when the inductor peak current demanded by the load exceeds $I_{PK\text{-}SFM}$.

For a programmed switching frequency (f_{SW}) and the inductance per the formula given in the Inductor Selection *Inductor Selection* section, at any given input voltage (V_{IN}), the SFM peak current ($I_{PK\text{-}SFM}$) is calculated as follows.

$$I_{PK\text{-}SFM} \cong 1.86 - 1.6 \times \left(\frac{V_{OUT}}{V_{IN}}\right) - 0.3 \times \left(\frac{V_{OUT}}{V_{IN}}\right)^2$$

Where

V_{OUT} = Output voltage (V).

For load currents less than half of $I_{PK\text{-}SFM}$, the output voltage ripple in SFM mode ($\Delta V_{OUT\text{-}RIPPLE}$) is calculated as follows:

$$\Delta V_{OUT\text{-}RIPPLE} = \frac{1}{2} \times \frac{L_{SEL} \times (I_{PK\text{-}SFM} - I_{OUT})^2}{C_{OUT\_SEL}} \times \left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}}\right)$$

Where

I_{OUT} = Load current (A),

C_{OUT_SEL} = Selected output capacitance (F) (calculated in the *Output Capacitor Selection* section),

L_{SEL} = Selected inductance (H) (calculated in the *Inductor Selection* section).

In SFM mode, when the device stays in a high impedance state in each switching cycle for more than 7.5µs, in eight consecutive switching cycles, the device enters hibernate mode from the subsequent switching cycle. In hibernate mode, whenever the device enters a high impedance state between two MOSFET switching cycles, most of the internal blocks are turned off to minimize quiescent current. When the hibernate period reduces below 6.5µs, the device exits hibernate mode.

SFM mode offers better efficiency compared to PWM mode at light load conditions. However, the output-voltage ripple is higher than PWM mode due to reduced switching frequency at light loads. The output capacitance may be adjusted to achieve a desired steady state output voltage ripple.

Linear Regulator (INTVCC and EXTVCC)

The MAX17793 has two internal low-dropout linear regulators, IN-LDO and EXT-LDO, that powers INTVCC. IN-LDO is powered from the IN pin, and EXT-LDO is powered from the EXTVCC pin. IN-LDO is enabled during V_{IN} power-up or EN/UVLO power-up. Only one of these two linear regulators operates depending on the voltage at the EXTVCC pin. During power-up, the switchover from IN-LDO to EXT-LDO occurs at the end of the programmed soft-start time if the EXTVCC pin voltage is greater than 2.3V (V_{EXTVCC_UVR}). Powering INTVCC from EXT-LDO reduces on-chip dissipation and increases efficiency at higher input voltages. Connect the EXTVCC pin to the converter output voltage node for output voltages ranging from 2.5V to 24V for improved efficiency. The typical INTVCC output voltage is 1.8V. Bypass INTVCC to SGND with a 2.2uF low-ESR ceramic capacitor. INTVCC powers the internal blocks, the low-side MOSFET driver and recharges the external bootstrap capacitor.

The MAX17793 starts switching only when the voltage at INTVCC is greater than 1.64V ($V_{INTVCC-UVR}$). The device employs an undervoltage lockout circuit that forces the converter off when the INTVCC voltage falls below 1.58V (V_{INTVCC_UVF}). The hysteresis of 65mV prevents chattering on power-up/power-down.

In applications where the converter output is connected to the EXTVCC pin, if the output is shorted to ground, the transfer from EXT-LDO to IN-LDO happens seamlessly without impacting the normal functionality. Connect EXTVCC pin to SGND when not in use.

Setting the Switching Frequency (RT)

The switching frequency of the device can be programmed from 300kHz to 1.5MHz by using a resistor connected from the RT pin to SGND. The switching frequency (f_{SW}) is related to the resistor (R_{RT}) connected at the RT pin by the following equation:

$$R_{RT} \cong \frac{31914}{f_{sw}} - 4.36$$

Where R_{RT} is in kΩ and f_{SW} is in kHz. Leave the RT pin open for a default switching frequency of 400kHz. See *Table 3* for R_{RT} resistor values for a few common switching frequencies.

Table 3. Switching Frequency vs. R_{RT} Resistor

Switching Frequency (kHz)	R_{RT} Resistor (kΩ)
400	Open
300	102
400	75
1500	16.9

Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage setting should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + I_{OUT(MAX)} \times \left(R_{DCR(MAX)} + R_{DS\text{-}ONL(MAX)}\right)}{1 - f_{SW(MAX)} \times t_{OFF\text{-}MIN(MAX)}} + I_{OUT(MAX)} \times \left(R_{DS\text{-}ONH(MAX)} - R_{DS\text{-}ONL(MAX)}\right)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON\text{-}MIN(MAX)}}$$

Where

V_{OUT} = Output voltage (V),

$I_{OUT(MAX)}$ = Maximum load current (A),

$R_{DCR(MAX)}$ = Worst-case DC resistance (Ω) of the inductor,

$f_{SW(MAX)}$ = Worst-case switching frequency (Hz),

$t_{OFF\text{-}MIN(MAX)}$ = Worst-case minimum switch off-time (s),

$t_{ON\text{-}MIN(MAX)}$ = Worst-case minimum switch on-time (s),

$R_{DS\text{-}ONL(MAX)}$ and $R_{DS\text{-}ONH(MAX)}$ = Worst-case on-state resistances (Ω) of low-side and high-side internal MOSFETs, respectively.

Overcurrent Protection (OCP)/Hiccup Mode

The MAX17793 provides a robust overcurrent protection (OCP) scheme that protects the device under overload and output short-circuit conditions. The OCP scheme protects the device by using a hysteretic control of the inductor current that avoids the inductor current run-away condition. In hysteretic control, whenever the inductor peak current exceeds an internal peak current limit of 5.3A ($I_{PEAK\text{-}LIMIT}$), the high-side MOSFET is turned off, and the low-side MOSFET is turned on. When the inductor current reduces by 2.36A, the low-side MOSFET is turned off, and the high-side MOSFET is turned on. In addition, if the FB node voltage drops below 0.36V (V_{FB_HICF}) due to a fault condition any time after soft-start is completed, hiccup mode is activated.

In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 130ms. Once the hiccup timeout period expires, a soft-start is attempted again. Note that when a soft-start is attempted under overload conditions if the FB node voltage does not exceed 0.41V, the device continues in hysteretic control for the total time duration of the programmed soft start time and 2ms. The hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

The device provides a valley current protection scheme that protects itself in PWM mode from large negative currents. Under strong external output bias conditions, when the inductor valley current falls below -3A ($I_{VALLEY\text{-}LIMIT}$), the device enters a high impedance state where both the MOSFETs are turned off and the inductor current reaches 0A. The device recovers from a high impedance state and starts switching when the output voltage falls below the regulation point when the external output bias is removed.

$\overline{\text{RESET}}$ Output and Die Temperature Monitor ($\overline{\text{RESET}}$/TJ)

The MAX17793 offers a $\overline{\text{RESET}}$/TJ pin that can be used to monitor either the status of the output voltage or the die temperature. The two functions cannot be used at the same time.

To monitor the status of the converter output voltage, the open-drain $\overline{\text{RESET}}$/TJ output requires an external pullup resistor to a bias supply voltage. During startup, $\overline{\text{RESET}}$/TJ goes high (high impedance) with a delay of 2ms after the feedback voltage (V_{FB}) increases above 95% ($V_{FB\text{-}OKR}$). $\overline{\text{RESET}}$/TJ is pulled low when V_{FB} drops below 92% ($V_{FB\text{-}OKF}$). $\overline{\text{RESET}}$/TJ is also pulled low during thermal shutdown or when the EN/UVLO pin goes below 1.15V (V_{ENF}).

To monitor the die temperature, connect a 20kΩ resistor from $\overline{RESET}$/TJ to SGND. The die temperature monitor feature is functional only when the output voltage is above 95% (V_{FB-OKR}) of its set point. During fault conditions like thermal shutdown, VIN UVLO, and VCC UVLO, this pin is pulled low and die temperature monitoring is not supported. Die temperature monitoring is also not supported during hibernation in SFM mode.

The die temperature (T_J) in °C is calculated as follows:

$$T_J = \frac{(V_{TJ} - V_{T25})}{(2 \times 10^{-3})} + 25$$

where
V_{TJ} is the $\overline{RESET}$/TJ pin voltage in V when the converter is loaded.

Prebiased Output

When the MAX17793 starts into a prebiased output, the high-side and the low-side switches remain turned off so that the converter does not sink current from the output. The switching of the MOSFETs commences only after the voltage at the SS pin (V_{SS}) crosses the voltage at the feedback pin (V_{FB}). V_{FB} then smoothly ramps up to V_{FB-REG} in alignment with the V_{SS}, and the output voltage reaches its target value.

Thermal-Shutdown Protection

The MAX17793 offers internal thermal shutdown protection to limit the junction temperature. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing the device to cool down. The device turns on with soft-start after the junction temperature cools down by 20°C. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown in normal operation.

APPLICATIONS INFORMATION

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source, reducing noise and voltage ripple on the input caused by the circuit's switching. The following equation defines the input capacitor RMS current requirement (I_{RMS}):

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{(V_{IN} - V_{OUT}) \times V_{OUT}}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current.

I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so

$$I_{RMS(MAX)} = \frac{I_{OUT(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where
$D = V_{OUT}/V_{IN}$ is the duty ratio of the converter,
f_{SW} = the switching frequency,
ΔV_{IN} = the allowable input voltage ripple,
η = the efficiency.

Actual derating of ceramic capacitors with DC-bias voltage must be considered while selecting the input capacitor. Derating curves are available from all major ceramic capacitor manufacturers.
In applications where the source is located distant from the device input, an appropriate electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}) and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductance value as follows:

$$L = \frac{0.55 \times V_{OUT}}{f_{SW}}$$

Where V_{OUT} and f_{SW} are nominal values and f_{SW} is in Hz. Select an inductor whose value is nearest to the value calculated by the previous formula. Select a low-loss inductor with acceptable dimensions and the lowest possible DC resistance. The saturation current rating (ISAT) of the inductor must be high enough to ensure that saturation can occur only above I_{PEAK_LIMIT}.

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are usually sized to support a step load of 40% of the maximum output current in the application, so the output-voltage deviation is contained to 3% of the output voltage. The minimum required output capacitance can be calculated as follows:

$$C_{OUT1} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \frac{0.35}{f_C}$$

where

I_{STEP} = Load current step,
$t_{RESPONSE}$ = Response time of the controller,
ΔV_{OUT} = Allowable output-voltage deviation,
f_C = Target closed-loop crossover frequency,
f_{SW} = Switching frequency.

Select f_C to be 1/9th of f_{SW} for the switching frequencies less than or equal to 500 kHz. If the switching frequency is more than 500 kHz, select f_C to be 60kHz.

The minimum required output capacitance required to meet the output voltage ripple specification ($\Delta V_{OUT\text{-}RIPPLE}$) in SFM mode at a particular load (I_O) is calculated as follows:

$$C_{OUT2} = \frac{1}{2} \times \frac{L_{SEL} \times (I_{PK\text{-}SFM} - I_O)^2}{\Delta V_{OUT\text{-}RIPPLE}} \times \left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}} \right)$$

where I_O is less than or equal to half of $I_{PK\text{-}SFM}$. See the *SFM Mode* section for more details on the calculation of $I_{PK\text{-}SFM}$.

Select the output capacitance to be the higher of C_{OUT1} and C_{OUT2}. Actual derating of ceramic capacitors with DC bias voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

Soft-Start capacitor selection

The MAX17793 implements an adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time. The selected output capacitance (C_{OUT_SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitance (C_{ss}) as follows:

$$C_{SS} \geq 33 \times 10^{-6} \times C_{OUT\_SEL} \times V_{OUT}$$

where C_{OUT_SEL} and C_{ss} are in Farad.

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{8.33 \times 10^{-6}}$$

Where C_{SS} is in Farad and t_{SS} is in seconds. For example, to program a 1ms soft-start time, an 8.2nF capacitor should be connected from the SS pin to SGND. MAX17793 offers a minimum programmable soft start time of 1ms. Note that, during start-up, the device operates at a variable switching frequency until the output voltage reaches 95% of the set output nominal voltage.

Setting the Input Undervoltage-Lockout Level

The MAX17793 offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{IN} to SGND (see *Figure 5*). Connect the center node of the divider to the EN/UVLO pin. Choose R_{UVL_TOP} to be 3.3MΩ and then calculate R_{UVL_BOTTOM} as follows:

$$R_{UVL\_BOTTOM} = \frac{R_{UVL\_TOP} \times V_{ENR}}{V_{INU} - V_{ENR}}$$

where V_{INU} is the voltage at which the device is required to turn on. It is recommended that V_{INU} is higher than 0.8 x V_{OUT} to avoid hiccups during slow power up (slower than soft start) / power down. If the EN/UVLO pin is driven from an external signal source, a series resistance of a minimum 1kΩ is recommended to be placed between the output pin of signal source and the EN/UVLO pin to reduce voltage ringing on the line.

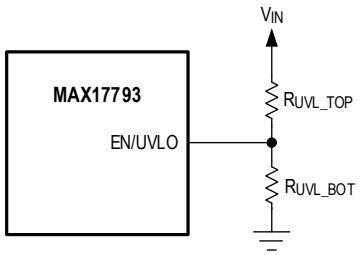


Figure 5. Setting the Input Undervoltage Lockout

Adjusting Output Voltage

Set the output voltage with a resistive voltage-divider connected from the output-voltage node (V_{OUT}) to SGND (see *Figure 6*). Connect the center node of the resistive divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R_{FB_TOP} (kΩ) from the output to the FB pin as follows:

$$R_{FB\_TOP} = \frac{200}{f_C \times C_{OUT\_SEL}}$$

where
f_C = Crossover frequency (Hz),
C_{OUT_SEL} = Actual capacitance (F) of selected output capacitor at DC-bias voltage.

Calculate resistor R_{FB_BOT} (kΩ) connected from the FB pin to SGND as follows:

$$R_{FB\_BOT} = \frac{R_{FB\_TOP} \times 0.6}{V_{OUT} - 0.6}$$

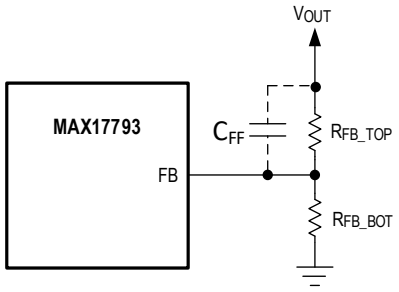


Figure 6. Setting the Output Voltage

Add a capacitor (C_{FF}) across R_{FB_TOP} when the part is used in SFM mode or when dynamic mode change is used in an application. C_{FF} is not needed when the part is used in PWM mode alone.

Calculate the capacitance (C_{FF}) value using the following equation:

$$\frac{550}{R_{FB\_TOP}} < C_{FF} < \frac{850}{R_{FB\_TOP}}$$

where
R_{FB_TOP} = top side feedback resistance (kΩ),
C_{FF} = Feedforward capacitance (pF). C_{FF} must be chosen to withstand output voltage.

Power dissipation

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{LOSS} = P_{OUT} \times \left(\frac{1}{\eta} - 1\right) - \left(I_{OUT}^2 \times R_{DCR}\right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

Where:

P_{OUT} is the output power (W),

η is the efficiency of the converter,

R_{DCR} is the DC resistance (Ω) of the inductor (see the *Typical Performance Characteristics* for more information on efficiency at typical operating conditions).

The die temperature (T_J) of the device may also be estimated at any given maximum ambient temperature (T_{AMB}) from the following equation, when the die temperature monitor ($\overline{RESET}$/TJ) feature is not used.

$$T_J = T_{AMB} + \left(\theta_{JA} \times P_{LOSS}\right)$$

Note: Junction temperatures greater than +125°C degrade operating lifetimes.

Printed Circuit Board (PCB) Layout Guidelines

All traces carrying pulsed currents must be very short and as wide as possible. The inductance of these traces must be kept to an absolute minimum due to the high di/dt of the currents. Since the inductance of a current-carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI. When routing the circuitry around the IC, the signal ground (SGND), and the power ground (PGND) for switching currents must be kept separate. PCB layout also affects the thermal performance of the design.

- Place the input capacitors as close to the IN and PGND pins as possible.
- Connect the INTVCC capacitor close to the INTVCC pin and connect the other terminal to the SGND plane.
- Place the BST capacitor close to the BST and LX pins.
- Place the inductor as close as possible to the LX pin. Minimize the length and area of the trace connection from the LX pin to the inductor.
- Place the output capacitors as close as possible to the non-switching side of the inductor.
- Place the PGND terminals of the input capacitor and output capacitor as close as possible to the PGND pins and connect them to the PGND plane.
- Place the RT resistor, SS capacitor and FB resistors as close as possible to their respective pins. Connect their other terminals to the SGND plane.
- Keep all the power and load connections short to keep inductances at minimum levels.
- Connect the PGND and SGND nodes at a point where the switching activity is at its minimum, at the negative terminal of the INTVCC bypass capacitor.
- Several thermal throughputs (vias) that connect to a large plane should be provided under IN, PGND and LX pins for efficient heat dissipation.

Refer to the MAX17793 evaluation board user guide for recommended PCB layout and routing.

TYPICAL APPLICATION CIRCUITS

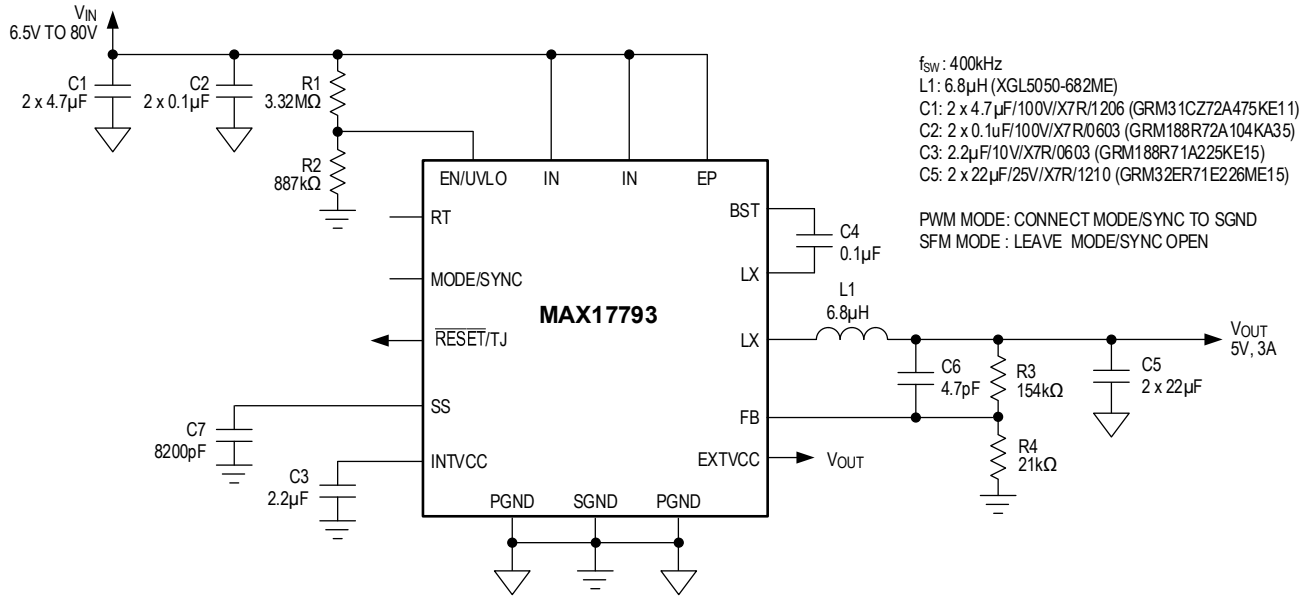


Figure 7. *5V Output with 400kHz Switching Frequency*

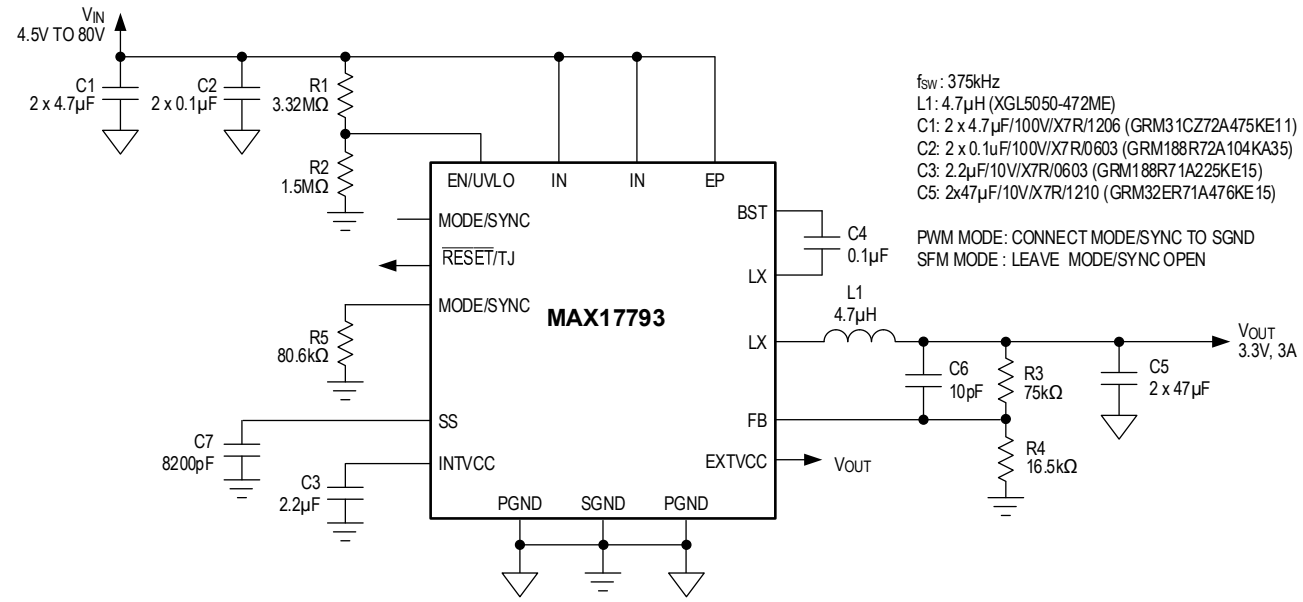


Figure 8. *3.3V Output with 400kHz Switching Frequency*

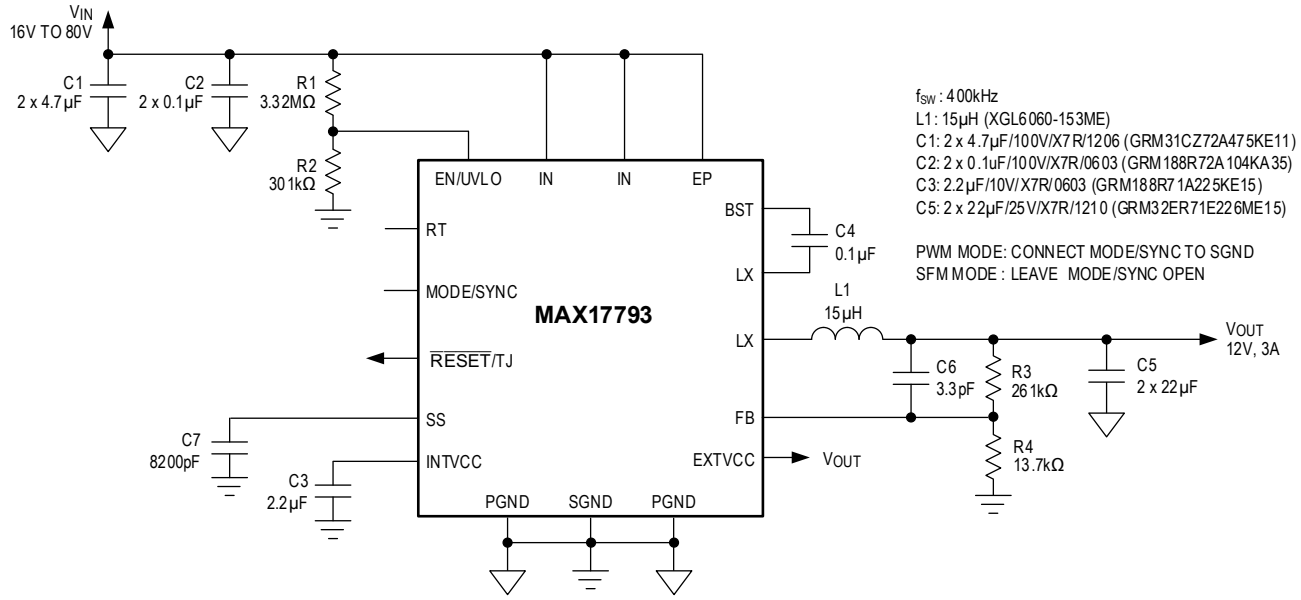


Figure 9. *12V Output with 400kHz Switching Frequency*

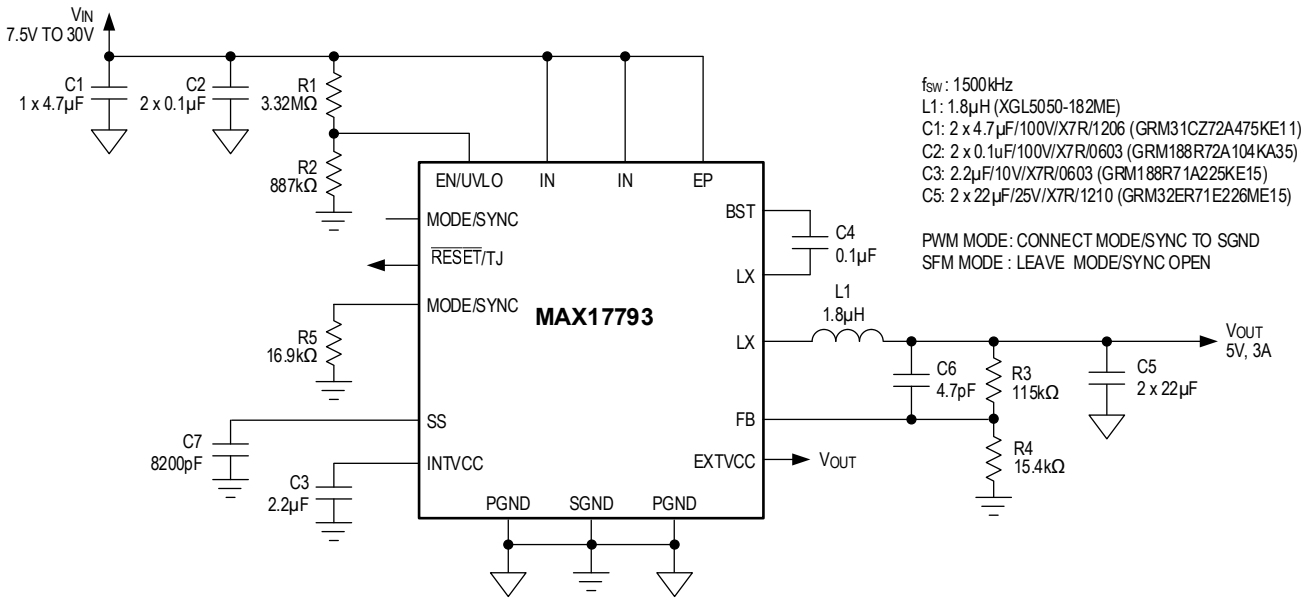


Figure 10. *5V Output with 1.5MHz Switching Frequency*

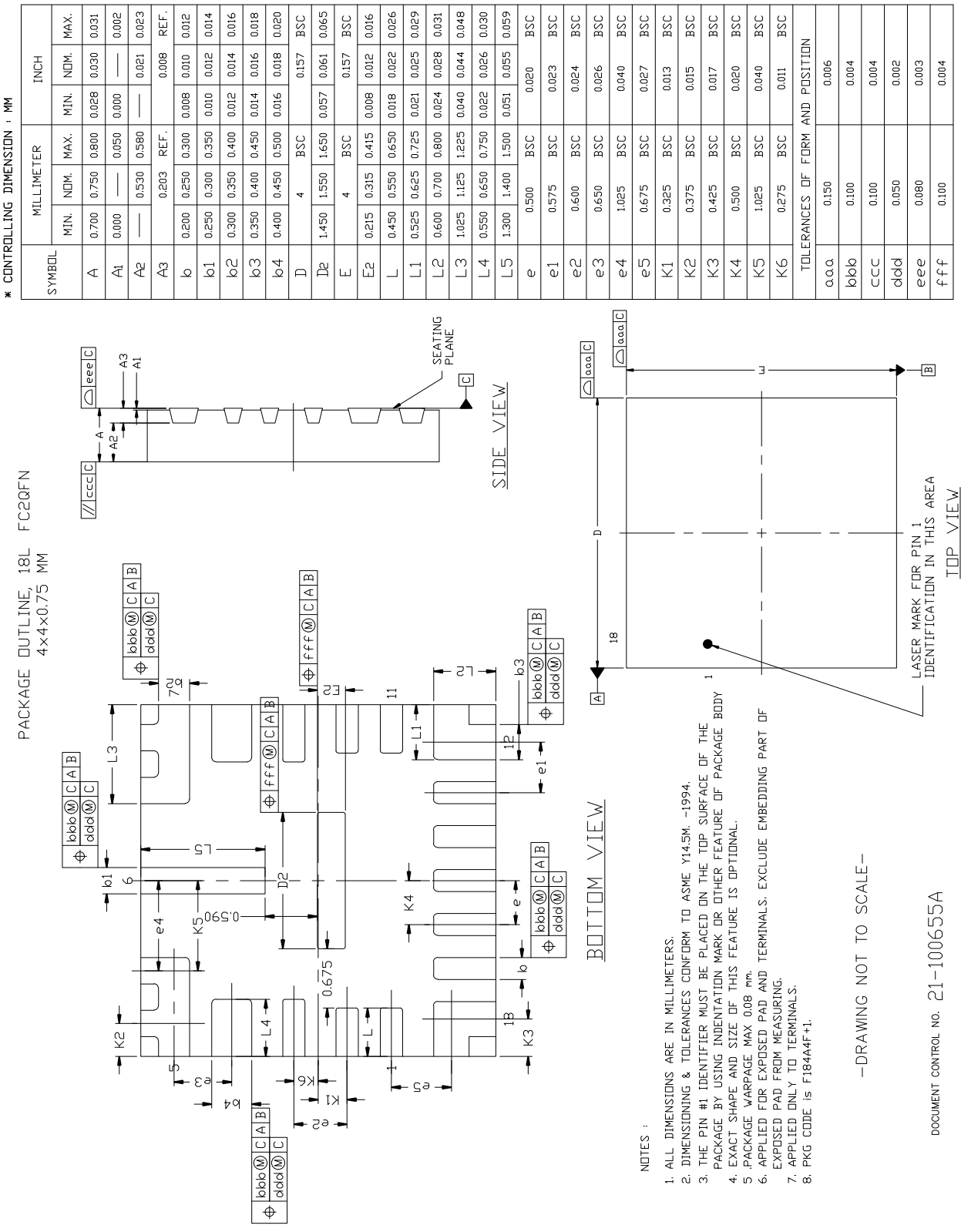
OUTLINE DIMENSIONS

Table 4.Thermal Resistance of 18L FC2QFN

Thermal Resistance, Four-Layer Board (Note 1)	
Junction to Ambient (θ_{JA})	19°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2.02°C/W

Note 1: Package thermal resistances were obtained using the MAX17793 evaluation kit with no airflow.

For the latest package outline information and land patterns (footprints), refer to *package index* at www.analog.com. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	—	0.050	0.000	—	0.002
A2	—	0.530	0.580	—	0.021	0.023
A3		0.203 REF.			0.008 REF.	
b	0.200	0.250	0.300	0.008	0.010	0.012
b1	0.250	0.300	0.350	0.010	0.012	0.014
b2	0.300	0.350	0.400	0.012	0.014	0.016
b3	0.350	0.400	0.450	0.014	0.016	0.018
b4	0.400	0.450	0.500	0.016	0.018	0.020
D		4 BSC			0.157 BSC	
D2	1.450	1.550	1.650	0.057	0.061	0.065
E		4 BSC			0.157 BSC	
E2	0.215	0.315	0.415	0.008	0.012	0.016
L	0.450	0.550	0.650	0.018	0.022	0.026
L1	0.525	0.625	0.725	0.021	0.025	0.029
L2	0.600	0.700	0.800	0.024	0.028	0.031
L3	1.025	1.125	1.225	0.040	0.044	0.048
L4	0.550	0.650	0.750	0.022	0.026	0.030
L5	1.300	1.400	1.500	0.051	0.055	0.059
e		0.500 BSC			0.020 BSC	
e1		0.575 BSC			0.023 BSC	
e2		0.600 BSC			0.024 BSC	
e3		0.650 BSC			0.026 BSC	
e4		1.025 BSC			0.040 BSC	
e5		0.675 BSC			0.027 BSC	
K1		0.325 BSC			0.013 BSC	
K2		0.375 BSC			0.015 BSC	
K3		0.425 BSC			0.017 BSC	
K4		0.500 BSC			0.020 BSC	
K5		1.025 BSC			0.040 BSC	
K6		0.275 BSC			0.011 BSC	
TOLERANCES OF FORM AND POSITION						
aaa		0.150			0.006	
bbb		0.100			0.004	
ccc		0.100			0.004	
ddd		0.050			0.002	
eee		0.080			0.003	
fff		0.100			0.004	

PACKAGE OUTLINE, 18L FC2QFN
4x4x0.75 MM

SIDE VIEW

BOTTOM VIEW

TOP VIEW

LASER MARK FOR PIN 1
IDENTIFICATION IN THIS AREA

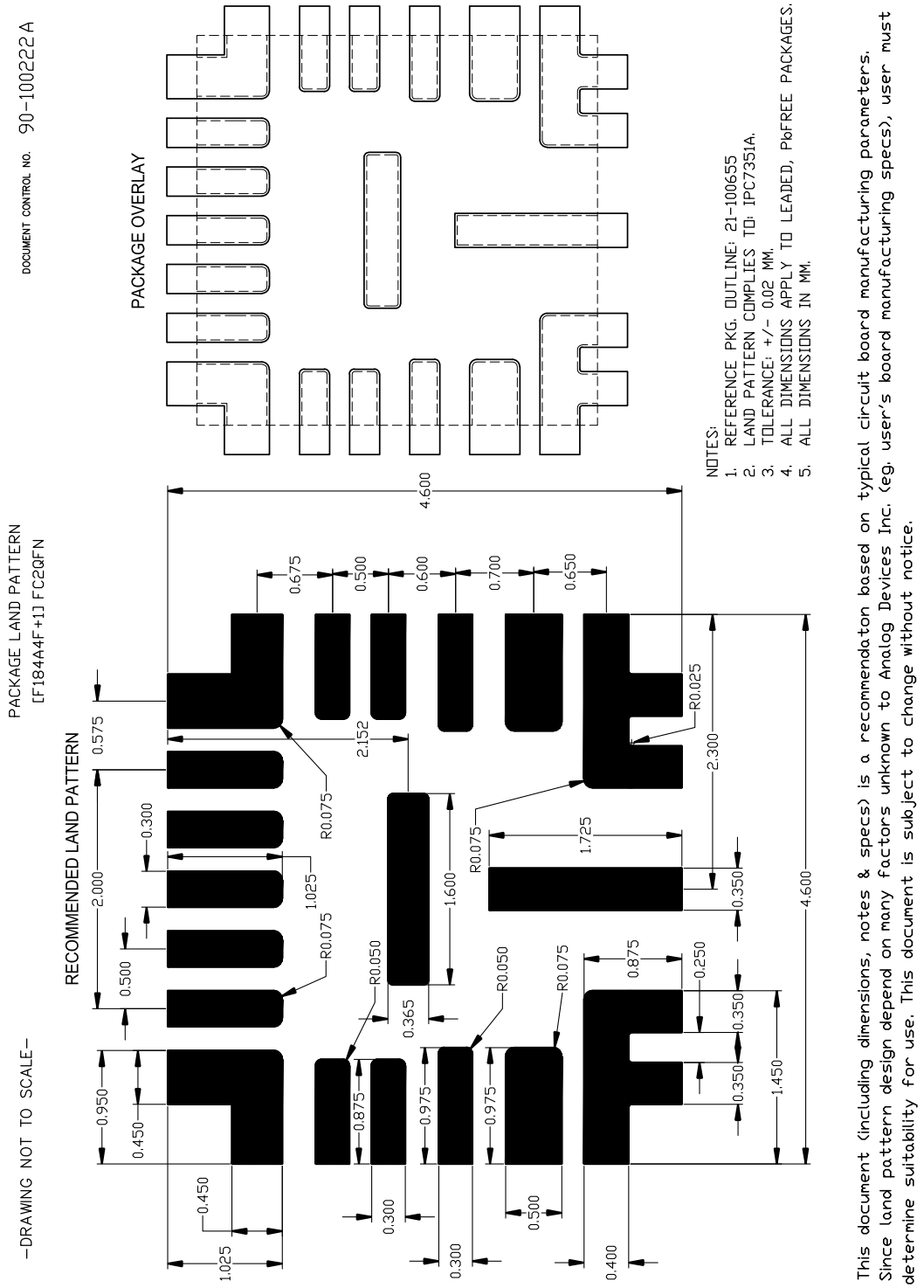
NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
3. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY
4. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
5. PACKAGE WARPAGE MAX 0.08 mm.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. APPLIED ONLY TO TERMINALS.
8. PKG CODE is F184A4F+1.

-DRAWING NOT TO SCALE-

DOCUMENT CONTROL NO. 21-100655A

Land Pattern



ORDERING GUIDE

Part Number	Temp Range	Pin Package
MAX17793AFN+	-40°C to 125°C	18-FC2QFN (4mm x 4mm)
MAX17793AFN+T	-40°C to 125°C	18-FC2QFN (4mm x 4mm)

+ Denotes a lead (Pb)-free/RoHS-compliant package.

T = Tape-and-reel.