EVALUATION KIT AVAILABLE

MAX186/MAX188

Low-Power, 8-Channel, Serial 12-Bit ADCs

General Description

The MAX186/MAX188 are 12-bit data-acquisition systems that combine an 8-channel multiplexer, high-bandwidth track/hold, and serial interface together with high conversion speed and ultra-low power consumption. The devices operate with a single +5V supply or dual ±5V supplies. The analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface directly connects to SPI, QSPI™ and MICROWIRE® devices without external logic. A serial strobe output allows direct connection to TMS320 family digital signal processors. The MAX186/MAX188 use either the internal clock or an external serial-interface clock to perform successive-approximation A/D conversions. The serial interface can operate beyond 4MHz when the internal clock is used.

The MAX186 has an internal 4.096V reference while the MAX188 requires an external reference. Both parts have a reference-buffer amplifier that simplifies gain trim .

The MAX186/MAX188 provide a hard-wired $\overline{SHDN}$ pin and two software-selectable power-down modes. Accessing the serial interface automatically powers up the devices, and the quick turn-on time allows the MAX186/MAX188 to be shut down between every conversion. Using this technique of powering down between conversions, supply current can be cut to under 10µA at reduced sampling rates.

The MAX186/MAX188 are available in 20-pin PDIP and SO packages, and in a shrink small-outline package (SSOP), that occupies 30% less area than an 8-pin PDIP. For applications that call for a parallel interface, see the MAX180/MAX181 data sheet. For anti-aliasing filters, consult the MAX274/MAX275 data sheet.

Applications

Portable Data Logging
Data-Acquisition
High-Accuracy Process Control
Automatic Testing
Robotics
Battery-Powered Instruments
Medical Instruments

QSPI is a trademark of Motorola.

MICROWIRE is a registered trademark of National Semiconductor.

Features

- **8-Channel Single-Ended or 4-Channel Differential Inputs**
- **Single +5V or ±5V Operation**
- **Low Power: 1.5mA (Operating Mode)**
  2µA (Power-Down Mode)
- **Internal Track/Hold, 133kHz Sampling Rate**
- **Internal 4.096V Reference (MAX186)**
- **SPI-/QSPI-/MICROWIRE-/TMS320-Compatible 4-Wire Serial Interface**
- **Software-Configurable Unipolar or Bipolar Inputs**
- **20-Pin PDIP, SO, SSOP Packages**
- **Evaluation Kit Available**

Ordering Information

PART†	TEMP RANGE	PIN-PACKAGE
MAX186_CPP+	0°C to +70°C	20 PDIP
MAX186_CWP+	0°C to +70°C	20 SO
MAX186_CAP+	0°C to +70°C	20 SSOP
MAX186DC/D	0°C to +70°C	Dice*
MAX186_EPP+	-40°C to +85°C	20 PDIP
MAX186_EWP+	-40°C to +85°C	20 SO
MAX186_EAP+	-40°C to +85°C	20 SSOP

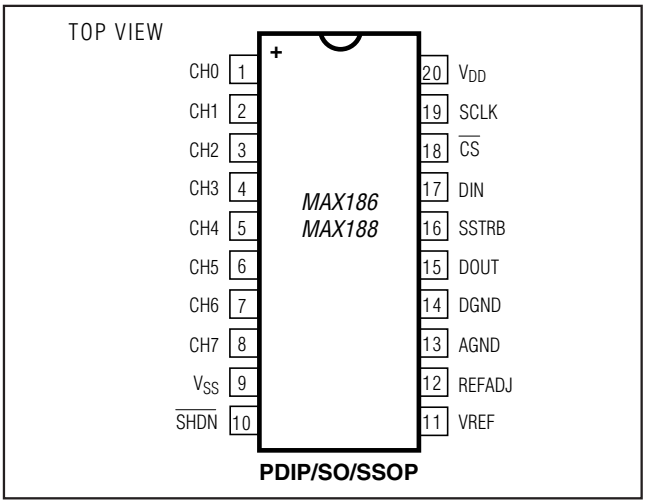
Ordering Information continued on last page.

†Parts are offered in grades A, B, C and D (grades defined in Electrical Characteristics). When ordering, please specify grade. Contact factory for availability of A-grade in SSOP package.

**Dice are specified at +25°C, DC parameters only.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configuration



PDIP/SO/SSOP

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-0123; Rev 5; 1/12

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +6V
V_{SS} to AGND .....+0.3V to -6V
V_{DD} to V_{SS} .....-0.3V to +12V
AGND to DGND .....-0.3V to +0.3V
CH0–CH7 to AGND, DGND .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
CH0–CH7 Total Input Current .....±20mA
VREF to AGND .....-0.3V to (V_{DD} + 0.3V)
REFADJ to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to (V_{DD} + 0.3V)
Digital Outputs to DGND .....-0.3V to (V_{DD} + 0.3V)
Digital Output Sink Current 25mA

Continuous Power Dissipation (TA = +70°C)
PDIP (derate 11.11mW/°C above +70°C) 889mW
SO (derate 10.00mW/°C above +70°C) 800mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges
MAX186_C/MAX188_C .....0°C to +70°C
MAX186_E/MAX188_E .....-40°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186—4.7µF capacitor at VREF pin; MAX188—external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				12			Bits
Relative Accuracy (Note 2)		MAX186A/MAX188A				±0.5	LSB
		MAX186B/MAX188B				±0.5	
		MAX186C				±1.0	
		MAX188C				±0.75	
		MAX186D/MAX188D				±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature				±1	LSB
Offset Error		MAX186A/MAX188A				±2.0	LSB
		MAX186B/MAX188B				±3.0	
		MAX186C/MAX188C				±3.0	
		MAX186D/MAX188D				±3.0	
Gain Error (Note 3)		MAX186 (all grades)				±3.0	LSB
		External reference 4.096V (MAX188)	MAX188A			±1.5	
			MAX188B			±2.0	
			MAX188C			±2.0	
			MAX188D			±3.0	
Gain Temperature Coefficient		External reference, 4.096V			±0.8		ppm/°C
Channel-to-Channel Offset Matching					±0.1		LSB
DYNAMIC SPECIFICATIONS (10kHz sine wave input, 4.096V_{P-P}, 133ksps, 2.0MHz external clock, bipolar input mode)							
Signal-to-Noise + Distortion Ratio	SINAD			70			dB
Total Harmonic Distortion (up to the 5th harmonic)	THD					-80	dB
Spurious-Free Dynamic Range	SFDR			80			dB
Channel-to-Channel Crosstalk		65kHz, V_{IN} = 4.096V_{P-P} (Note 4)			-85		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186—4.7µF capacitor at VREF pin; MAX188—external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Bandwidth		-3dB rolloff		4.5		MHz
Full-Power Bandwidth				800		kHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock	5.5		10	µs
		External clock, 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	t_{AZ}				1.5	µs
Aperture Delay				10		ns
Aperture Jitter				<50		ps
Internal Clock Frequency				1.7		MHz
External Clock Frequency Range		External compensation, 4.7µF	0.1		2.0	MHz
		Internal compensation (Note 6)	0.1		0.4	
		Used for data transfer only		10		
ANALOG INPUT						
Input Voltage Range, Single-Ended and Differential (Note 9)		Unipolar, V_{SS} = 0V			0 to VREF	V
		Bipolar, V_{SS} = -5V			±VREF/2	
Multiplexer Leakage Current		On/off leakage current, V_{IN} = ±5V		±0.01	±1	µA
Input Capacitance		(Note 6)		16		pF
INTERNAL REFERENCE (MAX186 only, reference buffer enabled)						
VREF Output Voltage		T_A = +25°C	4.076	4.096	4.116	V
VREF Short-Circuit Current					30	mA
VREF Tempco		MAX186A, MAX186B, MAX186C — MAX186_C		±30	±50	ppm/°C
		MAX186A, MAX186B, MAX186C — MAX186_E		±30	±60	
		MAX186D		±30		
Load Regulation (Note 7)		0 to 0.5mA output load		2.5		mV
Capacitive Bypass at VREF		Internal compensation	0			µF
		External compensation	4.7			
Capacitive Bypass at REFADJ		Internal compensation	0.01			µF
		External compensation	0.01			
REFADJ Adjustment Range				±1.5		%
EXTERNAL REFERENCE AT VREF (Buffer disabled, VREF = 4.096V)						
Input Voltage Range			2.50		V_{DD} + 50mV	V
Input Current				200	350	µA
Input Resistance			12	20		kΩ
Shutdown VREF Input Current				1.5	10	µA
Buffer Disable Threshold REFADJ			V_{DD} - 50mV			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186—4.7µF capacitor at VREF pin; MAX188—external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE AT REFADJ						
Capacitive Bypass at VREF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Reference-Buffer Gain		MAX186		1.678		V/V
		MAX188		1.638		
REFADJ Input Current		MAX186			±50	µA
		MAX188			±5	
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{INH}		2.4			V
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{INL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.15		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 6)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{INH}		V_{DD} - 0.5			V
$\overline{SHDN}$ Input Low Voltage	V_{INL}				0.5	V
$\overline{SHDN}$ Input Current, High	I_{INH}	$V_{\overline{SHDN}}$ = V_{DD}			4.0	µA
$\overline{SHDN}$ Input Current, Low	I_{INL}	$V_{\overline{SHDN}}$ = 0V	-4.0			µA
$\overline{SHDN}$ Input Mid Voltage	V_{IM}		1.5		V_{DD} -1.5	V
$\overline{SHDN}$ Voltage, Open	V_{FLT}	$V_{\overline{SHDN}}$ = open		2.75		V
$\overline{SHDN}$ Max Allowed Leakage, Mid Input		$V_{\overline{SHDN}}$ = open	-100		100	nA
DIGITAL OUTPUTS (DOUT, SSTRB)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA		0.3		
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	4			V
Three-State Leakage Current	I_L	$V_{\overline{CS}}$ = 5V			±10	µA
Three-State Output Capacitance	C_{OUT}	$V_{\overline{CS}}$ = 5V (Note 6)			15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}			5 ±5%		V
Negative Supply Voltage	V_{SS}			0 or -5 ±5%		V
Positive Supply Current	I_{DD}	Operating mode		1.5	2.5	mA
		Fast power-down		30	70	µA
		Full power-down		2	10	
Negative Supply Current	I_{SS}	Operating mode and fast power-down			50	µA
		Full power-down			10	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186—4.7µF capacitor at VREF pin; MAX188—external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Rejection (Note 8)	PSR	V_{DD} = 5V ±5%; external reference, 4.096V; full-scale input		±0.06	±0.5	mV
Negative Supply Rejection (Note 8)	PSR	V_{SS} = -5V ±5%; external reference, 4.096V; full-scale input		±0.01	±0.5	mV

TIMING CHARACTERISTICS

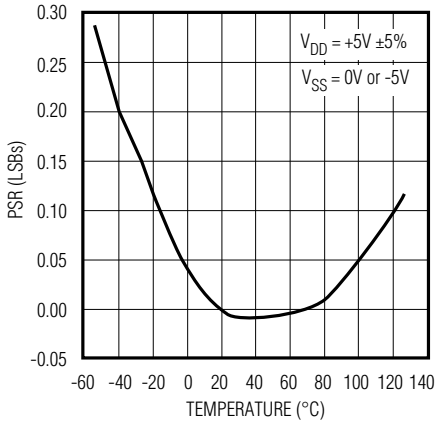
(V_{DD} = 5V ±5%; V_{SS} =0V or -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{AZ}			1.5			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}					0	ns
SCLK Fall to Output Data Valid	t_{DO}	C_{LOAD} = 100pF	MAX18_ _C/E	20		150	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}	C_{LOAD} = 100pF				100	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	C_{LOAD} = 100pF				100	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	C_{LOAD} = 100pF				200	ns
$\overline{CS}$ Fall to SSTRB Output Enable (Note 6)	t_{SDV}	External clock mode only, C_{LOAD} = 100pF				200	ns
$\overline{CS}$ Rise to SSTRB Output Disable (Note 6)	t_{STR}	External clock mode only, C_{LOAD} = 100pF				200	ns
SSTRB Rise to SCLK Rise (Note 6)	t_{SCK}	Internal clock mode only		0			ns

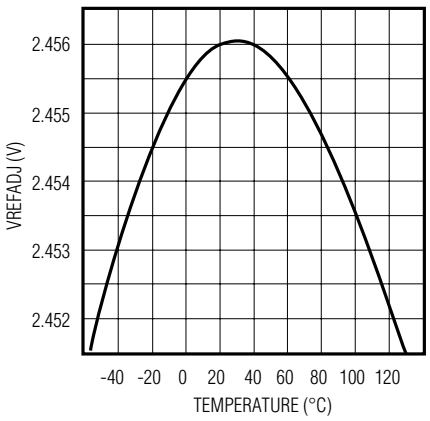
Note 1: Tested at V_{DD} = 5.0V; V_{SS} = 0V; unipolar input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: MAX186 – internal reference, offset nulled; MAX188 – external reference (VREF = +4.096V), offset nulled.
Note 4: Ground on-channel; sine wave applied to all off channels.
Note 5: Conversion time defined as the number of clock cycles times the clock period; clock has 50% duty cycle.
Note 6: Guaranteed by design. Not subject to production testing.
Note 7: External load should not change during conversion for specified accuracy.
Note 8: Measured at V_{SUPPLY} +5% and V_{SUPPLY} -5% only.
Note 9: The common-mode range for the analog inputs is from V_{SS} to V_{DD}.

Typical Operating Characteristics

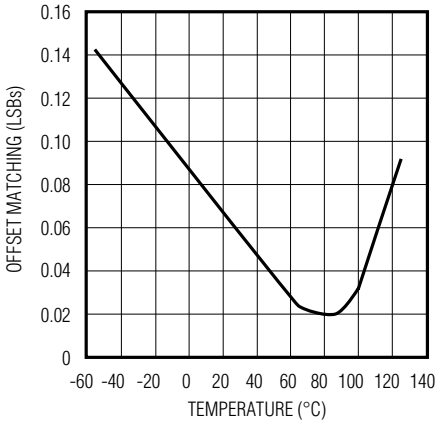
POWER-SUPPLY REJECTION vs. TEMPERATURE



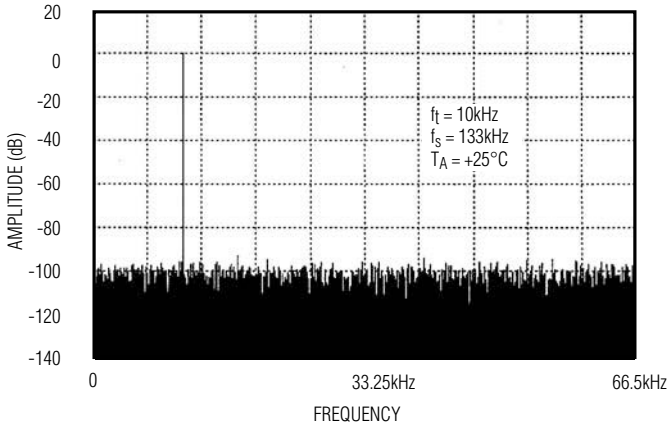
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



CHANNEL-TO-CHANNEL OFFSET MATCHING vs. TEMPERATURE



MAX186/MAX188 FFT PLOT – 133kHz



Pin Description

PIN	NAME	FUNCTION
1–8	CH0–CH7	Sampling Analog Inputs
9	VSS	Negative Supply Voltage. Connect to -5V ±5% or AGND
10	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX186/MAX188 down to 10µA (max) supply current, otherwise the MAX186/MAX188 are fully operational. Pulling $\overline{SHDN}$ high puts the reference-buffer amplifier in internal compensation mode. Leaving $\overline{SHDN}$ unconnected puts the reference-buffer amplifier in external compensation mode.
11	VREF	Reference Voltage for analog-to-digital conversion. Also, output of the reference buffer amplifier (4.096V in the MAX186, 1.638 x REFADJ in the MAX188). Add a 4.7µF capacitor to ground when using external compensation mode. Also functions as an input when used with a precision external

Pin Description (continued)

PIN	NAME	FUNCTION
12	REFADJ	Input to the Reference-Buffer Amplifier. To disable the reference-buffer amplifier, connect REFADJ to VDD.
13	AGND	Analog Ground. Also IN- Input for single-ended conversions.
14	DGND	Digital Ground
15	DOUT	Serial Data Output. Data is clocked out at the falling edge of SCLK. High impedance when $\overline{CS}$ is high.
16	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX186/MAX188 begin the A/D conversion and goes high when the conversion is done. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external mode).
17	DIN	Serial Data Input. Data is clocked in at the rising edge of SCLK.
18	CS	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60% in external clock mode.)
20	VDD	Positive Supply Voltage, +5V ±5%

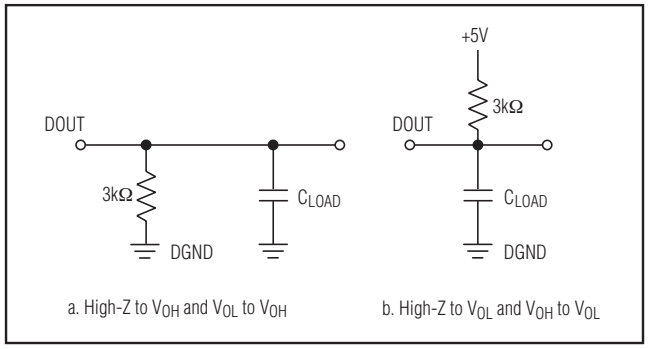


Figure 1. Load Circuits for Enable Time

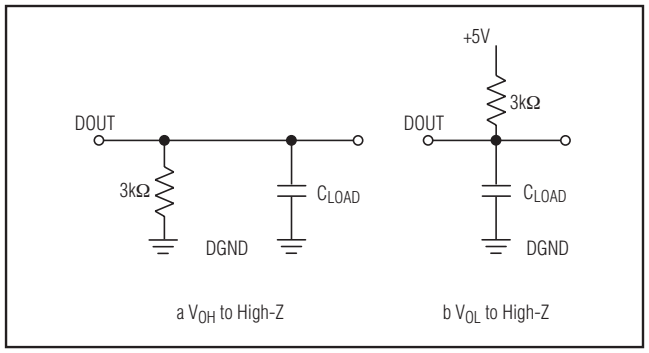


Figure 2. Load Circuits for Disabled Time

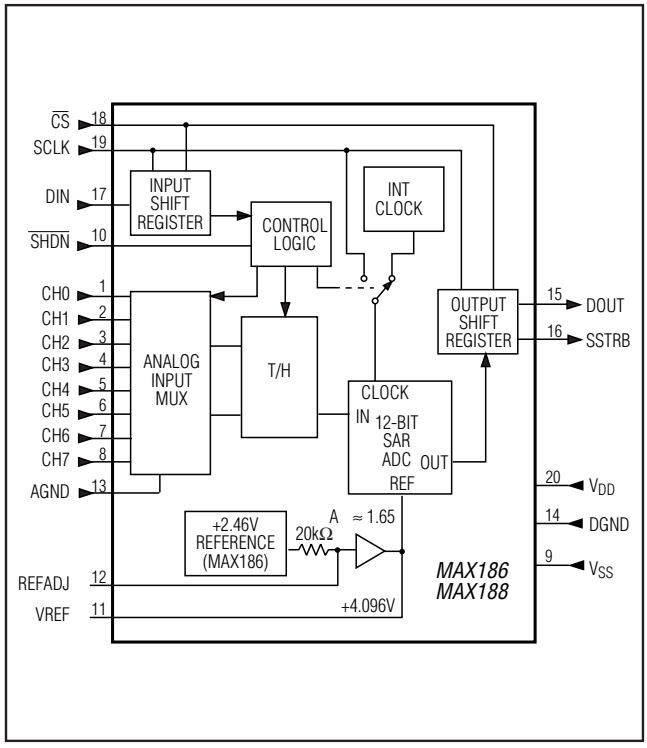


Figure 3. Block Diagram

Detailed Description

The MAX186/MAX188 use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. A flexible serial interface provides easy interface to microprocessors. No external hold capacitors are required. Figure 3 shows the block diagram for the MAX186/MAX188.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the Equivalent Input Circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0-CH7 and IN- is switched to AGND. In differential mode, IN+ and IN- are selected from pairs of CH0/CH1, CH2/CH3, CH4/CH5 and CH6/CH7. Configure the channels with Table 3 and Table 4.

In differential mode, IN- and IN+ are internally switched to either one of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. Accomplish this by connecting a 0.1µF capacitor from AIN- (the selected analog input, respectively) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply AGND. This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a charge of 16pF x $[(V_{IN}+) - (V_{IN}-)]$ from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. The T/H enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to AGND, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

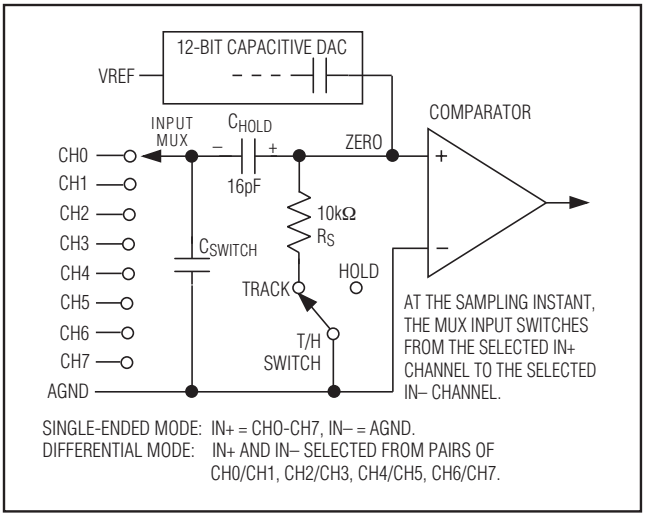


Figure 4. Equivalent Input Circuit

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{AZ} = 9 \times (R_S + R_{IN}) \times 16pF,$$

where R_{IN} = 5kΩ, R_S = the source impedance of the input signal, and t_{AZ} is never less than 1.5µs. Note that source impedances below 5kΩ do not significantly affect the AC performance of the ADC. Higher source impedances can be used if an input capacitor is connected to the analog inputs, as shown in Figure 5. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 4.5MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

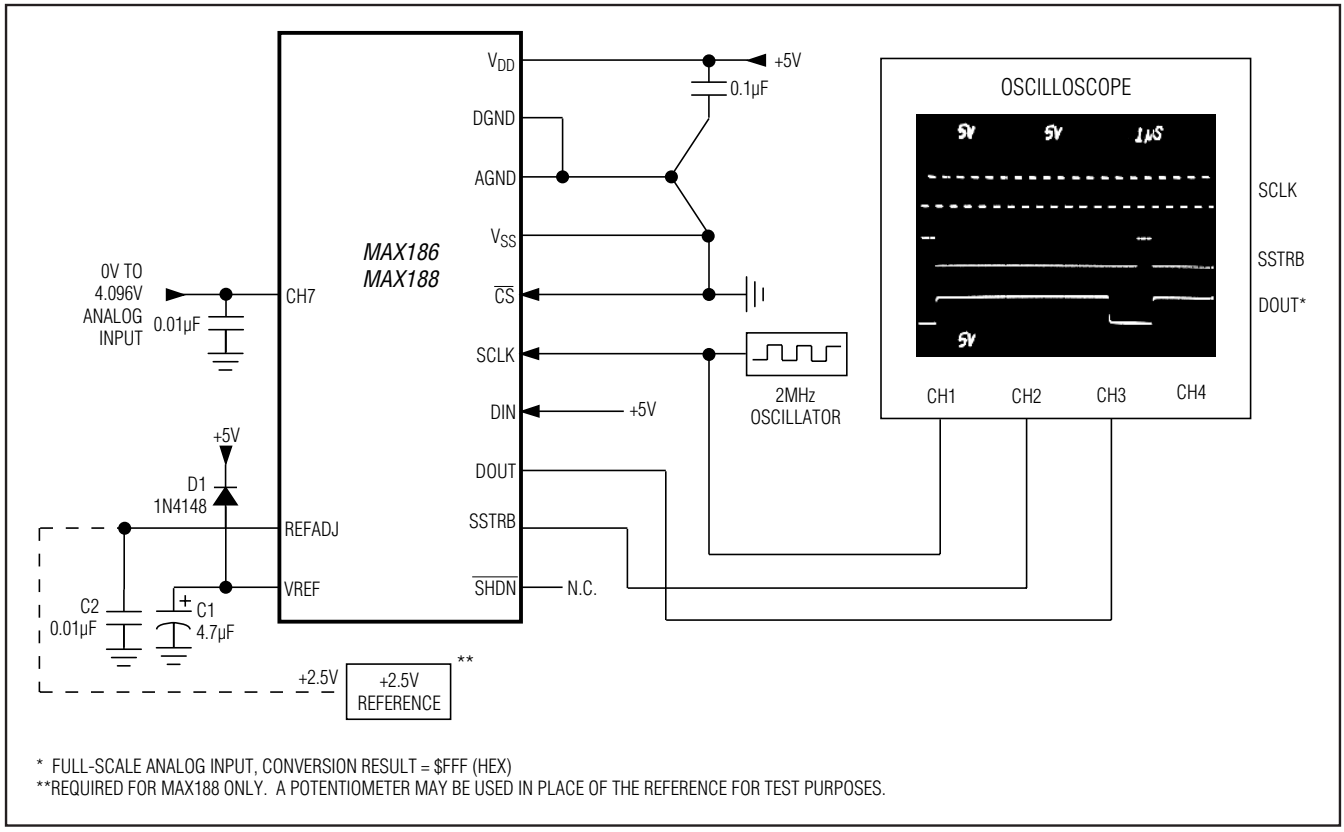


Figure 5. Quick-Look Circuit

Analog Input Range and Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and V_{SS}, allow the channel input pins to swing from V_{SS} - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV, or be lower than V_{SS} by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off-channels over two milliamperes, as excessive current will degrade the conversion accuracy of the on-channel.

The full-scale input voltage depends on the voltage at VREF. See Tables 1a and 1b.

Quick Look

To evaluate the analog performance of the MAX186/MAX188 quickly, use the circuit of Figure 5. The MAX186/MAX188 require a control byte to be written to DIN before each conversion. Tying DIN to +5V feeds in control bytes of $FF (HEX), which trigger

Table 1a. Unipolar Full Scale and Zero Scale

Reference	Zero Scale	Full Scale
Internal Reference (MAX186 only)	0V	+4.096V
External Reference at REFADJ	0V	V_{REFADJ} x A*
at VREF	0V	VREF

** A = 1.678 for the MAX186, 1.638 for the MAX188*

Table 1b. Bipolar Full Scale, Zero Scale, and Negative Full Scale

Reference	Negative Full Scale	Zero Scale	Full Scale
Internal Reference (MAX186 only)	-4.096V/2	0V	+4.096V/2
External Reference at REFADJ	$-1/2V_{REFADJ}$ x A*	0V	$+1/2V_{REFADJ}$ x A*
at VREF	-1/2 VREF	0V	+1/2 VREF

** A = 1.678 for the MAX186, 1.638 for the MAX188*

single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the 12-bit conversion result comes out of DOUT. Varying the analog input to CH7 should alter the sequence of bits from DOUT. A total of 15 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

How to Start a Conversion

A conversion is started on the MAX186/MAX188 by clocking a control byte into DIN. Each rising edge on SCLK, with $\overline{CS}$ low, clocks a bit from DIN into the MAX186/MAX188's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the MSB of the control byte. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 2 shows the control-byte format.

The MAX186/MAX188 are fully compatible with Microwire and SPI devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire and SPI both transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit*, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 12-bit conversion result).

Example: Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode, call it TB1. TB1 should be of the format: 1XXXXX11 Binary, where the Xs denote the particular channel and conversion-mode selected.

Table 2. Control-Byte Format

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

Bit	Name	Description
7(MSB)	START	The first logic "**1**" bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels are used for the conversion. See Tables 3 and 4.
3	UNI/$\overline{BIP}$	**1** = unipolar, **0** = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF/2 to +VREF/2.
2	SGL/$\overline{DIF}$	**1** = single ended, **0** = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to AGND. In differential mode, the voltage difference between two channels is measured. See Tables 3 and 4.
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode **0** **0** Full power-down (I_Q = 2µA) **0** **1** Fast power-down (I_Q = 30µA) **1** **0** Internal clock mode **1** **1** External clock mode

Table 3. Channel Selection in Single-Ended Mode (SGL/$\overline{DIFF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	AGND
0	0	0	+								–
1	0	0		+							–
0	0	1			+						–
1	0	1				+					–
0	1	0					+				–
1	1	0						+			–
0	1	1							+		–
1	1	1								+	–

Table 4. Channel Selection in Differential Mode (SGL/$\overline{DIFF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	–						
0	0	1			+	–				
0	1	0					+	–		
0	1	1							+	–
1	0	0	–	+						
1	0	1			–	+				
1	1	0					–	+		
1	1	1							–	+

2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ on the MAX186/MAX188 low.
3) Transmit TB1 and simultaneously receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 HEX) and simultaneously receive byte RB2.
5) Transmit a byte of all zeros ($00 HEX) and simultaneously receive byte RB3.
6) Pull $\overline{CS}$ on the MAX186/MAX188 high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 will contain the result of the conversion padded with one leading zero and three trailing zeros. The total conversion time is a function of the serial clock frequency and the amount of dead time between 8-bit transfers. Make sure that the total conversion time does not exceed 120µs, to avoid excessive T/H droop.

Digital Output

In unipolar input mode, the output is straight binary (see Figure 15). For bipolar inputs, the output is twos-complement (see Figure 16). Data is clocked out at the falling edge of SCLK in MSB-first format.

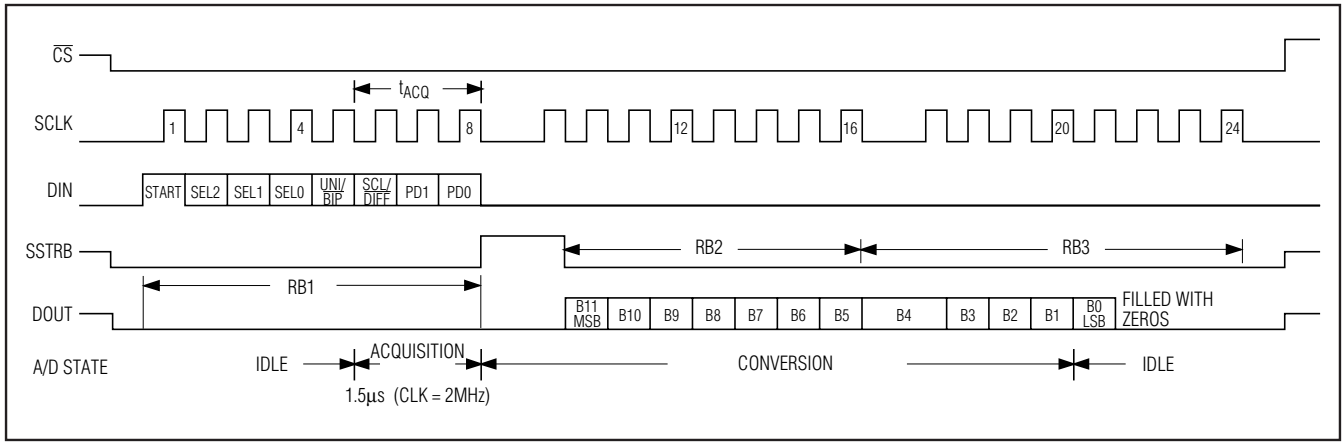


Figure 6. 24-Bit External Clock Mode Conversion Timing (SPI, QSPI and Microwire Compatible)

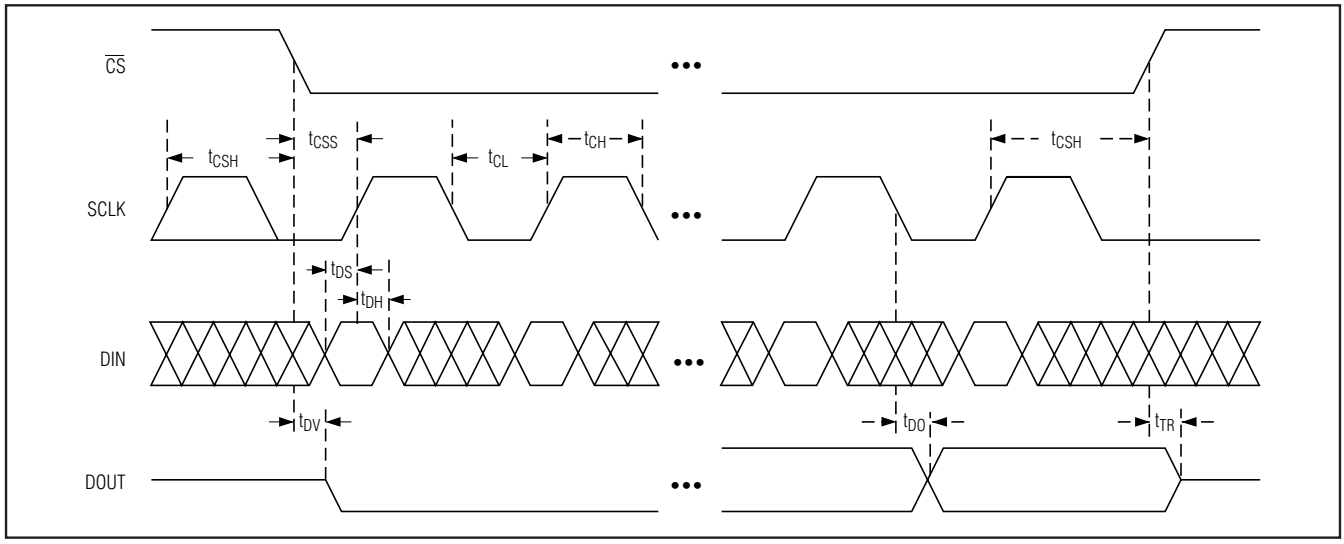


Figure 7. Detailed Serial-Interface Timing

Internal and External Clock Modes

The MAX186/MAX188 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX186/MAX188. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7 through 10 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (see Figure 6). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB will output a logic low. Figure 8 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or else droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the clock period exceeds 10µs, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

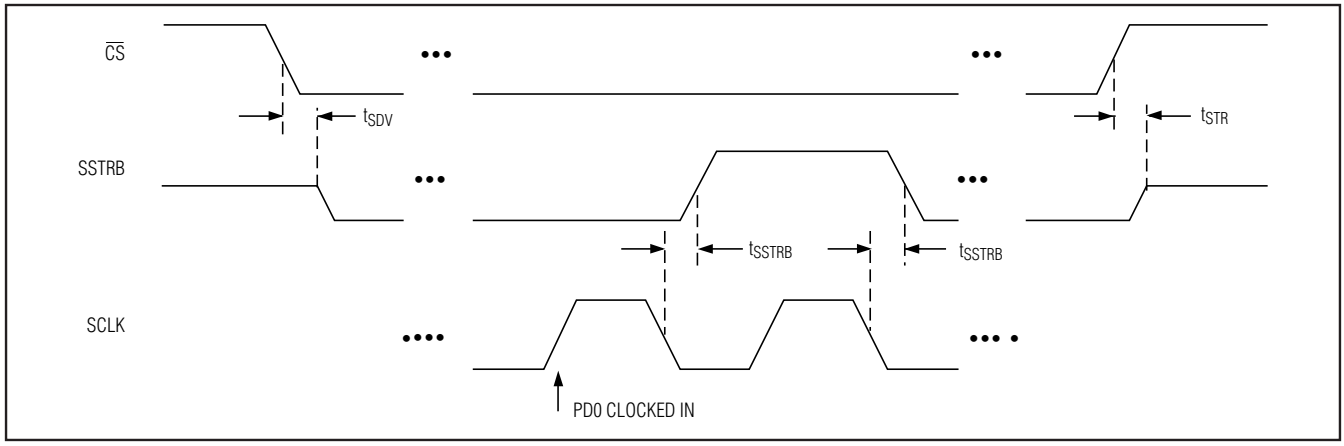


Figure 8. External Clock Mode SSTRB Detailed Timing

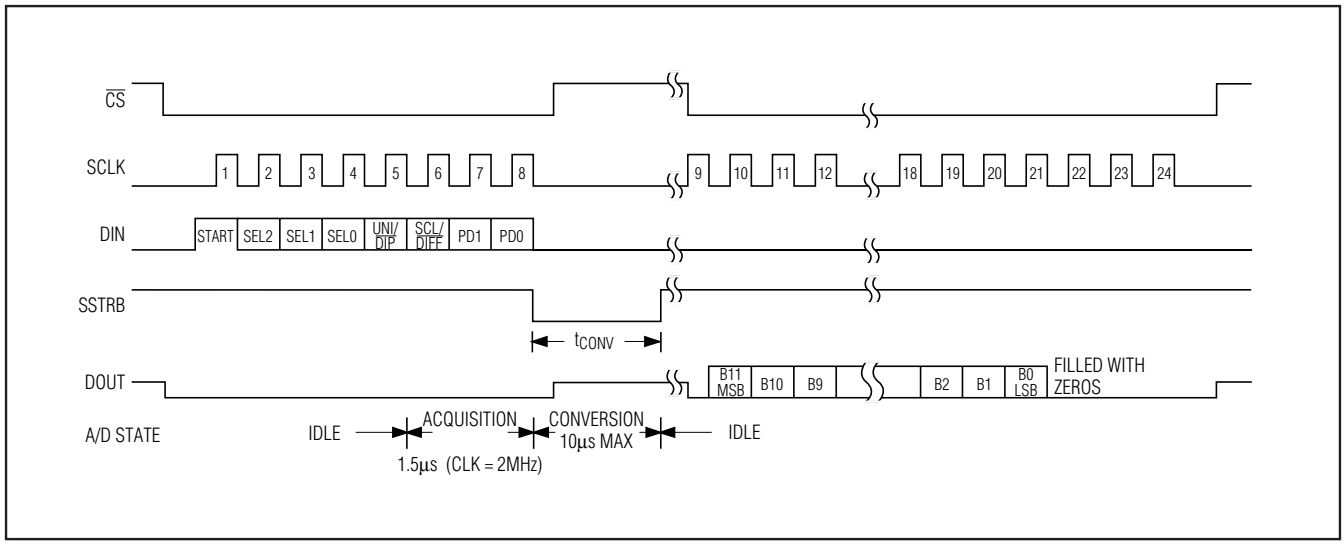


Figure 9. Internal Clock Mode Timing

Internal Clock

In internal clock mode, the MAX186/MAX188 generate their own conversion clock internally. This frees the microprocessor from the burden of running the SAR conversion clock, and allows the conversion results to be read back at the processor's convenience, at any clock rate from zero to typically 10MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB will be low for a maximum of 10µs, during which time SCLK should remain low for best noise performance. An internal register stores data when the conversion is in progress. SCLK clocks the data out at this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge will produce the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (see Figure 9). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX186/MAX188 and three-states DOUT, but it does not adversely effect an internal clock-mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 10 shows the SSTRB timing in internal clock mode. In internal clock mode, data can be shifted in and out of the MAX186/MAX188 at clock rates exceeding 4.0MHz, provided that the minimum acquisition time, t_{AZ}, is kept above 1.5µs.

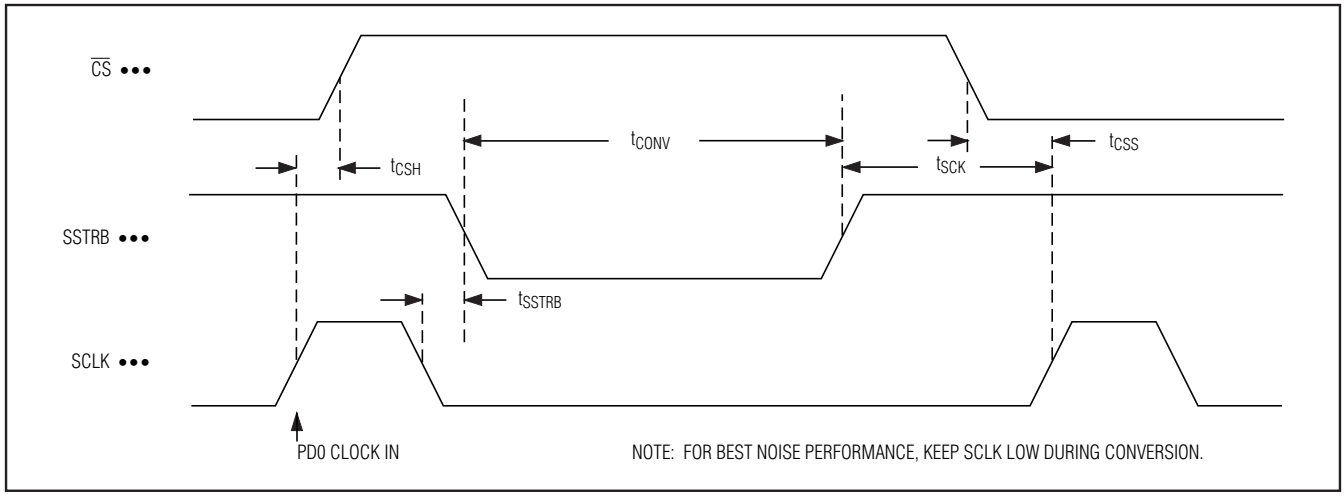


Figure 10. Internal Clock Mode SSTRB Detailed Timing

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion on the MAX186/MAX188. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low anytime the converter is idle, e.g. after V_{CC} is applied.

OR

The first high bit clocked into DIN after bit 5 of a conversion in progress is clocked onto the DOUT pin.

If a falling edge on $\overline{CS}$ forces a start bit before bit 5 (B5) becomes available, then the current conversion will be terminated and a new one started. Thus, the fastest the MAX186/MAX188 can run is 15 clocks per conversion. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion will typically be the fastest that a microcontroller can drive the MAX186/MAX188. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry will activate the MAX186/MAX188 in internal clock mode, ready to convert with SSTRB = high. After the power supplies have been stabilized, the internal reset time is 100µs and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN will be interpreted as a start bit. Until a conversion takes place, DOUT will shift out zeros.

Reference-Buffer Compensation

In addition to its shutdown function, the $\overline{SHDN}$ pin also selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. Compensated or not, the minimum clock rate is 100kHz due to droop on the sample-and-hold.

To select external compensation, open $\overline{SHDN}$. See the *Typical Operating Circuit*, which uses a 4.7µF capacitor at VREF. A value of 4.7µF or greater ensures stability and allows operation of the converter at the full clock speed of 2MHz. External compensation increases power-up time (see the *Choosing Power-Down Mode* section, and Table 5).

Internal compensation requires no external capacitor at VREF, and is selected by pulling $\overline{SHDN}$ high. Internal compensation allows for shortest power-up times, but is only available using an external clock and reduces the maximum clock rate to 400kHz.

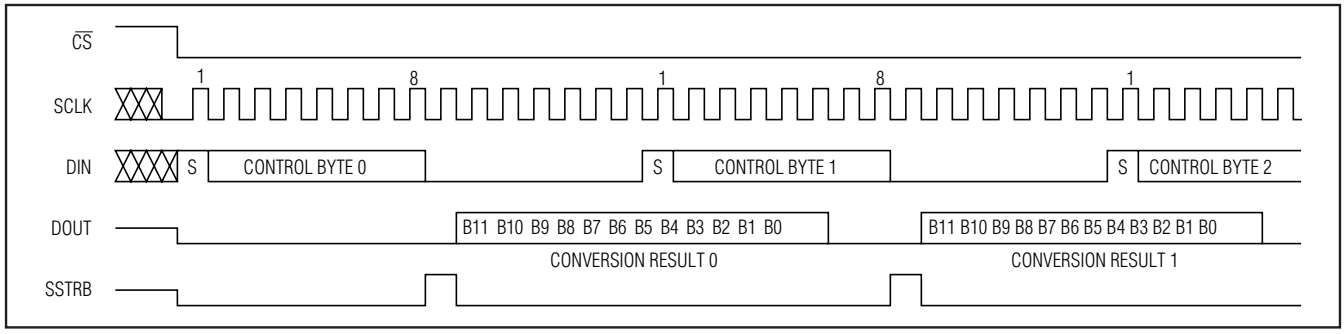


Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

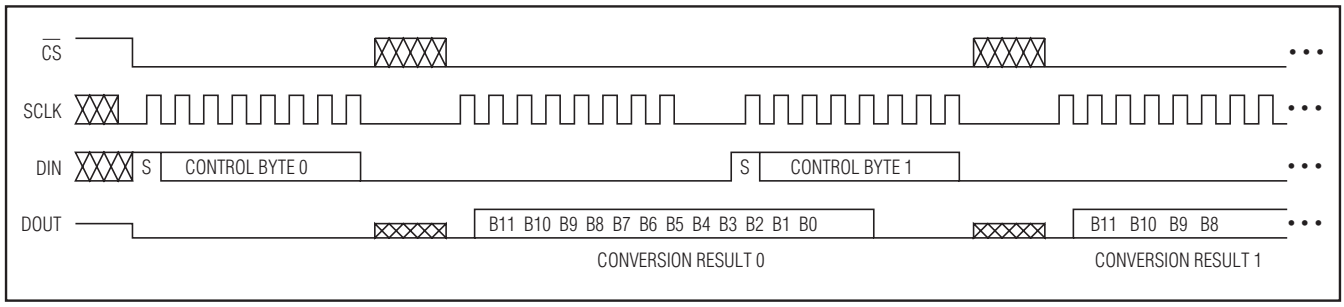


Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

Power-Down

Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down or fast power-down mode via bits 7 and 8 of the DIN control byte with $\overline{SHDN}$ high or open (see Tables 2 and 6). Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 7 and 8 of DIN word (see Table 7).

Full power-down mode turns off all chip functions that draw quiescent current, reducing I_{DD} and I_{SS} typically to 2µA.

Fast power-down mode turns off all circuitry except the bandgap reference. With the fast power-down mode, the supply current is 30µA. Power-up time can be shortened to 5µs in internal compensation mode.

In both software shutdown modes, the serial interface remains operational, however, the ADC will not convert. Table 5 illustrates how the choice of reference-buffer compensation and power-down mode affects both power-up delay and maximum sample rate.

In external compensation mode, the power-up time is 20ms with a 4.7µF compensation capacitor (200ms with a 33µF capacitor) when the capacitor is fully discharged. In fast power-down, you can eliminate start-up time by using low-leakage capacitors that will not discharge more than 1/2LSB while shut down. In shutdown, the capacitor has to supply the current into the reference (1.5µA typ) and the transient currents at power-up.

Figures 12a and 12b illustrate the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 6, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC will continue to operate in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results may be clocked out while the MAX186/MAX188 have already entered a software power-down.

The first logical 1 on DIN will be interpreted as a start bit, and powers up the MAX186/MAX188. Following the start bit, the data input word or control byte also determines clock and power-down modes. For example, if the DIN word contains PD1 = 1, then the chip will remain powered up. If PD1 = 0, a power-down will resume after one conversion.

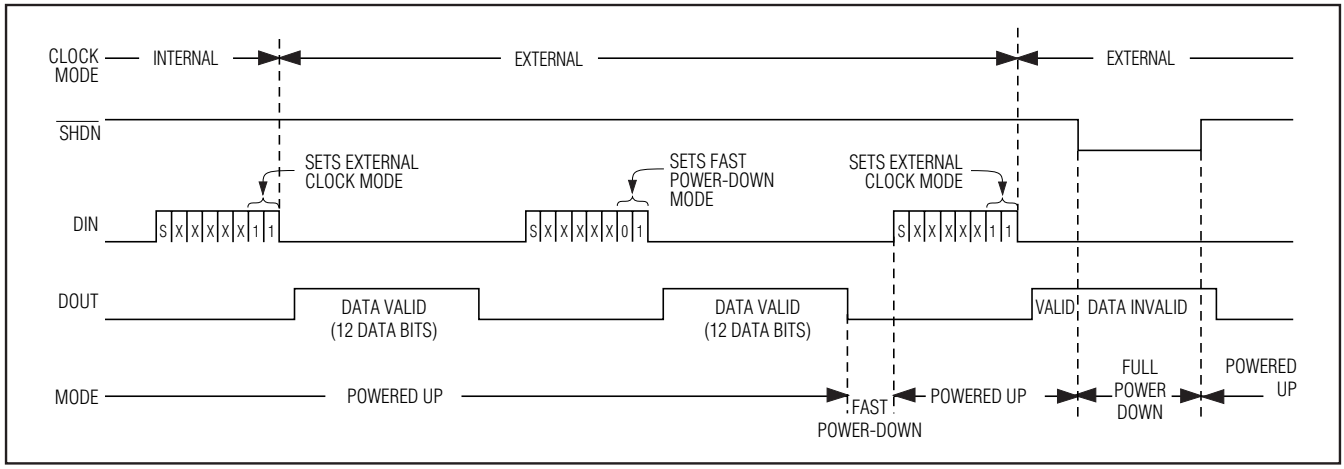


Figure 12a. Timing Diagram Power-Down Modes, External Clock

Table 5. Typical Power-Up Delay Times

Reference Buffer	Reference-Buffer Compensation Mode	VREF Capacitor (µF)	Power-Down Mode	Power-Up Delay (s)	Maximum Sampling Rate (ksps)
Enabled	Internal		Fast	5µ	26
Enabled	Internal		Full	300µ	26
Enabled	External	4.7	Fast	See Figure 14c	133
Enabled	External	4.7	Full	See Figure 14c	133
Disabled			Fast	2µ	133
Disabled			Full	2µ	133

Table 6. Software Shutdown and Clock Mode

PD1	PD0	Device Mode
1	1	External Clock Mode
1	0	Internal Clock Mode
0	1	Fast Power-Down Mode
0	0	Full Power-Down Mode

Table 7. Hard-Wired Shutdown and Compensation Mode

$\overline{SHDN}$ State	Device Mode	Reference-Buffer Compensation
1	Enabled	Internal Compensation
Open	Enabled	External Compensation
0	Full Power-Down	N/A

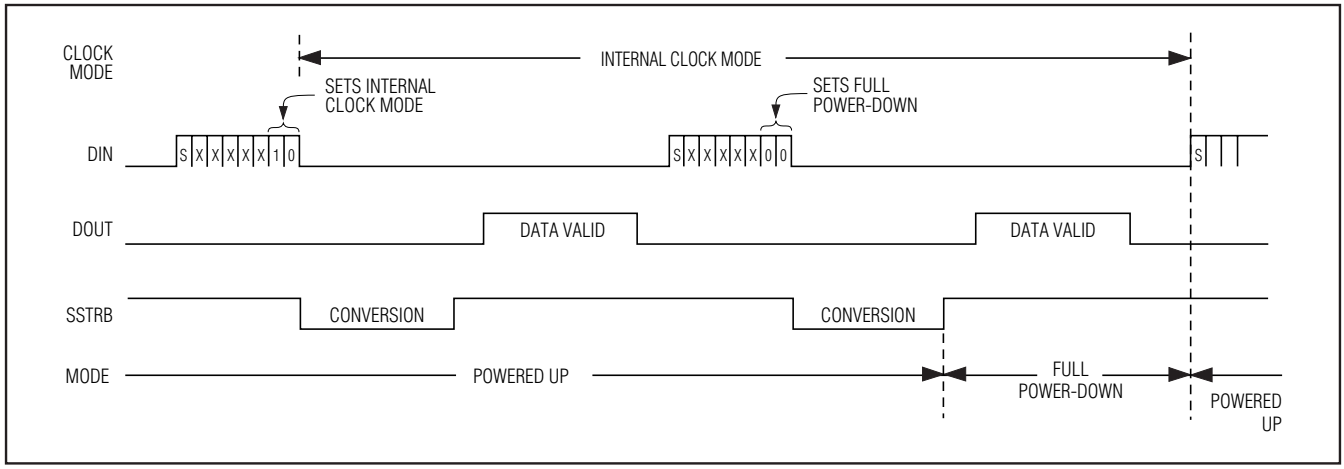


Figure 12b. Timing Diagram Power-Down Modes, Internal Clock

Hardware Power-Down

The $\overline{SHDN}$ pin places the converter into the full power-down mode. Unlike with the software shut-down modes, conversion is not completed. It stops coincidentally with $\overline{SHDN}$ being brought low. There is no power-up delay if an external reference is used and is not shut down. The $\overline{SHDN}$ pin also selects internal or external reference compensation (see Table 7).

Power-Down Sequencing

The MAX186/MAX188 auto power-down modes can save considerable power when operating at less than maximum sample rates. The following discussion illustrates the various power-down sequences.

Lowest Power at up to 500 Conversions/Channel/Second

The following examples illustrate two different power-down sequences. Other combinations of clock rates, compensation modes, and power-down modes may give lowest power consumption in other applications.

Figure 14a depicts the MAX186 power consumption for one or eight channel conversions utilizing full power-down mode and internal reference compensation. A 0.01µF bypass capacitor at REFADJ forms an RC filter with the internal 20kΩ reference resistor with a 0.2ms time constant. To achieve full 12-bit accuracy, 10 time constants or 2ms are required after power-up. Waiting 2ms in FASTPD mode instead of full power-up will reduce the power consumption by a factor of 10 or more. This is achieved by using the sequence shown in Figure 13.

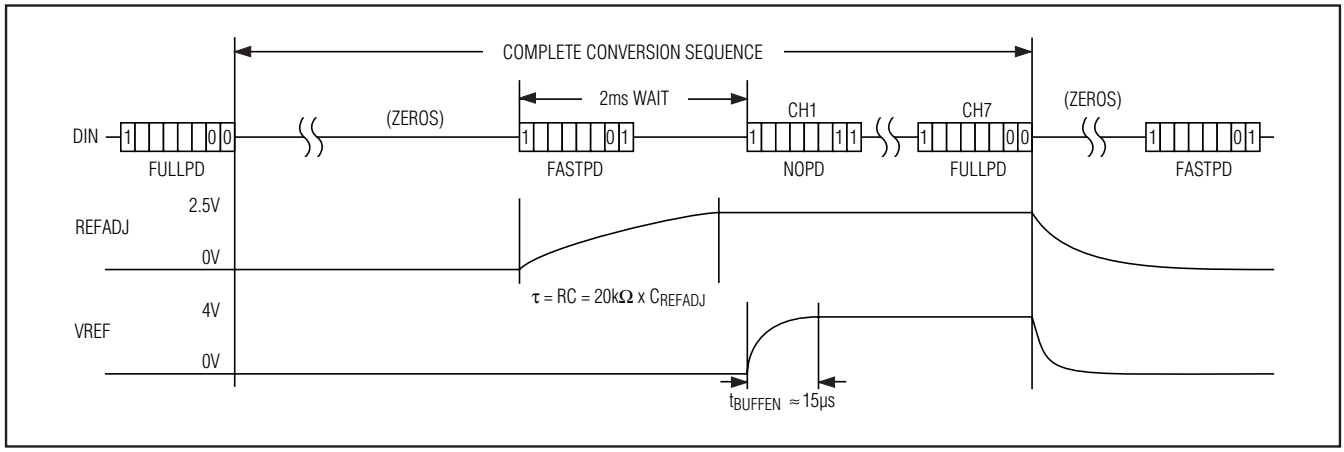


Figure 13. MAX186 FULLPD/FASTPD Power-Up Sequence

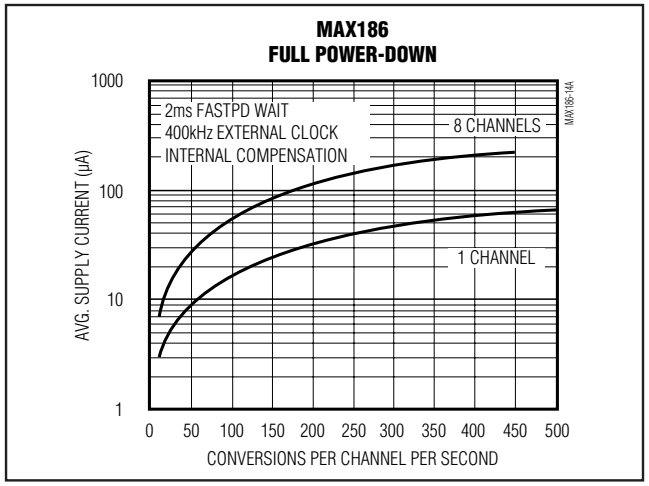


Figure 14a. MAX186 Supply Current vs. Sample Rate/Second, FULLPD, 400kHz Clock

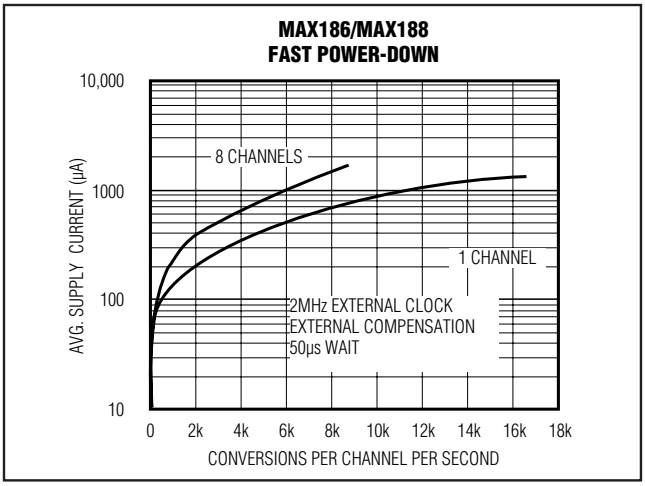


Figure 14b. MAX186/MAX188 Supply Current vs. Sample Rate/Second, FASTPD, 2MHz Clock

Lowest Power at Higher Throughputs

Figure 14b shows the power consumption with external-reference compensation in fast power-down, with one and eight channels converted. The external 4.7µF compensation requires a 50µs wait after power-up, accomplished by 75 idle clocks after a dummy conversion. This circuit combines fast multi-channel conversion with lowest power consumption possible. Full power-down mode may provide increased power savings in applications where the MAX186/MAX188 are inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

External and Internal References

The MAX186 can be used with an internal or external reference, whereas an external reference is required for the MAX188. Diode D1 shown in the *Typical Operating Circuit* ensures correct start-up. Any standard signal diode can be used. For both parts, an external reference can either be connected directly at the VREF terminal or at the REFADJ pin.

An internal buffer is designed to provide 4.096V at VREF for both the MAX186 and MAX188. The MAX186's internally trimmed 2.46V reference is buffered with a gain of 1.678. The MAX188's buffer is trimmed with a buffer gain of 1.638 to scale an external 2.5V reference at REFADJ to 4.096V at VREF.

MAX186 Internal Reference

The full-scale range of the MAX186 with internal reference is 4.096V with unipolar inputs, and ±2.048V with bipolar inputs. The internal reference voltage is adjustable to ±1.5% with the Reference-Adjust Circuit of Figure 17.

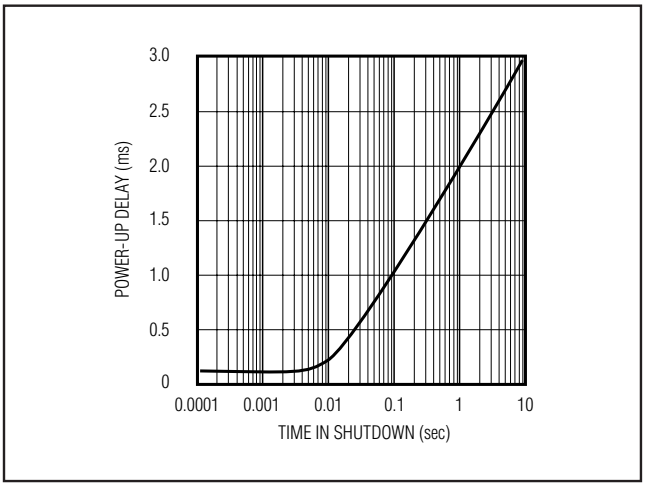


Figure 14c. Typical Power-Up Delay vs. Time in Shutdown

External Reference

With both the MAX186 and MAX188, an external reference can be placed at either the input (REFADJ) or the output (VREF) of the internal buffer amplifier. The REFADJ input impedance is typically 20kΩ for the MAX186 and higher than 100kΩ for the MAX188, where the internal reference is omitted. At VREF, the input impedance is a minimum of 12kΩ for DC currents. During conversion, an external reference at VREF must be able to deliver up to 350µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the VREF pin with a 4.7µF capacitor.

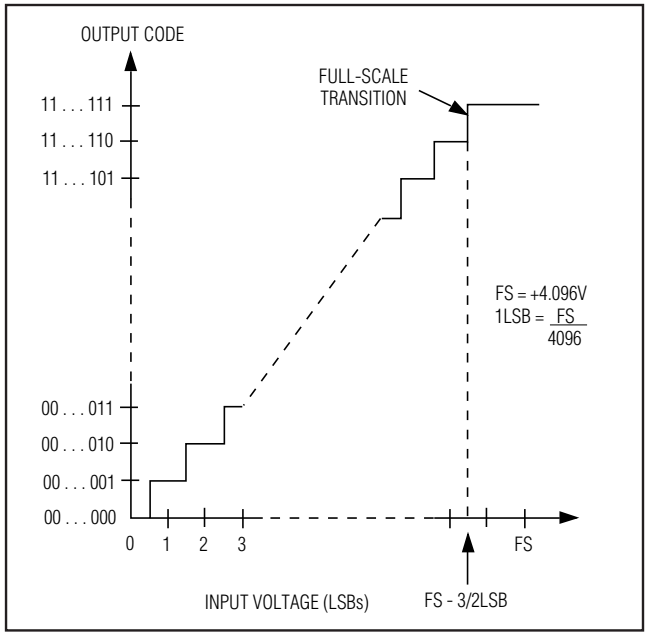


Figure 15. MAX186/MAX188 Unipolar Transfer Function, 4.096V = Full Scale

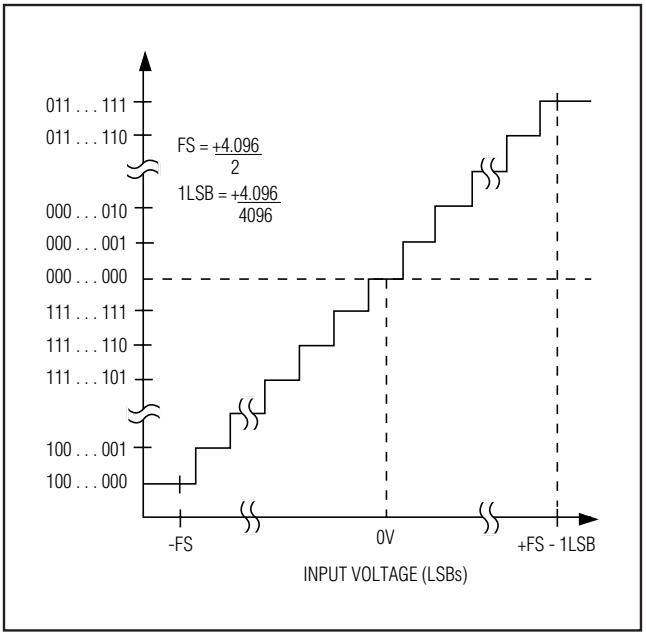


Figure 16. MAX186/MAX188 Bipolar Transfer Function, ±4.096V/2 = Full Scale

Using the buffered REFADJ input avoids external buffering of the reference. To use the direct VREF input, disable the internal buffer by tying REFADJ to V_{DD}.

Transfer Function and Gain Adjust

Figure 15 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 16 shows the bipolar input/output transfer function. Code transitions occur halfway between successive integer LSB values. Output coding is binary with 1 LSB = 1.00mV (4.096V/4096) for unipolar operation and 1 LSB = 1.00mV ((4.096V/2 - -4.096V/2)/4096) for bipolar operation.

Figure 17, the MAX186 Reference-Adjust Circuit, shows how to adjust the ADC gain in applications that use the internal reference. The circuit provides ±1.5% (±65LSBs) of gain adjustment range.

Layout, Grounding, Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 18 shows the recommended system ground connections. A single-point analog ground ("star" ground point) should be established at AGND, separate from the logic ground. All other analog grounds

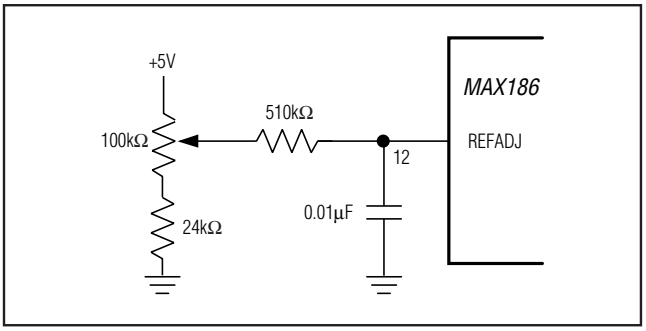


Figure 17. MAX186 Reference-Adjust Circuit

and DGND should be connected to this ground. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass these supplies to the single-point analog ground with 0.1µF and 4.7µF bypass capacitors close to the MAX186/MAX188. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected as a low-pass filter, as shown in Figure 18.

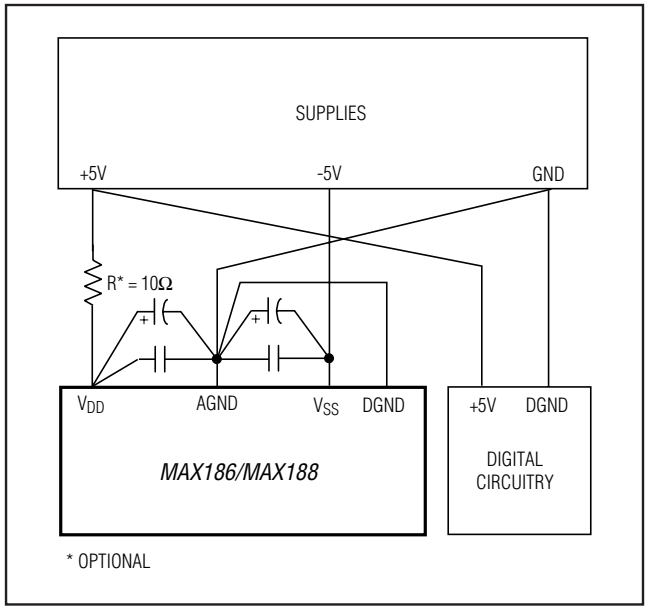


Figure 18. Power-Supply Grounding Connection

High-Speed Digital Interfacing with QSPI

The MAX186/MAX188 can interface with QSPI at high throughput rates using the circuit in Figure 19. This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU since QSPI incorporates its own micro-sequencer. Figure 19 depicts the MAX186, but the same circuit could be used with the MAX188 by adding an external reference to VREF and connecting REFADJ to V_{DD}.

Figure 20 details the code that sets up QSPI for autonomous operation. In external clock mode, the MAX186/MAX188 perform a single-ended, unipolar conversion on each of their eight analog input channels. Figure 21, QSPI Assembly-Code Timing, shows the timing associated with the assembly code of Figure 20. The first byte clocked into the MAX186/MAX188 is the control byte, which triggers the first conversion on CH0. The last two bytes clocked into the MAX186/MAX188 are all zero and clock out the results of the CH7 conversion.

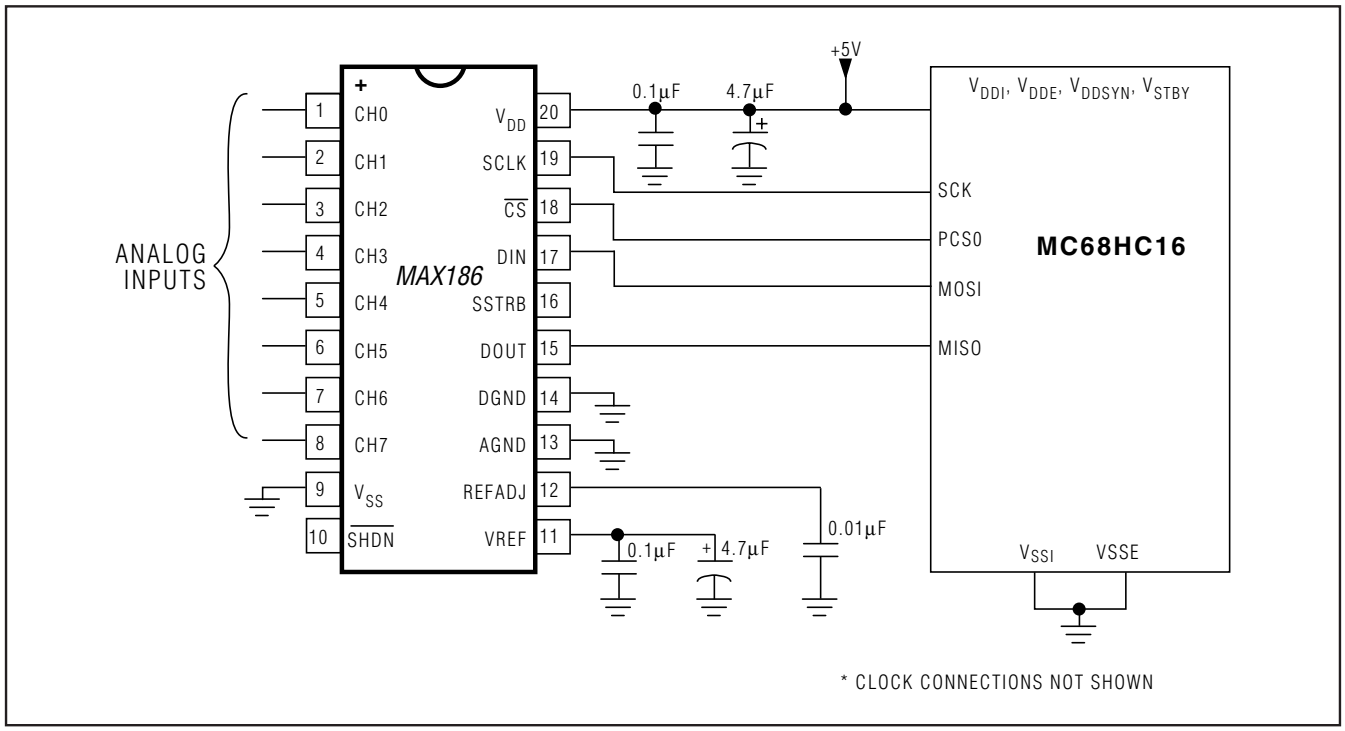


Figure 19. MAX186 QSPI Connection

```
*Title : MAX186.ASM
* Description :
*             This is a shell program for using a stand-alone 68HC16 without any external memory. The internal 1K RAM
*             is put into bank $0F to maintain 68HC11 code compatibility. This program was written with software
*             provided in the Motorola 68HC16 Evaluation Kit.
*
*  Roger J.A. Chen, Applications Engineer
*  MAXIM Integrated Products
*  November 20, 1992
*
*****************************************************************************************************************************************************************
      INCLUDE       'EQUATES.ASM'   ;Equates for common reg addrs
      INCLUDE       'ORG00000.ASM'  ;initialize reset vector
      INCLUDE       'ORG00008.ASM'  ;initialize interrupt vectors
      ORG     $0200                 ;start program after interrupt vectors
      INCLUDE  'INITSYS.ASM'        ;set EK=F,XK=0,YK=0,ZK=0
                                    ;set sys clock at 16.78 MHz, COP off
      INCLUDE  'INITRAM.ASM'        ;turn on internal SRAM at $10000
                                    ;set stack (SK=1, SP=03FE)
MAIN:
      JSR     INITQSPI
MAINLOOP:
      JSR     READ186
WAIT:
      LDAA    SPSR
      ANDA    #$80
      BEQ     WAIT                  ;wait for QSPI to finish
      BRA MAINLOOP
ENDPROGRAM:

INITQSPI:

;This routine sets up the QSPI microsequencer to operate on its own.
;The sequencer will read all eight channels of a MAX186/MAX188 each time
;it is triggered. The A/D converter results will be left in the
;receive data RAM. Each 16 bit receive data RAM location will
;have a leading zero, 12 bits of conversion result and three zeros.
;
;Receive RAM Bits 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
;A/D Result            0   MSB                                   LSB 0   0   0
*****  Initialize the QSPI Registers   ******
      PSHA
      PSHB
      LDAA    #%01111000
      STAA    QPDR              ;idle state for PCS0-3 = high
      LDAA    #%01111011
      STAA    QPAR              ;assign port D to be QSPI
      LDAA    #%01111110
      STAA    QDDR              ;only MISO is an input
      LDD     #$8008
      STD     SPCR0             ;master mode,16 bits/transfer,
                                ;CPOL=CPHA=0,1MHz Ser Clock
      LDD     #$0000
      STD     SPCR1             ;set delay between PCS0 and SCK,
```

Figure 20. MAX186/MAX188 Assembly-Code Listing

```
                                    ;set delay between transfers
      LDD    #$0800
      STD    SPCR2                 ;set ENDQP to $8 for 9 transfers
*****  Initialize QSPI Command RAM  *****

      LDAA   #$80          ;CONT=1,BITSE=0,DT=0,DSCK=0,PCS0=ACTIVE
      STAA   $FD40          ;store first byte in COMMAND RAM
      LDAA   #$C0          ;CONT=1,BITSE=1,DT=0,DSCK=0,PCS0=ACTIVE
      STAA   $FD41
      STAA   $FD42
      STAA   $FD43
      STAA   $FD44
      STAA   $FD45
      STAA   $FD46
      STAA   $FD47
      LDAA   #$40          ;CONT=0,BITSE=1,DT=0,DSCK=0,PCS0=ACTIVE
      STAA   $FD48
*****  Initialize QSPI Transmit RAM *****

      LDD    #$008F
                                    STD    $FD20
      LDD    #$00CF
                                    STD    $FD22
      LDD    #$009F
                                    STD    $FD24
      LDD    #$00DF
                                    STD    $FD26
      LDD    #$00AF
                                    STD    $FD28
      LDD    #$00EF
                                    STD    $FD2A
      LDD    #$00BF
                                    STD    $FD2C
      LDD    #$00FF
                                    STD    $FD2E
      LDD    #$0000
                                    STD    $FD30
      PULB
      PULA
      RTS

READ186:
;This routine triggers the QSPI microsequencer to autonomously
;trigger conversions on all 8 channels of the MAX186. Each
;conversion result is stored in the receive data RAM.
      PSHA
      LDAA   #$80
      ORAA   SPCR1
      STAA   SPCR1          ;just set SPE
      PULA
      RTS

*****  Interrupts/Exceptions  *****

BDM: BGND             ;exception vectors point here
                      ;and put the user in background debug mode
```

Figure 20. MAX186/MAX188 Assembly-Code Listing (continued)

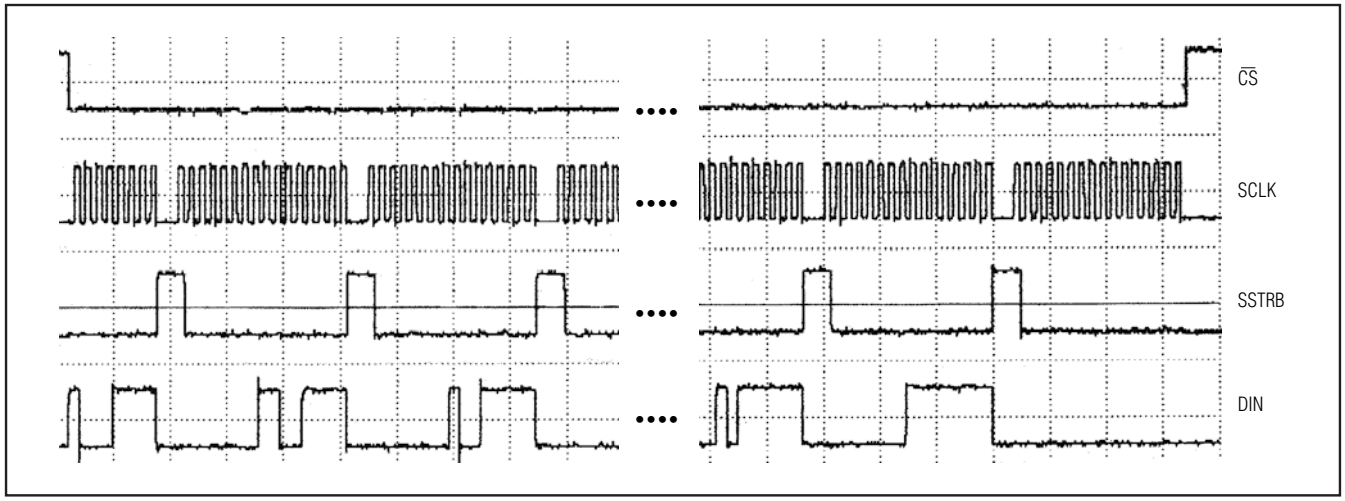


Figure 21. QSPI Assembly-Code Timing

TMS320C3x to MAX186 Interface

Figure 22 shows an application circuit to interface the MAX186/MAX188 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 23.

Use the following steps to initiate a conversion in the MAX186/MAX188 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR of the TMS320 are connected together with the SCLK input of the MAX186/MAX188.
2) The MAX186/MAX188 $\overline{CS}$ is driven low by the XF_ I/O port of the TMS320 to enable data to be clocked into DIN of the MAX186/MAX188.
3) An 8-bit word (1XXXXX11) should be written to the MAX186/MAX188 to initiate a conversion and place the device into external clock mode. Refer to Table 2 to select the proper XXXXX bit values for your specific application.
4) The SSTRB output of the MAX186/MAX188 is monitored via the FSR input of the TMS320. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX186/MAX188.

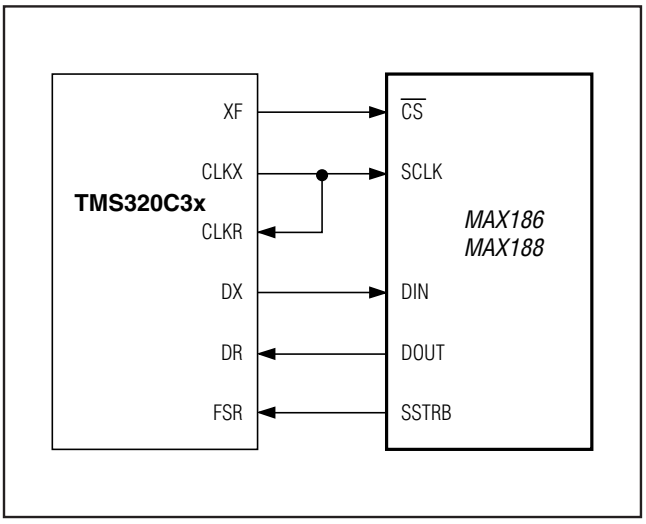


Figure 22. MAX186/MAX188 to TMS320 Serial Interface

5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 12-bit conversion result followed by four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX186/MAX188 until the next conversion is initiated.

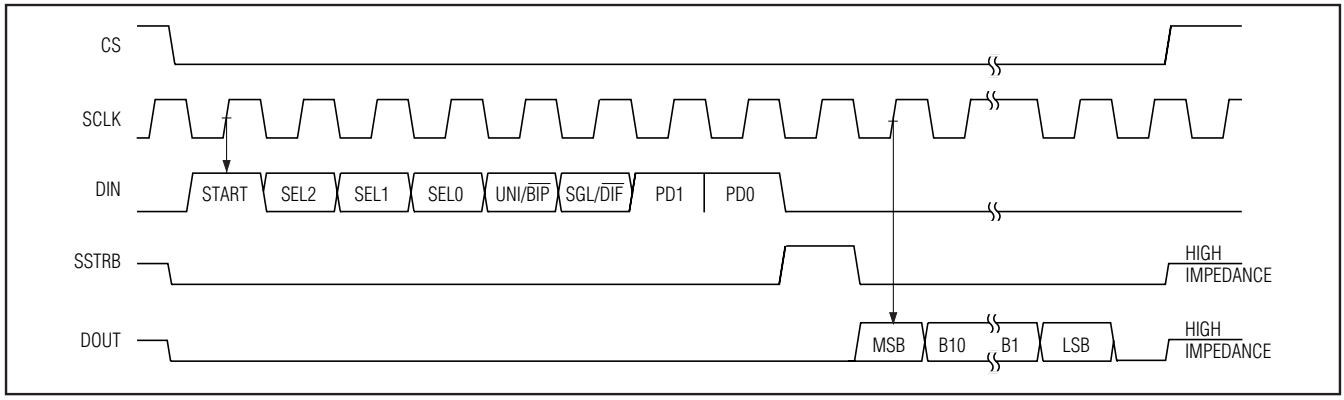
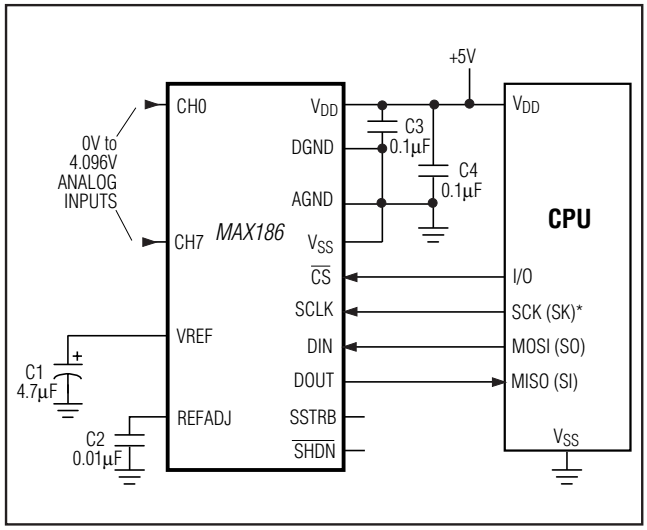


Figure 23. TMS320 Serial Interface Timing Diagram

Typical Operating Circuit



Ordering Information (continued)

PART†	TEMP RANGE	PIN-PACKAGE
MAX188_CPP+	0°C to +70°C	20 PDIP
MAX188_CWP+	0°C to +70°C	20 SO
MAX188_CAP+	0°C to +70°C	20 SSOP
MAX188DC/D	0°C to +70°C	Dice*
MAX188_EPP+	-40°C to +85°C	20 PDIP
MAX188_EWP+	-40°C to +85°C	20 SO
MAX188_EAP+	-40°C to +85°C	20 SSOP

PART	TEMP RANGE	BOARD TYPE
MAX186EVKIT-DIP	0°C to +70°C	Through-Hole

†Parts are offered in grades A, B, C and D (grades defined in Electrical Characteristics). When ordering, please specify grade. Contact factory for availability of A-grade in SSOP package.
**Dice are specified at +25°C, DC parameters only.*
+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

Substrate connected to V_{DD}

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 PDIP	P20+3	21-0043	—
20 SO	W20+3	21-0042	91-0108
20 SSOP	A20+1	21-0056	91-0094

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/93	Initial release	—
5	1/12	Updated the *Ordering Information* and *Electrical Characteristics*.	1, 3, 18