19-4689; Rev 0; 7/09

EVALUATION KIT AVAILABLE

1MHz, 2A, 2.6V to 5.5V Input, PWM DC-DC Step-Down Regulator with Enable

MAX1951A

General Description

The MAX1951A high-efficiency, DC-DC step-down switching regulator delivers up to 2A of output current. The device operates from an input voltage range of 2.6V to 5.5V and provides an adjustable output voltage from 0.8V to V_{IN}, making the MAX1951A ideal for on-board postregulation applications. The MAX1951A total output error is less than ±1.5% over load, line, and temperature.

The MAX1951A operates at a fixed frequency of 1MHz with an efficiency of up to 94%. The high operating frequency minimizes the size of external components. Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protection improve design reliability.

The MAX1951A can start up safely with a prebiased or without a preexisting output. This feature simplifies tracking supply designs for core and I/O applications and redundant supply designs.

The MAX1951A is available in an 8-pin SO package and operates over the -40°C to +85°C extended temperature range.

Applications

ASIC/DSP/µP/FPGA Core and I/O Voltages

Set-Top Boxes

Networking and Telecommunications

Servers

TVs

Features

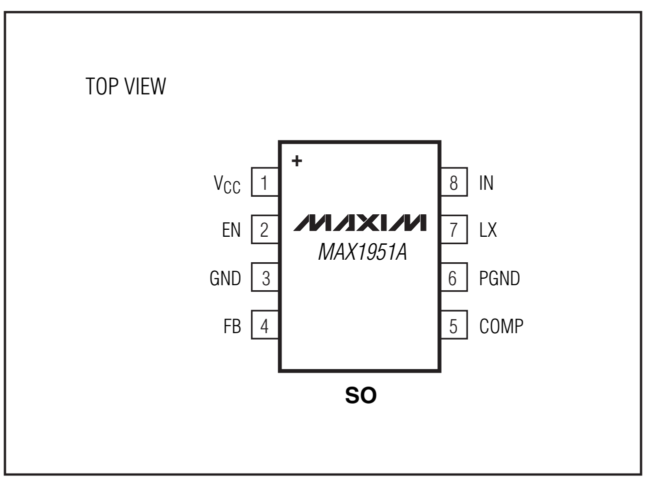
- **Compact 0.385in² Circuit Footprint**
- **10µF Ceramic Input and Output Capacitors, 2µH Inductor for 2A Output**
- **Efficiency Up to 94%**
- **1.5% Output Accuracy Over Load, Line, and Temperature**
- **Guaranteed 2A Output Current**
- **Operates from 2.6V to 5.5V Supply**
- **Adjustable Output from 0.8V to V_{IN}**
- **Internal Digital Soft-Soft**
- **Short-Circuit and Thermal-Overload Protection**
- **1MHz Switching Frequency Reduces Component Size**
- **Enable Input Audio Shutdown for Reducing Power Consumption**
- **Safe Startup into Prebiased Output**

Ordering Information

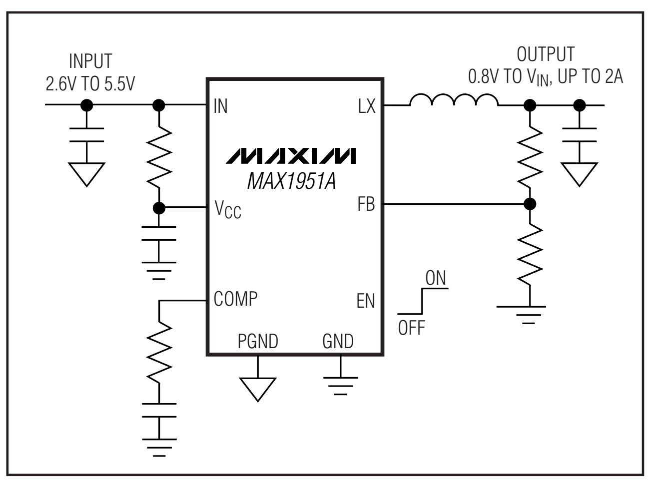
PART	TEMP RANGE	PIN-PACKAGE
MAX1951AESA+	-40°C to +85°C	8 SO

+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configuration



Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

1MHz, 2A, 2.6V to 5.5V Input, PWM DC-DC Step-Down Regulator with Enable

ABSOLUTE MAXIMUM RATINGS

IN, V_{CC} to GND ....-0.3V to +6V
COMP, FB, EN to GND..............................-0.3V to (V_{CC} + 0.3V)
LX Current (Note 1)..±4.5A
PGND to GND...Internally connected
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 12.2mW/°C above +70°C)................976mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 2)
8-Pin SO ....32°C/W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature Range ....-40°C to +150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: LX has internal clamp diodes to PGND and IN. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{CC} = V_{EN} = 3.3V, V_{PGND} = V_{GND} = 0V, FB in regulation, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN AND V_{CC}						
IN Voltage Range			2.6		5.5	V
Supply Current	Switching with no load, LX floating	V_{IN} = 5.5V		7	10	mA
Shutdown Current	EN = GND			0.1	0.4	mA
V_{CC} Undervoltage Lockout Threshold	When LX starts/stops switching	V_{CC} rising		2.19	2.32	V
		V_{CC} falling	1.92	2.07		
COMP						
COMP Transconductance	From FB to COMP, V_{COMP} = 0.8V		40	50	80	µS
COMP Clamp Voltage, Low	V_{IN} = 2.6V to 5.5V, V_{FB} = 0.9V		0.6	1	1.45	V
COMP Clamp Voltage, High	V_{IN} = 2.6V to 5.5V, V_{FB} = 0.7V		1.97	2.13	2.28	V
FB						
Output Voltage Range	When using external feedback resistors to drive FB		0.8		V_{IN}	V
FB Regulation Voltage (Error Amplifier Only)	I_{OUT} = 0A to 1.5A, V_{IN} = 2.6V to 5.5V	T_A = 0°C to +85°C	0.789	0.796	0.804	V
		T_A = -40°C to +85°C	0.786		0.804	
FB Input Bias Current	PNP input stage		-0.1		+0.1	µA
LX						
LX On-Resistance, PMOS	I_{LX} = -180mA	V_{IN} = 5V		119		mΩ
		V_{IN} = 3.3V		145	266	
		V_{IN} = 2.6V		171		
LX On-Resistance, NMOS	I_{LX} = 180mA	V_{IN} = 5V		122		mΩ
		V_{IN} = 3.3V		133	246	
		V_{IN} = 2.6V		142		

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = V_{CC} = V_{EN} = 3.3V$, $V_{PGND} = V_{GND} = 0V$, FB in regulation, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = +25°C$.) (Note 3)

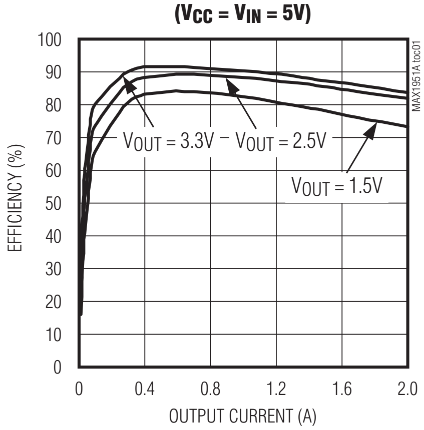
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LX Current-Sense Transimpedance	From LX to COMP, V_{IN} = 2.6V to 5.5V		0.16	0.24	0.35	Ω
LX Current-Limit Threshold	Duty = 100%, V_{IN} = 2.6V to 5.5V	High side	2.2	3.1	4.5	A
		Low side		-0.3		
LX Leakage Current	V_{IN} = 5.5V	V_{LX} = 5.5V			10	µA
		V_{LX} = 0V	-10			
LX Switching Frequency	V_{IN} = 2.6V to 5.5V		0.8	0.96	1.1	MHz
LX Maximum Duty Cycle	V_{COMP} = 1.5V, LX = Hi-Z, V_{IN} = 2.6V to 5.5V		100			%
LX Minimum Duty Cycle	V_{COMP} = 1V, IN = 2.6V to 5.5V			15		%
THERMAL						
Thermal Shutdown Threshold	When LX starts/stops switching	T_J rising		165		°C
		T_J falling		155		
EN						
Enable Low Threshold (V_{IL})			0.8			V
Enable High Threshold (V_{IH})					2.0	V
EN Input Current					1	µA

Note 3: Specifications to $T_A = -40°C$ are guaranteed by design and not production tested.

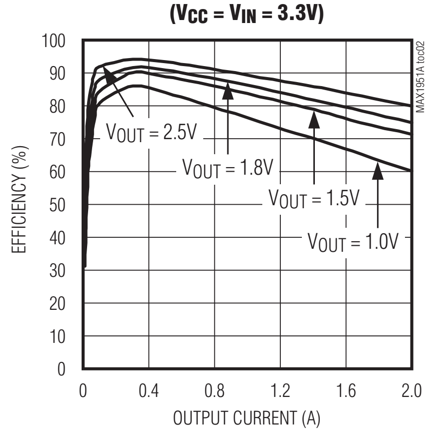
Typical Operating Characteristics

(Typical values are at $V_{IN} = V_{CC} = 5V$, $V_{OUT} = 1.5V$, $I_{OUT} = 1.5A$, and $T_A = +25°C$, unless otherwise noted. See Figure 2.)

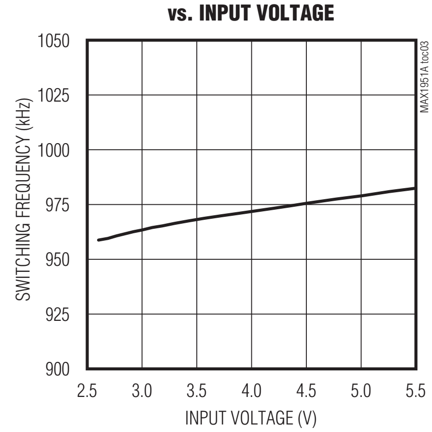
EFFICIENCY vs. OUTPUT CURRENT ($V_{CC} = V_{IN} = 5V$)



EFFICIENCY vs. OUTPUT CURRENT ($V_{CC} = V_{IN} = 3.3V$)



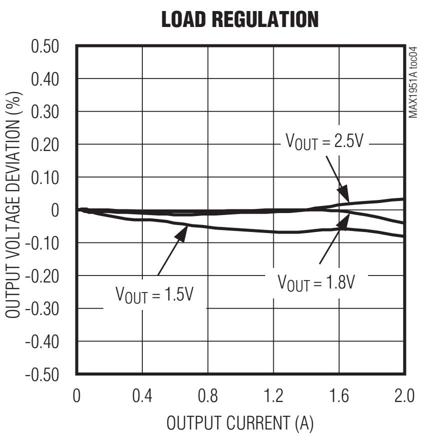
SWITCHING FREQUENCY vs. INPUT VOLTAGE

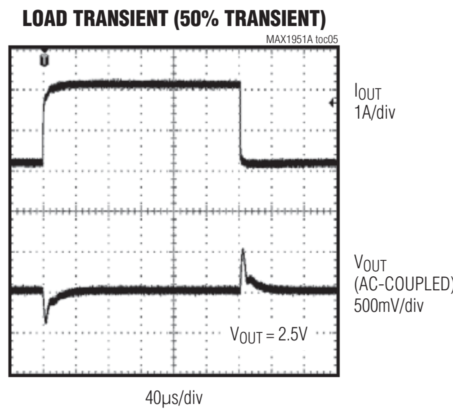


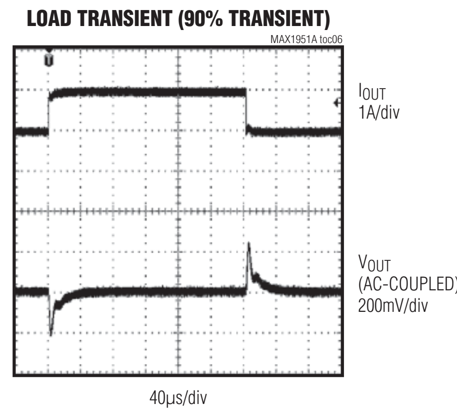
1MHz, 2A, 2.6V to 5.5V Input, PWM DC-DC Step-Down Regulator with Enable

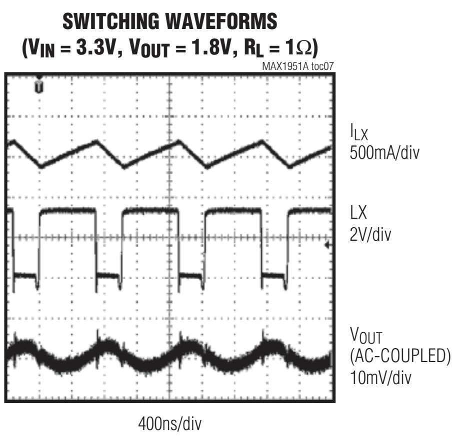
Typical Operating Characteristics (continued)

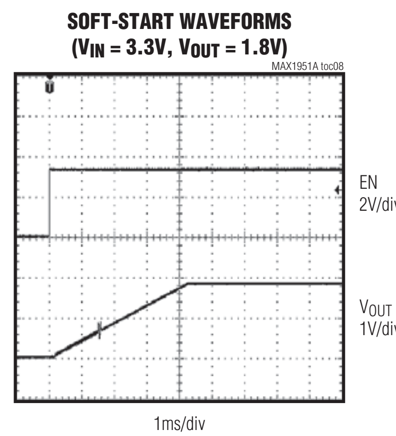
(Typical values are at V_{IN} = V_{CC} = 5V, V_{OUT} = 1.5V, I_{OUT} = 1.5A, and T_A = +25°C, unless otherwise noted. See Figure 2.)

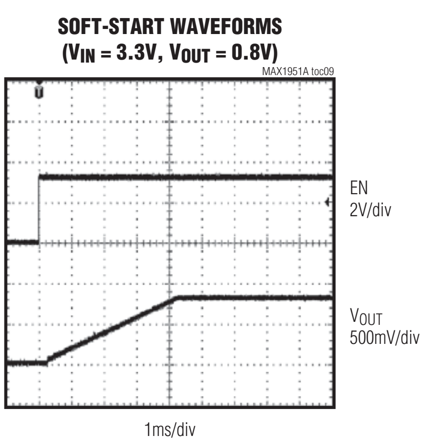


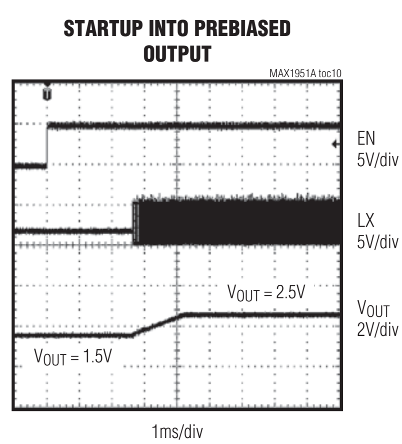










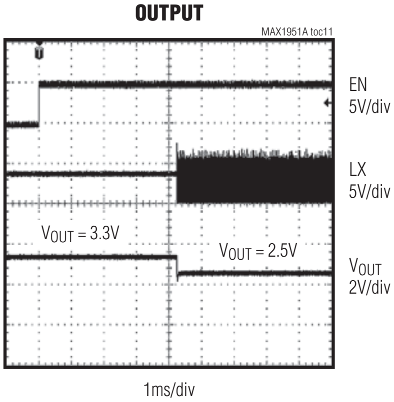


1MHz, 2A, 2.6V to 5.5V Input, PWM DC-DC Step-Down Regulator with Enable

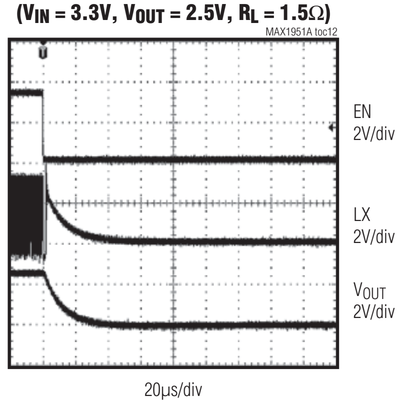
Typical Operating Characteristics (continued)

(Typical values are at V_{IN} = V_{CC} = 5V, V_{OUT} = 1.5V, I_{OUT} = 1.5A, and T_A = +25°C, unless otherwise noted. See Figure 2.)

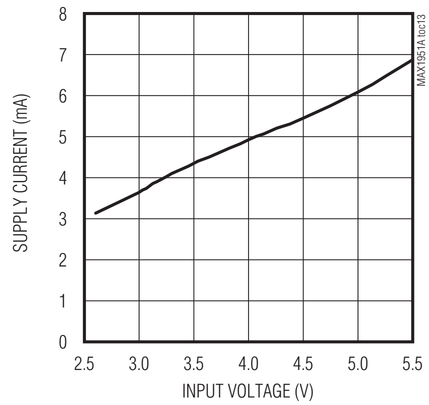
STARTUP INTO PREBIASED OUTPUT



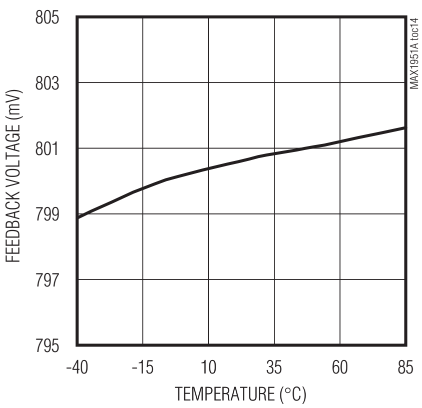
SHUTDOWN WAVEFORMS (V_{IN} = 3.3V, V_{OUT} = 2.5V, R_L = 1.5Ω)



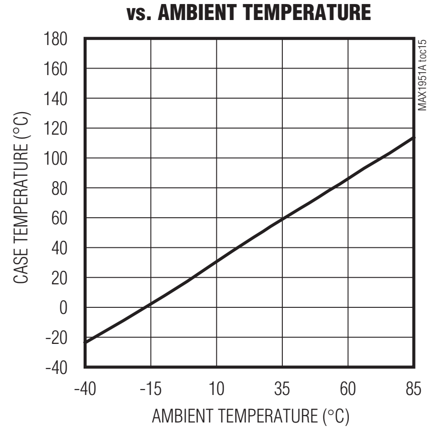
SUPPLY CURRENT vs. INPUT VOLTAGE



FEEDBACK VOLTAGE vs. TEMPERATURE



CASE TEMPERATURE vs. AMBIENT TEMPERATURE



1MHz, 2A, 2.6V to 5.5V Input, PWM DC-DC Step-Down Regulator with Enable

Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Supply Voltage. Bypass with a 0.1µF capacitor to ground and a 10Ω resistor to IN.
2	EN	Enable Input. Connect to V_{CC} for normal operation. Connect to GND to disable the MAX1951A.
3	GND	Signal Ground
4	FB	Feedback Input. Connect an external resistor-divider from the output to FB and GND to set the output to a voltage between 0.8V and V_{IN}.
5	COMP	Regulator Compensation. Connect series RC network to GND.
6	PGND	Power Ground. Internally connected to GND. Keep power ground and signal ground planes separate.
7	LX	Inductor Connection. Connect an inductor between LX and the regulator output.
8	IN	Power-Supply Voltage. Input voltage range from 2.6V to 5.5V. Bypass with a 10µF (min) ceramic capacitor to GND and a 10Ω resistor to V_{CC}.

Detailed Description

The MAX1951A high-efficiency switching regulator is a small, simple, current-mode DC-DC step-down converter capable of delivering up to 2A of output current. The device operates in pulse-width modulation (PWM) at a fixed frequency of 1MHz from a 2.6V to 5.5V input voltage and provides an output voltage from 0.8V to V_{IN}, making the MAX1951A ideal for on-board postregulation applications. The high switching frequency allows for the use of smaller external components, and an internal synchronous rectifier improves efficiency and eliminates the typical Schottky free-wheeling diode. Using the on-resistance of the internal high-side MOSFET to sense switching currents eliminates current-sense resistors, further improving efficiency and cost. The MAX1951A total output error over load, line, and temperature (-40°C to +85°C) is less than 1.5%.

Controller Block Function

The MAX1951A step-down converter uses a PWM current-mode control scheme. An open-loop comparator compares the integrated voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator trips. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current-mode feedback system regulates the peak inductor current as a function of the output-voltage error signal. Since the average inductor current is nearly the same as the peak inductor current (< 30% ripple current), the circuit acts as a switch-mode transconductance amplifier. To preserve inner-loop stability and eliminate inductor staircasing, a slope-compensation ramp is summed into the main PWM comparator. During the second half of the cycle, the internal high-side p-channel MOSFET turns off, and the internal low-side n-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output. The output capacitor stores charge when the inductor current exceeds the load current, and discharges when the inductor current is lower, smoothing the voltage across the load. Under overload conditions, when the inductor current exceeds the current limit (see the *Current Limit* section), the high-side MOSFET does not turn on at the rising edge of the clock and the low-side MOSFET remains on to let the inductor current ramp down.

Current Sense

An internal current-sense amplifier produces a current signal proportional to the voltage generated by the high-side MOSFET on-resistance and the inductor current ($R_{DS(ON)}$ x I_{LX}). The amplified current-sense signal and the internal slope compensation signal are summed together into the comparator's inverting input. The PWM comparator turns off the internal high-side MOSFET when this sum exceeds the output from the voltage-error amplifier.

Current Limit

The internal high-side MOSFET has a current limit of 3.1A (typ). If the current flowing out of LX exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. This lowers the duty cycle and causes the output voltage to droop until the current limit is no longer exceeded. A synchronous rectifier current limit of -0.6A (typ) protects the device from current flowing into LX. If the negative current limit is exceeded, the synchronous rectifier turns off, forcing the inductor current to flow through the high-side MOSFET body diode, back to the input, until the beginning of the next cycle or until the inductor current drops to zero. The MAX1951A utilizes a pulse-skip mode to prevent overheating during short-circuit output conditions. The device enters pulse-skip mode when the FB voltage drops below 300mV, limiting the current to 3A (typ) and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

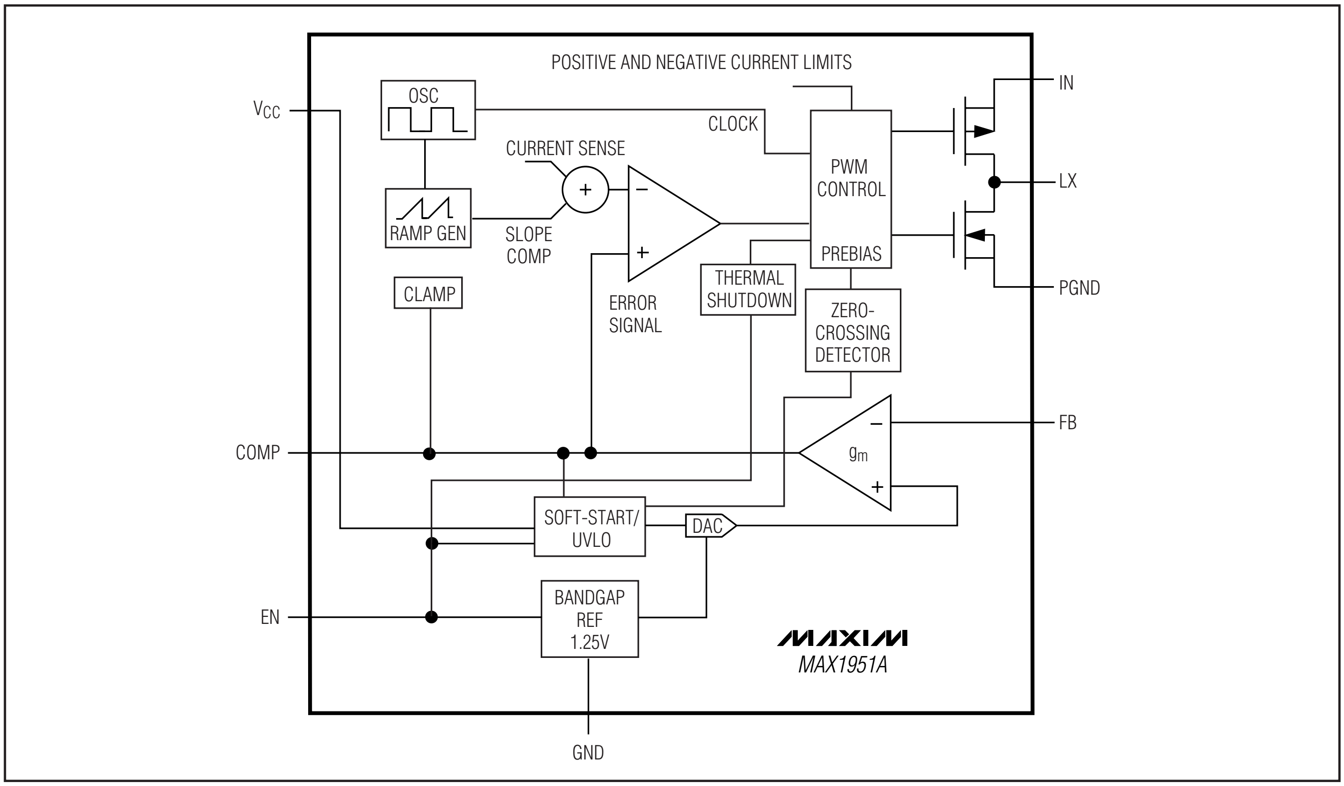


Figure 1. Functional Diagram

V_{CC} Decoupling

Due to the high switching frequency and tight output tolerance (1.5%), decouple V_{CC} with a 0.1µF capacitor connected from V_{CC} to GND, and a 10Ω resistor connected from V_{CC} to IN. Place the capacitor as close as possible to V_{CC}.

Soft-Start

The MAX1951A employs digital soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits undervoltage lockout (UVLO) shutdown mode, or restarts following a thermal-overload event, or EN is driven high, the digital soft-start circuitry slowly ramps up the voltage to the error-amplifier noninverting input.

Undervoltage Lockout

If V_{CC} drops below 2.07V, the UVLO circuit inhibits switching. Once V_{CC} rises above 2.19V, the UVLO clear and the soft-start sequence activates.

Shutdown Mode

Use the enable input, EN, to turn on or off the MAX1951A. Connect EN to V_{CC} for normal operation. Connect EN to GND to place the device in shutdown. Shutdown causes the internal switches to stop switching and forces LX into a high-impedance state. In shutdown, the MAX1951A draws 500µA of supply current. The device initiates a soft-start sequence when brought out of shutdown.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds T_J = +165°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 9°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

Safe Startup into Prebiased Output

The MAX1951A can start up safely even with a prebiased output. A zero crossover detection (ZCD) circuit turns on the switches only after the soft-start ramping voltage equals the prebiased output voltage. If the prebiased output voltage is greater than the set voltage, the ZCD circuit turns on the low-side switch (after the soft-start period is over) to discharge the output capacitor until its voltage equals the set voltage.

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Design Procedure

Adjustable Output Voltage

The MAX1951A provides an adjustable output voltage between 0.8V and V_{IN}. Connect FB to output for 0.8V output. To set the output voltage of the MAX1951A to a voltage greater than V_{FB} (0.8V typ), connect the output to FB and GND using a resistive divider, as shown in Figure 2. Choose R2 between 2kΩ and 20kΩ, and set R3 according to the following equation:

$$R3 = R2 \times [(V_{OUT}/V_{FB}) - 1]$$

The MAX1951A PWM circuitry is capable of a stable minimum duty cycle of 18%. This limits the minimum output voltage that can be generated to $0.18 \times V_{IN}$ with an absolute minimum of 0.8V. Instability may result for V_{IN}/V_{OUT} ratios below 0.18.

Output Inductor Design

Use a 2µH inductor with a minimum 2A-rated DC current for most applications. For best efficiency, use an inductor with a DC resistance of less than 20mΩ and a saturation current greater than 3A (min). See Table 2 for recommended inductors and manufacturers. For most designs, derive a reasonable inductor value (L_{INIT}) from the following equation:

$$L_{INIT} = V_{OUT} \times (V_{IN} - V_{OUT})/(V_{IN} \times LIR \times I_{OUT(MAX)} \times f_{SW})$$

where f_{SW} is the switching frequency (1MHz typ) of the oscillator. Keep the inductor current ripple percentage LIR between 20% and 40% of the maximum load current for the best compromise of cost, size, and performance. Calculate the maximum inductor current as:

$$I_{L(MAX)} = (1 + LIR/2) \times I_{OUT(MAX)}$$

Check the final values of the inductor with the output ripple voltage requirement. The output ripple voltage is given by:

$$V_{RIPPLE} = V_{OUT} \times (V_{IN} - V_{OUT}) \times ESR/(V_{IN} \times L_{FINAL} \times f_{SW})$$

where ESR is the equivalent series resistance of the output capacitors.

Input Capacitor Design

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = (1/V_{IN}) \times \sqrt{(I_{OUT}^2 \times V_{OUT} \times (V_{IN} - V_{OUT}))}$$

For duty ratios less than 0.5, the input capacitor RMS current is higher than the calculated current. Therefore, use a +20% margin when calculating the RMS current at lower duty cycles. Use ceramic capacitors for their low ESR and equivalent series inductance (ESL). Choose a capacitor that exhibits less than 10°C temperature rise at the maximum operating RMS current for optimum long-term reliability.

After determining the input capacitor, check the input ripple voltage due to capacitor discharge when the high-side MOSFET turns on. Calculate the input ripple voltage as follows:

$$V_{IN\_RIPPLE} = (I_{OUT} \times V_{OUT})/(f_{SW} \times V_{IN} \times C_{IN})$$

Keep the input ripple voltage less than 3% of the input voltage.

Output Capacitor Design

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and the voltage rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Calculate the output voltage ripple due to the output capacitance, ESR, and ESL as:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

where the output ripple due to output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = I_{P-P}/(8 \times C_{OUT} \times f_{SW})$$

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = (I_{P-P}/t_{ON}) \times ESL \text{ or } (I_{P-P}/t_{OFF}) \times ESL,$$
whichever is greater

and I_{P-P} the peak-to-peak inductor current is:

$$I_{P-P} = [(V_{IN} - V_{OUT})/f_{SW} \times L)] \times V_{OUT}/V_{IN}$$

Use these equations for initial capacitor selection, but determine final values by testing a prototype or evaluation circuit. As a rule, a smaller ripple current results in less output-voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output-voltage ripple decreases with larger inductance. Use ceramic capacitors for their low ESR and ESL at the switching frequency of the converter. The low ESL of ceramic capacitors makes ripple voltages negligible. Load-transient response depends on the selected output capacitor. During a load transient, the output instantly changes by ESR x ΔI_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time (see the Load Transient graph in the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on the closed-loop bandwidth. A higher bandwidth yields a faster response time, thus preventing the output from deviating further from its regulating value.

Compensation Design

The double pole formed by the inductor and output capacitor of most voltage-mode controllers introduces a large phase shift that requires an elaborate compensation network to stabilize the control loop. The MAX1951A utilizes a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor, eliminating the double pole caused by the inductor and output capacitor, and greatly simplifying the compensation network. A simple type 1 compensation with single compensation resistor (R_1) and compensation capacitor (C_2) in Figure 2 creates a stable and high-bandwidth loop.

An internal transconductance error amplifier compensates the control loop. Connect a series resistor and capacitor between COMP (the output of the error amplifier) and GND to form a pole-zero pair. The external inductor, internal current-sensing circuitry, output capacitor, and the external compensation circuit determine the loop system stability. Choose the inductor and output capacitor based on performance, size, and cost. Additionally, select the compensation resistor and capacitor to optimize control-loop stability. The component values shown in the typical application circuit (Figure 2) yield stable operation over a broad range of input-to-output voltages.

The basic regulator loop consists of a power modulator, an output feedback divider, and an error amplifier. The power modulator has DC gain set by $g_{mc} \times R_{LOAD}$, with a pole-zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. The following equations define the power modulator:

Modulator gain:

$$G_{MOD} = \Delta V_{OUT} / \Delta V_{COMP} = g_{mc} \times R_{LOAD}$$

Modulator pole frequency:

$$fp_{MOD} = 1/(2 \times \pi \times C_{OUT} \times (R_{LOAD} + ESR))$$

Modulator zero frequency:

$$fz_{ESR} = 1/(2 \times \pi \times C_{OUT} \times ESR)$$

where $R_{LOAD} = V_{OUT}/I_{OUT(MAX)}$ and gmc = 4.2S.

The feedback divider has a gain of $G_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is equal to 0.8V. The transconductance error amplifier has a DC gain, $G_{EA(DC)}$, of 70dB. The compensation capacitor, C_2, and the output resistance of the error amplifier, R_{OEA} (20MΩ), set the dominant pole. C_2 and R_1 set a compensation zero. Calculate the dominant pole frequency as:

$$fp_{EA} = 1/(2\pi \times C_2 \times R_{OEA})$$

Determine the compensation zero frequency as:

$$fz_{EA} = 1/(2\pi \times C_2 \times R_1)$$

For best stability and response performance, set the closed-loop unity-gain frequency much higher than the modulator pole frequency. In addition, set the closed-loop crossover unity-gain frequency less than, or equal to 1/5 of the switching frequency. However, set the maximum zero crossing frequency to less than 1/3 of the zero frequency set by the output capacitance and its ESR when using POSCAP, SPCAP, OSCON, or other electrolytic capacitors. The loop-gain equation at the unity-gain frequency is:

$$G_{EA(fc)} \times G_{MOD(fc)} \times V_{FB}/V_{OUT} = 1$$

where $G_{EA(fc)} = gm_{EA} \times R_1$, and $G_{MOD(fc)} = g_{mc} \times R_{LOAD} \times fp_{MOD}/f_C$, where $gm_{EA} = 60\mu S$.

R_1 calculated as:

$$R_1 = V_{OUT} \times K/(gm_{EA} \times V_{FB} \times G_{MOD(fc)})$$

where K is the correction factor due to the extra phase introduced by the current loop at high frequencies (>100kHz). K is related to the value of the output capacitance (see Table 1 for values of K vs. C). Set the error-amplifier compensation zero formed by R_1 and C_2 at the modulator pole frequency at maximum load. C_2 is calculated as follows:

$$C_2 = (2 \times V_{OUT} \times C_{OUT}/(R_1 \times I_{OUT(MAX)})$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly, resulting in a constant closed-loop unity-gain frequency. Use the following numerical example to calculate R_1 and C_2 values of the typical application circuit of Figure 2.

$V_{OUT} = 1.5V$

$I_{OUT(MAX)} = 2A$

Table 1. K Value

		DESCRIPTION
C_{OUT} (µF)	K	Values are for output inductance from 1.2µH to 2.2µH. Do not use output inductors larger than 2.2µH. Use f_C = 200kHz to calculate R_1.
10	0.55	
22	0.47	

$C_{OUT} = 10\mu F$

$R_{ESR} = 0.010\Omega$

$gm_{EA} = 60\mu S$

gmc = 4.2S

$f_{SWITCH} = 1MHz$

$R_{LOAD} = V_{OUT}/I_{OUT(MAX)} = 1.5V/2A = 0.75\Omega$

$fp_{MOD} = [1/(2\pi \times C_{OUT} \times (R_{LOAD} + R_{ESR})]$
$= [1/(2 \times \pi \times 10 \times 10^{-6} \times (0.75 + 0.01)] = 20.9Hz.$

$fz_{ESR} = [1/(2\pi \times C_{OUT} \times R_{ESR})]$
$= [1/(2 \times \pi \times 10 \times 10^{-6} \times 0.01)] = 1.59MHz.$

For a 2µH output inductor, pick the closed-loop unity-gain crossover frequency (f_C) at 200kHz. Determine the power modulator gain at f_C:

$$G_{MOD(fc)} = gmc \times R_{LOAD} \times fp_{MOD}/f_C = 4.2 \times 0.75 \times 20.9kHz/200kHz = 0.33$$

then:

$$R_1 = V_O \times K/(g_{mEA} \times V_{FB} \times G_{MOD(fC)}) = (1.5 \times 0.55)/(60 \times 10^{-6} \times 0.8 \times 0.33) \approx 52.3k\Omega \ (1\%)$$

$$C_2 = (2 \times V_{OUT} \times C_{OUT})/R_1 \times I_{OUT(MAX)} = (2 \times 1.5 \times 10 \times 10^{-6})/(52.3k\Omega \times 2) \approx 143pF, \text{ choose } 150pF, 10\%$$

Applications Information

PCB Layout Considerations

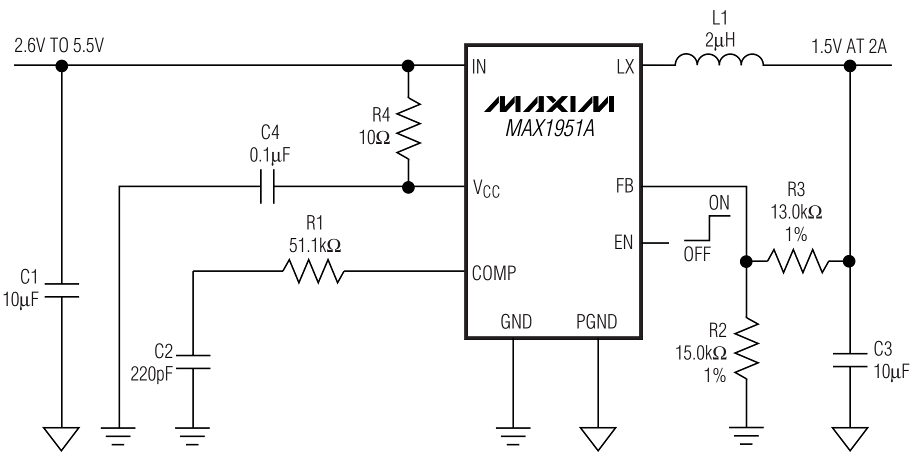
Careful PCB layout is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow these guidelines for good PCB layout:

1) Place decoupling capacitors as close as possible to the IC. Keep the power ground plane (connected to PGND) and signal ground plane (connected to GND) separate.
2) Connect input and output capacitors to the power ground plane; connect all other capacitors to the signal ground plane.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current (C1 to IN and C1 to PGND) short. Avoid vias in the switching paths.
4) If possible, connect IN, LX, and PGND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short and direct. Place the feedback resistors as close as possible to the IC.
6) Route high-speed switching nodes away from sensitive analog areas (FB, COMP).

Thermal Considerations

See the MAX1951A Evaluation Kit for an optimized layout example. Thermal performance can be further improved with one of the following options:

1) Increase the copper areas connected to GND, LX, and IN.
2) Provide thermal vias next to GND and IN, to the ground plane and power plane on the back side of PCB with openings in the solder mask next to the vias to provide better thermal conduction.
3) Provide forced-air cooling to further reduce case temperature.



OUTPUT VOLTAGE (V)	COMPONENT VALUES			
	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	C2 (pF)
0.8	10	OPEN	SHORT	470
1.5	52.3	15	13	150
2.5	86.6	15	31.6	150
3.3	115	15	46.4	150

Figure 2. MAX1951A Adjustable Output Typical Application Circuit

Table 2. External Components List

COMPONENT (FIGURE 2)	FUNCTION	DESCRIPTION
L1	Output inductor	2µH ±20% inductor Sumida CDRH4D28-1R8 or TOKO A915AY-2R0M
C1	Input filtering capacitor	10µF ±20%, 6.3V X5R capacitor Taiyo Yuden JMK316BJ106ML or TDK C3216X5R0J106MT
C2	Compensation capacitor	220pF ±10%, 50V capacitor Murata GRM1885C1HZZ1JA01 or Taiyo Yuden UMK107CH221KZ
C3	Output filtering capacitor	10µF ±20%, 6.3V X5R capacitor Taiyo Yuden JMK316BJ106ML or TDK C3216X5R0J106MT
C4	V_{CC} bypass capacitor	0.1µF ±20%, 16V X7R capacitor Taiyo Yuden EMK107BJ104MA, TDK C1608X7R1C104K, or Murata GRM188R171C104KA01
R1	Loop compensation resistor	Figure 2
R2	Feedback resistor	Figure 2
R3	Feedback resistor	Figure 2
R4	Bypass resistor	10Ω ±5% resistor

Table 3. Component Suppliers

MANUFACTURER	WEBSITE
Murata Electronics North America, Inc.	www.murata-northamerica.com
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 SO	S8-6F	21-0041

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