EVALUATION KIT AVAILABLE

Click here to ask an associate for production status of specific part numbers.

Automotive Hi-Speed USB 2.0 Protectors

MAX20042F–MAX20044F

General Description

The MAX20042F, MAX20043F, and MAX20044F devices provide high ESD and short-circuit protection for the low-voltage internal USB data and USB power line in automotive radio, navigation, connectivity, and USB hub applications. The devices support USB Hi-Speed (480Mbps), USB full-speed (12Mbps), and USB low-speed (1.5Mbps) operation, as well as USB on-the-go (OTG) functionality.

The short-circuit protection features include short-to-battery on the protected HVBUS, HVD+, and HVD- outputs, as well as short-to-HVBUS on the protected HVD+ and HVD- outputs. The devices are capable of a short-to-battery condition of up to +18V. Short-to-GND protection and overcurrent protection are also provided on the protected HVBUS output to protect the internal BUS power rail from an overcurrent fault.

The devices feature high ESD protection to ±15kV Air Gap and ±8kV Contact on the protected HVBUS, HVD+, and HVD- outputs.

The devices feature a low on-resistance (R_{ON}), 90mΩ (max) USB power switch, and two low on-resistance (R_{ON}), 4Ω (typ) USB 2.0 data switches. These devices also feature an enable input, a fault output, a 10ms fault-recovery time, a 1ms overcurrent blanking time, and an integrated overcurrent autoretry.

The MAX20042F, MAX20043F, and MAX20044F are available in a lead-free, 16-pin QSOP package and operate over the -40°C to +105°C temperature range.

Benefits and Features

- Accurate Bus Current Limiting with Minimal Voltage Drop
  - Low R_{ON} 90mΩ (max) USB Power Switch
  - 0.65A (typ), MAX20042F
  - 1.0A (typ), MAX20043F
  - 1.3A (typ), MAX20044F
- Targeted Features for Optimized USB Performance
  - Two R_{ON} 4Ω (typ) USB 2.0 Data Switches
  - 480Mbps or 12Mbps USB 2.0 Operation
  - 10ms Fault-Recovery Time
  - 1ms Overcurrent Blanking Time
  - 5.67V (typ) Fixed HVBUS Protection Trip Threshold
- Robust for the Automotive Environment
  - Short-to-Battery and Short-to-GND Protection on Protected HVBUS Output
  - Short-to-Battery and Short-to-BUS Protection on Protected HVD+ and HVD- Outputs
  - Tested to ISO 10605 and IEC 61000-4-2 ESD Standards
  - 16-Pin (3.90mm x 4.94mm) QSOP Package
  - -40°C to +105°C Operating Temperature Range
  - AEC-Q100 Qualified

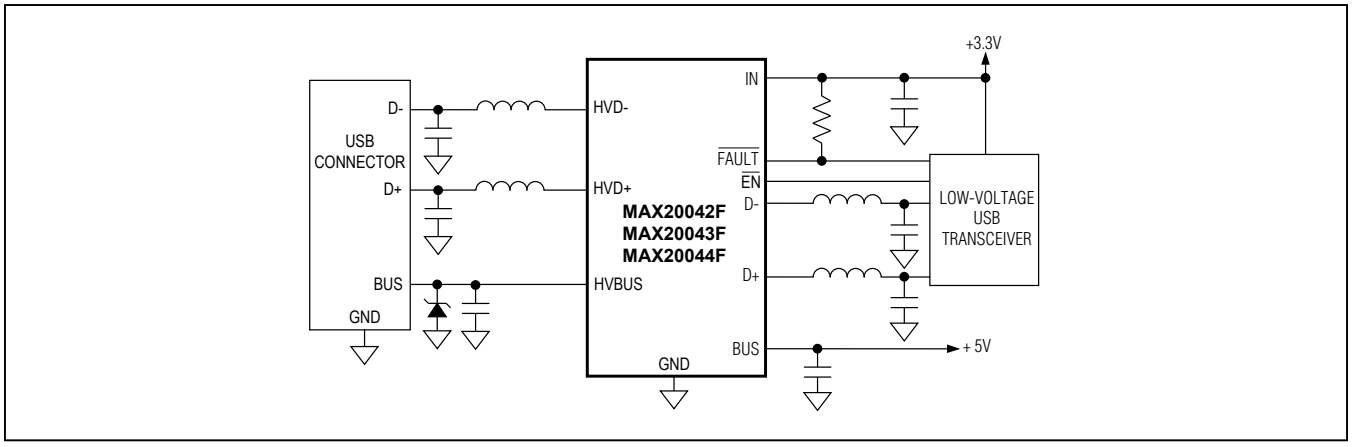
Applications

- Automotive USB Protection

***Ordering Information* appears at end of data sheet.**

***Functional Diagram* appears at end of data sheet.**

Typical Operating Circuit



19-8707; Rev 1; 3/24

Absolute Maximum Ratings

(All voltages referenced to GND.)
BUS, IN .....-0.3V to +6V
$\overline{FAULT}$, $\overline{EN}$, D+, D-.....-0.3V to +6V
D+, D- to IN .....+0.3V
HVD+, HVD-, HVBUS .....-0.3V to +18V

Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 9.6mW/°C above +70°C).....771.5mW
Operating Temperature Range ..... -40°C to +105°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

QSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....103.7°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....37°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **https://www.analog.com/en/resources/technical-articles/thermal-characterization-of-ic-packages.html**.

Electrical Characteristics

(V_{BUS} = 5.0V, V_{IN} = +3.3V, T_J = T_A = -40°C to +105°C. R_L = ∞, unless otherwise noted. Typical values are at $V_{\overline{EN}}$ = 0V or $V_{\overline{EN}}$ = 3.3V and T_A = +25°C, unless otherwise noted.) (*Note 2*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Range (BUS)	V_{BUS}		4.75		5.5	V
Power-Supply Range (IN)	V_{IN}		3.0		3.6	V
Input Current (BUS)	I_{BUS}	$V_{\overline{EN}}$ = 0V, I_L = 0A, no fault			400	µA
Input Current (IN)	I_{IN}	$V_{\overline{EN}}$ = 0V, I_L = 0A, no fault			10	µA
BUS Undervoltage Lockout	V_{UVLO}	V_{BUS} falling, Figure 1	3.85	4.2	4.55	V
BUS ANALOG SWITCH						
HVBUS Protection Trip Threshold	V_{OV_BUS}	HVBUS rising, Figure 2	5.55	5.67	5.8	V
Voltage Protection Response Time	t_{FP_BUS}	HVBUS rising, Figure 2		0.3	3.0	µs
Protection Recovery Time	t_{FPR_BUS}	HVBUS falling to below V_{OV_BUS}, Figure 2	4.5	10	22	ms
HVBUS Short-to-Ground Threshold	V_{SHRT}	Figure 3	0.7		2.2	V
Short-to-Ground Response Time	t_{FPS}	HVBUS falling to GND, Figure 3		0.3	1	µs
Short Detection Time	t_{SHRT_DET}	Enabled into short-to-ground	1	2	4	ms
On-Resistance	R_{ON}	V_{BUS} = 5V, I_{BUS} = 500mA (*Note 2*)		51	90	mΩ
Forward-Current Threshold (*Note 3*)	I_{THR}	MAX20042F, Figure 4	0.57	0.65	0.73	A
		MAX20043F, Figure 4	0.88	1.00	1.12	
		MAX20044F, Figure 4	1.14	1.30	1.46	
Overcurrent Blanking Time	t_{BLANK}	Figure 4 (*Note 4*)	0.35	1.2	2.8	ms
Overcurrent-Retry Blanking Time	t_{BLANK_RETRY}	Figure 4		12		ms
Overcurrent Autoretry Time	t_{RETRY}	Figure 4		128		ms

Electrical Characteristics (continued)

(V_{BUS} = 5.0V, V_{IN} = +3.3V, T_J = T_A = -40°C to +105°C. R_L = ∞, unless otherwise noted. Typical values are at $V_{\overline{EN}}$ = 0V or $V_{\overline{EN}}$ = 3.3V and T_A = +25°C, unless otherwise noted.) (*Note 2*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HVBUS Off-Leakage Current	I_{LKGOFF}	V_{HVBUS} = 18V, V_{BUS} = 4.75V			750	µA
		V_{HVBUS} = 18V, V_{BUS} = 0V, V_{IN} = 0V		560		
Thermal Shutdown				+175		°C
Thermal-Shutdown Hysteresis				15		°C
D+, D- ANALOG USB SWITCHES						
Analog Signal Range			0		3.6	V
Protection Trip Threshold	V_{OV_D}	HVD+, HVD- rises from V_{IN} to > V_{IN} + 1, Figure 2			3.9	V
Protection Response Time	t_{FP_D}	HVD+, HVD- rises from V_{IN} to > V_{IN} + 1, Figure 2		3.0	8.0	µs
Protection Recovery Time	t_{FPR_D}	HVD+, HVD- falling to below V_{OV_D}, Figure 2	4.5	10	22	ms
On-Resistance	R_{ON}	V_{BUS} = 5V, I_L = 40mA, 0 ≤ $V_{D\_}$ ≤ 3.6V		4		Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_{BUS} = 5V; I_L = 40mA; $V_{D\_}$ = 1.5V, 3.0V		0.7	1.5	Ω
On-Resistance Flatness	$R_{FLAT(ON)}$	I_L = 40mA, $V_{D\_}$ = 0V or 0.4V		1.0		Ω
HVD+, HVD- Off-Leakage Current	I_{HVD_OFF}	V_{HVD+}, V_{HVD-} = 18V; V_{D+}, V_{D-} = 0V	-200	+100	+200	µA
		V_{HVD+}, V_{HVD-} = 18V; V_{D+}, V_{D-} = 0V; V_{IN} = 0V; V_{BUS} = 0V		45		
HVD+, HVD- On-Leakage Current	I_{HVD_ON}	V_{HVD+}, V_{HVD-} = V_{IN} or 0V; $V_{\overline{EN}}$ = 0V		+2.2		µA
Propagation Delay	t_{PLH}, t_{PHL}	R_L = R_S = 50Ω, Figure 7		200		ps
Output Skew Between Switches	t_{SKB}	Skew between D+ and D- switch, Figure 7		40		ps
Output Skew Same Switch	t_{SKS}	Skew between opposite transitions in same switch, Figure 7		40		ps
FAULT OUTPUT						
FAULT Output Low Voltage	V_{OL}	I_{SINK} = 500µA			0.5	V
FAULT Output High-Leakage Current					1	µA
FAULT-Recovery Time	t_{FPR}	$V_{\overline{FAULT}}$ = V_{IN}, Figure 3 (*Note 3*)	4.5	10	22	ms
$\overline{EN}$ INPUT						
Input Logic-High	V_{IH}		1.65			V
Input Logic-Low	V_{IL}				0.5	V
Input Leakage Current	$I_{\overline{EN}}$	$V_{\overline{EN}}$ = 0V or V_{IN}			1	µA
Enable Delay Time	$t_{D\_\overline{EN}}$			40		µs

Electrical Characteristics (continued)

(V_{BUS} = 5.0V, V_{IN} = +3.3V, T_J = T_A = -40°C to +105°C. R_L = ∞, unless otherwise noted. Typical values are at $V_{\overline{EN}}$ = 0V or $V_{\overline{EN}}$ = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD PROTECTION HVD+, HVD-, HVBUS						
ESD Protection Level (Note 5)	V_{ESD}	ISO 10605 Air Gap (330pF, 2kΩ)		±25		kV
		ISO 10605 Contact (330pF, 2kΩ)		±8		
		IEC 61000-4-2 Air Gap (150pF, 330Ω)		±15		
		IEC 61000-4-2 Contact (150pF, 330Ω)		±8		
		IEC 61000-4-2 Air Gap (330pF, 330Ω)		±15		
		IEC 61000-4-2 Contact (330pF, 330Ω)		±8		

Note 2: Specifications with minimum and maximum limits are 100% production tested at T_A = +25°C and are guaranteed over the operating temperature range by design and characterization. Actual typical values may vary and are not guaranteed.
Note 3: Forward current is defined as current into BUS and out of HVBUS. See the *Functional Diagram*.
Note 4: Guaranteed by design. Limits are not production tested.
Note 5: Tested in the *Typical Application Circuit*, as shown on the MAX20044 evaluation kit.

Timing Diagrams/Test Circuits

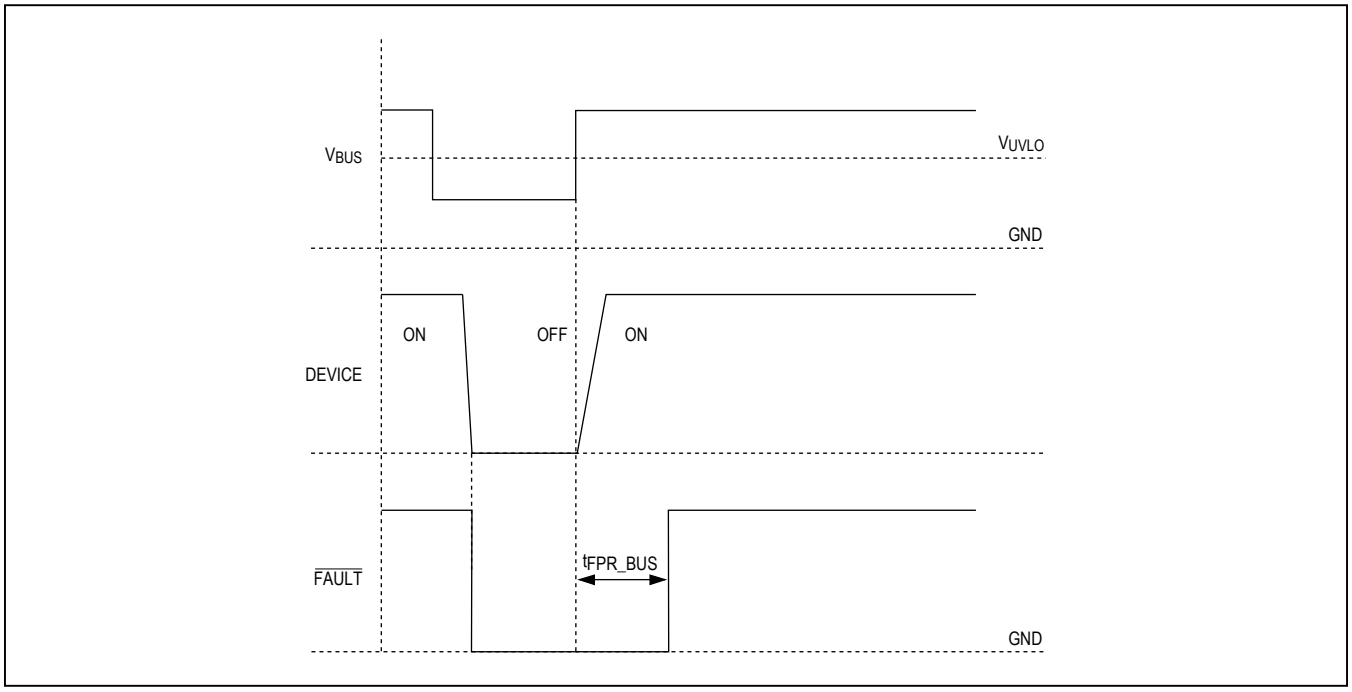


Figure 1. Timing Diagram for Undervoltage Lockout on BUS

Timing Diagrams/Test Circuits (continued)

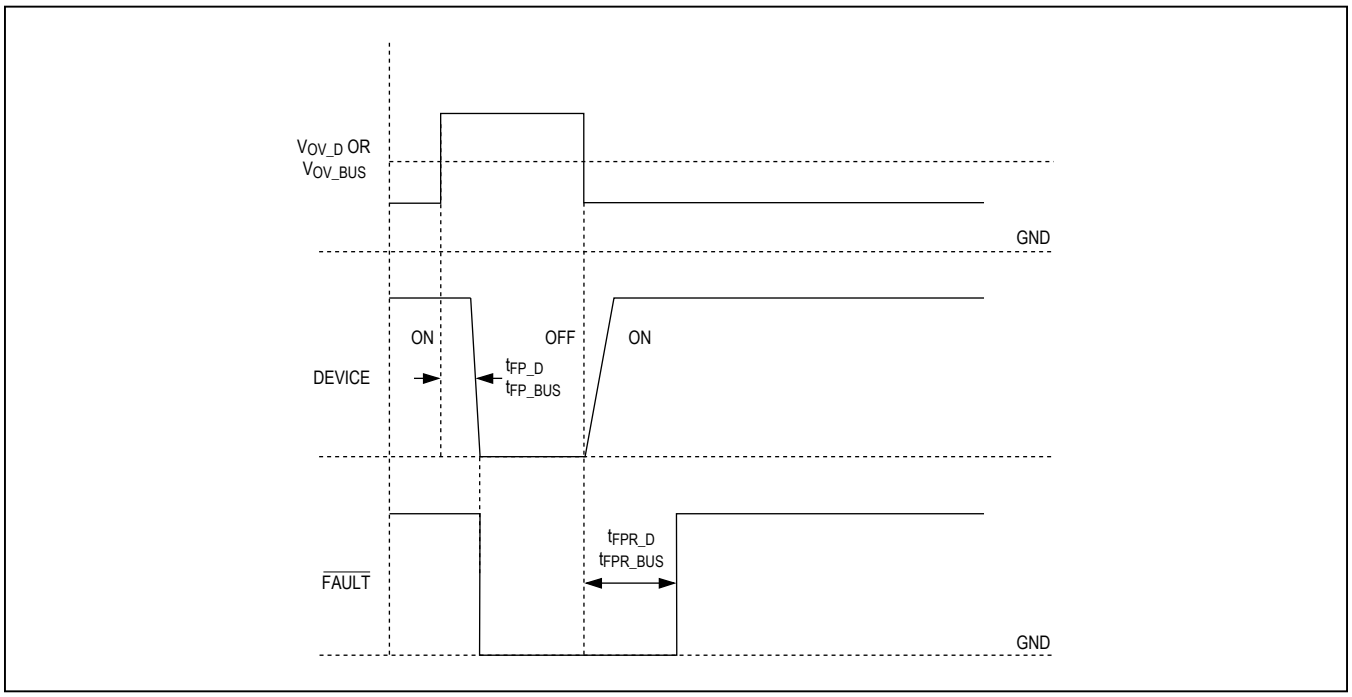


Figure 2. Timing Diagram for Overvoltage Protection on HVBUS, HVD+, and HVD-

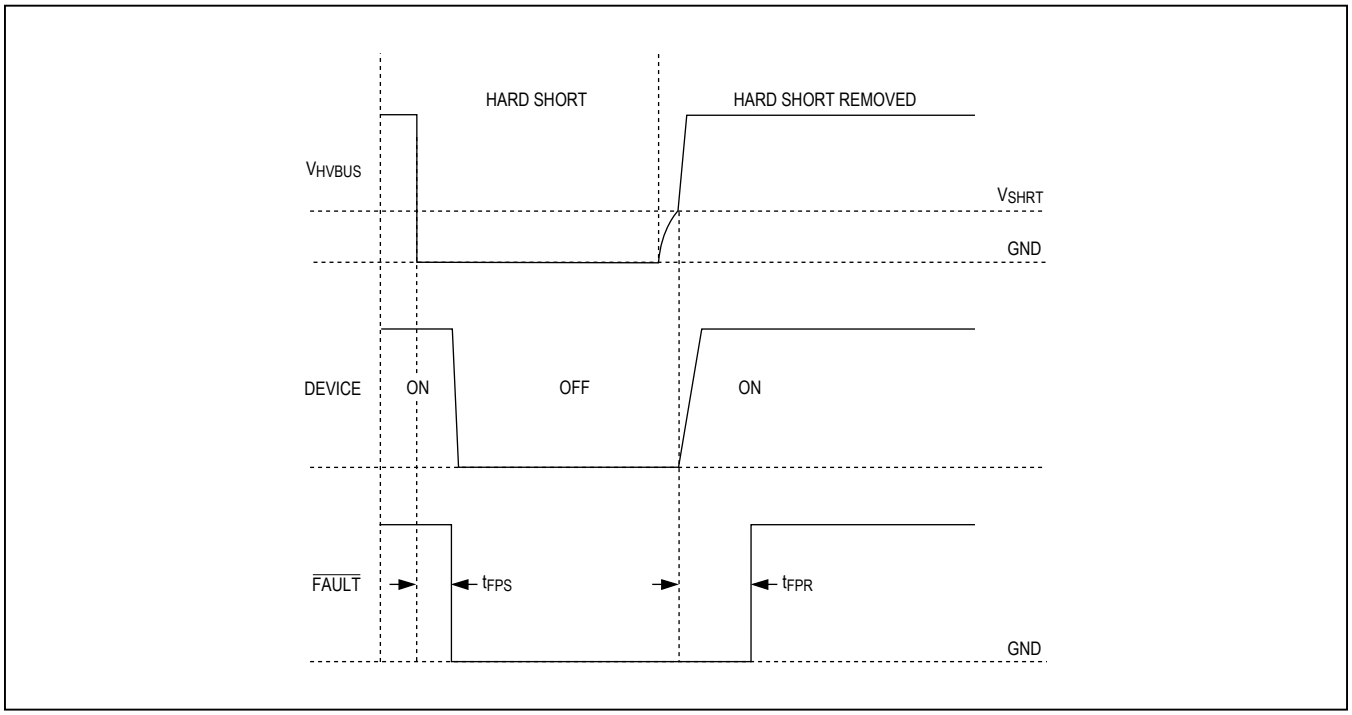


Figure 3. Timing Diagram for Short-to-Ground Protection

Timing Diagrams/Test Circuits (continued)

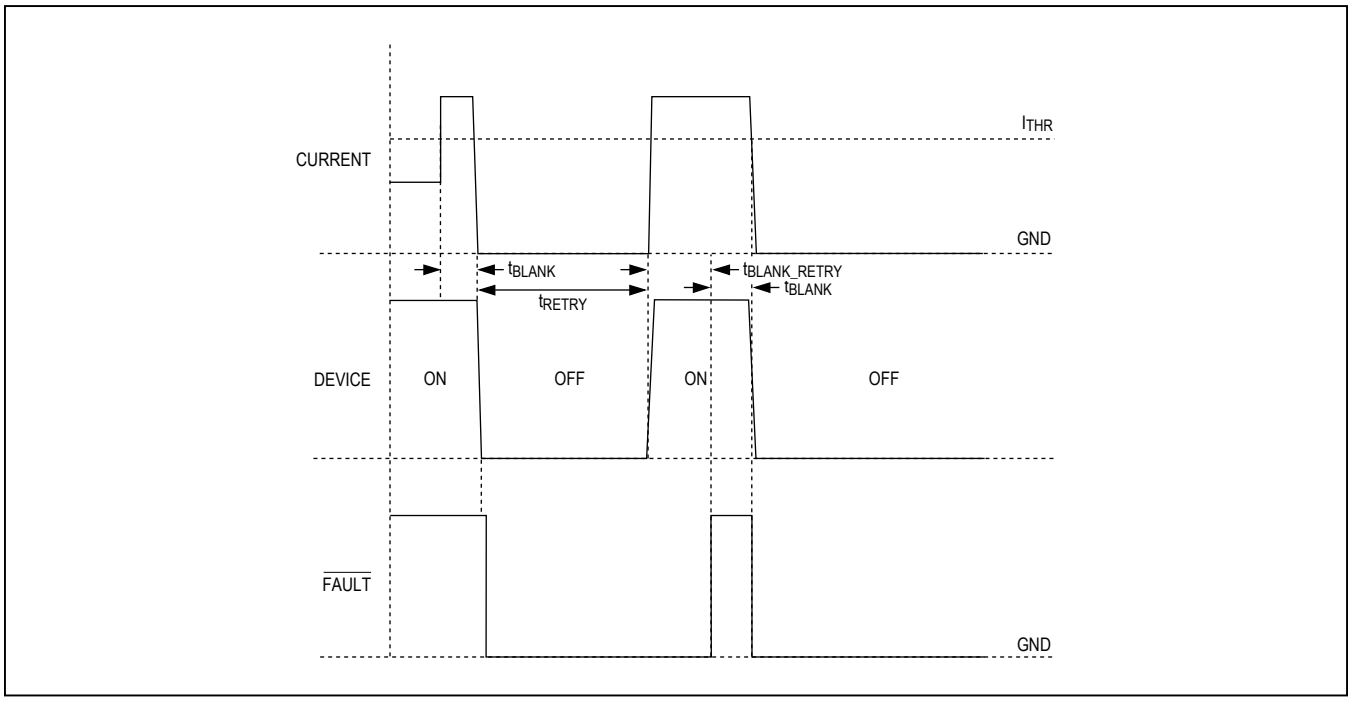


Figure 4. Timing Diagram for Overcurrent Protection

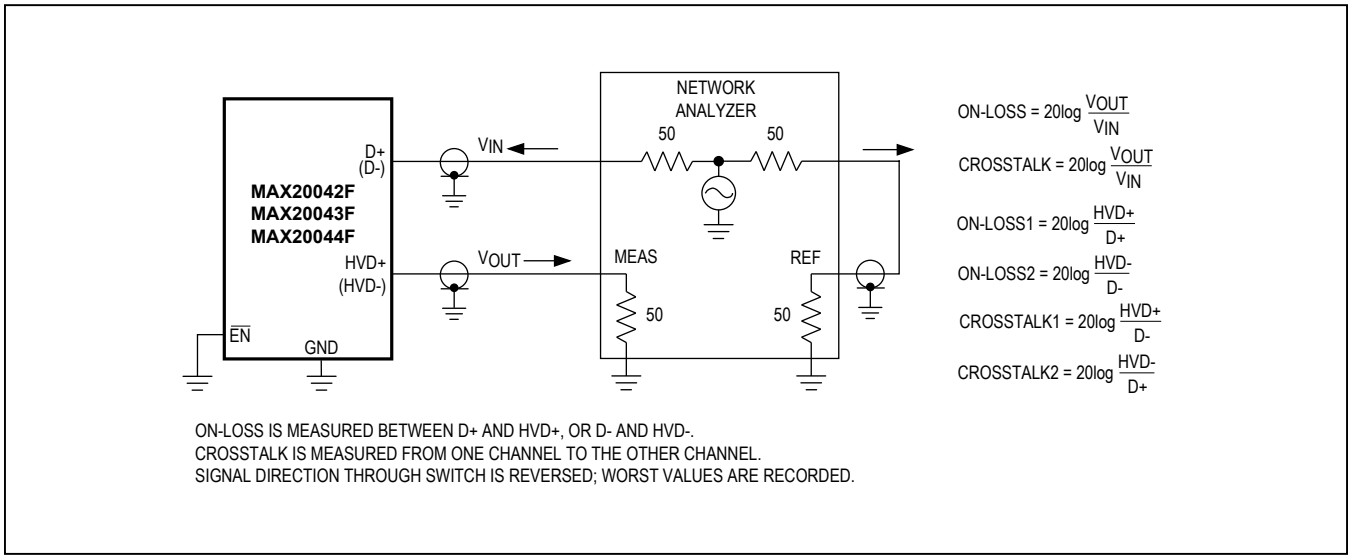


Figure 5. On-Channel -3dB Bandwidth and Crosstalk

Timing Diagrams/Test Circuits (continued)

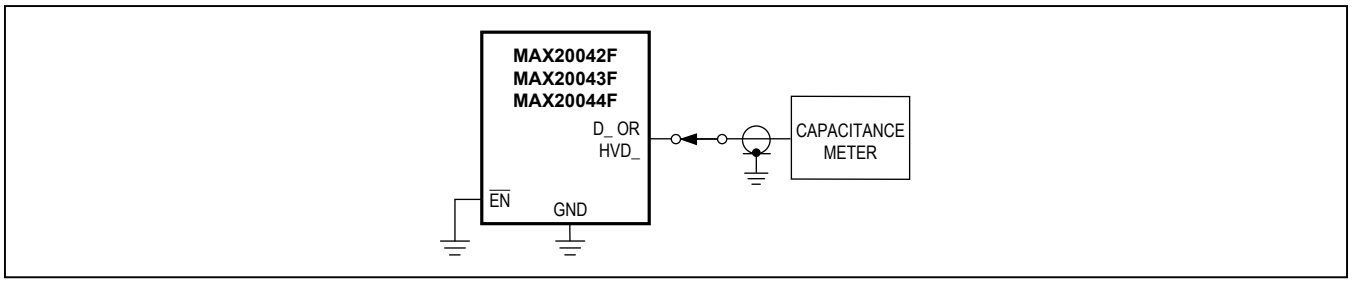


Figure 6. On-Capacitance

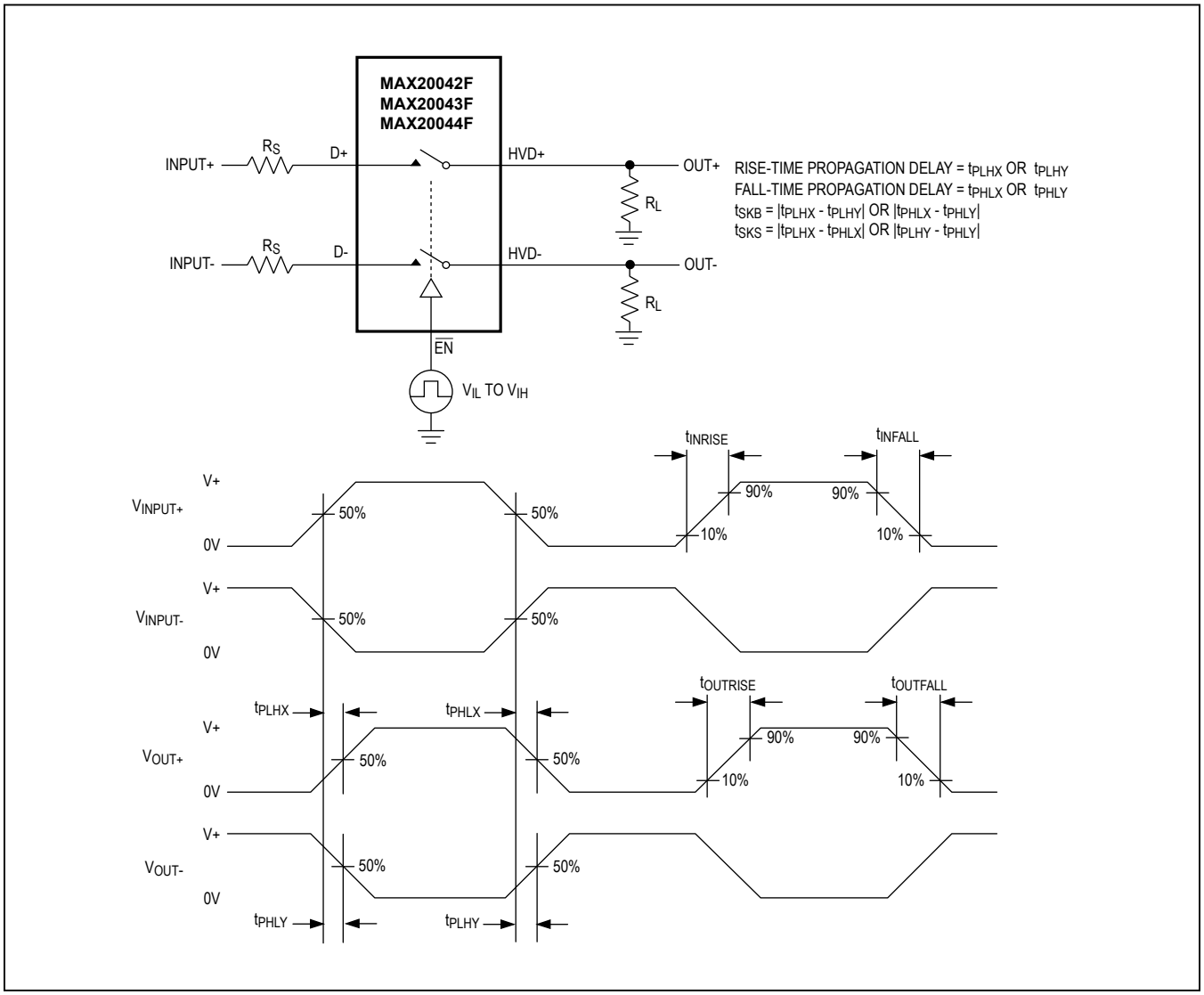
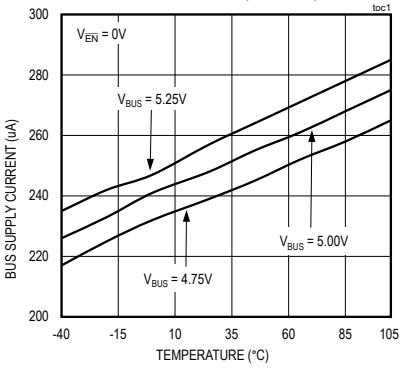


Figure 7. Propagation Delay and Output Skew

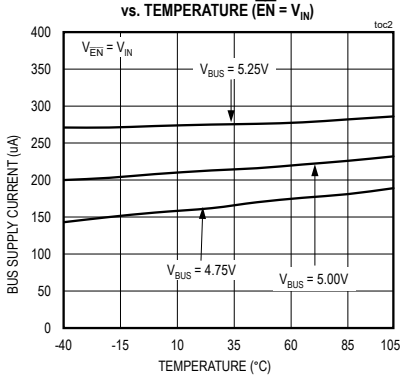
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

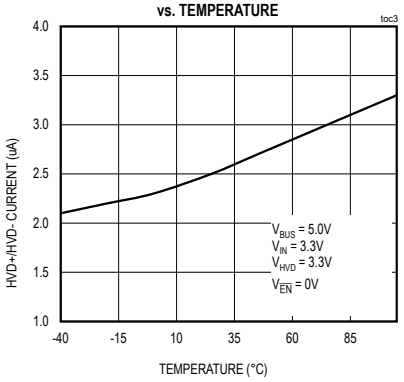
BUS SUPPLY CURRENT vs. TEMPERATURE ($\overline{EN}$ = GND)



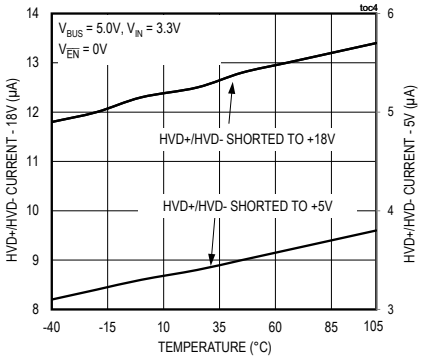
BUS SUPPLY CURRENT vs. TEMPERATURE ($\overline{EN}$ = V_{IN})



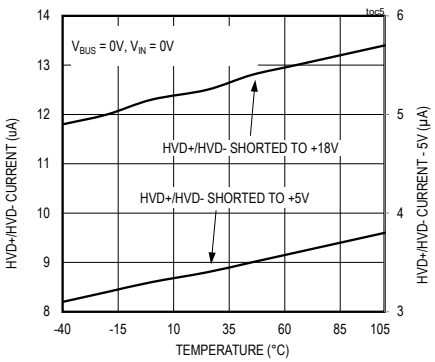
HVD+/HVD- LEAKAGE CURRENT vs. TEMPERATURE



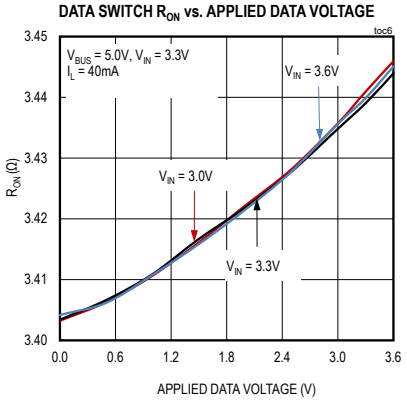
HVD+/HVD- LEAKAGE CURRENT vs. TEMPERATURE



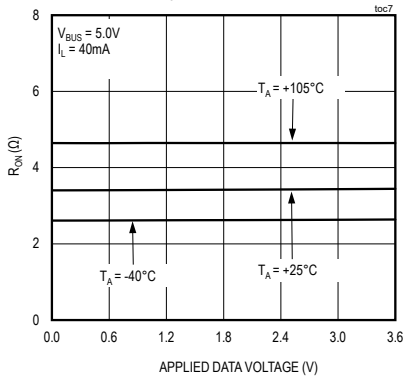
HVD+/HVD- LEAKAGE CURRENT vs. TEMPERATURE



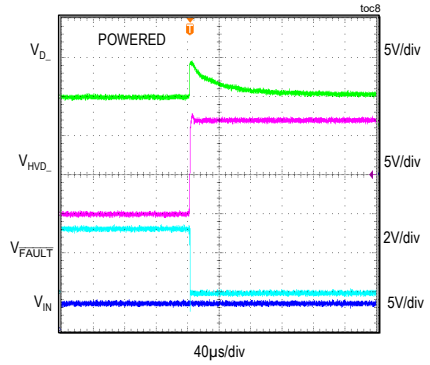
DATA SWITCH R_{ON} vs. APPLIED DATA VOLTAGE



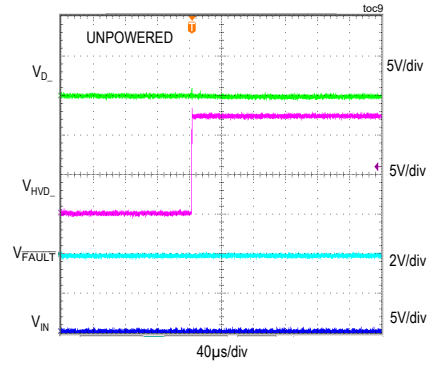
DATA SWITCH R_{ON} vs. APPLIED DATA VOLTAGE



HVD+/HVD-SHORT-TO-BATTERY TURN-OFF RESPONSE



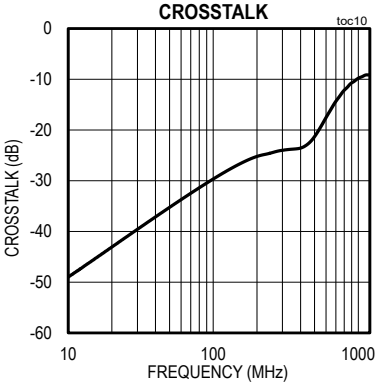
HVD+/HVD-SHORT-TO-BATTERY TURN-OFF RESPONSE



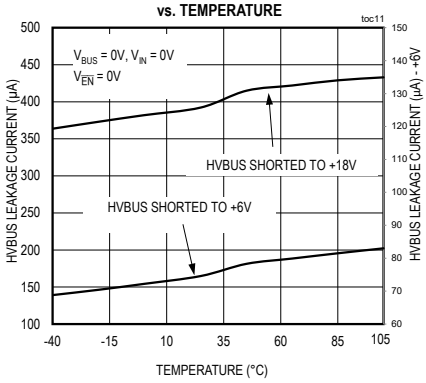
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

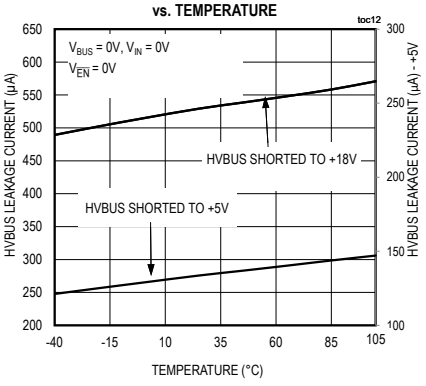
CROSSTALK



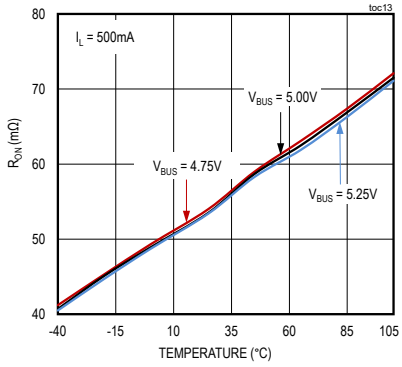
HVBUS LEAKAGE CURRENT vs. TEMPERATURE



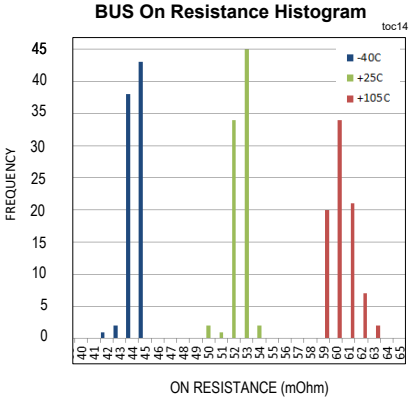
HVBUS LEAKAGE CURRENT vs. TEMPERATURE



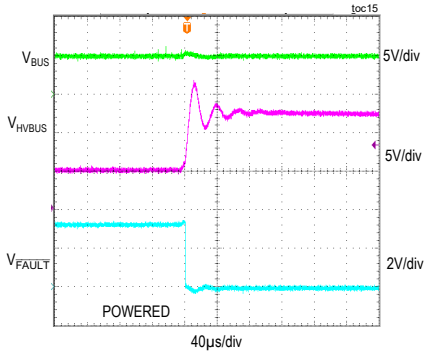
BUS ON RESISTANCE vs. TEMPERATURE



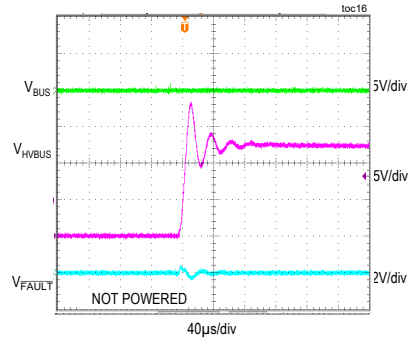
BUS On Resistance Histogram



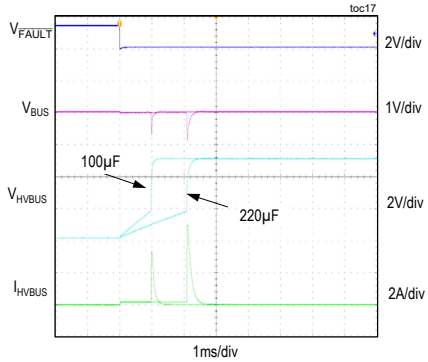
HVBUS SHORT-TO-BATTERY TURN-OFF RESPONSE



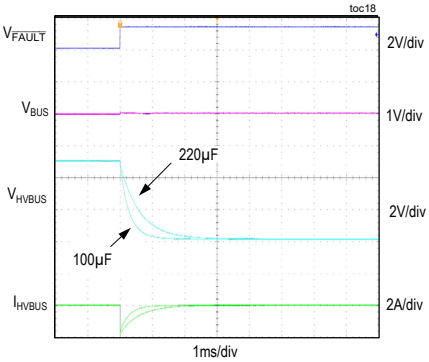
HVBUS SHORT-TO-BATTERY TURN-OFF RESPONSE



INRUSH CURRENT EN ON RESPONSE WITH RC LOAD



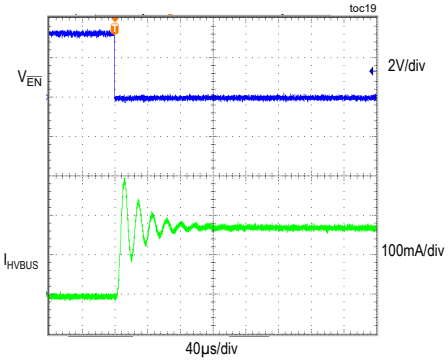
INRUSH CURRENT EN ON RESPONSE WITH RC LOAD



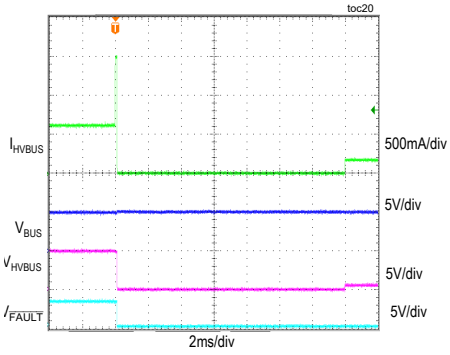
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

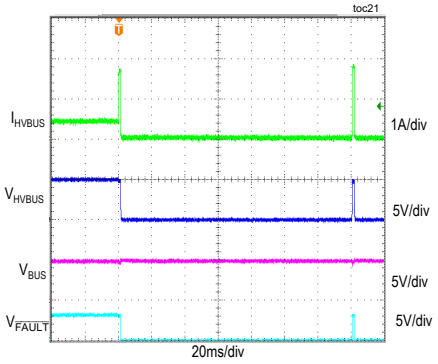
SHORT-CIRCUIT CURRENT, DEVICE ENABLED INTO SHORT-TO-GROUND



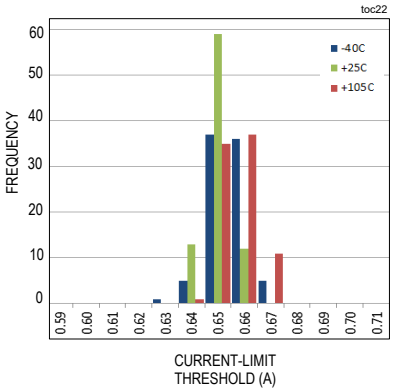
HVBUS OVERCURRENT AUTORETRY RESPONSE ($V_{HVBUS} < V_{SHRT}$)



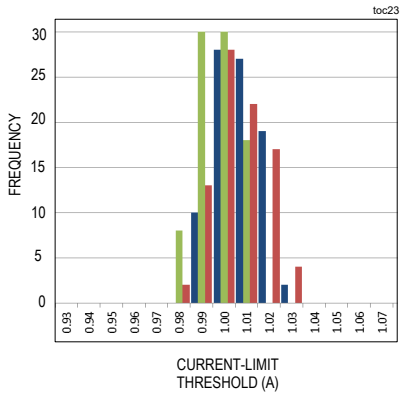
HVBUS OVERCURRENT AUTORETRY RESPONSE ($V_{HVBUS} > V_{SHRT}$)



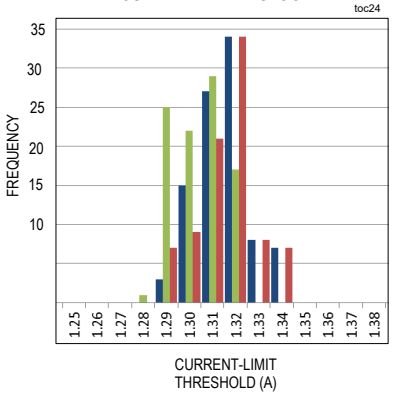
MAX20042F CURRENT-LIMIT HISTOGRAM



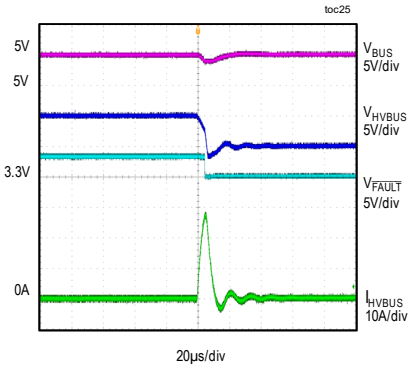
MAX20043F CURRENT-LIMIT HISTOGRAM



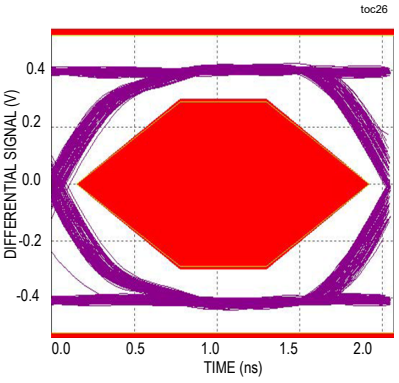
MAX20044F CURRENT-LIMIT HISTOGRAM



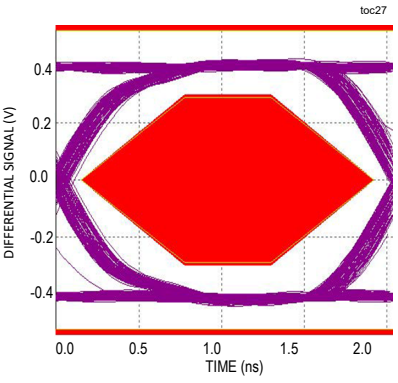
HVBUS INRUSH CURRENT FOR SHORT-TO-GROUND RESPONSE



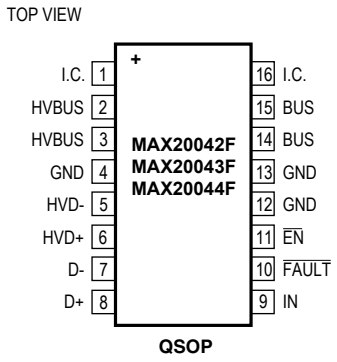
USB 2.0 HIGH-SPEED DIAGRAM (NO TUNING COMPONENTS)



USB 2.0 HIGH-SPEED EYE DIAGRAM W/STANDARD EV KIT TUNING COMPONENTS



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 16	I.C.	Internal Connection. Must be left unconnected.
2, 3	HVBUS	Protected BUS Output. Connect HVBUS directly to the USB connector. Connect both HVBUS outputs together for proper operation. Connect a 20V zener diode and a 0.1µF and 10µF capacitor from HVBUS to GND.
4, 12, 13	GND	Ground
5	HVD-	High-Voltage-Protected USB Differential Data D- Output. Connect HVD- directly to USB connector D-.
6	HVD+	High-Voltage-Protected USB Differential Data D+ Output. Connect HVD+ directly to USB connector D+.
7	D-	USB Differential Data D- Input. Connect D- to low-voltage USB transceiver D-.
8	D+	USB Differential Data D+ Input. Connect D+ to low-voltage USB transceiver D+.
9	IN	Logic Power-Supply Input. The supply voltage range is from +3.0V to +3.6V. Connect a 0.1µF and 10µF capacitor from IN to GND. Place these components on the same plane as the IC, close to the IN and GND pins.
10	$\overline{\text{FAULT}}$	Open-Drain Fault Indicator Output. Used to indicate if an overvoltage condition exists on HVD-, HVD+, or HVBUS, if an overcurrent condition exists on HVBUS, if a short-to-GND exists on HVBUS, or if an overtemperature condition occurs.
11	$\overline{\text{EN}}$	Active-Low Enable Input. Drive $\overline{\text{EN}}$ low to enable the device.
14, 15	BUS	USB Power Supply. Connect BUS to USB +5V supply. Connect both BUS inputs together for proper operation. Connect a 0.1µF and a 100µF, low-ESR ceramic capacitor from BUS to GND.

Detailed Description

The MAX20042F, MAX20043F, and MAX20044F devices provide high ESD and short-circuit protection for the low-voltage internal USB data and USB power line in automotive radio, navigation, connectivity, and USB hub applications. The devices support both USB Hi-Speed (480Mbps) and USB full-speed (12Mbps) operation.

The short-circuit protection features include short-to-battery on the protected HVBUS, HVD+, and HVD- outputs, as well as short-to-HVBUS on the protected HVD+ and HVD- outputs. These devices are capable of a short-to-battery condition of up to +18V. Short-to-GND protection and overcurrent protection are also provided on the protected HVBUS output to protect the internal BUS power rail from overcurrent faults.

The devices feature high ESD protection to ±15kV Air Gap Discharge and ±8kV Contact Discharge on all protected HVBUS, HVD+, and HVD- outputs.

The devices feature a low on-resistance (R_{ON}) 0.14Ω (max) USB power switch and two low on-resistance (R_{ON}) of 4Ω (typ) USB 2.0 switches. These devices also feature an enable input, a fault output, a 10ms fault-recovery time, a 1ms overcurrent blanking time, and an integrated overcurrent autoretry.

BUS Undervoltage Lockout (Power-On Reset)

The devices have a 4.2V (typ) undervoltage-lockout threshold (V_{UVLO}). When V_{BUS} is less than V_{UVLO}, $\overline{FAULT}$ is enabled and all the device switches are high impedance.

HVBUS Overvoltage Protection

The devices have a fixed 5.57V (typ) HVBUS protection trip threshold; when HVBUS rises from V_{BUS} to > 5.57V, the device is turned off. Connect a 20V zener diode or RC snubber network from HVBUS to GND to limit positive inductive voltage spikes that are caused by the inductance from long wires at turn-off.

HVBUS Short-to-Ground

The devices have a 0.7V (min) HVBUS short-to-ground threshold (V_{SHRT}). When HVBUS falls below the V_{SHRT} threshold, the main power switch is turned off. During continuous short-to-ground conditions, an approximately 250mA autoreset current remains active to detect removal of the short circuit.

HVBUS Overcurrent Protection

The devices have a 0.65A/1.0A/1.3A (typ) forward current threshold ITHR. When the HVBUS forward current exceeds the ITHR threshold, the device is turned off. Forward current is defined as current into BUS and out of HVBUS. See the *Functional Diagram*.

HVD+ and HVD- Overvoltage Protection

The devices have a 4.1V (typ) overvoltage threshold (VOV_D). When HVD+, or HVD- is greater than VOV_D, $\overline{FAULT}$ is enabled and all the device switches are high impedance. Note that HVD+ and HVD- do not have short-to-ground protection. Forward current is limited by the upstream transceiver.

$\overline{FAULT}$ Output

$\overline{FAULT}$ goes low when a fault is detected on HVD+, HVD-, or HVBUS. The $\overline{FAULT}$ output is asserted low when the device is enabled and the switches are disabled due to a fault. Fault detection includes short-to-battery, short-to-GND or overcurrent on HVBUS, and short-to-battery or short-to-HVBUS on HVD+ or HVD-. Connect a 100kΩ pullup resistor from $\overline{FAULT}$ to IN. See Table 1 for more information.

Table 1. FAULT Table

$\overline{EN}$ PIN	$\overline{FAULT}$ PIN ASSERTION*	
	B-SUFFIX (OTG) VARIANTS	A-SUFFIX (NON-OTG) VARIANTS
$\overline{EN}$ = 1 (off)	HVBUS overvoltage	Always asserted
	HVD+/HVD- overvoltage	
	Thermal shutdown	
$\overline{EN}$ = 0 (on)	HVBUS overvoltage	HVBUS overvoltage
	HVD+/HVD- overvoltage	HVD+/HVD- overvoltage
	Thermal shutdown	Thermal shutdown
	HVBUS overcurrent	HVBUS overcurrent
	HVBUS short to GND	HVBUS short to GND

* V_{BUS} > V_{UVLO}, and V_{IN} is within the power-supply range.

$\overline{EN}$ Input

$\overline{EN}$ is an active-low enable input. Drive $\overline{EN}$ low for normal operation and enable the protection switches. This allows BUS power, D+, and D- USB signaling to pass through the device if a fault is not present. Drive $\overline{EN}$ high to disable the device.

The MAX20042F, MAX20043F, and MAX20044F devices support USB OTG. With these units, disabling the device through the $\overline{EN}$ pin disables the +5V BUS power switch, but leaves the D+ and D- data switches closed. This allows for a downstream device to assume the role of host when negotiated per the USB Host Negotiation Protocol. In this mode, the HVBUS, HVD+, and HVD- outputs continue to be protected and $\overline{FAULT}$ continues to assert normally in response to overvoltage conditions on these pins.

Applications Information

Power-Supply Bypass Capacitor

Bypass HVBUS to GND with a 10µF and a 0.1µF ceramic capacitor as close to the device as possible to provide ±15kV (HBM) ESD protection on the pin. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection if necessary to prevent violation of the +6V absolute maximum rating on BUS. Connect a 100µF low-ESR ceramic capacitor from BUS to GND. Connect a 0.1µF and 10µF ceramic capacitor from both BUS and IN to GND. Place these components on the same plane as the IC, close to the IN and GND pins.

Layout of USB Data Line Traces

USB Hi-Speed requires careful PCB layout with 90Ω controlled-impedance matched traces of equal lengths. Use LC tuning components on the data lines as shown in the *Typical Operating Circuit*. The values of these components are layout and captive-cable dependent. Contact Analog Devices technical support for more detailed information.

±15kV ESD Protection

As with all Analog Devices ICs, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The devices have extra protection against static electricity. Analog Devices engineers have developed state-of-the-art structures to protect against ESD of ±15kV at the HVD+, HVD-, and HVBUS ports without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the devices keep working without latchup, whereas other solutions can latch and must be powered down to remove latchup. ESD protection can be tested in various ways; this product is characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ±15kV using IEC 61000-4-2's Air-Gap Discharge method, EN = GND
- ±8kV using the Contact Discharge method specified in IEC 61000-4-2, EN = GND

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Analog Devices for a reliability report that documents test setup, test methodology, and test results.

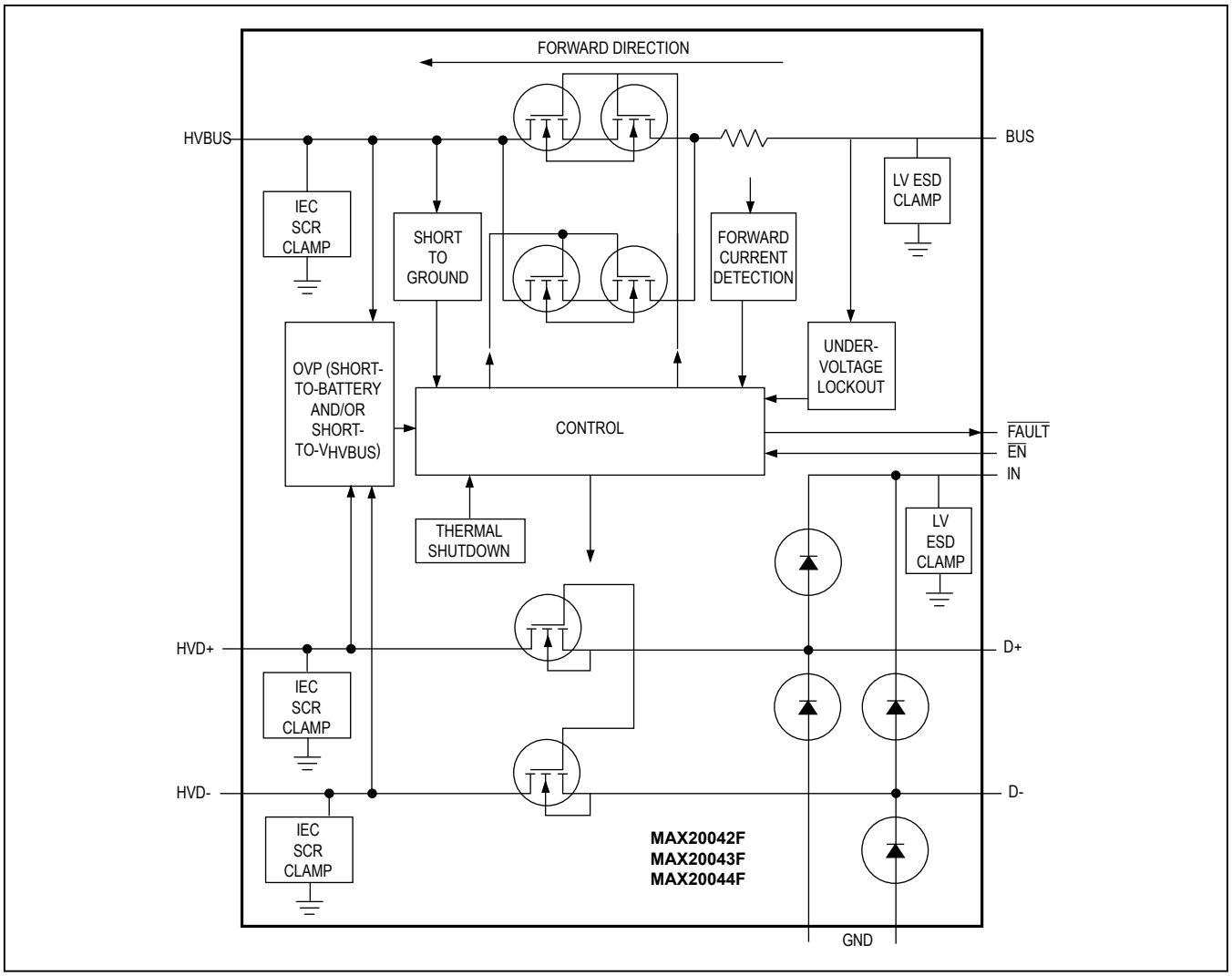
Human Body Model

Figure 8 shows the Human Body Model, and Figure 9 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The MAX20042F, MAX20043F, and MAX20044F devices help users design equipment that meets Level 4 of IEC 61000-4-2. The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 10), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 11 shows the current waveform for the ±8kV, IEC 61000-4-2 Level 4, ESD Contact Discharge test. The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Functional Diagram



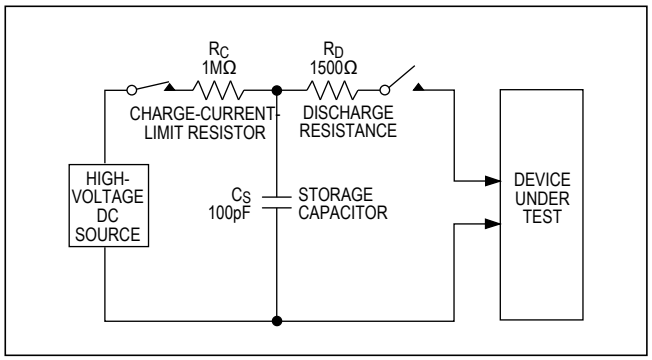


Figure 8. Human Body ESD Test Model

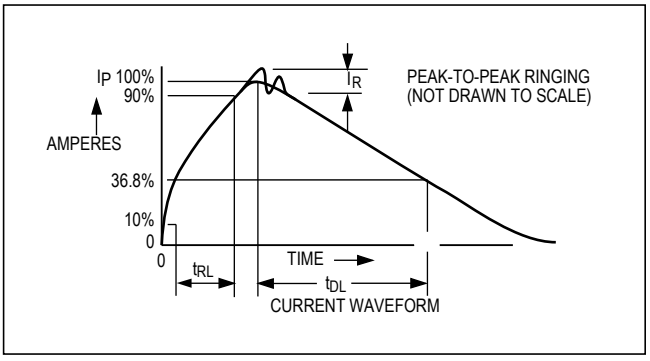


Figure 9. Human Body Current Waveform

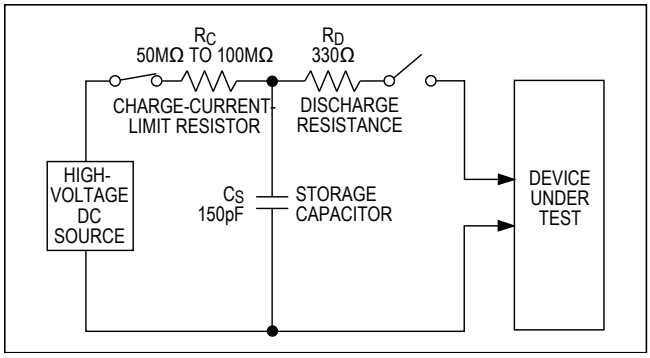


Figure 10. IEC 61000-4-2 ESD Test Model

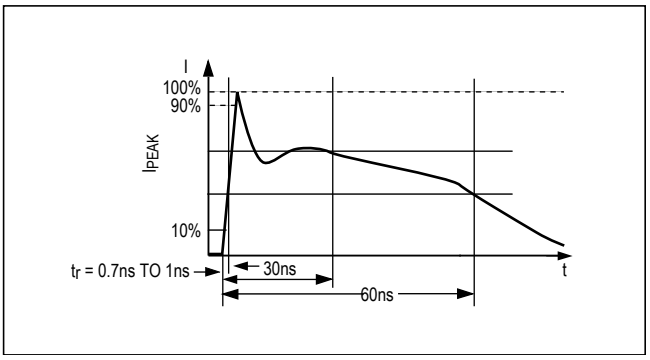


Figure 11. IEC 61000-4-2 ESD Generator Current Waveform

Ordering Information

PART	CURRENT RATING (A) (typ)	OTG SUPPORT	PIN-PACKAGE
MAX20042FGEEA/V+	0.65	No	16 QSOP
MAX20042FGEEB/V+	0.65	Yes	16 QSOP
MAX20043FGEEA/V+	1.0	No	16 QSOP
MAX20043FGEEB/V+	1.0	Yes	16 QSOP
MAX20044FGEEA/V+	1.3	No	16 QSOP
MAX20044FGEEB/V+	1.3	Yes	16 QSOP

Note: *All devices are specified over the -40°C to +105°C operating temperature range.*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **analog.com/en/resources/packaging-quality-symbols-footprints/package-index.html**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 QSOP	E16+12C	**21-0055**	**90-0167**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/17	Initial release	—
1	3/24	Updated Detailed Description	12