MAX20091

35-Channel Contact Monitor

General Description

The MAX20091 is a 35-channel automotive contact monitor for automotive applications. Ten contact monitor inputs can be used with either ground- or battery-connected switches; the other 25 inputs are for use with ground-connected switches.

The IC operates over a 5.5V to 28V voltage range and withstands voltages up to 42V. It protects low-voltage circuitry from high voltages and reverse-battery conditions. The IC's low-current operation under all operating conditions makes it suitable for use in electronic control units (ECUs) that are connected directly to the automotive battery. The IC has an adjustable scan mode that reduces the current drawn in key-off while maintaining polling capability.

The IC features an SPI interface to monitor the switch status and set the device configuration. An interrupt output allows the device to wake a local microcontroller when a switch status change is detected. In addition, a switch status change turns on the internal regulator.

The MAX20091 is available in a compact 48-pin TQFN package and operates over the -40°C to +125°C temperature range.

Applications

- Automotive Body Computers
- Smart Junction Boxes
- Door Modules

Benefits and Features

- Reduces Cost by Eliminating Multiple Microprocessors for Switch-Monitoring Functions
  - Configurable Wetting Current Improves Switch Performance
  - SPI Interface for Control/Readback
  - Built-In Hysteresis and Deglitching
  - Interrupt Output to Processor
- High Channel Count Reduces PCB Area Requirements
- Very Low Operating Current Enables Scanning in Key-Off State with Minimal Current Draw from 12V Battery
  - Ultra-Low 88µA (typ) Operating Current in Polling Mode
- Robust Switch Input Eliminate Need for External Protection Components
  - 5.5V to 28V Operating Voltage Range
  - Switch Inputs Withstand 42V and Reverse Battery
  - IN0-34 ESD Performance to ISO 10605 (In-Circuit): ±10kV Contact

***Ordering Information* and *Typical Operating Circuit* appears at end of data sheet.**

19-6935; Rev 3; 12/15

maxim integrated™

Absolute Maximum Ratings

BATT to GND .....-0.3V to +42V
IN0–IN34 to GND .....-18V to +42V
Current into Any Pin .....+20mA
V_{IO}, PVL, SCK, SDI, $\overline{INT}$ to GND .....-0.3V to +6.0V
$\overline{CS}$ to GND .....-0.3V to +6.0V
SDO to GND.....-0.3V to V_{IO} + 0.3V
ESD Protection, All Pins (HBM) .....±2kV
ESD Protection on Pins IN0–IN35 to ISO 10605 Specification (with added 0.047µF capacitor and/or 100Ω resistor).....±10kV

Continuous Power Dissipation (T_A = +70°C)
4877+6C on SLB (derate 27.8mW/°C above +70°C) 2222mW
4877+6C on MLB (derate 40mW/°C above +70°C).....3200mW
Operating Temperature Range..... -40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN (Four-Layer Board)
Junction-to-Ambient Thermal Resistance (θ_{JA}).....25°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1°C/W

TQFN (Single-Layer Board)
Junction-to-Ambient Thermal Resistance (θ_{JA}).....36°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{BATT} = 14V, V_{IO} = 5V, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{BATT}	(Note 3)		7.5		28	V
Battery OVP Threshold	V_{BATTOV}	Polling disabled above V_{BATT} rising	V_{BATT} rising	28.4	29.5	30.9	V
			V_{BATT} falling	28.1	29	30.4	
V_{IO} Voltage Range	V_{VIO}			3		5.5	V
BATT Undervoltage Lockout	V_{UVLO}	Rising		4	4.5	4.8	V
		Falling		3.5	4	4.5	
Supply Current	I_{BATT}	t_{POLL} = 64ms, t_{POLL_ACT} = 128µs, 35 channels active, all switches open, I_{WETT} set to 2mA, V_{BATT} = 7.5V to 28V			88	130	µA
		t_{POLL} = 64ms, t_{POLL_ACT} = 128µs, 35 channels active, all switches open, I_{WETT} set to 2mA, V_{BATT} = 7.5V to 28V			88	110	
		Continuous mode, I_{WETT} set to 10mA, all switches open, V_{BATT} = 7.5V to 28V			3.3	5.5	mA
V_{IO} Supply Current	I_{VIO}	Continuous mode, I_{WETT} set to 10mA, all switches open, V_{BATT} = 7.5V to 28V		10	55	200	nA
PVL Voltage	V_{PVL}	+7.5V ≤ V_{BATT} ≤ +28V		4.75	5	5.25	V

Electrical Characteristics (continued)

(V_{BATT} = 14V, V_{IO} = 5V, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCH INPUTS						
Input Voltage Threshold (Open to Closed)	V_{THR}	V_{BATT} = 7.5V to 28V, SPI setting 00	3.7		4.3	V
		V_{BATT} = 7.5V to 28V, SPI setting 01	3.5	3.8	4.1	
		V_{BATT} = 7.5V to 28V, SPI setting 10	2.75	3	3.25	
		V_{BATT} = 7.5V to 28V, SPI setting 11	1.8	2	2.2	
Input Hysteresis	V_{HYST}	V_{BATT} = 7.5V to 28V		0.2		V
Wetting Current Accuracy	I_{WETT}	2mA setting, 5.5V < V_{BATT} < 28V	1.7	2	2.3	mA
		5mA setting, 5.5V < V_{BATT} < 28V	4.25	5	5.75	
		10mA setting, 5.5V < V_{BATT} < 28V	8.5	10	11.5	
IN0–IN34 Input Current	$I_{IN\_}$	V_{BATT} = 14V, wetting current set to zero, T_A = +25°C	-2	1	+2	µA
Dropout Voltage with GND-Connected Switch	$V_{DROPOUT}$	V_{BATT} - $V_{IN\_}$, wetting current at 90% of set value (90% of actual value when set to 10mA)			2.9	V
		V_{BATT} - $V_{IN\_}$, wetting current at 90% of set value (90% of actual value when set to of 2mA)			1.5	
Polling Active Time Accuracy	$t_{POLLACT}$		-10		+10	%
Polling Time Accuracy	t_{POLL}		-10		+10	%
LOGIC LEVELS						
$\overline{INT}$ Output Voltage Low	V_{OUTL}	Sinking 2mA			0.4	V
SDO Output Voltage Low	V_{SDOL}	Sinking 2mA			0.2 x V_{IO}	V
SDO Output Voltage High	V_{SDOH}	Sourcing 1mA	0.8 x V_{IO}			V
SDO Leakage Current in High-Impedance Mode	I_{LKSDO}	$\overline{CS}$ = V_{IO}	-1		+1	µA
SDI, CLK, $\overline{CS}$ Input Voltage Low	V_{INL}				1	V
SDI, CLK, $\overline{CS}$ Input Voltage High	V_{INH}		2.2			V
$\overline{INT}$ Output Leakage Current			-5		+5	µA
SDI Internal Pulldown Resistor	R_{SDI}			50		kΩ
THERMAL PROTECTION						
Thermal Warning	T_{WARN}	$\overline{INT}$ asserted low and T bit set in SPI word		145		°C
Thermal Shutdown	T_{SHDN}			165		°C
Thermal-Shutdown Hysteresis	$T_{SHDN.HYS}$			15		°C

Electrical Characteristics (continued)

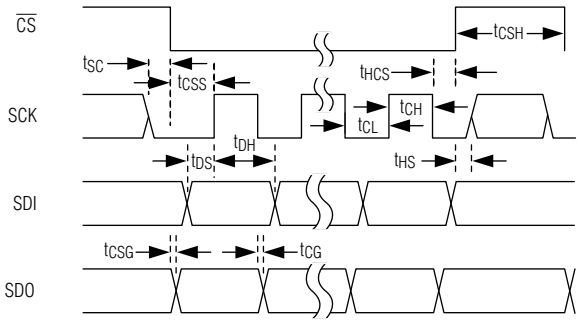
(V_{BATT} = 14V, V_{IO} = 5V, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING						
SCK Frequency Range			0.1		4	MHz
Falling Edge of $\overline{CS}$ to Rising Edge of SCK Setup Time				15		ns
Falling Edge of SCK to Rising Edge of $\overline{CS}$ Setup Time				60		ns
Minimum SCK Low After Rising Edge of $\overline{CS}$ Hold Time	t_{HS}			15		ns
Minimum Data Valid to SCK Rising-Edge Setup Time	t_{DS}			30		ns
Minimum Data Valid to SCK Rising-Edge Hold Time	t_{DH}			15		ns
Minimum SCK High Pulse Width	t_{CH}			120		ns
Minimum SCK Low Pulse Width	t_{CL}			120		ns
Minimum $\overline{CS}$ High Pulse Width	t_{CSH}			120		ns
Maximum Transition Time from Falling Edge of $\overline{CS}$ to Valid SDO	t_{CSG}	C_L = 10pF load capacitance from SDO to ground		40		ns
Maximum Transition Time from Falling Edge of SCK to Valid SDO	t_{CG}	C_L = 10pF load capacitance from SDO to ground		40		ns

Note 2: All devices 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

Note 3: When BATT is above 28V, the wetting current is disabled to limit power dissipation, and the switch inputs are not monitored. When BATT returns below 28V, there is a 1ms blanking time before the external switches are polled.

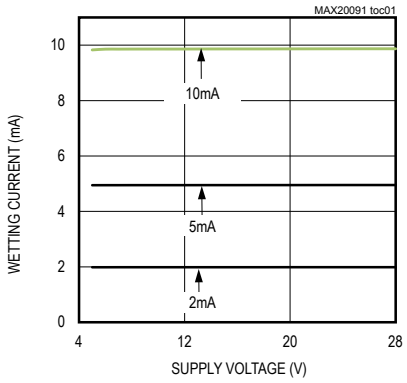
SPI Timing Diagram



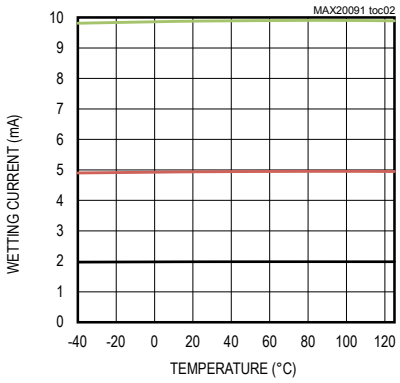
Typical Operating Characteristics

(V_{BATT} = 14V, T_A = +25°C, unless otherwise noted.)

WETTING CURRENT vs. SUPPLY VOLTAGE



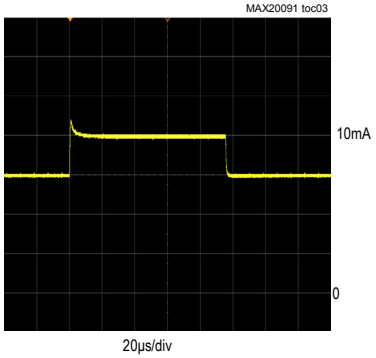
WETTING CURRENT vs. TEMPERATURE



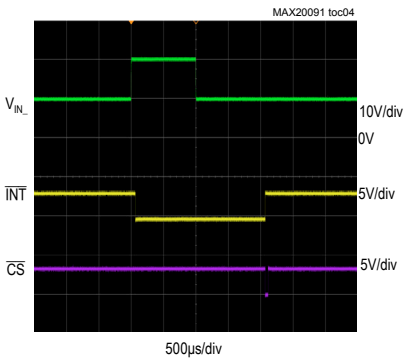
Typical Operating Characteristics (continued)

(V_{BATT} = 14V, T_A = +25°C, unless otherwise noted.)

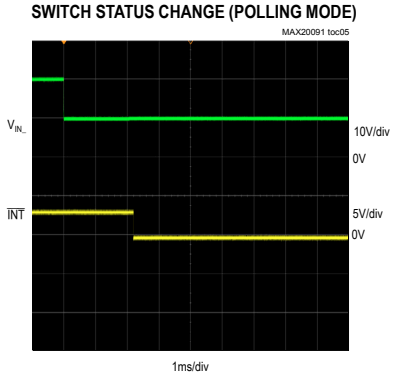
WETTING CURRENT RISE/FALL TIME



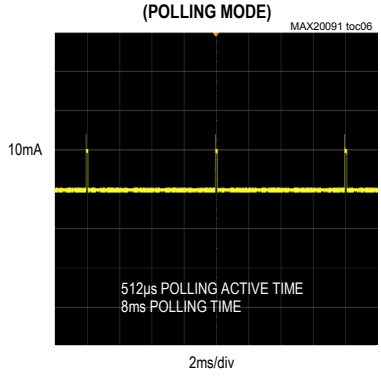
SWITCH STATUS CHANGE (CONTINUOUS MODE)



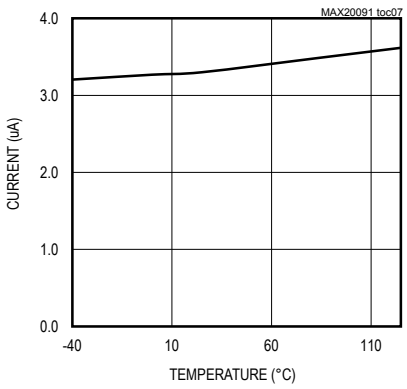
SWITCH STATUS CHANGE (POLLING MODE)



WETTING CURRENT (POLLING MODE)



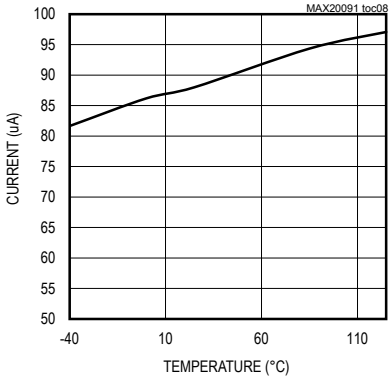
QUIESCENT CURRENT IN CONTINUOUS MODE



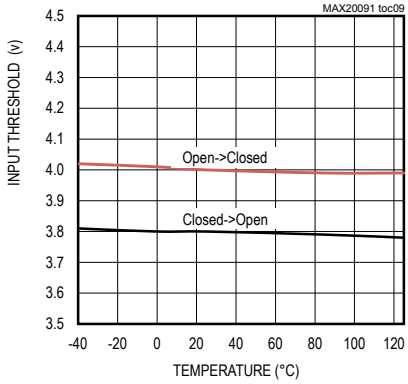
Typical Operating Characteristics (continued)

(V_{BATT} = 14V, T_A = +25°C, unless otherwise noted.)

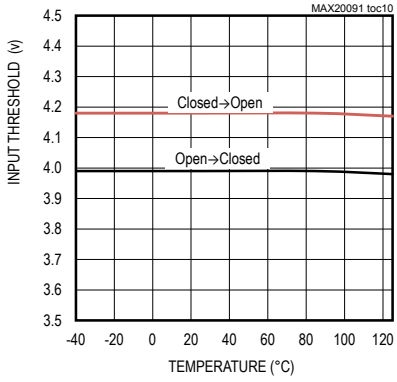
QUIESCENT CURRENT IN POLLING MODE
(PT = 64ms, PAT =128µs)



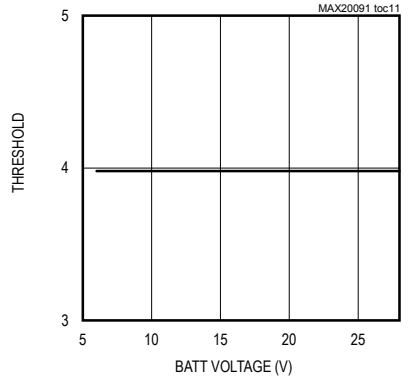
INPUT THRESHOLD vs. TEMPERATURE
(HIGH-SIDE SWITCH, TH_.1 = TH_.0 = 0)



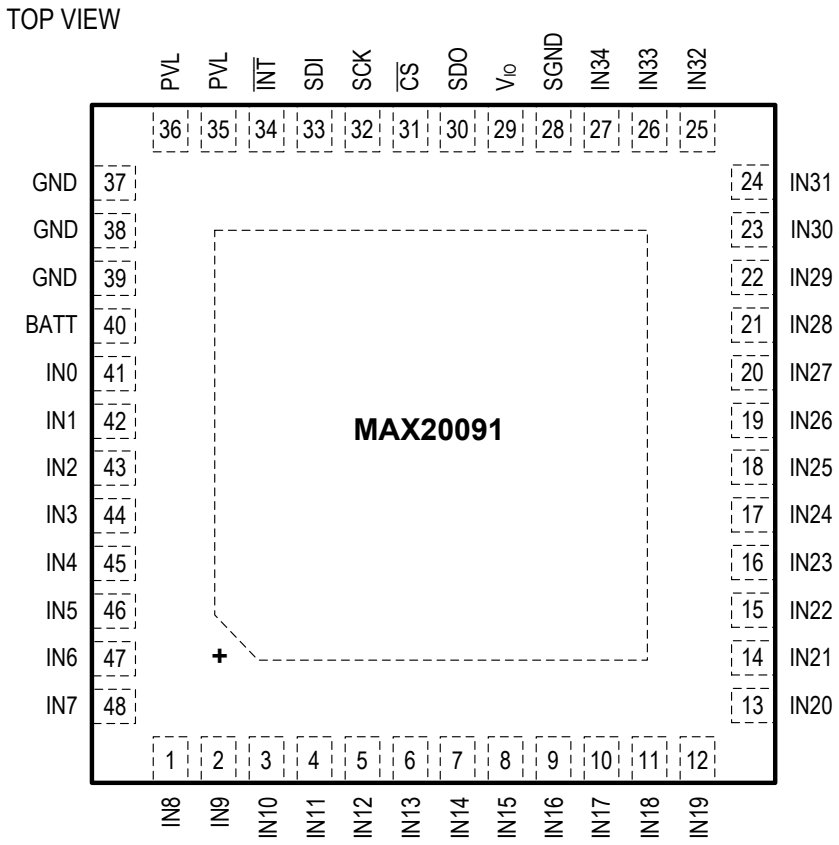
INPUT THRESHOLD vs. TEMPERATURE
(LOW-SIDE SWITCH, TH_.1 = TH_.0 = 0)



SWITCH THRESHOLD vs. BATT VOLTAGE
(TH_.1 = TH_.0 = 0)



Pin Configuration

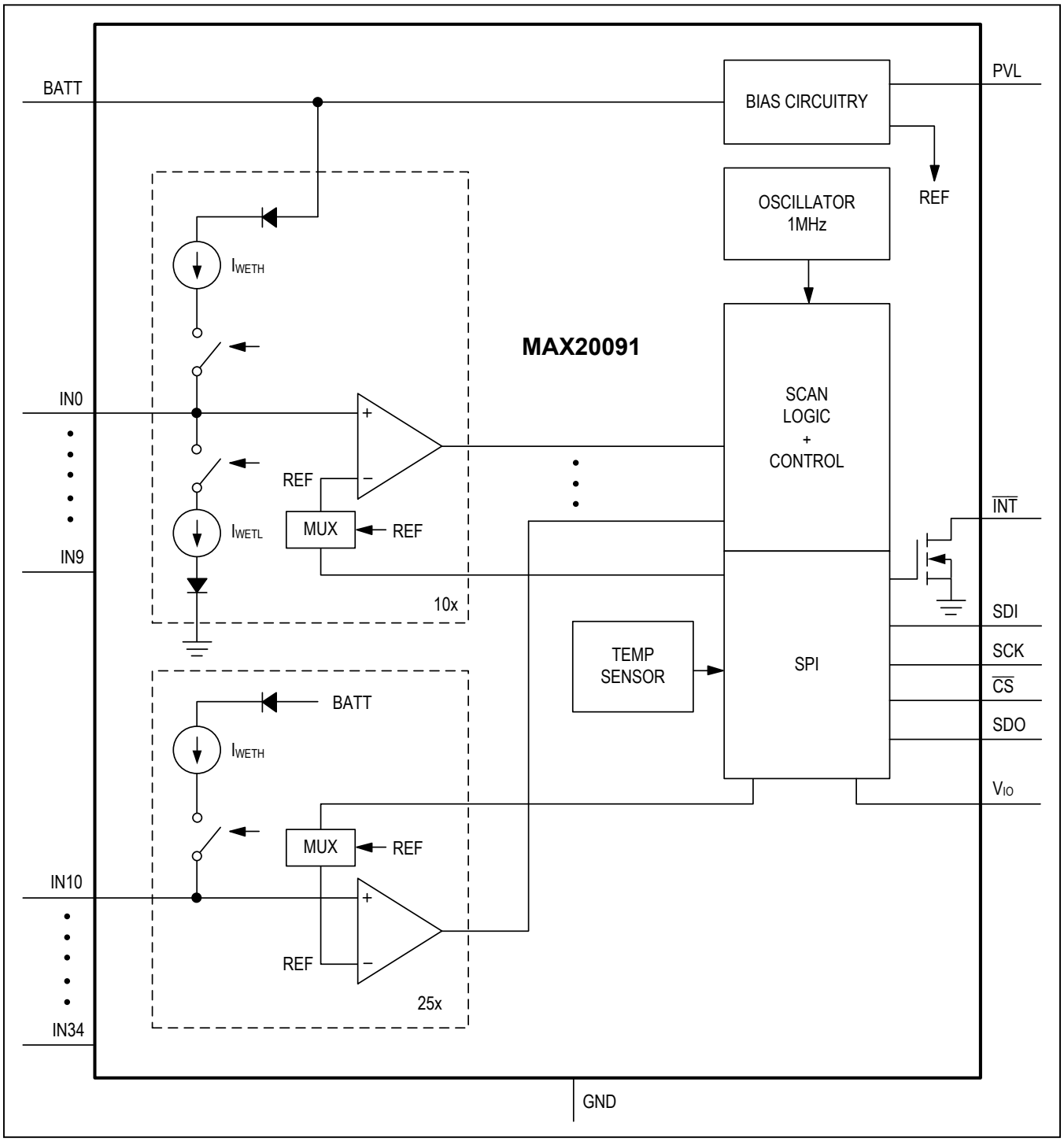


TQFN
(7mm x 7mm, 0.5mm PITCH)

Pin Description

PIN	NAME	FUNCTION
1, 2	IN8, IN9	Switch Monitor Input Channels 8 and 9. Connect to a battery-connected or ground-connected switch. When used for a battery-connected switch, add a 100Ω series protection resistor to the input.
3–27	IN10, IN34	Switch Monitor Input Channels 10–34. Connect to a ground-connected switch.
28	GND	Ground Connection
29	V_{IO}	Logic Supply for SPI Interface Pins. Connect to a supply between 3V and 5V. Bypass VIO to GND with a 0.1µF capacitor placed as close to VIO as possible.
30	SDO	SPI Data Output. SDO is high impedance when $\overline{CS}$ is high.
31	$\overline{CS}$	SPI Active-Low Chip-Select. Drive $\overline{CS}$ low to enable clocking of data into and out of the IC. SPI data is latched into the device on the rising edge of $\overline{CS}$. In polling mode $\overline{CS}$ must be maintained high to ensure correct operation of the $\overline{INT}$ output. If needed, the PVL output can be used as the pullup power.
32	SCK	SPI Clock Input
33	SDI	SPI Data Input. SPI data is latched into the internal shift register on the rising edges of SCK while $\overline{CS}$ is held low. SDI has an internal 75kΩ pulldown resistor. Connect SDI to the SDO of a preceding device in a daisy chain or to the microcontroller data output.
34	$\overline{INT}$	Open-Drain Interrupt Output. $\overline{INT}$ goes low when an input switch change has been detected in scan mode.
35, 36	PVL	Internal Linear Regulator Output. PVL is the supply for the internal blocks. Bypass PVL with a 2.2µF capacitor to ground.
37–39	GND	Ground
40	BATT	Battery Voltage Connection. BATT should be protected from reverse battery using a series diode. Bypass BATT to GND with a 0.1µF ceramic capacitor placed as close as possible to the pin. In addition, bypass BATT with a 47µF or greater capacitor.
41–48	IN0–IN7	Switch Monitor Input Channels 0–7. Connect to a battery-connected or ground-connected switch. When used for a battery-connected switch, add a 100Ω series protection resistor to the input.
—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the only IC ground connection. EP must be connected to GND.

Functional Diagram



Detailed Description

The MAX20091 is a 35-channel automotive contact monitor designed as an interface between mechanical switches and low-voltage microcontrollers or other logic circuits. It features an SPI interface to monitor individual switch inputs and to configure interrupt capability, wetting current, switch configuration (battery-connected or ground-connected), polling time, and polling active time. Any switch status change causes an interrupt signal if the switch is interrupt enabled. The IC has two modes of operation: continuous mode and polling mode.

BATT and V_{IO}

V_{IO} is the power-supply input for the logic output circuitry. Connect V_{IO} to a 3V to 5.5V logic-level supply. Bypass V_{IO} to GND with at least a 0.1µF capacitor placed as close as possible to the V_{IO} pin.

BATT is the main power-supply input. Bypass BATT to GND with a 0.1µF ceramic capacitor placed as close as possible to the pin. In addition, bypass BATT with a 47µF or greater capacitor. When BATT exceeds 28V (typ) wetting current is disabled, switch scanning is stopped and the OVP bit in SPI register 0x04 is set.

PVL is the output of an internal ultra-low current regulator that is always enabled when BATT is above its undervoltage lockout. Bypass PVL with a 2.2µF capacitor.

Operating Modes

The IC features two modes of operation: continuous mode and polling mode. In continuous mode, the wetting currents (if enabled) are continuously applied to closed switches. In polling mode, the wetting currents are applied to the closed switches for a preset duration to reduce the power consumption.

Continuous Mode Operation (P2:P0 = 0)

In continuous mode, reading of the switch status is initiated by a falling edge on $\overline{CS}$. The microcontroller initiates a low pulse on $\overline{CS}$ to update the IC's switch status register. If $\overline{INT}$ remains high, no action needs be taken by the microcontroller. If $\overline{INT}$ goes low, the microcontroller may perform a read operation to read the updated switch status. On the rising edge of $\overline{CS}$, $\overline{INT}$ is updated. To get correct data, the microcontroller must wait at least 4µs before initiating a switch status read operation.

Polling-Mode Operation

In polling mode, each switch input is sampled for a programmable polling active time set by the PA[2:0] bits between 96µs and 4ms (see Table 5). Sampling is repeated at a period set by the P[3:0] bits (from 8ms to continuous, see Table 4). All switch inputs are sampled simultaneously at the end of the polling active time. Wetting currents (if enabled) are applied to closed switches during the polling active time. Polling mode thus reduces the current consumption from the BATT power supply to a value dependent on the polling time and polling active time chosen.

Mechanical Switch Inputs (IN0–IN34)

IN0–IN34 are the inputs for remote mechanical switches. The switch status is indicated by the SS[34:0] bits in the switch status registers, and each switch input can be programmed to assert an interrupt ($\overline{INT}$) by writing to the IE[34:0] bits in registers 0x07 to 0x0B. All switch inputs are interrupt-disabled upon power-up.

The IN10–IN34 inputs are intended for ground-connected switches. The IN0–IN9 inputs can be programmed for either ground-connected switches or battery-connected switches by writing to the LH[9:0] bits in registers 0x05 and 0x06. The default configuration of the IN0–IN9 inputs after power-up is for ground-connected switches. All inputs have an internal glitch filter with a typical filter time of 50µs.

Wetting Current

The IC applies a programmable wetting current to any closed switch to clean switch contacts that are exposed to adverse conditions. The wetting current for each switch can be set to 0mA, 2mA, 5mA, or 10mA by the W_.[1:0] data bits in the wetting current registers by means of SPI.

When using wetting current, special care must be taken to avoid exceeding the maximum power dissipation of the IC (see the *Applications Information* section). Disabling the wetting current or limiting the active-wetting current time reduces power consumption. The default state upon power-up is with wetting current set to 2mA.

Interrupt Output ($\overline{INT}$)

$\overline{INT}$ is an active-low, open-drain output that asserts low when any of the switch inputs change state and is enabled for interrupts, or when the overtemperature warning threshold is exceeded. An external pullup resistor to V_{IO} is needed on $\overline{INT}$. $\overline{INT}$ is cleared when $\overline{CS}$ is driven low for a read/write operation. However, in polling mode, any switch state change or overtemperature change that occurs during an SPI transaction is stored and causes an additional interrupt after the SPI transaction is over and $\overline{CS}$ goes high. If V_{IO} is absent, the $\overline{INT}$ output is functional provided that it is pulled up to a different supply voltage and that $\overline{CS}$ is kept high.

Serial Peripheral Interface

The IC is controlled by means of an SPI interface with the local microcontroller. Any number of 8-bit data bursts can be sent within one cycle of $\overline{CS}$ low to allow for burst-write of all or a subset of the registers. The SPI logic counts the number of bits clocked into the IC and enables data latching only after each 8 bits. The first 8-bit byte is the command byte that is followed by an 8-bit address byte and then by n 8-bit data bytes (write) or n further addresses (read).

SPI Commands

The following four SPI commands are implemented:

Write: Within the same $\overline{CS}$ cycle, a write command is implemented as follows:

SDI: <0x01> <Initial Address> <Data 1> <Data 2> … <Data N>

With this command, Data 1 is written to the address given by <Initial Address>, Data 2 is written to <Initial Address + 1>, and so on.

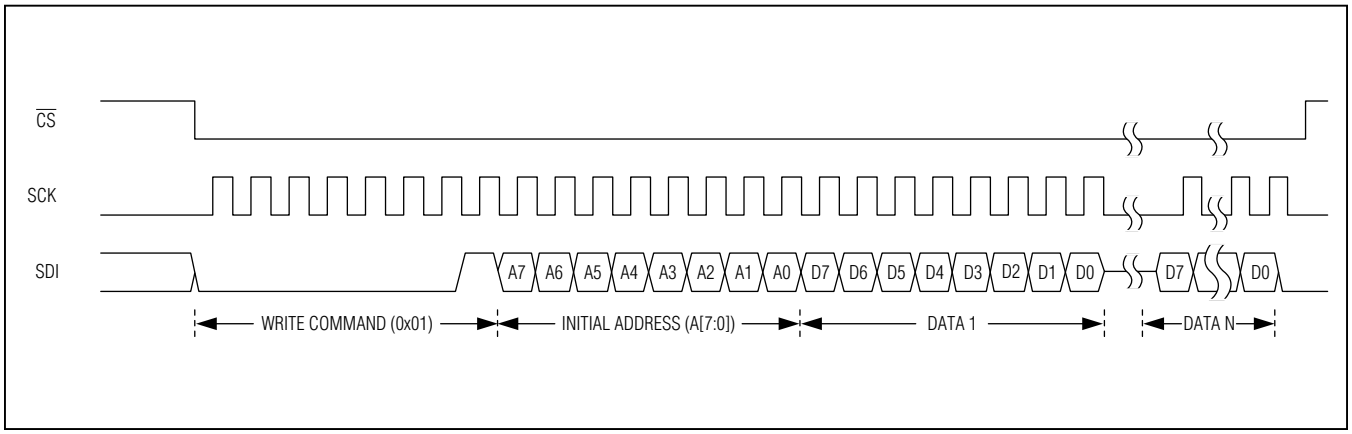


Figure 1. Write Sequence

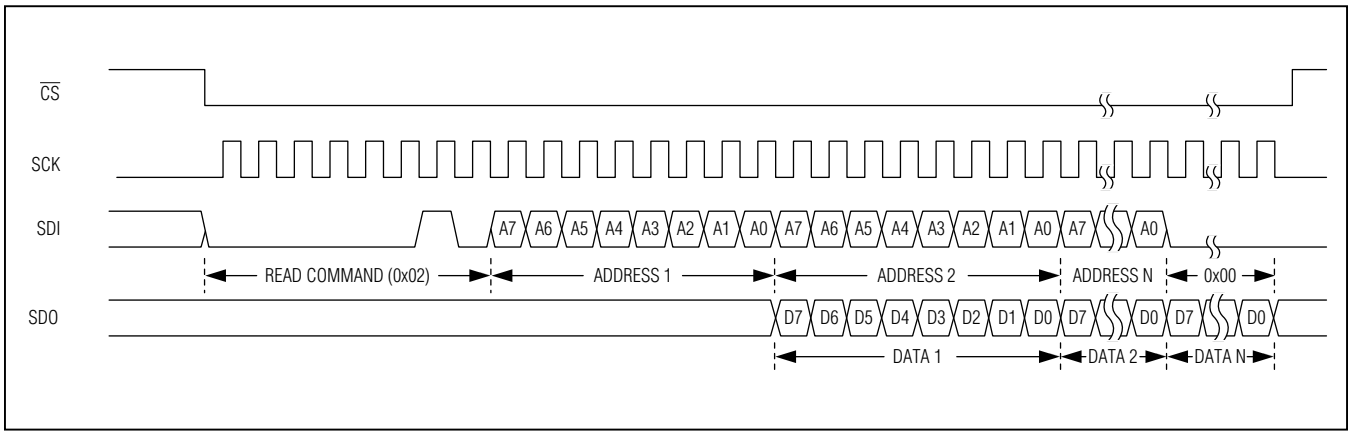


Figure 2. Read Sequence

Table 1. Register Summary

ADDRESS	DESCRIPTION
0x00	Switch state register 1
0x01	Switch state register 2
0x02	Switch state register 3
0x03	Switch state register 4
0x04	Switch state/status register 5
0x05	Configuration register 1
0x06	Configuration register 2
0x07	Interrupt enable register 1
0x08	Interrupt enable register 2
0x09	Interrupt enable register 3
0x0A	Interrupt enable register 4
0x0B	Interrupt enable register 5
0x0C	Wetting current register 1
0x0D	Wetting current register 2
0x0E	Wetting current register 3
0x0F	Wetting current register 4
0x10	Wetting current register 5
0x11	Wetting current register 6
0x12	Wetting current register 7
0x13	Wetting current register 8
0x14	Wetting current register 9
0x15	Threshold select register 1
0x16	Threshold select register 2
0x17	Threshold select register 3
0x18	Threshold select register 4
0x19	Threshold select register 5
0x1A	Threshold select register 6
0x1B	Threshold select register 7
0x1C	Threshold select register 8
0x1D	Threshold select register 9

Read: Within the same $\overline{CS}$ cycle, a read command is implemented as follows:

SDI: <0x02> <Address 1> <Address 2> <Address 3> … <Address N> <0x00>

SDO: <0xXX> <0xXX> <Data 1> <Data 2> … <Data N - 1> <Data N>

With this command, all the registers can be read within the same cycle of $\overline{CS}$. The addresses can be given in any order.

Read All: Within two $\overline{CS}$ cycles, the read-all command is implemented as follows:

$\overline{CS}$_DEV Cycle 1 $\overline{CS}$_DEV Cycle 2

SDI_PWR1: <0x03> <Address N> <0x00> <0x00> <0x00> ... <0x00>

SDO: <Data N><Data N + 1><Data N + 2> ... <Data N + n>

Reset: An SPI reset command is implemented as follows:

SDI_PWR1: <0x04>

An internal master reset pulse is generated from the falling edge of the last SCK signal to the falling edge of the following $\overline{CS}$ signal.

The command bits indicate the registers to be addressed according to Table 2.

Switch State Bits

The SS[34:0] bits indicate the state of the switches connected to inputs IN0–IN34, respectively. SS_ is 0 when the switch is open and 1 when the switch is closed.

Table 2. Register Map

ADDRESS	DATA								MODE
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
0x00	SS34	SS33	SS32	SS31	SS30	SS29	SS28	SS27	R
0x01	SS26	SS25	SS24	SS23	SS22	SS21	SS20	SS19	R
0x02	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	R
0x03	SS10	SS9	SS8	SS7	SS6	SS5	SS4	SS3	R
0x04	SS2	SS1	SS0	—	—	OVP	OTW	OT	R
0x05	P2	P1	P0	PA2	PA1	PA0	LH9	LH8	R/W
0x06	LH7	LH6	LH5	LH4	LH3	LH2	LH1	LH0	R/W
0x07	IE34	IE33	IE32	IE31	IE30	IE29	IE28	IE27	R/W
0x08	IE26	IE25	IE24	IE23	IE22	IE21	IE20	IE19	R/W
0x09	IE18	IE17	IE16	IE15	IE14	IE13	IE12	IE11	R/W
0x0A	IE10	IE9	IE8	IE7	IE6	IE5	IE4	IE3	R/W
0x0B	IE2	IE1	IE0	—	—	—	—	—	R/W
0x0C	—	—	W34.1	W34.0	W33.1	W33.0	W32.1	W32.0	R/W
0x0D	W31.1	W31.0	W30.1	W30.0	W29.1	W29.0	W28.1	W28.0	R/W

Table 2. Register Map (continued)

ADDRESS	DATA								MODE
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
0x0E	W27.1	W27.0	W26.1	W26.0	W25.1	W25.0	W24.1	W24.0	R/W
0x0F	W23.1	W23.0	W22.1	W22.0	W21.1	W21.0	W20.1	W20.0	R/W
0x10	W19.1	W19.0	W18.1	W18.0	W17.1	W17.0	W16.1	W16.0	R/W
0x11	W15.1	W15.0	W14.1	W14.0	W13.1	W13.0	W12.1	W12.0	R/W
0x12	W11.1	W11.0	W10.1	W10.0	W9.1	W9.0	W8.1	W8.0	R/W
0x13	W7.1	W7.0	W6.1	W6.0	W5.1	W5.0	W4.1	W4.0	R/W
0x14	W3.1	W3.0	W2.1	W2.0	W1.1	W1.0	W0.1	W0.0	R/W
0x15	—	—	TH34.1	TH34.0	TH33.1	TH33.0	TH32.1	TH32.0	R/W
0x16	TH31.1	TH31.0	TH30.1	TH30.0	TH29.1	TH29.0	TH28.1	TH28.0	R/W
0x17	TH27.1	TH27.0	TH26.1	TH26.0	TH25.1	TH25.0	TH24.0	TH24.0	R/W
0x18	TH23.1	TH23.0	TH22.1	TH22.0	TH21.1	TH21.0	TH20.1	TH20.0	R/W
0x19	TH19.1	TH19.0	TH18.1	TH18.0	TH17.1	TH17.0	TH16.1	TH16.0	R/W
0x1A	TH15.1	TH15.0	TH14.1	TH14.0	TH13.1	TH13.0	TH12.1	TH12.0	R/W
0x1B	TH11.1	TH11.0	TH10.1	TH10.0	TH9.1	TH9.0	TH8.1	TH8.0	R/W
0x1C	TH7.1	TH7.0	TH6.1	TH6.0	TH5.1	TH5.0	TH4.1	TH4.0	R/W
0x1D	TH3.1	TH3.0	TH2.1	TH2.0	TH1.1	TH1.0	TH0.1	TH0.0	R/W

OVP Bit

When 1, the OVP bit indicates that the IC is in overvoltage shutdown due to BATT being over 29.5V (typ).

OTW/OT Bits

The OTW bit indicates an overtemperature warning, while the OT bit indicates overtemperature shutdown when 1.

Interrupt Enable Bits

The IE[34:0] bits program the switch input channel (IN_) to be interrupt-enabled or interrupt-disabled (0 = interrupt disabled, 1 = interrupt enabled). The default value after power-on is 0.

Switch Configuration for IN0–IN9

The LH[9:0] bits set the switch configuration for IN0–IN9, respectively. Set LH[9:0] to 0 to configure the input channel for a ground-connected switch. Set LH[9:0] to 1 to configure the input channel to battery connected. The default value after power-on is 0.

Wetting Current-Setting Bits

The W_.[1:0] bits set the corresponding switch channel-wetting current as shown in Table 3.

Table 3. Wetting Current Setting

W_.1	W_.0	WETTING CURRENT (mA)
0	0	0
0	1	2*
1	0	5
1	1	10

**Default POR value.*

Table 4. Polling Time Setting

P2	P1	P0	POLLING TIME (ms)
0	0	0	Continuous*
0	0	1	8
0	1	0	16
0	1	1	32
1	0	0	64
1	0	1	128
1	1	0	256
1	1	1	512

**Default POR value.*

Table 5. Polling Active Time Setting

PA2	PA1	PA0	POLLING ACTIVE TIME (Fs)
0	0	0	96
0	0	1	128*
0	1	0	192
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	2048
1	1	1	4096

**Default POR value.*

Table 6. Switch Threshold Setting

TH_.1	TH_.0	SWITCH THRESHOLD
0	0	4V*
0	1	3.8
1	0	3
1	1	2

**Default POR value.*

Applications Information

Power Dissipation

Calculate the total power dissipation of the IC using the following formula:

$$P = V_{BATT} \times (I_{BATT} + I_{WETT})$$

where I_{WETT} is the total wetting current flowing in all closed switches.

The junction-to-ambient thermal resistance is PCB-dependent and is between 26°C/W (JEDEC multilayer board) and 37°C/W (JEDEC single-layer board) for this package. The junction temperature rise is somewhere between P x 26°C/W and P x 37°C/W. Ensure that the junction temperature does not exceed 150°C during normal operation.

If the IC junction temperature exceeds +165°C, an interrupt signal is generated and the wetting currents are disabled to reduce the on-chip power dissipation. During an overtemperature event, the last switch status is retained in internal memory and the switch status is not updated. The interrupt output is cleared when $\overline{CS}$ goes high, but the overtemperature bit T in the output word remains for as long as the overtemperature condition persists. When the junction temperature drops by 15°C, the wetting currents are reenabled and there is a 1ms blanking time before the switches can be polled.

Reverse-Battery Tolerance

The IN0–IN23 switch inputs withstand up to -18V DC voltage without damage. A reverse-battery diode is needed to protect BATT, as shown in the *Typical Application Circuit*.

ISO 7637 Pulse Immunity

The BATT pin and the IN0–IN35 pins are potentially exposed to ISO 7637 pulses. Bypass BATT with a 0.1µF and a 47µF capacitor. The BATT voltage must be limited below 42V during load dump. Bypass IN0–IN35 with at least 0.047µF capacitors at the ECU connector. When IN0–IN9 are used with battery-connected switches, a 100Ω series resistor is needed. These external components allow BATT and IN0–IN35 to withstand ISO 7637 pulses in the application circuit.

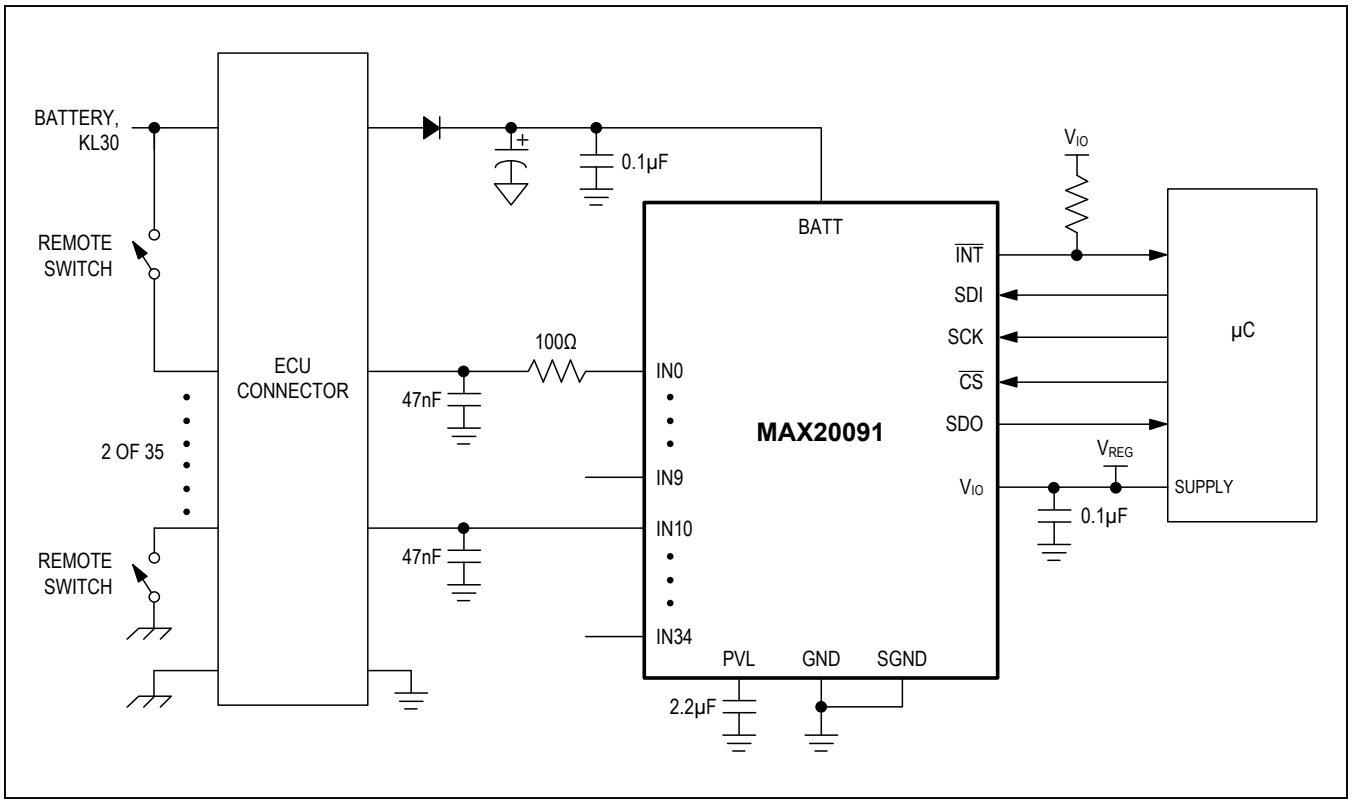
Mechanical Switch Characteristics

The IC is designed to operate with switches that have the following characteristics:

1) Minimum resistance value with switch open (due to leakage): 10kΩ.
2) Maximum resistance value with switch closed: 100Ω.

The above resistor value limits vary with the value of wetting current used and the maximum expected ground shift in the system.

Typical Operating Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN-EP	T4877+6C	21-0144	90-0132

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20091ATM/V+T	-40°C to +125°C	48 TQFN

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/14	Initial release	—
1	2/15	Updated the *Benefits and Features* section	1
2	11/15	Changed SDI, CLK, $\overline{CS}$ input voltage low in *Electrical Characteristics* table from 0.8V to 1V, updated pin 31 in *Pin Description* table, corrected package code in *Package Information* table and moved it and *Chip Information* from page 19 to page 18, removed Selector Guide from *Ordering Information* header and deleted package code column from the table and page 19 from the data sheet	3, 9, 18
3	12/15	Added 5mA and 10mA Wetting Current Accuracy specs to the *Electrical Characteristics* table	3