

## MAX20345

## PMIC with Ultra-Low $I_Q$ Voltage Regulators, Buck-Boost for Optical Sensing and Charger for Small Lithium Ion Systems

### General Description

The MAX20345 is a power management solution featuring ultra-low  $I_Q$  voltage regulators, ideal for low-power wearable applications. The device includes a linear battery charger with a smart power selector and several power-optimized peripherals. The device features three buck regulators, three low-dropout (LDO) linear regulators, and a Buck-Boost regulator, providing up to seven regulated voltages, each with an ultra-low quiescent current. Two load switches allow disconnecting system peripherals to minimize the total quiescent load of the system. MAX20345 allows system designers to minimize power consumption and extend battery life in 24/7 operation devices, such as those in the wearable market.

The three synchronous, high-efficiency buck regulators use a pulse frequency modulated (PFM) control scheme for increased efficiency during light-load operation. The output voltage of these regulators can be programmed through I<sup>2</sup>C down to voltages as low as 0.7V. Additionally, the buck regulators support dynamic voltage scaling (DVS) allowing the system designer to further improve system power consumption when using devices that can take advantage of DVS.

Each of the three LDO regulators output voltage can be programmed through I<sup>2</sup>C. For additional flexibility, each LDO can be configured as a load switch that can be used to disconnect the quiescent load of the system peripherals.

The integrated Buck-Boost converter provides a convenient way to power system peripherals that require voltages higher and/or lower than the battery voltage, and is optimized for optical sensing systems such as optical heart rate (OHR)/PPG and SpO<sub>2</sub> measurements. The output noise of the Buck-Boost is minimized to provide the least impact possible on sensitive measurements in such systems. The addition of DVS offers further power savings during favorable measurement conditions.

The MAX20345 also features a programmable power controller that allows the device to be configured for applications that require the device be in a true-off, or always-on, state. The controller provides a delayed reset signal and voltage sequencing. The MAX20345 is available in a 56-bump, 0.4mm pitch, 3.37mm x 3.05mm wafer-level package (WLP).

### Applications

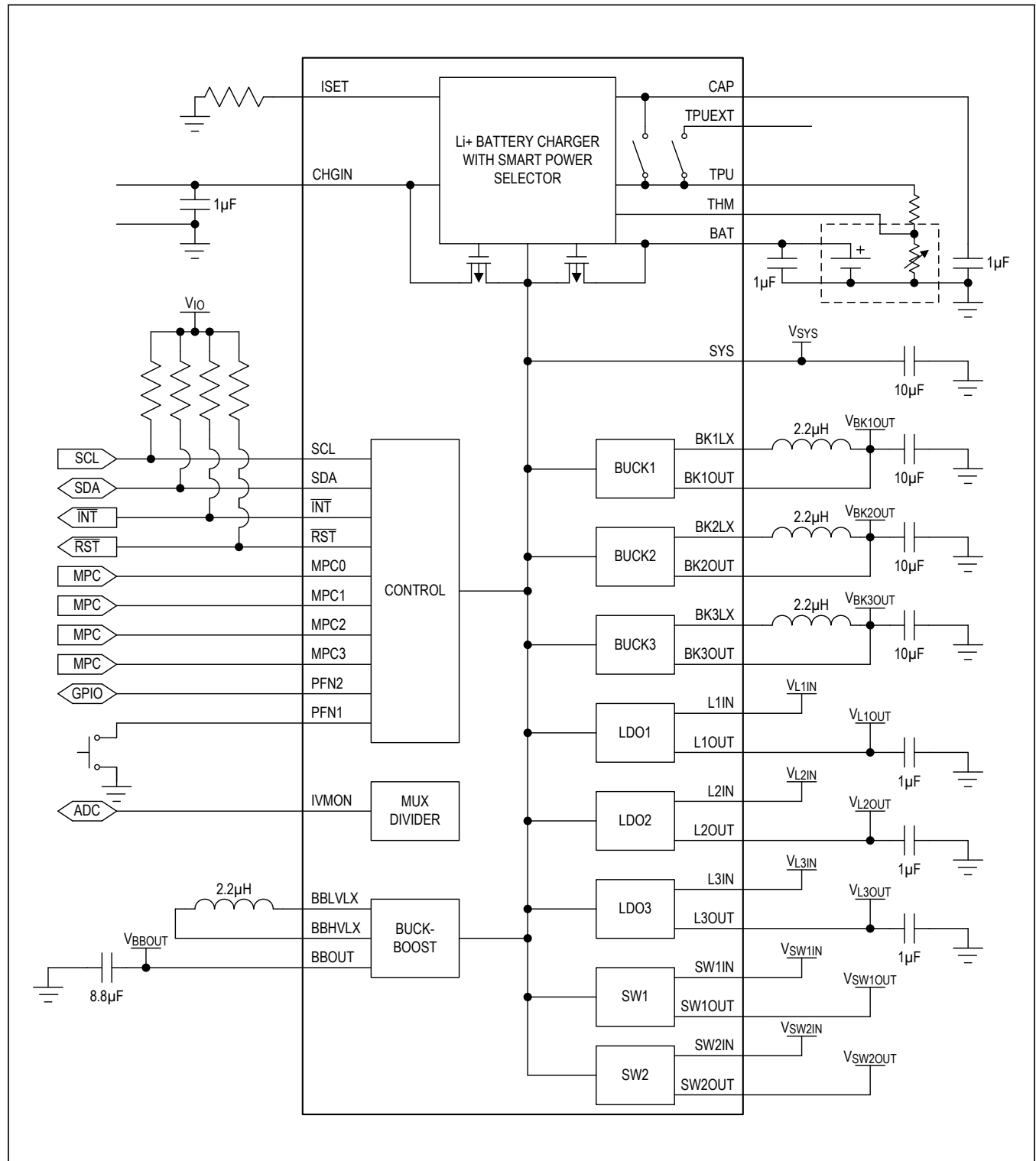
- Wearable Devices
- IoT

[Ordering Information](#) appears at end of data sheet.

### Benefits and Features

- Extend Battery-Use Time Between Charging
  - 3 x Low  $I_Q$  Buck Regulators ( $I_Q = 0.9\mu\text{A typ}$ )
    - 220mA Output Current
    - Noise Mitigation by Flexible Adjustment of Switching Frequency
    - Buck1: 0.700V to 1.330V Output Voltage in 10mV Steps
    - Buck2: 0.700V to 2.275V Output Voltage in 25mV Steps
    - Buck3: 0.700V to 3.850V Output Voltage in 50mV Steps
  - LDO1 ( $I_Q = 0.55\mu\text{A typ}$ )
    - 100mA Output
    - 2.7V to 5.5V Input Voltage Range
    - 0.8V to 3.6V Output Voltage in 100mV Steps
  - LDO2 ( $I_Q = 1\mu\text{A typ}$ )
    - 100mA Output
    - 1.71V to 5.50V Input Voltage Range
    - 0.9V to 4.0V Output Voltage in 100mV Steps
  - LDO3 ( $I_Q = 1\mu\text{A typ}$ )
    - 50mA Output
    - 1.00V to 2.00V Input Voltage Range
    - 0.50V to 1.95V Output Voltage in 25mV Steps
  - 2 x Load Switches
    - 0.65V to 5.50V Input Voltage Range
    - $1\Omega R_{ON}$  at  $\text{SYS} = 3.0\text{V}$
  - Low  $I_Q$  Buck-Boost Regulator ( $I_Q = 2\mu\text{A typ}$ )
    - 1.5W Output Capability
    - 2.6V to 5.5V Output Voltage in 50mV Steps
- Easy to Implement Li+ Battery Charging
  - Linear Li-Ion Battery Charger
    - 5mA to 500mA Charge current
    - +28V / -5.5V Tolerant Input
    - Step Charging (See the [Step Charging](#) Section)
  - Thermistor Monitor
  - Smart Power Selector
- Optimize System Control
  - Power On/ Reset Controller
  - Push-Button Monitor
  - Factory Shipping Mode
  - System Interface
    - Monitor Multiplexer with Programmable Divider to Monitor System Voltages and Charging Current

## Functional Diagram



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## Absolute Maximum Ratings

(Voltages referenced to GND)

|                                                                                        |                                                           |
|----------------------------------------------------------------------------------------|-----------------------------------------------------------|
| CHGIN                                                                                  | -6.0V to +30.0V                                           |
| SDA, SCL, THM, RST, SYS, PFN_, INT_, IVMON, BAT, L1IN, L2IN, BBOUT, SW_IN, TPUEXT, TPU | -0.3V to +6.0V                                            |
| CAP                                                                                    | -0.3V to min ( V <sub>CHGIN</sub>   + 0.3V, +6.0V)        |
| L3IN                                                                                   | -0.3V to 2.2V                                             |
| MPC_, BK_LX, BK_OUT, BBLVLX                                                            | -0.3V to (V <sub>SYS</sub> + 0.3V)                        |
| BBHVLX                                                                                 | -0.3V to min (V <sub>BBOUT</sub> + 0.3V, +6.0V)           |
| ISSET                                                                                  | -0.3V to min (V <sub>BAT</sub> , V <sub>SYS</sub> + 0.3V) |
| L_OUT                                                                                  | -0.3V to (V <sub>L_IN</sub> + 0.3V)                       |
| LSW_OUT                                                                                | -0.3V to (V <sub>LSW_IN</sub> + 0.3V)                     |

|                                                                          |                 |
|--------------------------------------------------------------------------|-----------------|
| Continuous Current into                                                  |                 |
| CHGIN, BAT, SYS                                                          | ±1000mA         |
| Continuous Current into                                                  |                 |
| Any Other Terminal                                                       | ±100mA          |
| Continuous Power Dissipation (multilayer board at +70°C):                |                 |
| 8 x 7 Array 56-Ball, 3.37mm x 3.05mm 0.4mm Pitch WLP (derate 24.79mW/°C) | 1115.5mW        |
| Operating Temperature Range                                              | -40°C to +85°C  |
| Junction Temperature                                                     | +150°C          |
| Storage Temperature Range                                                | -65°C to +150°C |
| Lead Temperature (soldering, 10s)                                        | +300°C          |
| Soldering Temperature (reflow)                                           | +260°C          |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

|                                              |                                                |
|----------------------------------------------|------------------------------------------------|
| <b>PACKAGE TYPE: 56 WLP</b>                  |                                                |
| Package Code                                 | W563H3+1                                       |
| Outline Number                               | <a href="#">21-100260</a>                      |
| Land Pattern Number                          | <a href="#">Refer to Application Note 1891</a> |
| <b>THERMAL RESISTANCE, FOUR-LAYER BOARD:</b> |                                                |
| Junction to Ambient (θ <sub>JA</sub> )       | 40.35°C/W                                      |

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                              | SYMBOL                     | CONDITIONS                                                                                                                                                                                                                  | MIN  | TYP   | MAX  | UNITS |
|----------------------------------------|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|------|-------|
| GLOBAL SUPPLY CURRENT                  |                            |                                                                                                                                                                                                                             |      |       |      |       |
| CHGIN Input Current                    | I <sub>CHGIN</sub>         | V <sub>CHGIN</sub> = 5V, on state, charger disabled, battery thermal monitoring disabled, all rails disabled                                                                                                                | 0.72 | 1.20  |      | mA    |
| BAT Input Current                      | I <sub>BAT</sub>           | V <sub>CHGIN</sub> = 0V, off state, LDO1 disabled                                                                                                                                                                           | 0.40 | 0.96  |      | μA    |
|                                        |                            | V <sub>CHGIN</sub> = 0V, off state, LDO1 enabled, L1IN connected to BAT                                                                                                                                                     | 1.10 | 2.20  |      |       |
|                                        |                            | V <sub>CHGIN</sub> = 0V, on state, all rails disabled                                                                                                                                                                       | 1.45 | 2.50  |      |       |
|                                        |                            | V <sub>CHGIN</sub> = 0V, on state, Buck1 enabled, V <sub>BK1OUT</sub> = 0.9V                                                                                                                                                | 2.30 | 3.70  |      |       |
|                                        |                            | V <sub>CHGIN</sub> = 0V, on state, Buck1 enabled, Buck2 enabled, V <sub>BK1OUT</sub> = 0.9V, V <sub>BK2OUT</sub> = 1.2V                                                                                                     | 2.75 | 4.30  |      |       |
|                                        |                            | V <sub>CHGIN</sub> = 0V, on state, Buck1 enabled, Buck2 enabled, Buck3 enabled, V <sub>BK1OUT</sub> = 0.9V, V <sub>BK2OUT</sub> = 1.2V, V <sub>BK3OUT</sub> = 1.8V                                                          | 3.20 | 5.00  |      |       |
|                                        |                            | V <sub>CHGIN</sub> = 0V, on state, all rails enabled, LDOs in LDO mode, load switch voltage protection enabled, V <sub>BK1OUT</sub> = 0.9V, V <sub>BK2OUT</sub> = 1.2V, V <sub>BK3OUT</sub> = 1.8V, V <sub>BBOUT</sub> = 4V | 9.00 | 14.30 |      |       |
| UVLOS AND BAT OCP                      |                            |                                                                                                                                                                                                                             |      |       |      |       |
| VCCINT UVLO Threshold (POR)            | V <sub>VCCINT_UVLO</sub>   | Rising (Note 2)                                                                                                                                                                                                             | 2.25 | 2.45  | 2.80 | V     |
|                                        |                            | Falling (Note 2)                                                                                                                                                                                                            | 2.20 | 2.40  | 2.70 |       |
| VCCINT UVLO Threshold (POR) Hysteresis | V <sub>VCCINT_UVLO_H</sub> | (Note 2)                                                                                                                                                                                                                    | 50   |       |      | mV    |
| Internal CAP Regulator                 | V <sub>CAP</sub>           | V <sub>CHGIN</sub> = 4.3V to 28V                                                                                                                                                                                            | 3.75 | 4.10  | 4.55 | V     |
| CAP Detect Threshold                   | V <sub>CAP_DET</sub>       | V <sub>CHGIN</sub> = V <sub>CAP</sub> rising                                                                                                                                                                                | 3.15 | 3.40  | 3.60 | V     |
|                                        |                            | V <sub>CHGIN</sub> = V <sub>CAP</sub> falling                                                                                                                                                                               | 2.60 | 2.80  | 3.00 |       |
| CAP Detect Threshold Hysteresis        | V <sub>CAP_DET_H</sub>     |                                                                                                                                                                                                                             | 600  |       |      | mV    |
| CHGIN Detect Threshold                 | V <sub>CHGIN_DET</sub>     | Rising                                                                                                                                                                                                                      | 4.00 | 4.15  | 4.30 | V     |
|                                        |                            | Falling                                                                                                                                                                                                                     | 3.20 | 3.30  | 3.40 |       |
| CHGIN Detect Threshold Hysteresis      | V <sub>CHGIN_DET_H</sub>   |                                                                                                                                                                                                                             | 850  |       |      | mV    |

**Electrical Characteristics (continued)**

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                              | SYMBOL                      | CONDITIONS                                                                             |                                                        | MIN             | TYP  | MAX  | UNITS |
|----------------------------------------|-----------------------------|----------------------------------------------------------------------------------------|--------------------------------------------------------|-----------------|------|------|-------|
| CHGIN Detection Debounce Time          | t <sub>CHGIN_DET</sub>      | CHGIN insertion                                                                        |                                                        | 108             |      |      | ms    |
|                                        |                             | CHGIN detachment                                                                       |                                                        | 100             |      |      |       |
| SYS UVLO Threshold                     | V <sub>SYS_UVLO</sub>       | Rising                                                                                 |                                                        | 2.65            | 2.75 | 2.85 | V     |
|                                        |                             | Falling                                                                                |                                                        | 2.60            | 2.70 | 2.80 |       |
| SYS UVLO Threshold Hysteresis          | V <sub>SYS_UVLO_H</sub>     |                                                                                        |                                                        | 50              |      |      | mV    |
| SYS UVLO Falling Debounce Time         | t <sub>SYS_UVLO_FDEB</sub>  | SYS Falling                                                                            |                                                        | 20              |      |      | μs    |
| BATOC Threshold Accuracy               | I <sub>BAT_OC_ACC</sub>     | From 200mA to 1.6A in 200mA steps, device specific (see I <sub>BatOc</sub> in Table 3) |                                                        | -40             |      | +40  | %     |
| BATOC Threshold Hysteresis             | I <sub>BAT_OC_H</sub>       |                                                                                        |                                                        | 6               |      |      | %     |
| BATOC Rising Debounce Time             | t <sub>BAT_OC_D</sub>       | BAT load current rising                                                                |                                                        | 50              |      |      | ms    |
| OVP AND INPUT CURRENT LIMITER          |                             |                                                                                        |                                                        |                 |      |      |       |
| CHGIN Overvoltage Threshold            | V <sub>CHGIN_OV</sub>       |                                                                                        |                                                        | 7.2             | 7.5  | 7.8  | V     |
| CHGIN Overvoltage Threshold Hysteresis | V <sub>CHGIN_OV_H</sub>     |                                                                                        |                                                        | 200             |      |      | mV    |
| CHGIN Valid Trip Point                 | V <sub>CHGIN_SYS_TP</sub>   | V <sub>CHGIN</sub> - V <sub>SYS</sub> rising                                           |                                                        | 30              | 145  | 290  | mV    |
| CHGIN Valid Trip Point Hysteresis      | V <sub>CHGIN_SYS_TP_H</sub> |                                                                                        |                                                        | 275             |      |      | mV    |
| Input Overcurrent Max Limit            | I <sub>LIM_MAX</sub>        | Device Specific (see Table 3)                                                          | t < t <sub>ILIM_BLANK</sub> , I <sub>LimMax</sub> = 0. | 400             | 450  | 500  | mA    |
|                                        |                             |                                                                                        | t < t <sub>ILIM_BLANK</sub> , I <sub>LimMax</sub> = 1. | 900             | 1000 | 1100 |       |
| Input Current Limit                    | I <sub>LIM</sub>            | ILimCntl = 000                                                                         |                                                        | 50              |      |      | mA    |
|                                        |                             | ILimCntl = 001                                                                         |                                                        | 80    90    100 |      |      |       |
|                                        |                             | ILimCntl = 010                                                                         |                                                        | 150             |      |      |       |
|                                        |                             | ILimCntl = 011                                                                         |                                                        | 200             |      |      |       |
|                                        |                             | ILimCntl = 100                                                                         |                                                        | 300             |      |      |       |
|                                        |                             | ILimCntl = 101                                                                         |                                                        | 400             |      |      |       |
|                                        |                             | ILimCntl = 110                                                                         |                                                        | 400             | 450  | 500  |       |
|                                        |                             | ILimCntl = 111                                                                         |                                                        | 900             | 1000 | 1100 |       |
| Input Current Limit Blanking Time      | t <sub>ILIM_BLANK</sub>     | ILimBlank = 00                                                                         |                                                        | 0.0             |      |      | ms    |
|                                        |                             | ILimBlank = 01                                                                         |                                                        | 0.5             |      |      |       |
|                                        |                             | ILimBlank = 10                                                                         |                                                        | 1.0             |      |      |       |
|                                        |                             | ILimBlank = 11                                                                         |                                                        | 10.0            |      |      |       |

**Electrical Characteristics (continued)**

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                     | SYMBOL                     | CONDITIONS                                                                                 |                 | MIN                         | TYP                         | MAX                         | UNITS |
|-----------------------------------------------|----------------------------|--------------------------------------------------------------------------------------------|-----------------|-----------------------------|-----------------------------|-----------------------------|-------|
| SYS Regulation Voltage                        | V <sub>SYS_REG</sub>       |                                                                                            |                 | V <sub>BAT_REG</sub> + 0.14 | V <sub>BAT_REG</sub> + 0.20 | V <sub>BAT_REG</sub> + 0.26 | V     |
| SYS Regulation Voltage Dropout                | V <sub>CHGIN_SYS</sub>     |                                                                                            |                 | 40                          |                             |                             | mV    |
| CHGIN to SYS On-Resistance                    | R <sub>CHGIN_SYS</sub>     |                                                                                            |                 | 0.37                        | 0.66                        |                             | Ω     |
| Input Current Soft-Start Time                 | t <sub>I</sub> LIM_SFT     |                                                                                            |                 | 1                           |                             |                             | ms    |
| Thermal Shutdown Temperature                  | T <sub>CHG_SHDN</sub>      | Device Specific<br>(see Table 3)                                                           | TShdn = 000     | 50                          |                             |                             | °C    |
|                                               |                            |                                                                                            | TShdn = 001     | 60                          |                             |                             |       |
|                                               |                            |                                                                                            | TShdn = 010     | 70                          |                             |                             |       |
|                                               |                            |                                                                                            | TShdn = 011     | 80                          |                             |                             |       |
|                                               |                            |                                                                                            | TShdn = 100     | 90                          |                             |                             |       |
|                                               |                            |                                                                                            | TShdn = 101     | 100                         |                             |                             |       |
|                                               |                            |                                                                                            | TShdn = 110     | 110                         |                             |                             |       |
|                                               |                            |                                                                                            | TShdn = 111     | 120                         |                             |                             |       |
| CHGIN Boot Retry Timeout                      | t <sub>CHG_RETRY_TMO</sub> | ChgAlwTry = 1                                                                              |                 | 0.5                         |                             |                             | s     |
| BATTERY CHARGER                               |                            |                                                                                            |                 |                             |                             |                             |       |
| BAT-to-SYS On-Resistance                      | R <sub>BAT_SYS</sub>       | V <sub>BAT</sub> = 4.2V, I <sub>BAT</sub> = 300mA                                          |                 | 80                          | 140                         |                             | mΩ    |
| Thermal Regulation Temperature                | T <sub>CHG_LIM</sub>       |                                                                                            |                 | T <sub>CHG_SHDN</sub> - 3   |                             |                             | °C    |
| BAT-to-SYS Switch On Threshold                | V <sub>BAT_SYS_ON</sub>    | SYS falling, measured as V <sub>BAT</sub> - V <sub>SYS</sub>                               |                 | 10                          | 19                          | 35                          | mV    |
| BAT-to-SYS Switch Off Threshold               | V <sub>BAT_SYS_OFF</sub>   | SYS rising, measured as V <sub>BAT</sub> - V <sub>SYS</sub>                                |                 | -3.0                        | -1.5                        | 0.0                         | mV    |
| SYS-to-BAT Charge Current Reduction Threshold | V <sub>SYS_BAT_LIM</sub>   | Measured as V <sub>SYS</sub> - V <sub>BAT</sub> , SysMinVlt = 000, V <sub>BAT</sub> > 3.6V |                 | 100                         |                             |                             | mV    |
| Minimum SYS Voltage                           | V <sub>SYS_LIM</sub>       | V <sub>BAT</sub> < 3.4V                                                                    | SysMinVlt = 000 | 3.6                         |                             |                             | V     |
|                                               |                            |                                                                                            | SysMinVlt = 001 | 3.7                         |                             |                             |       |
|                                               |                            |                                                                                            | SysMinVlt = 010 | 3.8                         |                             |                             |       |
|                                               |                            |                                                                                            | SysMinVlt = 011 | 3.9                         |                             |                             |       |
|                                               |                            |                                                                                            | SysMinVlt = 100 | 4.0                         |                             |                             |       |
|                                               |                            |                                                                                            | SysMinVlt = 101 | 4.1                         |                             |                             |       |
|                                               |                            |                                                                                            | SysMinVlt = 110 | 4.2                         |                             |                             |       |
|                                               |                            |                                                                                            | SysMinVlt = 111 | 4.3                         |                             |                             |       |
| Charger Current Soft-Start Time               | t <sub>CHG_SOFT</sub>      |                                                                                            |                 | 1                           |                             |                             | ms    |

**Electrical Characteristics (continued)**

(V<sub>BAT</sub> = V<sub>SYSTUVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYSEFF</sub> = 10μF, C<sub>BATEFF</sub> = 1μF, C<sub>BKOUTEFF</sub> = 10μF, C<sub>LIN</sub> = 1μF, C<sub>LOUTEFF</sub> = 1μF, C<sub>BBOUTEFF</sub> = 8.8μF, L<sub>BK</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                      | SYMBOL                  | CONDITIONS              | MIN                         | TYP                         | MAX                         | UNITS |
|--------------------------------|-------------------------|-------------------------|-----------------------------|-----------------------------|-----------------------------|-------|
| Precharge Current              | I <sub>PCHG</sub>       | IPChg = 00              |                             | 0.05 x<br>I <sub>FCHG</sub> |                             | mA    |
|                                |                         | IPChg = 01              | 0.09 x<br>I <sub>FCHG</sub> | 0.10 x<br>I <sub>FCHG</sub> | 0.11 x<br>I <sub>FCHG</sub> |       |
|                                |                         | IPChg = 10              |                             | 0.20 x<br>I <sub>FCHG</sub> |                             |       |
|                                |                         | IPChg = 11              |                             | 0.30 x<br>I <sub>FCHG</sub> |                             |       |
| Precharge Threshold            | V <sub>BAT_PCHG</sub>   | VPChg = 000             |                             | 2.10                        |                             | V     |
|                                |                         | VPChg = 001             |                             | 2.25                        |                             |       |
|                                |                         | VPChg = 010             |                             | 2.40                        |                             |       |
|                                |                         | VPChg = 011             |                             | 2.55                        |                             |       |
|                                |                         | VPChg = 100             |                             | 2.70                        |                             |       |
|                                |                         | VPChg = 101             |                             | 2.85                        |                             |       |
|                                |                         | VPChg = 110             |                             | 3.00                        |                             |       |
|                                |                         | VPChg = 111             |                             | 3.15                        |                             |       |
| Precharge Threshold Hysteresis | V <sub>BAT_PCHG_H</sub> |                         |                             | 90                          |                             | mV    |
| Step-Charge Threshold          | V <sub>BAT_STPCHG</sub> | V <sub>BAT</sub> rising | ChgStepRise = 0000          | 3.80                        |                             | V     |
|                                |                         |                         | ChgStepRise = 0001          | 3.85                        |                             |       |
|                                |                         |                         | ChgStepRise = 0010          | 3.90                        |                             |       |
|                                |                         |                         | ChgStepRise = 0011          | 3.95                        |                             |       |
|                                |                         |                         | ChgStepRise = 0100          | 4.00                        |                             |       |
|                                |                         |                         | ChgStepRise = 0101          | 4.05                        |                             |       |
|                                |                         |                         | ChgStepRise = 0110          | 4.10                        |                             |       |
|                                |                         |                         | ChgStepRise = 0111          | 4.15                        |                             |       |
|                                |                         |                         | ChgStepRise = 1000          | 4.20                        |                             |       |
|                                |                         |                         | ChgStepRise = 1001          | 4.25                        |                             |       |
|                                |                         |                         | ChgStepRise = 1010          | 4.30                        |                             |       |
|                                |                         |                         | ChgStepRise = 1011          | 4.35                        |                             |       |
|                                |                         |                         | ChgStepRise = 1100          | 4.40                        |                             |       |
|                                |                         |                         | ChgStepRise = 1101          | 4.45                        |                             |       |
|                                |                         |                         | ChgStepRise = 1110          | 4.50                        |                             |       |
|                                |                         |                         | ChgStepRise = 1111          | 4.55                        |                             |       |

**Electrical Characteristics (continued)**

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                        | SYMBOL                    | CONDITIONS                | MIN | TYP                        | MAX | UNITS |
|--------------------------------------------------|---------------------------|---------------------------|-----|----------------------------|-----|-------|
| Step-Charge Threshold Hysteresis                 | V <sub>BAT_STPCHG_H</sub> | ChgStepHyst = 000         |     | 100                        |     | mV    |
|                                                  |                           | ChgStepHyst = 001         |     | 200                        |     |       |
|                                                  |                           | ChgStepHyst = 010         |     | 300                        |     |       |
|                                                  |                           | ChgStepHyst = 011         |     | 400                        |     |       |
|                                                  |                           | ChgStepHyst = 100         |     | 500                        |     |       |
|                                                  |                           | ChgStepHyst = 101         |     | 600                        |     |       |
| Fast Charge Current Reduction Due to Step-Charge | I <sub>FCHG_STPCHG</sub>  | ChgIStep = 000            |     | I <sub>FCHG</sub><br>x 0.2 |     | mA    |
|                                                  |                           | ChgIStep = 001            |     | I <sub>FCHG</sub><br>x 0.3 |     |       |
|                                                  |                           | ChgIStep = 010            |     | I <sub>FCHG</sub><br>x 0.4 |     |       |
|                                                  |                           | ChgIStep = 011            |     | I <sub>FCHG</sub><br>x 0.5 |     |       |
|                                                  |                           | ChgIStep = 100            |     | I <sub>FCHG</sub><br>x 0.6 |     |       |
|                                                  |                           | ChgIStep = 101            |     | I <sub>FCHG</sub><br>x 0.7 |     |       |
|                                                  |                           | ChgIStep = 110            |     | I <sub>FCHG</sub><br>x 0.8 |     |       |
|                                                  |                           | ChgIStep = 111            |     | I <sub>FCHG</sub>          |     |       |
| ISET Current Gain Factor                         | K <sub>ISET</sub>         |                           |     | 2000                       |     | A/A   |
| ISET Regulation Voltage                          | V <sub>ISET</sub>         |                           |     | 1                          |     | V     |
| BAT Fast Charge Current Set Range                | I <sub>FCHG</sub>         | R <sub>ISET</sub> = 400kΩ |     | 5                          |     | mA    |
|                                                  |                           | R <sub>ISET</sub> = 40kΩ  | 45  | 50                         | 55  |       |
|                                                  |                           | R <sub>ISET</sub> = 4kΩ   |     | 500                        |     |       |

**Electrical Characteristics (continued)**

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                  | SYMBOL                 | CONDITIONS                           | MIN                             | TYP                          | MAX                             | UNITS |
|----------------------------|------------------------|--------------------------------------|---------------------------------|------------------------------|---------------------------------|-------|
| Battery Regulation Voltage | V <sub>BAT_REG</sub>   | BatReg = 0000                        |                                 | 4.050                        |                                 | V     |
|                            |                        | BatReg = 0001                        |                                 | 4.100                        |                                 |       |
|                            |                        | BatReg = 0010                        |                                 | 4.150                        |                                 |       |
|                            |                        | BatReg = 0011, T <sub>A</sub> = 25°C | 4.179                           | 4.200                        | 4.221                           |       |
|                            |                        | BatReg = 0011                        | 4.158                           | 4.200                        | 4.242                           |       |
|                            |                        | BatReg = 0100                        |                                 | 4.250                        |                                 |       |
|                            |                        | BatReg = 0101                        |                                 | 4.300                        |                                 |       |
|                            |                        | BatReg = 0110                        |                                 | 4.350                        |                                 |       |
|                            |                        | BatReg = 0111                        |                                 | 4.400                        |                                 |       |
|                            |                        | BatReg = 1000                        |                                 | 4.450                        |                                 |       |
|                            |                        | BatReg = 1001                        |                                 | 4.500                        |                                 |       |
|                            |                        | BatReg = 1010                        |                                 | 4.550                        |                                 |       |
|                            |                        | BatReg = 1011                        |                                 | 4.600                        |                                 |       |
| Battery Recharge Threshold | V <sub>BAT_RECHG</sub> | BatReChg = 00                        |                                 | 70                           |                                 | mV    |
|                            |                        | BatReChg = 01                        |                                 | 120                          |                                 |       |
|                            |                        | BatReChg = 10                        |                                 | 170                          |                                 |       |
|                            |                        | BatReChg = 11                        |                                 | 220                          |                                 |       |
| Maximum Precharge Time     | t <sub>PCHG</sub>      | PChgTmr = 00                         |                                 | 30                           |                                 | min   |
|                            |                        | PChgTmr = 01                         |                                 | 60                           |                                 |       |
|                            |                        | PChgTmr = 10                         |                                 | 120                          |                                 |       |
|                            |                        | PChgTmr = 11                         |                                 | 240                          |                                 |       |
| Maximum Fast Charge Time   | t <sub>FCHG</sub>      | FChgTmr = 00                         |                                 | 75                           |                                 | min   |
|                            |                        | FChgTmr = 01                         |                                 | 150                          |                                 |       |
|                            |                        | FChgTmr = 10                         |                                 | 300                          |                                 |       |
|                            |                        | FChgTmr = 11                         |                                 | 600                          |                                 |       |
| Charge Done Qualification  | I <sub>CHG_DONE</sub>  | IChgDone = 00                        |                                 | I <sub>FCHG</sub><br>x 0.050 |                                 | mA    |
|                            |                        | IChgDone = 01                        | I <sub>FCHG</sub><br>x<br>0.085 | I <sub>FCHG</sub><br>x 0.100 | I <sub>FCHG</sub><br>x<br>0.115 |       |
|                            |                        | IChgDone = 10                        |                                 | I <sub>FCHG</sub><br>x 0.200 |                                 |       |
|                            |                        | IChgDone = 11                        |                                 | I <sub>FCHG</sub><br>x 0.300 |                                 |       |

**Electrical Characteristics (continued)**

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOU\_T\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOU\_T</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                               | SYMBOL                   | CONDITIONS                | MIN | TYP                          | MAX | UNITS              |
|---------------------------------------------------------|--------------------------|---------------------------|-----|------------------------------|-----|--------------------|
| Maximum Maintain Charge Time                            | t <sub>MTCHG</sub>       | MtChgTmr = 00             |     | 0                            |     | min                |
|                                                         |                          | MtChgTmr = 01             |     | 15                           |     |                    |
|                                                         |                          | MtChgTmr = 10             |     | 30                           |     |                    |
|                                                         |                          | MtChgTmr = 11             |     | 60                           |     |                    |
| Timer Accuracy                                          | t <sub>CHG_ACC</sub>     |                           | -10 |                              | +10 | %                  |
| Fast Charge Current Timer Extend Threshold              | I <sub>FCHG_TEXT</sub>   | See Figure 4              |     | 50                           |     | %I <sub>FCHG</sub> |
| Fast Charge Current Timer Suspend Threshold             | I <sub>FCHG_TSUS</sub>   | See Figure 4              |     | 20                           |     | %I <sub>FCHG</sub> |
| Battery Regulation Voltage Reduction Due to Temperature | V <sub>BAT_REG_JTA</sub> | Cool/Room/WarmBatReg = 00 |     | V <sub>BAT_REG</sub> - 150mV |     | V                  |
|                                                         |                          | Cool/Room/WarmBatReg = 01 |     | V <sub>BAT_REG</sub> - 100mV |     |                    |
|                                                         |                          | Cool/Room/WarmBatReg = 10 |     | V <sub>BAT_REG</sub> - 50mV  |     |                    |
|                                                         |                          | Cool/Room/WarmBatReg = 11 |     | V <sub>BAT_REG</sub>         |     |                    |
| Fast Charge Current Reduction Due to Temperature        | I <sub>FCHG_JTA</sub>    | Cool/Room/WarmIFChg = 000 |     | I <sub>FCHG</sub> x 0.20     |     | mA                 |
|                                                         |                          | Cool/Room/WarmIFChg = 001 |     | I <sub>FCHG</sub> x 0.30     |     |                    |
|                                                         |                          | Cool/Room/WarmIFChg = 010 |     | I <sub>FCHG</sub> x 0.40     |     |                    |
|                                                         |                          | Cool/Room/WarmIFChg = 011 |     | I <sub>FCHG</sub> x 0.50     |     |                    |
|                                                         |                          | Cool/Room/WarmIFChg = 100 |     | I <sub>FCHG</sub> x 0.60     |     |                    |
|                                                         |                          | Cool/Room/WarmIFChg = 101 |     | I <sub>FCHG</sub> x 0.70     |     |                    |
|                                                         |                          | Cool/Room/WarmIFChg = 110 |     | I <sub>FCHG</sub> x 0.80     |     |                    |
|                                                         |                          | Cool/Room/WarmIFChg = 111 |     | I <sub>FCHG</sub>            |     |                    |

## Electrical Characteristics (continued)

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                            | SYMBOL                    | CONDITIONS                                                                                                                                                    |                                         | MIN   | TYP   | MAX   | UNITS             |
|--------------------------------------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|-------|-------|-------|-------------------|
| BAT UVLO Threshold                   | V <sub>BAT_UVLO</sub>     | Rising (valid only when CHGIN is present, when V <sub>BAT</sub> < V <sub>BAT_UVLO</sub> the BAT-SYS switch opens and BAT is connected to SYS through a diode) |                                         | 1.95  | 2.05  | 2.15  | V                 |
| BAT UVLO Threshold Hysteresis        | V <sub>BAT_UVLO_H</sub>   |                                                                                                                                                               |                                         | 50    |       |       | mV                |
| THERMISTOR MONITOR AND NTC DETECTION |                           |                                                                                                                                                               |                                         |       |       |       |                   |
| THM Hot Threshold                    | V <sub>THM_HOT</sub>      | Device specific (see Table 3)                                                                                                                                 | V <sub>THM</sub> falling, JEITASet = 0. | 21.53 | 23.53 | 25.53 | %V <sub>CAP</sub> |
|                                      |                           |                                                                                                                                                               | V <sub>THM</sub> falling, JEITASet = 1, | 30.94 | 32.94 | 34.94 |                   |
| THM Warm Threshold                   | V <sub>THM_WARM</sub>     | Device specific (see Table 3)                                                                                                                                 | V <sub>THM</sub> falling, JEITASet = 0  | 30.94 | 32.94 | 34.94 | %V <sub>CAP</sub> |
|                                      |                           |                                                                                                                                                               | V <sub>THM</sub> falling, JEITASet = 1  | 48.20 | 50.20 | 52.20 |                   |
| THM Cool Threshold                   | V <sub>THM_COOL</sub>     | V <sub>THM</sub> rising                                                                                                                                       |                                         | 62.31 | 64.31 | 66.31 | %V <sub>CAP</sub> |
| THM Cold Threshold                   | V <sub>THM_COLD</sub>     | V <sub>THM</sub> rising                                                                                                                                       |                                         | 71.73 | 73.73 | 75.73 | %V <sub>CAP</sub> |
| THM Disable Threshold                | V <sub>THM_DIS</sub>      | V <sub>THM</sub> rising                                                                                                                                       |                                         | 90.94 | 92.94 | 94.94 | %V <sub>CAP</sub> |
| THM Threshold Hysteresis             | V <sub>THM_H</sub>        |                                                                                                                                                               |                                         | 60    |       |       | mV                |
| THM Input Leakage                    | I <sub>LK_THM</sub>       | V <sub>THM</sub> = 0V to 5.5V                                                                                                                                 |                                         | -1    |       | +1    | μA                |
| TPU Input Leakage                    | I <sub>LK_TPU</sub>       | V <sub>TPU</sub> = 0V to 5.5V                                                                                                                                 |                                         | -1    |       | +1    | μA                |
| TPUEXT Input Leakage                 | I <sub>LK_TPUEXT</sub>    | V <sub>TPUEXT</sub> = 0V to 5.5V                                                                                                                              |                                         | -1    |       | +1    | μA                |
| TPUEXT-to-TPU Switch Resistance      | R <sub>TPUEXT_TPU</sub>   | V <sub>TPUEXT</sub> = [1.0V, V <sub>SYS</sub> ], 3mA through switch                                                                                           |                                         |       | 3     | 10    | Ω                 |
| CAP-to-TPU Switch Resistance         | R <sub>CAP_TPU</sub>      | 3mA through switch                                                                                                                                            |                                         |       | 3     | 10    | Ω                 |
| THM One-Shot Measurement Time        | t <sub>THM_MEAS</sub>     | THM automatically selected as IVMON multiplexer output                                                                                                        |                                         | 450   | 500   |       | ms                |
| IVMON MULTIPLEXER                    |                           |                                                                                                                                                               |                                         |       |       |       |                   |
| IVMON Multiplexer Output Ratio       | V <sub>IVMON_DIV_RT</sub> | No load on IVMON pin. Inputs: Charger Current, BAT, SYS, BK1OUT, BK2OUT, BK3OUT, L1OUT, L2OUT, L3OUT, BBOUT, THM, TPU                                         | MONRatioCfg = 00                        | 100.0 |       |       | %                 |
|                                      |                           |                                                                                                                                                               | MONRatioCfg = 01                        | 50.0  |       |       |                   |
|                                      |                           |                                                                                                                                                               | MONRatioCfg = 10                        | 33.3  |       |       |                   |
|                                      |                           |                                                                                                                                                               | MONRatioCfg = 11                        | 25.0  |       |       |                   |

**Electrical Characteristics (continued)**

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                       | SYMBOL                    | CONDITIONS                                                                                                                                     | MIN   | TYP  | MAX   | UNITS |
|-------------------------------------------------|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|-------|-------|
| IVMON Multiplexer Output Impedance              | R <sub>IVMON_DIV</sub>    | 10μA load on IVMON pin.<br>Inputs: Charger Current, BAT, SYS, BK1OUT, BK2OUT, BK3OUT, L1OUT, L2OUT, L3OUT, BBOUT, THM, TPU<br>MONRatioCfg = 00 |       | 5.5  |       | kΩ    |
|                                                 |                           | 1μA load on IVMON pin.<br>Inputs: Charger Current, BAT, SYS, BK1OUT, BK2OUT, BK3OUT, L1OUT, L2OUT, L3OUT, BBOUT, THM, TPU<br>MONRatioCfg = 01  |       | 31.0 |       |       |
|                                                 |                           | MONRatioCfg = 10                                                                                                                               |       | 28.0 |       |       |
|                                                 |                           | MONRatioCfg = 11                                                                                                                               |       | 24.0 |       |       |
| IVMON Input Leakage                             | I <sub>LK_IVMON</sub>     | IVMON multiplexer disabled, pulldown resistance disabled, V <sub>IVMON</sub> = 0V to 5.5V                                                      | -1    |      | +1    | μA    |
| IVMON Multiplexer Off-State Pulldown Resistance | R <sub>IVMON_OFF_PD</sub> | IVMON multiplexer disabled, pulldown resistance enabled                                                                                        |       | 59   |       | kΩ    |
| <b>BUCK</b>                                     |                           |                                                                                                                                                |       |      |       |       |
| Input Voltage Range                             | V <sub>IN</sub>           | Input voltage = V <sub>SYS</sub>                                                                                                               | 2.700 |      | 5.500 | V     |
| Output Voltage Range                            | V <sub>BK_OUT</sub>       | 10mV step resolution                                                                                                                           | 0.700 |      | 1.330 | V     |
|                                                 |                           | 25mV step resolution                                                                                                                           | 0.700 |      | 2.275 |       |
|                                                 |                           | 50mV step resolution                                                                                                                           | 0.700 |      | 3.850 |       |
| Output Voltage UVLO                             | V <sub>UVLO_BK_</sub>     | Falling edge, hysteresis = 75mV                                                                                                                | 0.15  | 0.38 | 0.58  | V     |

## Electrical Characteristics (continued)

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                             | SYMBOL                    | CONDITIONS                                                                                       |                                                  | MIN  | TYP  | MAX  | UNITS |
|-------------------------------------------------------|---------------------------|--------------------------------------------------------------------------------------------------|--------------------------------------------------|------|------|------|-------|
| Quiescent Supply Current                              | I <sub>Q_BK_</sub>        | I <sub>BK_OUT</sub> = 0, V <sub>SYS</sub> = 3.7V (Note 3)                                        | V <sub>BK_OUT</sub> = 0.9V, 10mV step resolution |      | 0.80 | 1.30 | μA    |
|                                                       |                           |                                                                                                  | V <sub>BK_OUT</sub> = 1.2V, 25mV step resolution |      | 0.83 | 1.30 |       |
|                                                       |                           |                                                                                                  | V <sub>BK_OUT</sub> = 1.8V, 50mV step resolution |      | 0.90 | 1.35 |       |
| Quiescent Supply Current in Dropout                   | I <sub>Q_DO_BK_</sub>     | I <sub>BK_OUT</sub> = 0, V <sub>SYS</sub> - V <sub>BK_OUT</sub> ≤ 0.1V                           |                                                  |      | 300  |      | μA    |
| Shutdown Supply Current with Active Discharge Enabled | I <sub>SD_BK_</sub>       | Buck_ disabled, Buck_ActDsc = 1                                                                  |                                                  |      | 60   |      | μA    |
| Output Average Voltage Accuracy                       | ACC_BK_                   | I <sub>BK_OUT</sub> = 1mA                                                                        |                                                  | -2.5 |      | +2.5 | %     |
| Peak-to-Peak Voltage Ripple                           | V <sub>RPP_BK_</sub>      | Buck_ISet = 0100 (100mA), C <sub>BK_OUT_EFF</sub> = 2.2μF, I <sub>BK_OUT</sub> = 1mA             |                                                  |      | 10   |      | mV    |
| Peak Current Set Range                                | I <sub>PSET_BK_</sub>     | 25mA step resolution. The accuracy of codes below 75mA is limited by t <sub>ON_MIN_BK_</sub>     |                                                  | 0    |      | 375  | mA    |
| Load Regulation Error                                 | LOAD_REG_BK_              | Buck_ISet = 0110 (150mA), Buck_IAdptEn = 1, I <sub>BK_OUT</sub> = 300mA                          |                                                  |      | -3   |      | %     |
| Line Regulation Error                                 | V <sub>LINE_REG_BK_</sub> | V <sub>SYS</sub> from 2.7 to 5.5V                                                                |                                                  |      | 2    |      | mV    |
| Maximum Operative Output Current                      | I <sub>BK_MAX</sub>       | V <sub>SYS</sub> = 3.7V, Buck_ISet = 1000 (200mA), Buck_IAdptEn = 1, load regulation error = -5% |                                                  | 220  |      |      | mA    |
| BK_OUT Pulldown Current with Buck Enabled             | I <sub>PD_BK_E</sub>      | Buck_ enabled                                                                                    | 10mV step resolution                             |      | 40   | 100  | nA    |
|                                                       |                           |                                                                                                  | 25mV step resolution                             |      | 100  | 200  |       |
|                                                       |                           |                                                                                                  | 50mV step resolution                             |      | 200  | 400  |       |
| BK_OUT Pulldown Resistance with Buck Disabled         | R <sub>PD_BK_D</sub>      | Buck_ disabled                                                                                   |                                                  |      | 17.5 |      | MΩ    |
| PMOS On-Resistance                                    | R <sub>P_ON_BK_</sub>     | Buck_FETScale = 0                                                                                |                                                  |      | 0.35 | 0.49 | Ω     |
|                                                       | R <sub>P_ON_BK_FS</sub>   | Buck_FETScale = 1                                                                                |                                                  |      | 0.70 | 0.98 |       |

**Electrical Characteristics (continued)**

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                   | SYMBOL                   | CONDITIONS                                                            | MIN                                                                    | TYP  | MAX  | UNITS |
|---------------------------------------------|--------------------------|-----------------------------------------------------------------------|------------------------------------------------------------------------|------|------|-------|
| NMOS On-Resistance                          | R <sub>N_ON_BK_</sub>    | Buck_FETScale = 0                                                     |                                                                        | 0.25 | 0.40 | Ω     |
|                                             | R <sub>N_ON_BK_FS</sub>  | Buck_FETScale = 1                                                     |                                                                        | 0.50 | 0.70 |       |
| Freewheeling On-Resistance                  | R <sub>ON_BK_FRWHL</sub> | V <sub>SYS</sub> = 3.7V                                               |                                                                        | 7.5  | 12.5 | Ω     |
| Minimum On-Time                             | t <sub>ON_MIN_BK_</sub>  |                                                                       |                                                                        | 60   | 90   | ns    |
| Maximum Duty Cycle                          | D_MAX_BK_                | Buck_IAdptEn = 1                                                      |                                                                        | 95   |      | %     |
| Switching Frequency                         | FREQ_BK_                 | Load Regulation Error = -5%                                           |                                                                        | 3    |      | MHz   |
| Average Current During Short-Circuit to GND | I <sub>SHRT_BK_</sub>    | Buck_ISet = 0110 (150mA), Buck_IAdptEn = 1, V <sub>BK_OUT</sub> = 0V  |                                                                        | 100  |      | mA    |
| BK_LX Leakage Current                       | I <sub>LK_BK_LX</sub>    | Buck_disabled                                                         |                                                                        |      | 1    | μA    |
| Active Discharge Current                    | I <sub>ACTD_BK_</sub>    |                                                                       | 5                                                                      | 18   | 50   | mA    |
| Passive Discharge Resistance                | R <sub>PSV_BK_</sub>     |                                                                       |                                                                        | 10   |      | kΩ    |
| Full Turn-On Time                           | t <sub>ON_BK_</sub>      | Time from enable to full current capability, Buck_SftStrt = 1         |                                                                        | 58   |      | ms    |
| Efficiency                                  | EFFIC_BK_                | I <sub>BK_OUT</sub> = 10mA,<br>Inductor:<br>Murata<br>DFE201610E-2R2M | Buck_VSet = 0.9V,<br>10mV step<br>resolution, Buck_ISet = 0111 (175mA) | 87   |      | %     |
|                                             |                          |                                                                       | Buck_VSet = 1.2V,<br>25mV step<br>resolution, Buck_ISet = 1000 (200mA) | 89   |      |       |
|                                             |                          |                                                                       | Buck_VSet = 1.8V,<br>50mV step<br>resolution, Buck_ISet = 1001 (225mA) | 92   |      |       |
| BK_LX Rising/Falling Slew Rate              | SLW_BK_                  | Buck_LowEMI = 0                                                       |                                                                        | 2.0  |      | V/ns  |
|                                             | SLW_BK_L                 | Buck_LowEMI = 1                                                       |                                                                        | 0.5  |      |       |
| Thermal Shutdown Threshold                  | T <sub>SHDN_BK_</sub>    |                                                                       |                                                                        | 140  |      | °C    |

## Electrical Characteristics (continued)

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOU\_T\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOU\_T</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                             | SYMBOL                    | CONDITIONS                                                                                | MIN   | TYP   | MAX   | UNITS |
|-------------------------------------------------------|---------------------------|-------------------------------------------------------------------------------------------|-------|-------|-------|-------|
| <b>LDO1 (ALWAYS ON LDO OPTION)</b>                    |                           |                                                                                           |       |       |       |       |
| Input Voltage                                         | V <sub>L1IN</sub>         | LDO mode                                                                                  | 2.7   |       | 5.5   | V     |
|                                                       |                           | Switch mode                                                                               | 1.2   |       | 5.5   |       |
| Quiescent Supply Current                              | I <sub>Q_L1</sub>         | LDO enabled, I <sub>L1OUT</sub> = 0μA, V <sub>L1IN</sub> = 3.7V, LDO1VSet = 3.0V (Note 3) |       | 0.50  | 1.10  | μA    |
|                                                       |                           | LDO enabled, I <sub>L1OUT</sub> = 0μA, switch mode, V <sub>L1IN</sub> = 3.7V (Note 3)     |       | 0.32  | 0.55  |       |
| Quiescent Supply Current in Dropout                   | I <sub>Q_L1_DRP</sub>     | I <sub>L1OUT</sub> = 0μA, V <sub>L1IN</sub> = 2.9V, LDO1VSet = 3.0V (Note 3)              |       | 88    | 120   | μA    |
| Shutdown Supply Current with Active Discharge Enabled | I <sub>SD_L1</sub>        | LDO disabled, LDO1ActDsc = 1                                                              |       | 55    |       | μA    |
| Output Leakage                                        | I <sub>LK_L1OUT</sub>     | V <sub>L1OUT</sub> = GND, LDO disabled                                                    |       |       | 1     | μA    |
| Maximum Output Current                                | I <sub>L1OUT_MAX</sub>    |                                                                                           | 100   |       |       | mA    |
| Output Voltage Range                                  | V <sub>L1OUT</sub>        | 100mV step resolution                                                                     | 0.8   |       | 3.6   | V     |
| Output Voltage Accuracy                               | ACC_LDO1                  | V <sub>L1IN</sub> = (V <sub>L1OUT</sub> + 0.5V) or higher, I <sub>L1OUT</sub> = 1mA       | -2.7  |       | +2.7  | %     |
| Dropout Voltage                                       | V <sub>DRP_L1</sub>       | V <sub>L1IN</sub> = 2.9V, I <sub>L1OUT</sub> = 100mA, LDO1VSet = 3.0V                     |       |       | 95    | mV    |
| Line Regulation Error                                 | V <sub>LINE_REG_L1</sub>  | V <sub>L1IN</sub> = (V <sub>L1OUT</sub> + 0.5V) to 5.5V, I <sub>L1OUT</sub> = 1mA         | -0.12 |       | +0.12 | %/V   |
| Load Regulation Error                                 | V <sub>LOAD_REG_L1</sub>  | I <sub>L1OUT</sub> = 100μA to 100mA                                                       |       | 0.002 | 0.005 | %/mA  |
| Line Transient                                        | V <sub>LINE_TRAN_L1</sub> | V <sub>L1IN</sub> = 4V to 5V, 200ns rise time                                             |       | ±36   |       | mV    |
|                                                       |                           | V <sub>L1IN</sub> = 4V to 5V, 1μs rise time                                               |       | ±28   |       |       |
| Load Transient                                        | V <sub>LOAD_TRAN_L1</sub> | I <sub>L1OUT</sub> = 0mA to 10mA, 200ns rise time                                         |       | 130   |       | mV    |
|                                                       |                           | I <sub>L1OUT</sub> = 0mA to 100mA, 200ns rise time                                        |       | 290   |       |       |
| Passive Discharge Resistance                          | R <sub>PSV_L1</sub>       |                                                                                           | 4     | 10    | 17    | kΩ    |
| Active Discharge Current                              | I <sub>ACTD_L1</sub>      | V <sub>L1IN</sub> = 3.7V                                                                  | 7     | 20    | 36    | mA    |
| Switch Mode Resistance                                | R <sub>ON_L1</sub>        | V <sub>L1IN</sub> = 1.8V, I <sub>L1OUT</sub> = 100mA                                      |       | 0.63  | 1.00  | Ω     |
|                                                       |                           | V <sub>L1IN</sub> = 1.2V, I <sub>L1OUT</sub> = 5mA                                        |       | 1.40  | 2.30  |       |
| Turn-On Time                                          | t <sub>ON_L1</sub>        | I <sub>L1OUT</sub> = 0mA, time from 10% to 90% of final value                             |       | 1.60  |       | ms    |
|                                                       |                           | I <sub>L1OUT</sub> = 0mA, time from 10% to 90% of final value, switch mode                |       | 0.25  |       |       |
| Short-Circuit Current Limit                           | I <sub>SHRT_L1</sub>      | V <sub>L1IN</sub> = 2.7V, V <sub>L1OUT</sub> = 0V                                         | 220   | 400   | 590   | mA    |
| Thermal Shutdown Temperature                          | T <sub>SHDN_L1</sub>      |                                                                                           |       | 150   |       | °C    |

**Electrical Characteristics (continued)**

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                             | SYMBOL                    | CONDITIONS                                                                          |                 | MIN   | TYP   | MAX   | UNITS             |
|-------------------------------------------------------|---------------------------|-------------------------------------------------------------------------------------|-----------------|-------|-------|-------|-------------------|
| Thermal Shutdown Temperature Hysteresis               | T <sub>SHDN_HYS_L1</sub>  |                                                                                     |                 | 20    |       |       | °C                |
| Output Noise                                          | V <sub>NOISE_L1</sub>     | 10Hz to 100kHz, V <sub>L1IN</sub> = 5V                                              | LDO1VSet = 3.3V | 110   |       |       | μV <sub>RMS</sub> |
|                                                       |                           |                                                                                     | LDO1VSet = 2.5V | 95    |       |       |                   |
|                                                       |                           |                                                                                     | LDO1VSet = 1.2V | 60    |       |       |                   |
|                                                       |                           |                                                                                     | LDO1VSet = 0.8V | 60    |       |       |                   |
| LDO2                                                  |                           |                                                                                     |                 |       |       |       |                   |
| Input Voltage                                         | V <sub>L2IN</sub>         | LDO mode                                                                            |                 | 1.71  | 5.50  |       | V                 |
|                                                       |                           | Switch mode                                                                         |                 | 1.20  | 5.50  |       |                   |
| Quiescent Supply Current                              | I <sub>Q_L2</sub>         | LDO enabled, I <sub>L2OUT</sub> = 0μA (Note 3)                                      |                 | 1.00  | 2.00  |       | μA                |
|                                                       |                           | LDO enabled, I <sub>L2OUT</sub> = 0μA, switch mode (Note 3)                         |                 | 0.32  | 0.60  |       |                   |
| Quiescent Supply Current in Dropout                   | I <sub>Q_L2_DRP</sub>     | I <sub>L2OUT</sub> = 0μA, V <sub>L2IN</sub> = 2.9V, LDO2VSet = 3.0V                 |                 | 2.0   | 3.8   |       | μA                |
| Shutdown Supply Current with Active Discharge Enabled | I <sub>SD_L2</sub>        | LDO disabled, LDO2ActDsc = 1                                                        |                 | 50    |       |       | μA                |
| Output Leakage                                        | I <sub>LK_L2OUT</sub>     | V <sub>L2OUT</sub> = GND, LDO disabled                                              |                 | 1     |       |       | μA                |
| Maximum Output Current                                | I <sub>L2OUT_MAX</sub>    | V <sub>L2IN</sub> > 1.8V                                                            |                 | 100   |       |       | mA                |
|                                                       |                           | V <sub>L2IN</sub> ≤ 1.8V                                                            |                 | 50    |       |       |                   |
| Output Voltage Range                                  | V <sub>L2OUT</sub>        | 100mV step resolution                                                               |                 | 0.9   | 4.0   |       | V                 |
| Output Voltage Accuracy                               | ACC_LDO2                  | V <sub>L2IN</sub> = (V <sub>L2OUT</sub> + 0.5V) or higher, I <sub>L2OUT</sub> = 1mA |                 | -2.7  | +2.7  |       | %                 |
| Dropout Voltage                                       | V <sub>DRP_L2</sub>       | V <sub>L2IN</sub> = 2.9V, I <sub>L2OUT</sub> = 100mA, LDO2VSet = 3V                 |                 | 90    |       |       | mV                |
| Line Regulation Error                                 | V <sub>LINE_REG_L2</sub>  | V <sub>L2IN</sub> = (V <sub>L2OUT</sub> + 0.5V) to 5.5V, I <sub>L2OUT</sub> = 1mA   |                 | -0.45 | +0.45 |       | %/V               |
| Load Regulation Error                                 | V <sub>LOAD_REG_L2</sub>  | I <sub>L2OUT</sub> = 100μA to 100mA                                                 |                 | 0.001 | 0.007 | % /mA |                   |
| Line Transient                                        | V <sub>LINE_TRAN_L2</sub> | V <sub>L2IN</sub> = 4V to 5V, 200ns rise time                                       |                 | ±35   |       |       | mV                |
|                                                       |                           | V <sub>L2IN</sub> = 4V to 5V, 1μs rise time                                         |                 | ±25   |       |       |                   |
| Load Transient                                        | V <sub>LOAD_TRAN_L2</sub> | I <sub>L2OUT</sub> = 0mA to 10mA, 200ns rise time                                   |                 | 100   |       |       | mV                |
|                                                       |                           | I <sub>L2OUT</sub> = 0mA to 100mA, 200ns rise time                                  |                 | 200   |       |       |                   |
| Passive Discharge Resistance                          | R <sub>PSV_L2</sub>       |                                                                                     |                 | 4     | 10    | 17    | kΩ                |
| Active Discharge Current                              | I <sub>ACTD_L2</sub>      | V <sub>L2IN</sub> = 3.7V                                                            |                 | 7     | 20    | 36    | mA                |
| Switch Mode Resistance                                | R <sub>ON_L2</sub>        | V <sub>L2IN</sub> = 1.8V, I <sub>L2OUT</sub> = 100mA                                |                 | 0.60  | 0.97  |       | Ω                 |
|                                                       |                           | V <sub>L2IN</sub> = 1.2V, I <sub>L2OUT</sub> = 5mA                                  |                 | 1.30  | 2.20  |       |                   |

**Electrical Characteristics (continued)**

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                             | SYMBOL                   | CONDITIONS                                                                          |                 | MIN   | TYP  | MAX   | UNITS             |
|-------------------------------------------------------|--------------------------|-------------------------------------------------------------------------------------|-----------------|-------|------|-------|-------------------|
| Turn-On Time                                          | t <sub>ON_L2</sub>       | I <sub>L2OUT</sub> = 0mA, time from 10% to 90% of final value                       |                 | 1.50  |      |       | ms                |
|                                                       |                          | I <sub>L2OUT</sub> = 0mA, time from 10% to 90% of final value, switch mode          |                 | 0.25  |      |       |                   |
| Short-Circuit Current Limit                           | I <sub>SHRT_L2</sub>     | V <sub>L2IN</sub> = 2.7V, V <sub>L2OUT</sub> = GND                                  |                 | 220   | 400  | 590   | mA                |
| Thermal Shutdown Temperature                          | T <sub>SHDN_L2</sub>     |                                                                                     |                 | 150   |      |       | °C                |
| Thermal Shutdown Temperature Hysteresis               | T <sub>SHDN_HYS_L2</sub> |                                                                                     |                 | 20    |      |       | °C                |
| L2IN UVLO                                             | V <sub>UVLO_L2</sub>     | V <sub>L2IN</sub> falling                                                           |                 | 1.14  | 1.32 |       | V                 |
|                                                       |                          | V <sub>L2IN</sub> rising                                                            |                 |       | 1.35 | 1.59  |                   |
| Output Noise                                          | V <sub>NOISE_L2</sub>    | 10Hz to 100kHz, V <sub>L2IN</sub> = 5V                                              | LDO2VSet = 3.3V | 110   |      |       | μV <sub>RMS</sub> |
|                                                       |                          |                                                                                     | LDO2VSet = 2.5V | 95    |      |       |                   |
|                                                       |                          |                                                                                     | LDO2VSet = 1.2V | 60    |      |       |                   |
|                                                       |                          |                                                                                     | LDO2VSet = 0.9V | 60    |      |       |                   |
| LDO3                                                  |                          |                                                                                     |                 |       |      |       |                   |
| Input Voltage                                         | V <sub>L3IN</sub>        | LDO mode                                                                            |                 | 1.0   |      | 2.0   | V                 |
|                                                       |                          | Switch mode                                                                         |                 | 0.7   |      | 2.0   |                   |
| Quiescent Supply Current                              | I <sub>Q_L3</sub>        | LDO enabled, I <sub>L3OUT</sub> = 0μA (Note 3)                                      |                 | 1.05  |      | 2.65  | μA                |
|                                                       |                          | LDO enabled, I <sub>L3OUT</sub> = 0μA, switch mode (Note 3)                         |                 | 0.26  |      | 0.60  |                   |
|                                                       |                          | LDO enabled, I <sub>L3OUT</sub> = 0μA, LDO3_MPC0CNT = 1, MPC0 high (Note 3)         |                 | 0.70  |      | 1.35  |                   |
| Quiescent Supply Current in Dropout                   | I <sub>Q_L3_DRP</sub>    | I <sub>L3OUT</sub> = 0μA, V <sub>L3IN</sub> = 1.2V, LDO3VSet = 1.3V (Note 3)        |                 | 2.4   |      | 4.6   | μA                |
| Output Leakage                                        | I <sub>LK_L3OUT</sub>    | V <sub>L3OUT</sub> = GND, LDO disabled                                              |                 | 0.015 |      | 2.500 | μA                |
| Shutdown Supply Current with Active Discharge Enabled | I <sub>SD_L3</sub>       | LDO disabled, LDO3ActDsc = 1                                                        |                 | 50    |      |       | μA                |
| Maximum Output Current                                | I <sub>L3OUT_MAX</sub>   |                                                                                     |                 | 50    |      |       | mA                |
| Output Voltage Range                                  | V <sub>L3OUT</sub>       | 25mV step resolution                                                                |                 | 0.50  |      | 1.95  | V                 |
| Output Voltage Accuracy                               | ACC_LDO3                 | V <sub>L3IN</sub> = (V <sub>L3OUT</sub> + 0.2V) or higher, I <sub>L3OUT</sub> = 1mA |                 | -3    |      | +3    | %                 |
| Dropout Voltage                                       | V <sub>DRP_L3</sub>      | V <sub>L3IN</sub> = 1V, I <sub>L3OUT</sub> = 50mA, LDO3VSet = 1.025V                |                 |       |      | 75    | mV                |
| Line Regulation Error                                 | V <sub>LINE_REG_L3</sub> | V <sub>L3IN</sub> = (V <sub>L3OUT</sub> + 0.2V) to 2V, I <sub>L3OUT</sub> = 1mA     |                 | -0.4  |      | +0.4  | %/V               |
| Load Regulation Error                                 | V <sub>LOAD_REG_L3</sub> | I <sub>L3OUT</sub> = 100μA to 50mA                                                  |                 | 0.003 |      | 0.013 | %/mA              |

**Electrical Characteristics (continued)**

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                             | SYMBOL                    | CONDITIONS                                                                                                               | MIN  | TYP  | MAX  | UNITS             |
|-------------------------------------------------------|---------------------------|--------------------------------------------------------------------------------------------------------------------------|------|------|------|-------------------|
| Line Transient                                        | V <sub>LINE_TRAN_L3</sub> | V <sub>L3IN</sub> = 1V to 2V, 200ns rise time                                                                            |      | ±45  |      | mV                |
|                                                       |                           | V <sub>L3IN</sub> = 1V to 2V, 1μs rise time                                                                              |      | ±25  |      |                   |
| Load Transient                                        | V <sub>LOAD_TRAN_L3</sub> | I <sub>L3OUT</sub> = 0mA to 10mA, 200ns rise time                                                                        |      | 80   |      | mV                |
|                                                       |                           | I <sub>L3OUT</sub> = 0mA to 50mA, 200ns rise time                                                                        |      | 130  |      |                   |
| Passive Discharge Resistance                          | R <sub>PSV_L3</sub>       |                                                                                                                          | 4    | 10   | 17   | kΩ                |
| Active Discharge Current                              | I <sub>ACTD_L3</sub>      | V <sub>L3IN</sub> = 1.8V                                                                                                 | 10   | 30   | 60   | mA                |
| Switch Mode Resistance                                | R <sub>ON_L3</sub>        | V <sub>L3IN</sub> = 1.8V, I <sub>L3OUT</sub> = 50mA                                                                      |      | 0.40 | 0.64 | Ω                 |
|                                                       |                           | V <sub>L3IN</sub> = 0.7V, I <sub>L3OUT</sub> = 1mA                                                                       |      | 1.50 | 3.30 |                   |
| Turn-On Time                                          | t <sub>ON_L3</sub>        | I <sub>L3OUT</sub> = 0mA, time from 10% to 90% of final value                                                            |      | 380  |      | μs                |
|                                                       |                           | I <sub>L3OUT</sub> = 0mA, time from 10% to 90% of final value, switch mode                                               |      | 65   |      |                   |
|                                                       |                           | I <sub>L3OUT</sub> = 0mA, LDO3_MPC0CNT = 1, time from MPC0 rising to 90% of L3OUT final value, C <sub>L3OUT</sub> = 10nF |      | 155  | 350  | ns                |
| Short-Circuit Current Limit                           | I <sub>SHRT_L3</sub>      | V <sub>L3IN</sub> = 1.2V, V <sub>L3OUT</sub> = GND                                                                       |      | 345  | 950  | mA                |
|                                                       |                           | V <sub>L3IN</sub> = 1.2V, V <sub>L3OUT</sub> = GND, switch mode                                                          |      | 310  | 700  |                   |
| Thermal Shutdown Temperature                          | T <sub>SHDN_L3</sub>      |                                                                                                                          |      | 150  |      | °C                |
| Thermal Shutdown Temperature Hysteresis               | T <sub>SHDN_HYS_L3</sub>  |                                                                                                                          |      | 20   |      | °C                |
| L3IN UVLO                                             | V <sub>UVLO_L3</sub>      | V <sub>L3IN</sub> falling                                                                                                | 0.65 | 0.77 |      | V                 |
|                                                       |                           | V <sub>L3IN</sub> rising                                                                                                 |      | 0.78 | 0.95 |                   |
| Output Noise                                          | V <sub>NOISE_L3</sub>     | 10Hz to 100kHz, V <sub>L3IN</sub> = 2V                                                                                   |      | 120  |      | μV <sub>RMS</sub> |
|                                                       |                           | LDO3VSet = 1.8V                                                                                                          |      |      |      |                   |
|                                                       |                           | LDO3VSet = 1.0V                                                                                                          |      | 95   |      |                   |
|                                                       |                           | LDO3VSet = 0.5V                                                                                                          |      | 70   |      |                   |
| <b>BUCK-BOOST</b>                                     |                           |                                                                                                                          |      |      |      |                   |
| Input Voltage Range                                   | V <sub>BBIN</sub>         | Input voltage = V <sub>SYS</sub>                                                                                         | 2.7  |      | 5.5  | V                 |
| Output Voltage Range                                  | V <sub>BBOUT</sub>        | 50mV step resolution, do not exceed the valid voltage range.                                                             | 2.6  |      | 5.5  | V                 |
| Quiescent Supply Current                              | I <sub>Q_BB</sub>         | I <sub>BBOUT</sub> = 0μA, V <sub>BBOUT</sub> = 5V (Note 3)                                                               |      | 2.5  | 5.0  | μA                |
| Shutdown Supply Current with Active Discharge Enabled | I <sub>SD_BB</sub>        | Buck-Boost disabled, BBstActDsc = 1                                                                                      |      | 60   |      | μA                |

## Electrical Characteristics (continued)

(V<sub>BAT</sub> = V<sub>SYSTUVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGINDET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYSEFF</sub> = 10μF, C<sub>BATEFF</sub> = 1μF, C<sub>BKOUTEFF</sub> = 10μF, C<sub>LIN</sub> = 1μF, C<sub>LOUTEFF</sub> = 1μF, C<sub>BBOUTEFF</sub> = 8.8μF, L<sub>BK</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                                          | SYMBOL                     | CONDITIONS                                                                                              | MIN  | TYP  | MAX  | UNITS |
|--------------------------------------------------------------------|----------------------------|---------------------------------------------------------------------------------------------------------|------|------|------|-------|
| Maximum Output Operative Power                                     | P <sub>MAX_BBOUT</sub>     | BBStlpPadPENb = 0, V <sub>BBIN</sub> ≥ 3.2V, V <sub>BBOUT</sub> ≥ 3.2V at 7.5% load regulation (Note 3) | 1.5  |      |      | W     |
| Load Regulation Error                                              | LOAD_REG_ERR               | BBStlpPadPENb = 0, BBStVSet > 3.3V, P <sub>OUT</sub> = 1.5W                                             |      | -3.5 |      | %     |
| Average Output Voltage Accuracy                                    | ACC_BBOUT                  | I <sub>BBOUT</sub> = 1mA, C <sub>BBOUTEFF</sub> ≥ 5μF                                                   | -3   |      | +3   | %     |
| Maximum Output Current During Startup                              | I <sub>LOAD_MAX_STUP</sub> | V <sub>BBIN</sub> > 3V, BBStlpPadPENb = 0                                                               | 100  |      |      | mA    |
| Startup time                                                       | t <sub>STUP</sub>          | I <sub>LOAD</sub> < I <sub>LOAD_MAX_STUP</sub> , time from V <sub>BBOUT</sub> = 0V to final value       |      | 13   |      | ms    |
| Input Supply Current During Startup                                | I <sub>BBIN_STUP</sub>     | V <sub>BBIN</sub> = 3.6V, V <sub>BBOUT</sub> = 5V, C <sub>BBOUTEFF</sub> = 10μF, I <sub>BBOUT</sub> = 0 |      | 10   |      | mA    |
| Output UVLO Threshold                                              | V <sub>BBOUT_UVLO</sub>    | Falling edge (50mV hysteresis)                                                                          |      | 1.85 | 2.46 | V     |
| HVLX Leakage Current                                               | I <sub>LK_BBH_VLX</sub>    |                                                                                                         |      |      | 1    | μA    |
| LVLX Leakage Current                                               | I <sub>LK_BBL_VLX</sub>    |                                                                                                         |      |      | 1    | μA    |
| Passive Discharge Resistance                                       | R <sub>PSV_BB</sub>        |                                                                                                         | 5    | 10   | 17   | kΩ    |
| Active Discharge Current                                           | I <sub>ACTD_BB</sub>       | V <sub>BBOUT</sub> = 2.5V                                                                               | 5    | 20   | 50   | mA    |
| BBOUT Pulldown Current                                             | I <sub>PD_BB_E</sub>       | BB enabled                                                                                              |      | 200  |      | nA    |
| Thermal Shutdown Threshold                                         | T <sub>SHDN_BB</sub>       |                                                                                                         |      | 150  |      | °C    |
| <b>LOAD SWITCHES (TYPICAL VALUES AT V<sub>LSW_IN</sub> = 1.2V)</b> |                            |                                                                                                         |      |      |      |       |
| Input Voltage                                                      | V <sub>LSW_IN</sub>        |                                                                                                         | 0.65 |      | 5.50 | V     |
| Quiescent Supply Current                                           | I <sub>Q_LSW_</sub>        | Load switch on, voltage protection enabled, V <sub>LSW_IN</sub> = 1.2V (Note 3)                         |      | 0.80 | 1.20 | μA    |
|                                                                    |                            | Load switch on, voltage protection disabled, V <sub>LSW_IN</sub> = 1.2V (Note 3)                        |      | 0.26 | 0.45 |       |
| On-Resistance                                                      | R <sub>ON_LSW_</sub>       | V <sub>SYST</sub> = 3V, V <sub>LSW_IN</sub> = 1.2V, I <sub>LSW_OUT</sub> = 50mA                         |      | 0.44 | 0.75 | Ω     |
| Startup Current                                                    | I <sub>LSW_START</sub>     | V <sub>LSW_IN</sub> = 1.2V, V <sub>LSW_OUT</sub> = 0V initially                                         | 22   | 63   | 108  | mA    |
| Voltage Protection Threshold                                       | V <sub>LSW_PROT</sub>      | Rising                                                                                                  |      | 130  | 250  | mV    |
|                                                                    |                            | Falling                                                                                                 | 4    | 120  |      |       |
| Turn-On Time                                                       | t <sub>ON_LSW_</sub>       | V <sub>LSW_IN</sub> = 1.2V, 1μF output capacitance, from 10% to 90% of final value                      |      | 15   |      | μs    |
| Startup Time-Out Time                                              | t <sub>STUP_LSW</sub>      |                                                                                                         |      | 5    |      | ms    |

**Electrical Characteristics (continued)**

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                                                                     | SYMBOL                  | CONDITIONS                                                                                        | MIN  | TYP                       | MAX  | UNITS |
|-----------------------------------------------------------------------------------------------|-------------------------|---------------------------------------------------------------------------------------------------|------|---------------------------|------|-------|
| Startup Retry Time                                                                            | t <sub>RETRY_LSW_</sub> |                                                                                                   |      | 5                         |      | ms    |
| Passive Discharge Resistance                                                                  | R <sub>PSV_LSW_</sub>   |                                                                                                   | 4    | 10                        | 17   | kΩ    |
| Active Discharge Current                                                                      | I <sub>ACTD_LSW_</sub>  |                                                                                                   | 7    | 20                        | 36   | mA    |
| Output Leakage                                                                                | I <sub>LK_LSW_</sub>    | LSW_OUT = GND, load switch disabled                                                               |      |                           | 1    | μA    |
| <b>DIGITAL</b>                                                                                |                         |                                                                                                   |      |                           |      |       |
| SDA, SCL, MPC_, PFN_, $\overline{\text{RST}}$ , $\overline{\text{INT}}$ Input Leakage Current | I <sub>LK_IO</sub>      | Input pullup/pulldown resistances disabled, V <sub>IO</sub> = 0V to 5.5V                          | -1   |                           | +1   | μA    |
| SDA, SCL, MPC_ Input Logic High                                                               | V <sub>IO_IH</sub>      |                                                                                                   | 1.4  |                           |      | V     |
| SDA, SCL, MPC_ Input Logic Low                                                                | V <sub>IO_IL</sub>      |                                                                                                   |      |                           | 0.4  | V     |
| PFN_ Input Logic High                                                                         | V <sub>PFN_IH_C</sub>   | Off mode                                                                                          |      | 0.7 x V <sub>VCCINT</sub> |      | V     |
| PFN_ Input Logic Low                                                                          | V <sub>PFN_IL_C</sub>   | Off mode                                                                                          |      | 0.3 x V <sub>VCCINT</sub> |      | V     |
| PFN_ Input Logic High                                                                         | V <sub>PFN_IH_T</sub>   | On mode                                                                                           | 1.4  |                           |      | V     |
| PFN_ Input Logic Low                                                                          | V <sub>PFN_IL_T</sub>   | On mode                                                                                           |      |                           | 0.4  | V     |
| MPC_, PFN_ Input Pullup Resistance                                                            | R <sub>IO_PU</sub>      | Pullup resistance to VCCINT (Note 2)                                                              |      | 170                       |      | kΩ    |
| MPC_, PFN_ Input Pulldown Resistance                                                          | R <sub>IO_PD</sub>      |                                                                                                   |      | 170                       |      | kΩ    |
| MPC_ Output Logic-High                                                                        | V <sub>IO_OH</sub>      | I <sub>OH</sub> = 1mA, MPC_ configured as push-pull output, pullup voltage is V <sub>BK3OUT</sub> |      | V <sub>BK3OUT</sub> - 0.4 |      | V     |
| SDA, $\overline{\text{RST}}$ , $\overline{\text{INT}}$ , MPC_, PFN_ Output Logic Low          | V <sub>IO_OL</sub>      | I <sub>OL</sub> = 4mA                                                                             |      |                           | 0.4  | V     |
| SCL Clock Frequency                                                                           | f <sub>SCL</sub>        |                                                                                                   | 0    |                           | 1000 | kHz   |
| Bus Free Time Between STOP and START Condition                                                | t <sub>BUF</sub>        |                                                                                                   | 0.5  |                           |      | μs    |
| START Condition (Repeated) Hold Time                                                          | t <sub>HD_STA</sub>     |                                                                                                   | 0.26 |                           |      | μs    |
| Low Period of SCL Clock                                                                       | t <sub>LOW</sub>        |                                                                                                   | 0.5  |                           |      | μs    |
| High Period of SCL Clock                                                                      | t <sub>HIGH</sub>       |                                                                                                   | 0.26 |                           |      | μs    |
| Setup Time for a Repeated START Condition                                                     | t <sub>SU_STA</sub>     |                                                                                                   | 0.26 |                           |      | μs    |
| Data Hold Time                                                                                | t <sub>HD_DAT</sub>     |                                                                                                   | 0.0  |                           | 0.9  | μs    |
| Data Setup Time                                                                               | t <sub>SU_DAT</sub>     |                                                                                                   | 50   |                           |      | ns    |

**Electrical Characteristics (continued)**

(V<sub>BAT</sub> = V<sub>SYS\_UVLO</sub> (falling) to +5.5V, V<sub>CHGIN</sub> = unconnected or V<sub>CHGIN\_DET</sub> to +28V. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, V<sub>BAT</sub> = 3.7V, V<sub>CHGIN</sub> = 5V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 8.8μF, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH. Limits are 100% tested at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                     | SYMBOL                | CONDITIONS | MIN  | TYP | MAX | UNITS |
|-----------------------------------------------|-----------------------|------------|------|-----|-----|-------|
| Setup Time for STOP Condition                 | t <sub>SU_STO</sub>   |            | 0.26 |     |     | μs    |
| Spike Pulse Widths Suppressed by Input Filter | t <sub>SP</sub>       |            | 50   |     |     | ns    |
| <b>SPI</b>                                    |                       |            |      |     |     |       |
| SCLK Frequency                                | f <sub>SCLK</sub>     | (Note 3)   |      |     | 10  | MHz   |
| $\overline{\text{CS}}$ Setup Time             | t <sub>CS</sub>       |            | 10   |     |     | ns    |
| $\overline{\text{CS}}$ Hold Time              | t <sub>CH</sub>       |            | 100  |     |     | ns    |
| $\overline{\text{CS}}$ Pulse-Width High       | t <sub>IDLE</sub>     |            |      | 60  |     | ns    |
| DIN Setup Time                                | t <sub>DS</sub>       |            | 10   |     |     | ns    |
| DIN Hold Time                                 | t <sub>DH</sub>       |            | 20   |     |     | ns    |
| SCLK Pulse-Width Low                          | t <sub>LOW_SPI</sub>  |            | 20   |     |     | ns    |
| SCLK Pulse-Width High                         | t <sub>HIGH_SPI</sub> |            | 20   |     |     | ns    |

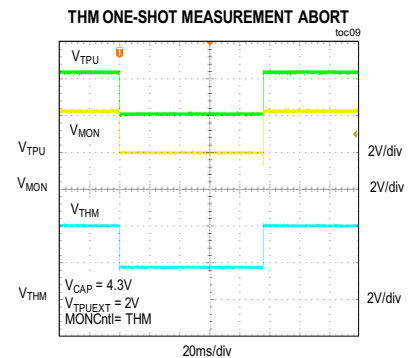
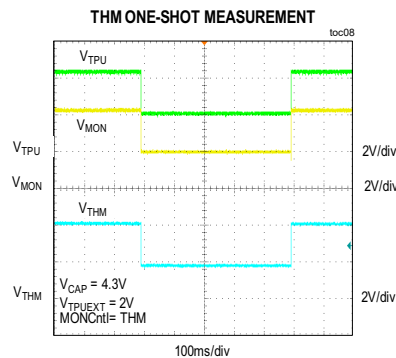
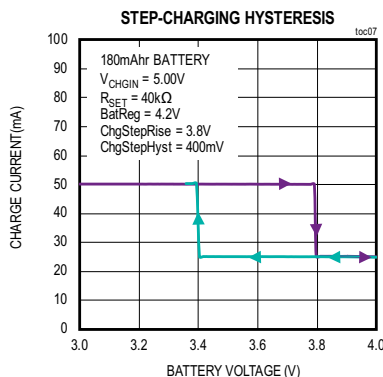
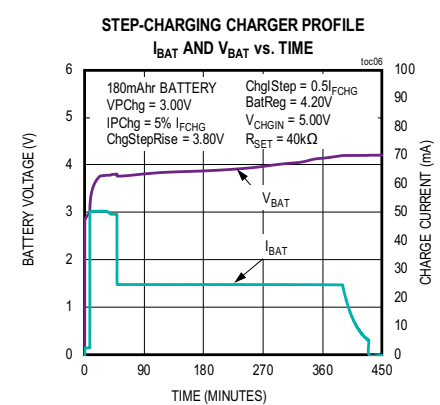
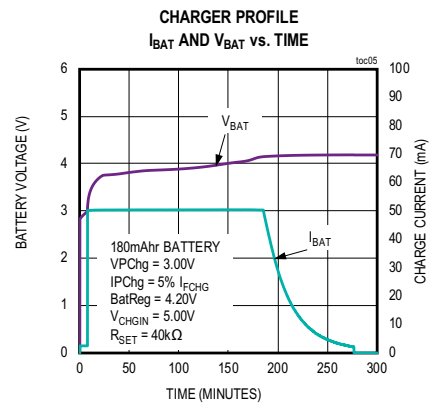
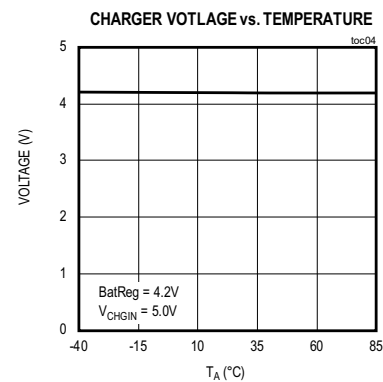
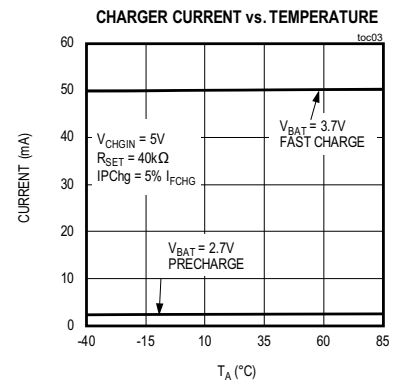
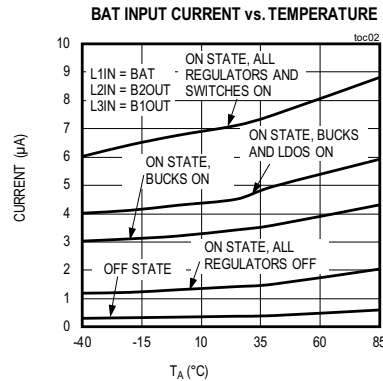
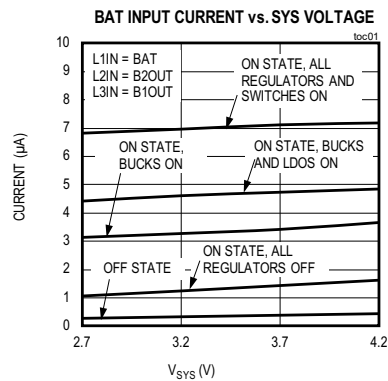
**Note 1:** All devices are 100% production tested at T<sub>A</sub> = +25°C. Limits over the operating temperature range are guaranteed by design.

**Note 2:** V<sub>VCCINT</sub> is an internal voltage supply generated from either V<sub>BAT</sub> or V<sub>CAP</sub>. The source is determined by the following: if [( V<sub>CHGIN</sub> > V<sub>CHGIN\_DET</sub> AND V<sub>CAP</sub> > V<sub>CAP\_DET</sub> ) or V<sub>CAP</sub> > ( V<sub>BAT</sub> + V<sub>THSWOVER</sub> )], then V<sub>VCCINT</sub> = V<sub>CAP</sub>, ELSE V<sub>VCCINT</sub> = V<sub>BAT</sub> where V<sub>THSWOVER</sub> = [0-300]mV

**Note 3:** Quiescent current is guaranteed by design only and not production tested.

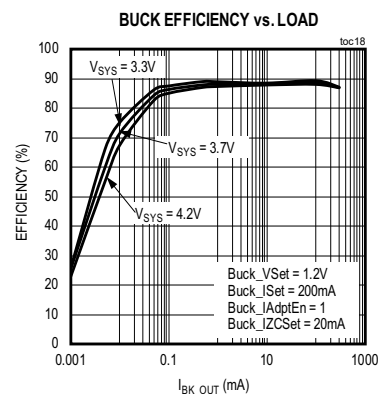
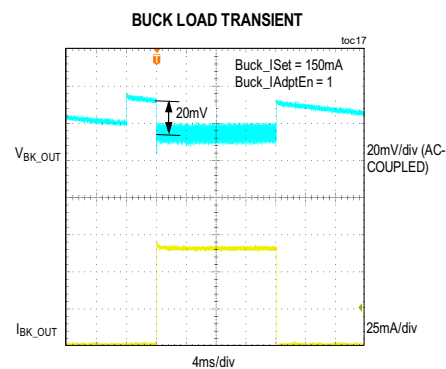
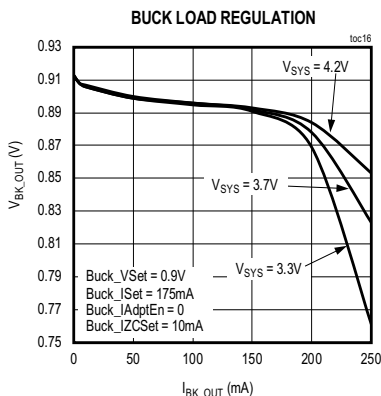
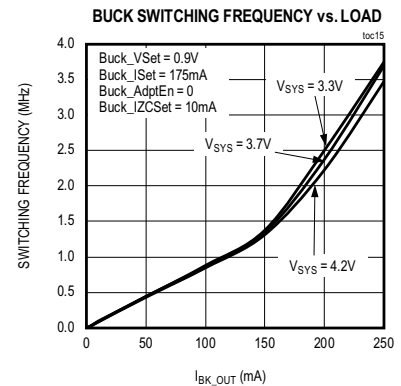
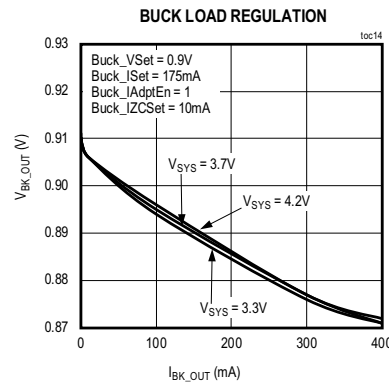
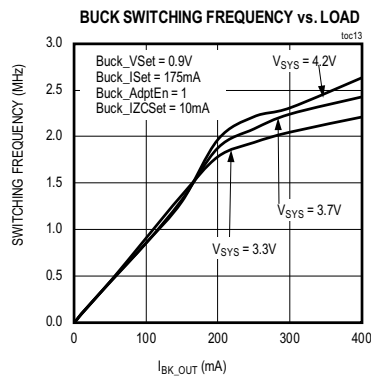
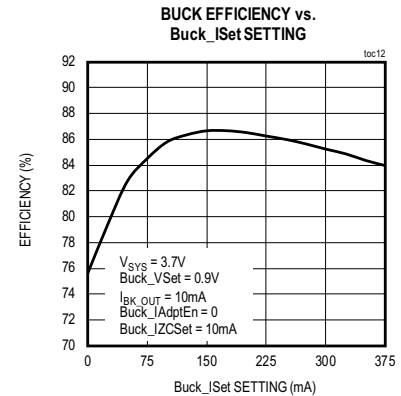
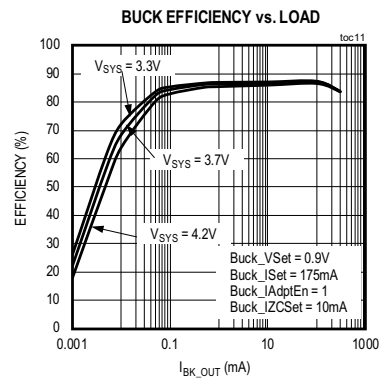
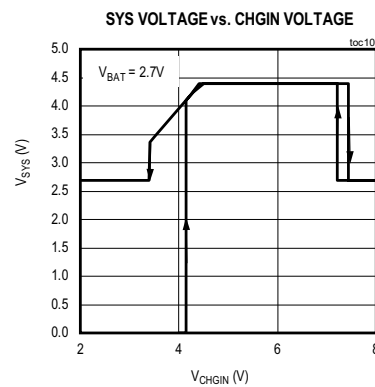
## Typical Operating Characteristics

(V<sub>BAT</sub> = +3.7V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 4.4μF, V<sub>BBOUT</sub> = 5V, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH, T<sub>A</sub> = +25°C, unless otherwise noted.)



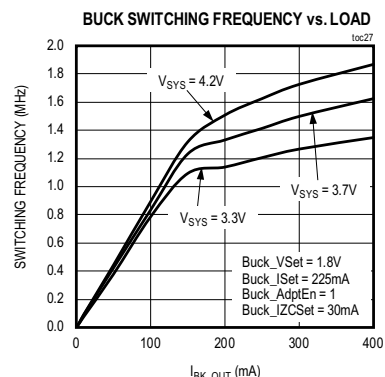
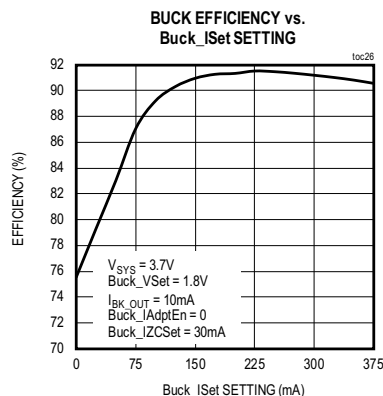
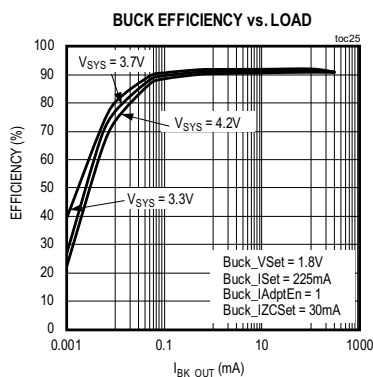
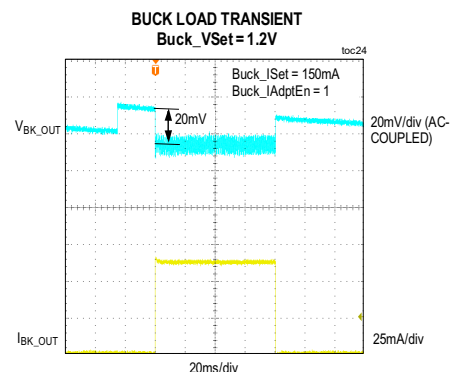
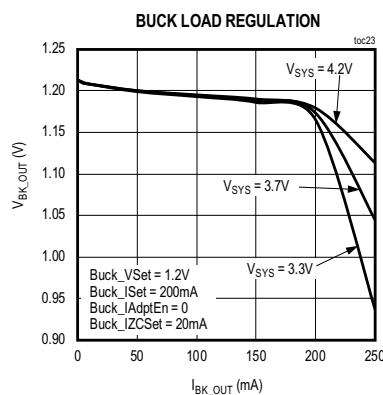
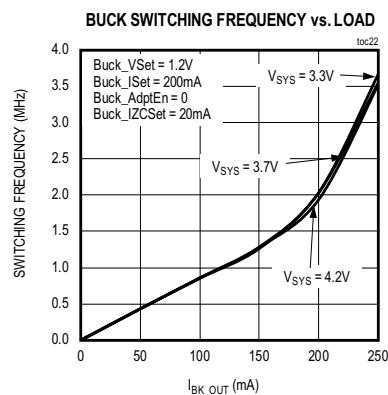
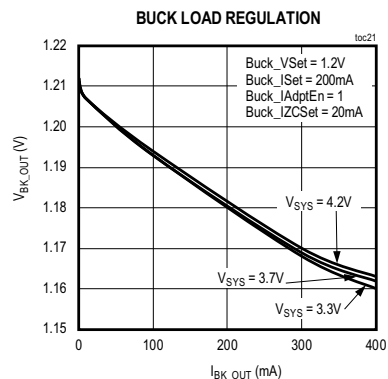
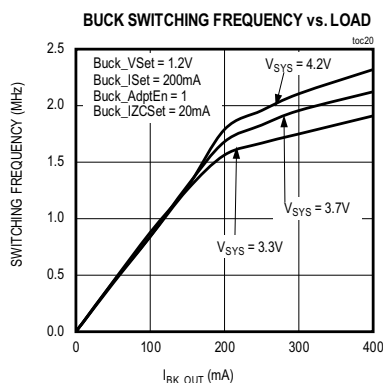
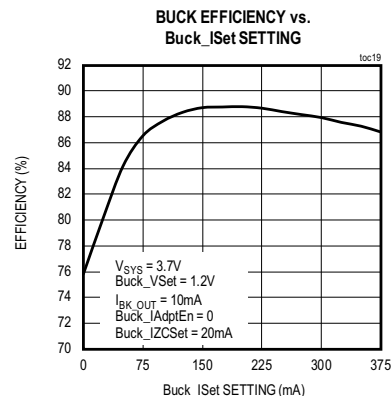
## Typical Operating Characteristics (continued)

(V<sub>BAT</sub> = +3.7V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYN\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BOUT\_EFF</sub> = 4.4μF, V<sub>BOUT</sub> = 5V, L<sub>BK\_</sub> = 2.2μH, L<sub>BOUT</sub> = 2.2μH, T<sub>A</sub> = +25°C, unless otherwise noted.)



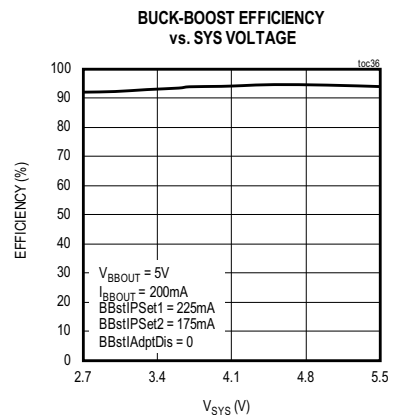
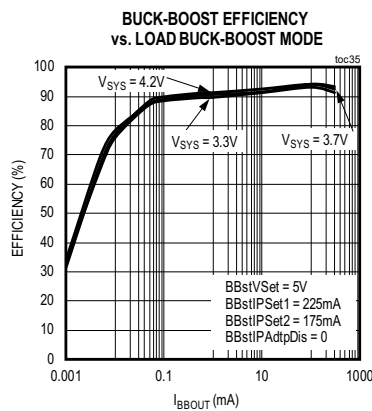
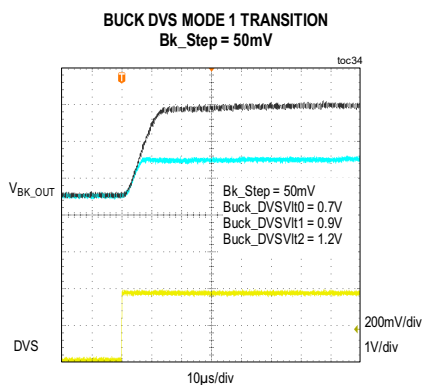
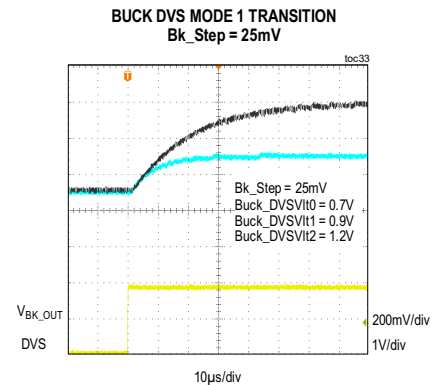
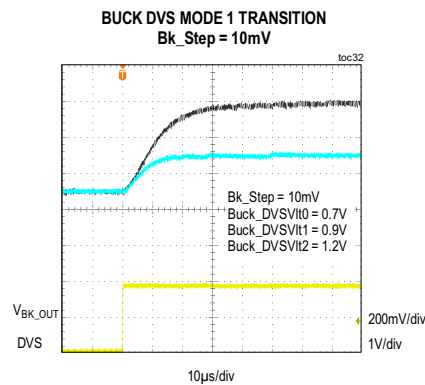
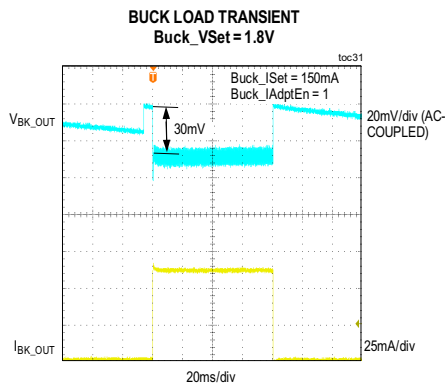
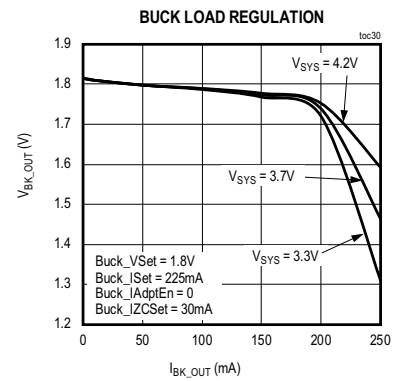
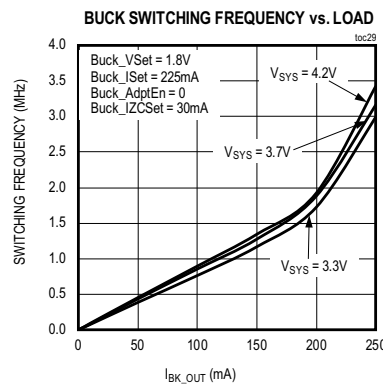
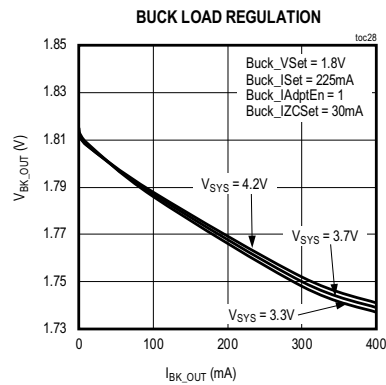
## Typical Operating Characteristics (continued)

(V<sub>BAT</sub> = +3.7V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYN\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 4.4μF, V<sub>BBOUT</sub> = 5V, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH, T<sub>A</sub> = +25°C, unless otherwise noted.)



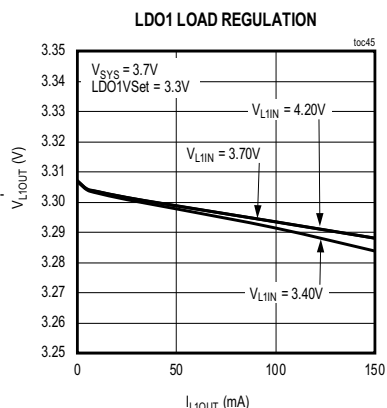
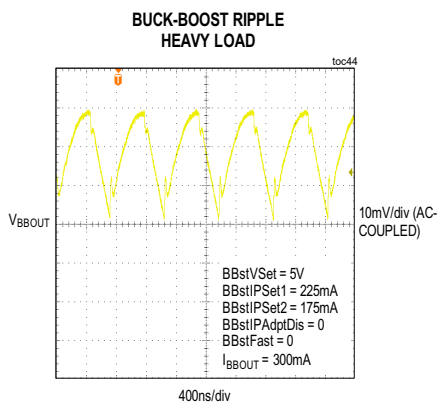
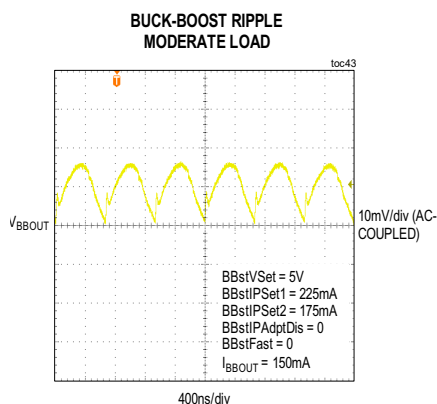
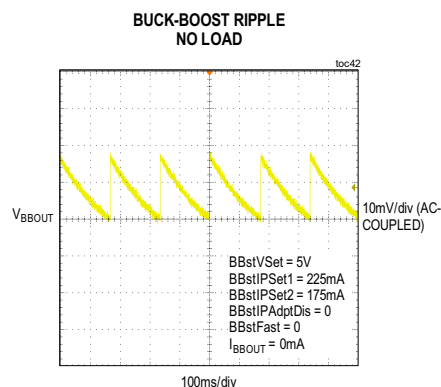
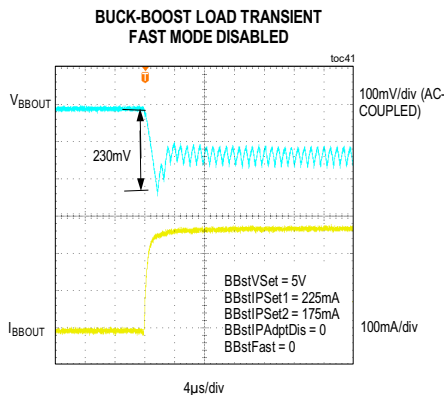
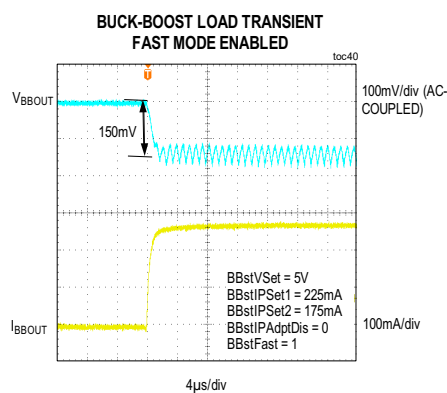
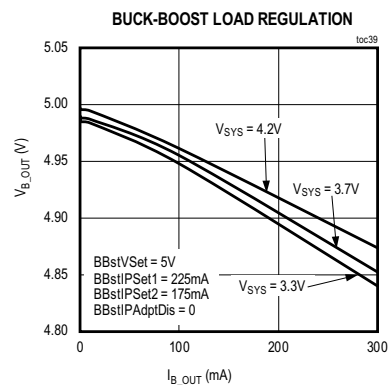
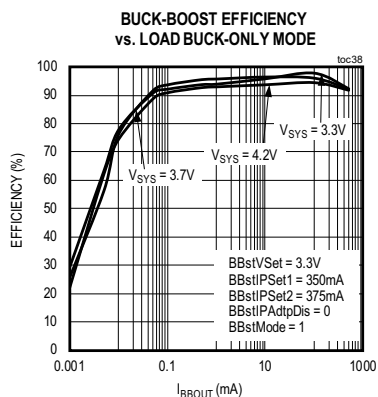
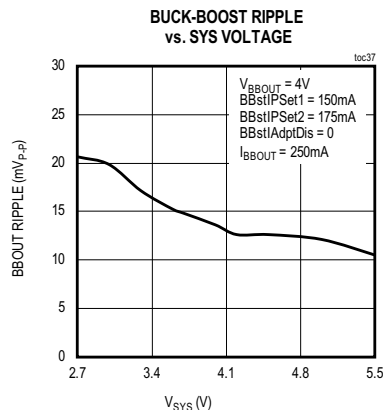
## Typical Operating Characteristics (continued)

(V<sub>BAT</sub> = +3.7V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYSEFF</sub> = 10μF, C<sub>BATEFF</sub> = 1μF, C<sub>BKOUTEFF</sub> = 10μF, C<sub>LIN</sub> = 1μF, C<sub>LOUTEFF</sub> = 1μF, C<sub>BBOUTEFF</sub> = 4.4μF, V<sub>BBOUT</sub> = 5V, L<sub>BK</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH, T<sub>A</sub> = +25°C, unless otherwise noted.)



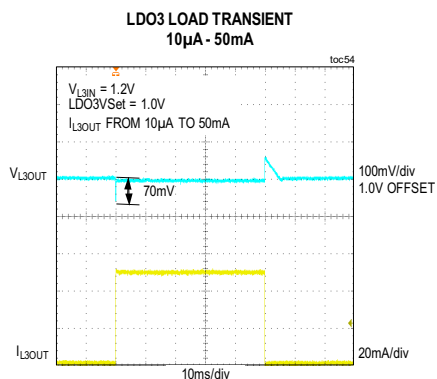
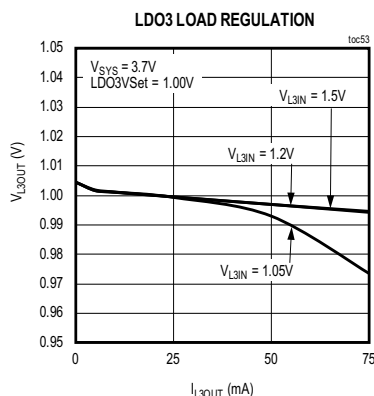
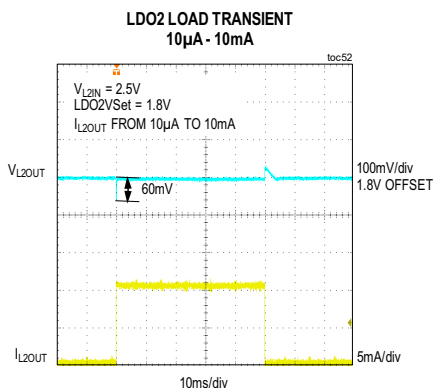
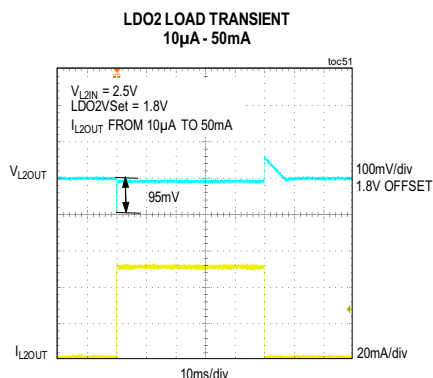
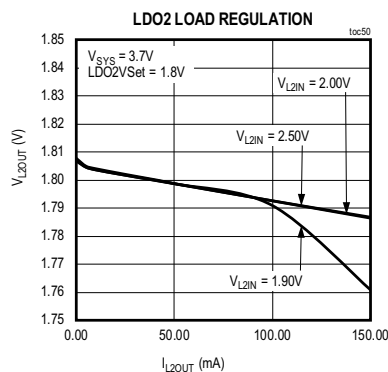
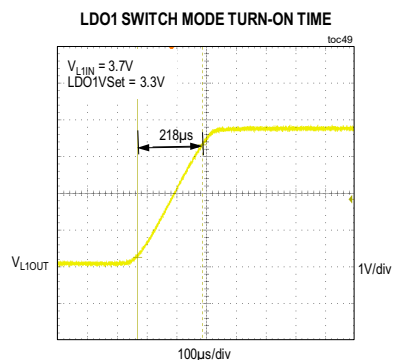
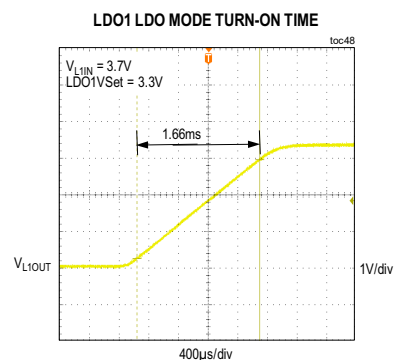
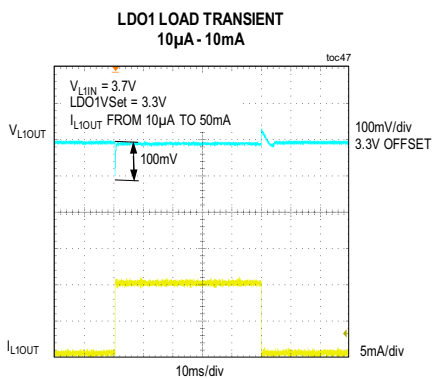
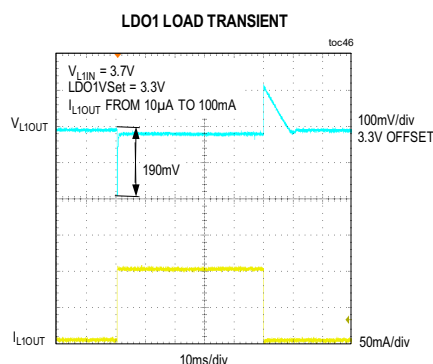
## Typical Operating Characteristics (continued)

(V<sub>BAT</sub> = +3.7V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYS\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 4.4μF, V<sub>BBOUT</sub> = 5V, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH, T<sub>A</sub> = +25°C, unless otherwise noted.)



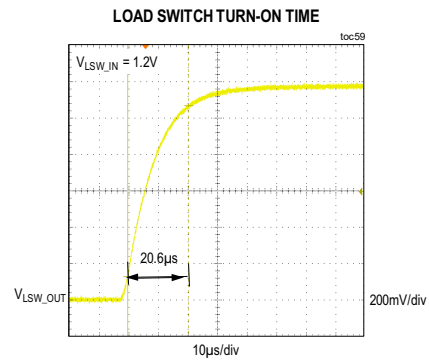
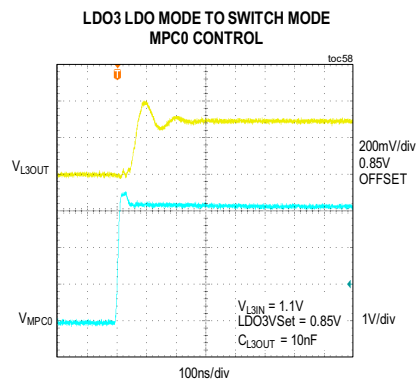
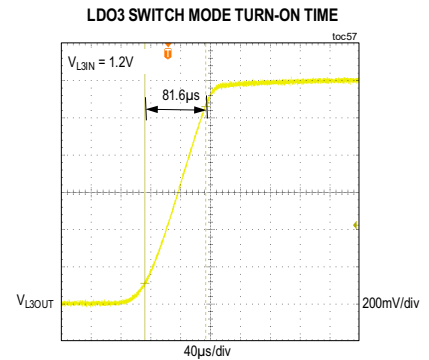
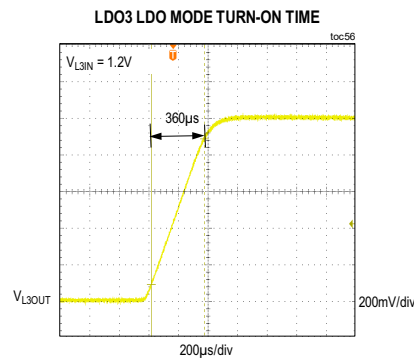
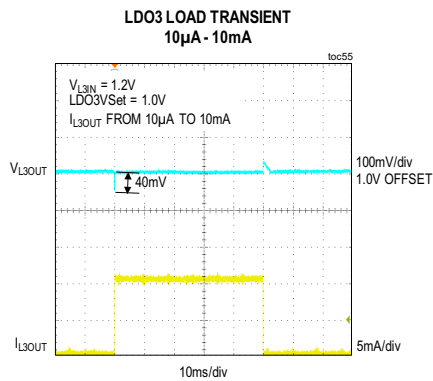
## Typical Operating Characteristics (continued)

(V<sub>BAT</sub> = +3.7V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYSEFF</sub> = 10μF, C<sub>BATEFF</sub> = 1μF, C<sub>BKOUTEFF</sub> = 10μF, C<sub>LIN</sub> = 1μF, C<sub>LOUTEFF</sub> = 1μF, C<sub>BBOUTEFF</sub> = 4.4μF, V<sub>BBOUT</sub> = 5V, L<sub>BK</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH, T<sub>A</sub> = +25°C, unless otherwise noted.)



## Typical Operating Characteristics (continued)

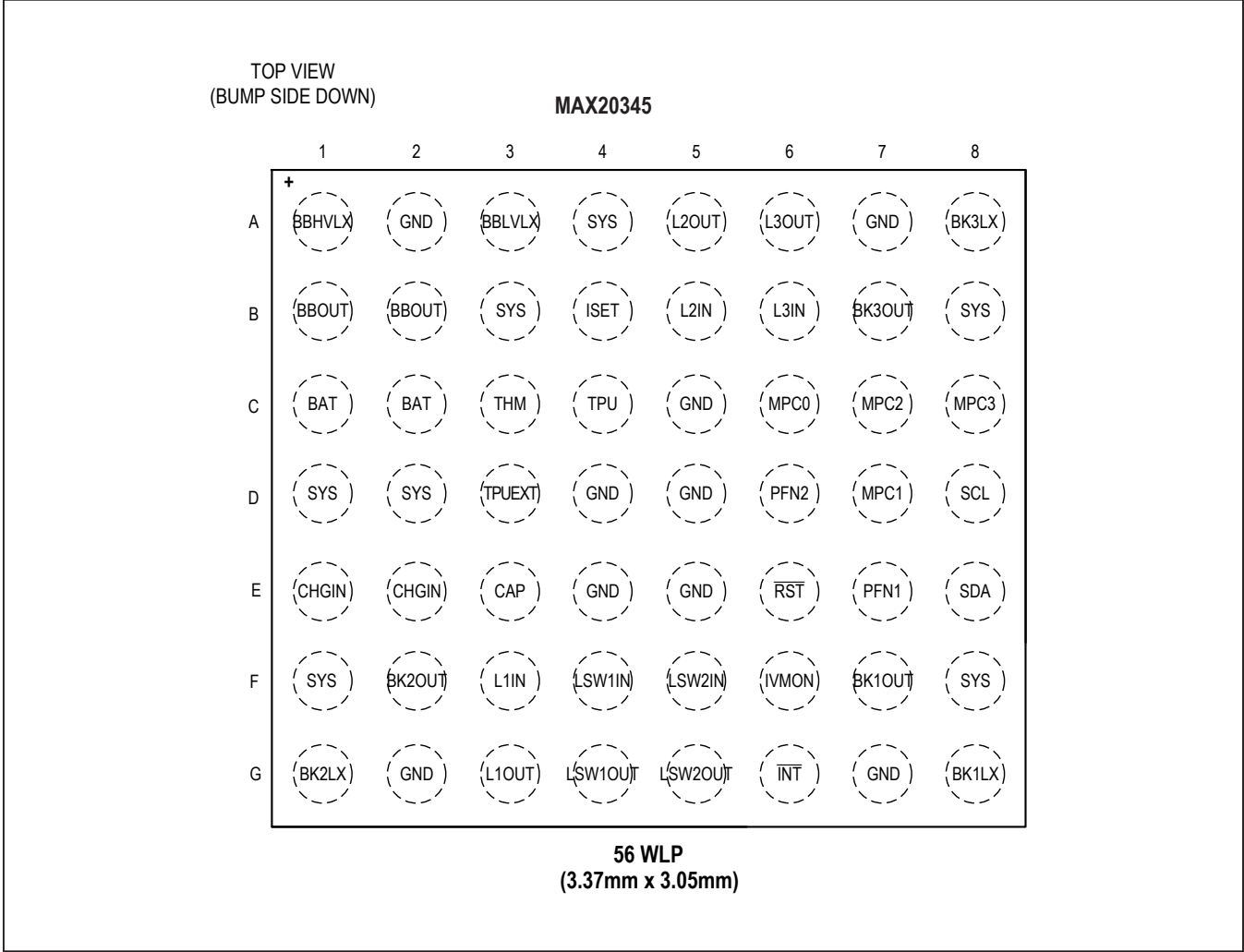
(V<sub>BAT</sub> = +3.7V, C<sub>CHGIN</sub> = 1μF, C<sub>CAP</sub> = 1μF, C<sub>SYN\_EFF</sub> = 10μF, C<sub>BAT\_EFF</sub> = 1μF, C<sub>BK\_OUT\_EFF</sub> = 10μF, C<sub>L\_IN</sub> = 1μF, C<sub>L\_OUT\_EFF</sub> = 1μF, C<sub>BBOUT\_EFF</sub> = 4.4μF, V<sub>BBOUT</sub> = 5V, L<sub>BK\_</sub> = 2.2μH, L<sub>BBOUT</sub> = 2.2μH, T<sub>A</sub> = +25°C, unless otherwise noted.)



MAX20345

PMIC with Ultra-Low I<sub>Q</sub> Voltage Regulators,  
Buck-Boost for Optical Sensing and  
Charger for Small Lithium Ion Systems

Pin Configuration



## Pin Description

| PIN                                         | NAME             | FUNCTION                                                                                                                                                                                                                      |
|---------------------------------------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A1                                          | BBHVLX           | Buck-Boost Regulator Switch HV Side. Connect through 2.2μH inductor to BBLVLX.                                                                                                                                                |
| A2, A7,<br>C5, D4,<br>D5, E4,<br>E5, G2, G7 | GND              | Ground. All GND bumps must be connected on PCB using a low-impedance trace or GND plane.                                                                                                                                      |
| A3                                          | BBLVLX           | Buck-Boost Regulator Switch LV Side. Connect through 2.2μH inductor to BBHVLX.                                                                                                                                                |
| A4, B3,<br>B8, D1,<br>D2, F1, F8            | SYS              | System Load Connection. All SYS bumps must be connected on PCB using a low-impedance trace or SYS plane. Bypass common node with a minimum 10μF of capacitance to GND.                                                        |
| A5                                          | L2OUT            | LDO2 Output. Bypass with 1μF of capacitance to GND.                                                                                                                                                                           |
| A6                                          | L3OUT            | LDO3 Output. Bypass with 1μF of capacitance to GND.                                                                                                                                                                           |
| A8                                          | BK3LX            | Buck3 Regulator Switch. Connect through 2.2μH to BK3OUT.                                                                                                                                                                      |
| B1, B2                                      | BBOUT            | Buck-Boost Regulator Output. Bypass to GND with effective capacitance equal to the value of the derating curve ( <a href="#">Figure 5</a> ) for a bias voltage V <sub>OUT</sub> , placed as close to the device as possible.. |
| B4                                          | ISET             | External Resistor for Battery Charge Current Level Setting. Do not connect any capacitance on this pin. Maximum allowed capacitance: C <sub>ISET</sub> < (5μs/R <sub>ISET</sub> ) pF.                                         |
| B5                                          | L2IN             | LDO2 Input. Bypass with 1μF capacitor to GND                                                                                                                                                                                  |
| B6                                          | L3IN             | LDO3 Input. Bypass with 1μF capacitor to GND                                                                                                                                                                                  |
| B7                                          | BK3OUT           | Buck3 Regulator Output. Bypass with 10μF of capacitance to GND.                                                                                                                                                               |
| C1, C2                                      | BAT              | Battery Connection. Connect to positive battery terminal. Bypass with a minimum 1μF capacitance to GND.                                                                                                                       |
| C3                                          | THM              | Battery Temperature Measurement Thermistor Sensing Connection.                                                                                                                                                                |
| C4                                          | TPU              | Battery Temperature Measurement Pullup Resistor Connection.                                                                                                                                                                   |
| C6                                          | MPC0             | Multipurpose Control I/O 0. LDO3 direct control option.                                                                                                                                                                       |
| C7                                          | MPC2             | Multipurpose Control I/O 2                                                                                                                                                                                                    |
| C8                                          | MPC3             | Multipurpose Control I/O 3                                                                                                                                                                                                    |
| D3                                          | TPUEXT           | External Voltage Connection to be used as Supply of the Battery Temperature Measurement Resistive Divider.                                                                                                                    |
| D6                                          | PFN2             | Configurable Power Mode Control Pin (e.g. $\overline{KOUT}$ )                                                                                                                                                                 |
| D7                                          | MPC1             | Multipurpose Control I/O 1. Buck-Boost FAST control option.                                                                                                                                                                   |
| D8                                          | SCL              | I <sup>2</sup> C Serial Clock Input                                                                                                                                                                                           |
| E1, E2                                      | CHGIN            | +28V/-5.5V Protected Charger Input. Bypass with 1μF capacitor to GND.                                                                                                                                                         |
| E3                                          | CAP              | Internal Reference Supply. Bypass with 1μF capacitor to GND.                                                                                                                                                                  |
| E6                                          | $\overline{RST}$ | Reset Open-Drain Output. Active-low.                                                                                                                                                                                          |
| E7                                          | PFN1             | Configurable Power Mode Control Pin (e.g., $\overline{KIN}$ ).                                                                                                                                                                |
| E8                                          | SDA              | I <sup>2</sup> C Serial Data Input / Open-Drain Output                                                                                                                                                                        |
| F2                                          | BK2OUT           | Buck2 Regulator Output. Bypass with 10μF of capacitance to GND.                                                                                                                                                               |
| F3                                          | L1IN             | LDO1 Input. Bypass with 1μF capacitor to GND.                                                                                                                                                                                 |
| F4                                          | LSW1IN           | Load Switch 1 Input                                                                                                                                                                                                           |
| F5                                          | LSW2IN           | Load Switch 2 Input                                                                                                                                                                                                           |
| F6                                          | IVMON            | Voltages and Charging Current Monitor Multiplexer Output                                                                                                                                                                      |

**Pin Description (continued)**

| PIN | NAME    | FUNCTION                                                          |
|-----|---------|-------------------------------------------------------------------|
| F7  | BK1OUT  | Buck1 Regulator Output. Bypass with 10μF of capacitance to GND.   |
| G1  | BK2LX   | Buck2 Regulator Switch. Connect through 2.2μH inductor to BK2OUT. |
| G3  | L1OUT   | LDO1 Output. Bypass with 1μF of capacitance to GND.               |
| G4  | LSW1OUT | Load Switch 1 Output                                              |
| G5  | LSW2OUT | Load Switch 2 Output                                              |
| G6  | INT     | Interrupt Open-Drain Output. Active-low.                          |
| G8  | BK1LX   | Buck1 Regulator Switch. Connect through 2.2μH inductor to BK1OUT. |

**Detailed Description****Power Regulation**

The MAX20345 features three high-efficiency, low-quiescent-current buck regulators, a Buck-Boost regulator, two load switches, and three low-quiescent-current, low-drop-out (LDO) linear regulators that are configurable as load switches. Excellent light-load efficiency allows the switching regulators to run continuously without significant energy cost. The buck and Buck-Boost regulators can operate in a fixed peak current mode for low-current applications, as well as an adaptive peak current mode to improve load regulation, and extend the high-efficiency range.

**LDO3 MPC0 Control**

All of MAX20345s LDOs can be enabled using an MPC input and are configurable as load switches. The low voltage LDO3 offers an additional, on-the-fly configuration option. Setting the LDO3\_MPC0CNT bit to 1 configures LDO3 to be adjusted by MPC0 based on the state of LDO3\_MPC0CNF. If LDO3\_MPC0CNF = 0, MPC0 toggles LDO3 between LDO mode and switch mode. If LDO3\_MPC0CNF = 1, then MPC0 enables or disables LDO3 in switch mode. Using this MPC control allows the state of LDO3 to be changed much more quickly than through I<sup>2</sup>C writes, on the order of microseconds. Rapid control of LDO3 supports applications that require minimal delays. For example, quickly increasing the LDO3 voltage reduces the time required for an application processor to transition from a low-power sleep mode to a higher voltage active state.

**Load Switches**

The MAX20345s load switches allow a system to disconnect loads when inactive to reduce quiescent current. Each load switch initially behaves as a constant current source with the value I<sub>LSW\_START</sub>. A switch charges its output until it meets the condition  $V_{LSW\_IN} - V_{LSW\_OUT} < V_{LSW\_PROT}$ . Once the condition is met, the switch turns fully on and connects LSW\_IN to LSW\_OUT. If this condition is not met within the startup time-out t<sub>STUP\_LSW</sub>, the switch attempts to turn on after a retry delay t<sub>RTRY\_LSW</sub>.

Both switches feature optional voltage protection at their inputs. A protection comparator monitors the difference between the input and output voltages. If the difference exceeds V<sub>SW\_PROT</sub>, the switch is opened to protect downstream circuitry. The comparator can be disabled with the LSW\_LowIq bit to reduce quiescent current.

**Power Switch and Reset Control**

The MAX20345 features a power switch that provides the ability to execute a reset sequence or to turn off the main system power and enter Off mode to extend battery life. Shutdown and reset events are triggered by an external control through the power function (PFN) control inputs, I<sup>2</sup>C commands, or if other conditions are met. The behavior of the PFN pins is preconfigured to support one of the multiple types of wearable application cases. [Table 1](#) describes the behavior of the PFN1 and PFN2 pins based on the PwrRstCfg[3:0] bits, while [Figure 1a](#) through [Figure 1g](#) shows basic flow diagrams associated with each mode.

A soft-reset sends a 10ms pulse on  $\overline{\text{RST}}$  and either leaves register settings unchanged or resets them to their default values depending on the device version (see [Table 3](#) for device settings). A hard reset on any device initiates a complete power-on reset (POR) sequence.

The device enters Off mode on cold boot (initial battery attach,  $V_{\text{CHGIN}} = 0\text{V}$ ), in response to a power-off I<sup>2</sup>C command or to a valid PFN signal based on the PwrRstCfg[3:0] setting, in the case of an undervoltage (UVLO) condition on SYS and in the case of an over-current (OCP) condition on BAT. When the device is in Off

mode, the BAT-SYS connection is opened and all functions are disabled except for the power function controller and LDO1 (if configured as always-on).

The MAX20345 exits Off mode and turns the main power back on when there is a qualified PFN1 signal (PwrRstCfg[3:0] = 0000, 0001, 0110, 0111, 1000, 1001, 1010) or when a valid voltage is applied to CHGIN. In the powered-on state, the SYS node is enabled and other functions can be controlled through the I<sup>2</sup>C registers. When the power-on event occurs, the power path to SYS is enabled after a 30ms delay. [Figure 2](#) illustrates a complete boot sequence coming out of the Off state.

**Table 1. PwrRstCfg Settings**

| PwrRstCfg[3:0] | MODE                        | PFN1 FUNCTION                           | PFN2 FUNCTION                           | BEHAVIOR                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------------|-----------------------------|-----------------------------------------|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0000           | On/ $\overline{\text{Off}}$ | Enable                                  | Manual $\overline{\text{RESET}}$        | On/Off Mode with 10ms Debounce. PFN1 is the active-high on/off control input. PFN2 is the active-low soft-reset input.                                                                                                                                                                                                                                                                                                        |
| 0001           | $\overline{\text{On}}$ /Off | Disable                                 | Manual $\overline{\text{RESET}}$        | On/Off Mode with 10ms Debounce. PFN1 is the active-low on/off control input. PFN2 is the active-low soft-reset input.                                                                                                                                                                                                                                                                                                         |
| 0010           | Always-On                   | Hard-Reset on Rising Edge               | Soft-Reset on Rising Edge               | Always-On Mode. A rising edge on PFN1 generates a hard-reset after a 200ms delay. A rising edge on PFN2 generates a soft-reset after a 200ms delay. The device can only enter the off state by writing to the PwrCmd register.                                                                                                                                                                                                |
| 0011           | Always-On                   | Hard-Reset on Falling Edge              | Soft-Reset on Falling Edge              | Always-On Mode. A falling edge on PFN1 generates a hard-reset after a 200ms delay. A falling edge on PFN2 generates a soft-reset after a 200ms delay. The device can only enter the off state by writing to the PwrCmd register.                                                                                                                                                                                              |
| 0100           | Always-On                   | Hard-Reset when High on CHGIN Insertion | Soft-Reset when High on CHGIN Insertion | Always-On Mode. Holding PFN1 high during a CHGIN insertion generates a hard-reset after a 200ms delay. Holding PFN2 high during a CHGIN insertion triggers a soft-reset after a 200ms delay. The device can only enter the off state by writing to the PwrCmd register.                                                                                                                                                       |
| 0101           | Always-On                   | Hard-Reset when Low on CHGIN Insertion  | Soft-Reset when Low on CHGIN Insertion  | Always-On Mode. Holding PFN1 low during a CHGIN insertion generates a hard-reset after a 200ms delay. Holding PFN2 low during a CHGIN insertion triggers a soft-reset after a 200ms delay. The device can only enter the off state by writing to the PwrCmd register.                                                                                                                                                         |
| 0110           | $\overline{\text{KIN}}$     | $\overline{\text{KIN}}$                 | KOUT                                    | On/Off Through Key Presses. PFN1 is the active-low $\overline{\text{KIN}}$ button. PFN2 is the open-drain KOUT output, which buffers the $\overline{\text{KIN}}$ input. The device enters on mode through a short (400ms) $\overline{\text{KIN}}$ press or a CHGIN insertion. The device enters off mode through a long (> 12s) $\overline{\text{KIN}}$ press or through the PwrCmd register.                                 |
| 0111           | $\overline{\text{KIN}}$     | $\overline{\text{KIN}}$                 | KOUT                                    | On/Reset Through Key Presses. PFN1 is the active-low $\overline{\text{KIN}}$ button. PFN2 is the open-drain KOUT output, which buffers the $\overline{\text{KIN}}$ input. The device enters on mode through a long (> 3s) $\overline{\text{KIN}}$ press or a CHGIN insertion. A long (> 12s) $\overline{\text{KIN}}$ press generates a soft-reset. The device can only enter the off state by writing to the PwrCmd register. |

Table 1. PwrRstCfg Settings (continued)

| PwrRstCfg[3:0] | MODE                    | PFN1<br>FUNCTION                                                     | PFN2<br>FUNCTION                                                     | BEHAVIOR                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------------|-------------------------|----------------------------------------------------------------------|----------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1000           | $\overline{\text{KIN}}$ | $\overline{\text{KIN}}$                                              | Manual $\overline{\text{RESET}}$                                     | On/Reset Through Key Presses. PFN1 is the active-low $\overline{\text{KIN}}$ button. The device enters on mode through a long (3s) $\overline{\text{KIN}}$ press or a CHGIN insertion. A long (> 12s) PFN2 press generates a soft-reset. The device can only enter the off state by writing to the PwrCmd register.                                                                                                                               |
| 1001           | Always-On               | Hard-Reset when High on CHGIN Insertion or Abort Hard-Reset when Low | Soft-Reset when High on CHGIN Insertion or Abort Soft-Reset when Low | Always-On Mode. The device can only enter the on state through a CHGIN insertion. Holding PFN1 high during a CHGIN insertion generates a hard-reset after a 15 second delay. If PFN1 is brought low during this delay (10ms debounce), the hard-reset is aborted. Holding PFN2 high during a CHGIN insertion generates a soft-reset after a 15 second delay. If PFN2 is brought low during this delay (10ms debounce), the hard-reset is aborted. |
| 1010           | Always-On               | Hard-Reset when Low on CHGIN Insertion or Abort Hard-Reset when High | Soft-Reset when Low on CHGIN Insertion or Abort Soft-Reset when High | Always-On Mode. The device can only enter the on state through a CHGIN insertion. Holding PFN1 low during a CHGIN insertion generates a hard-reset after a 15 second delay. If PFN1 is brought high during this delay (10ms debounce), the hard-reset is aborted. Holding PFN2 low during a CHGIN insertion generates a soft-reset after a 15 second delay. If PFN2 is brought high during this delay (10ms debounce), the hard-reset is aborted. |
| 1011-1111      | RFU                     |                                                                      |                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

## PwrRstCfg Diagrams

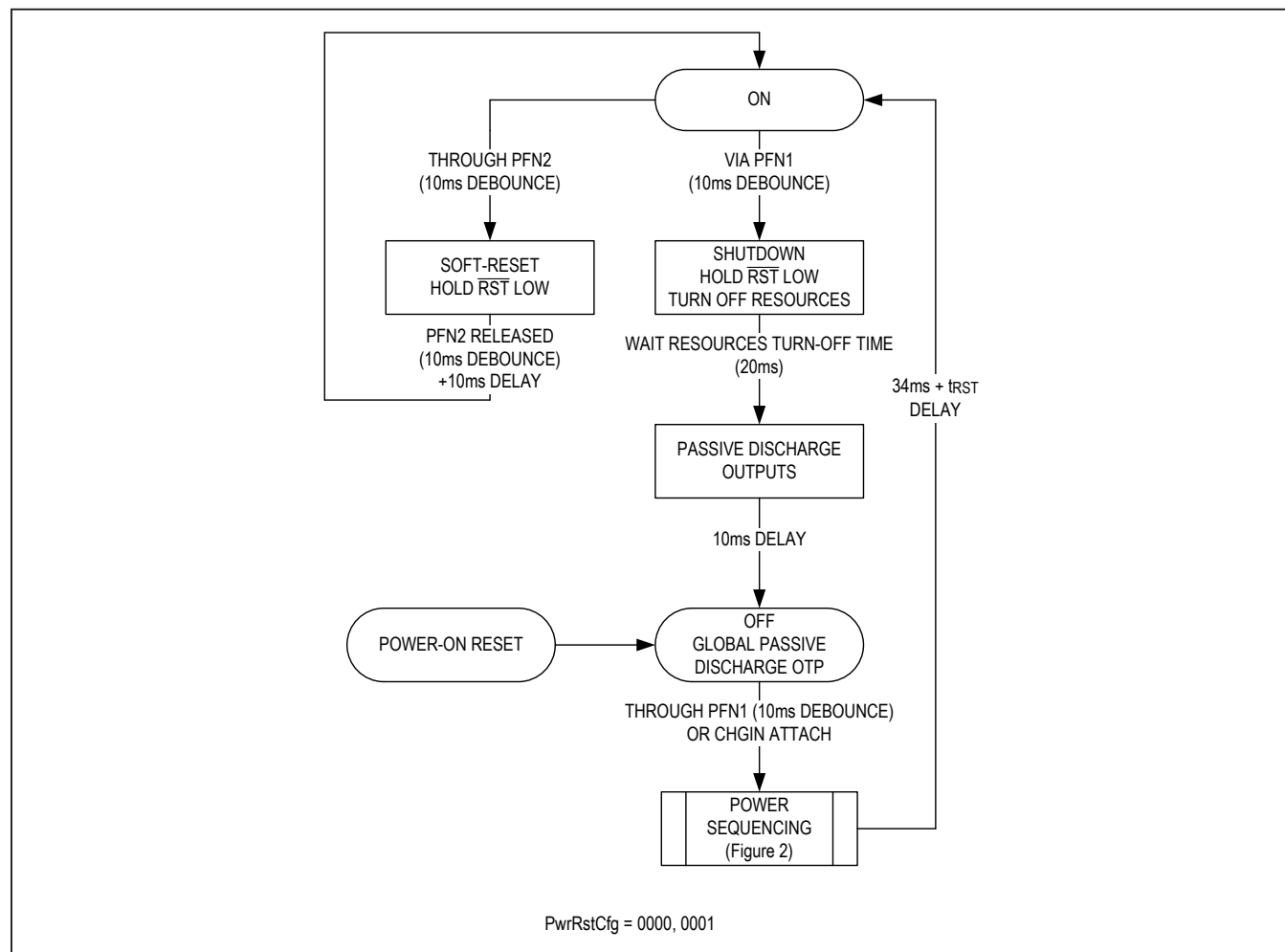


Figure 1a. PwrRstCfg = 0000,0001

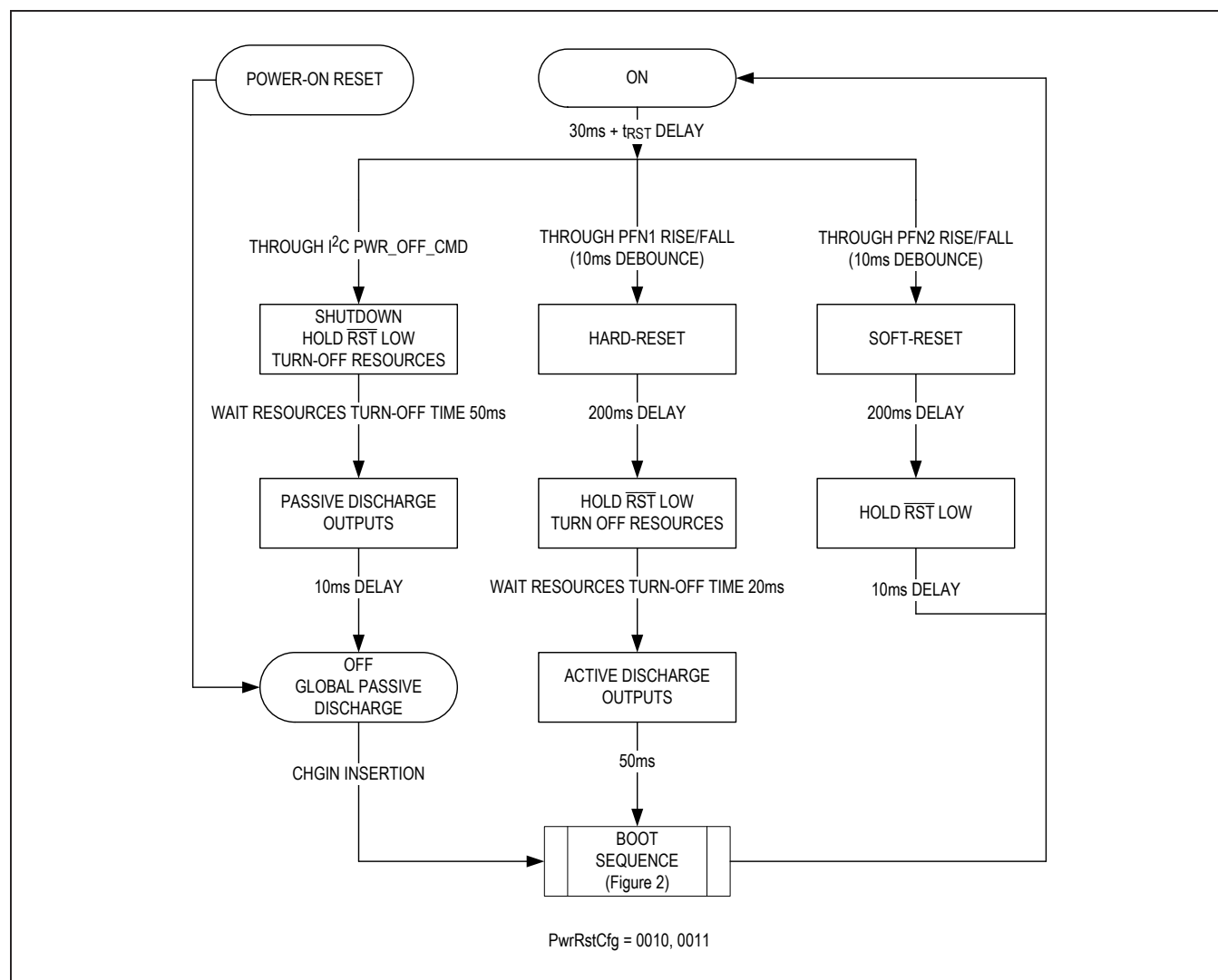
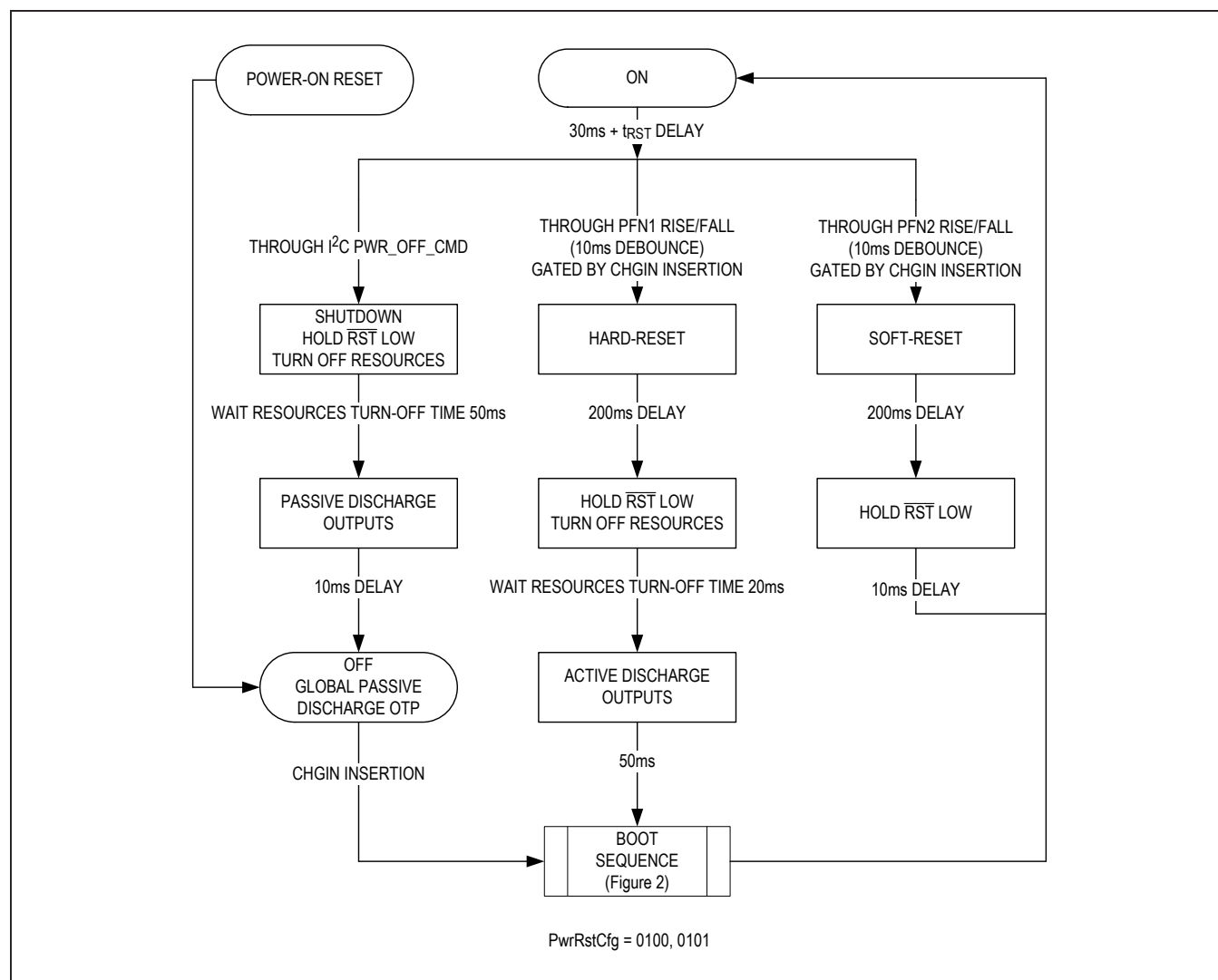
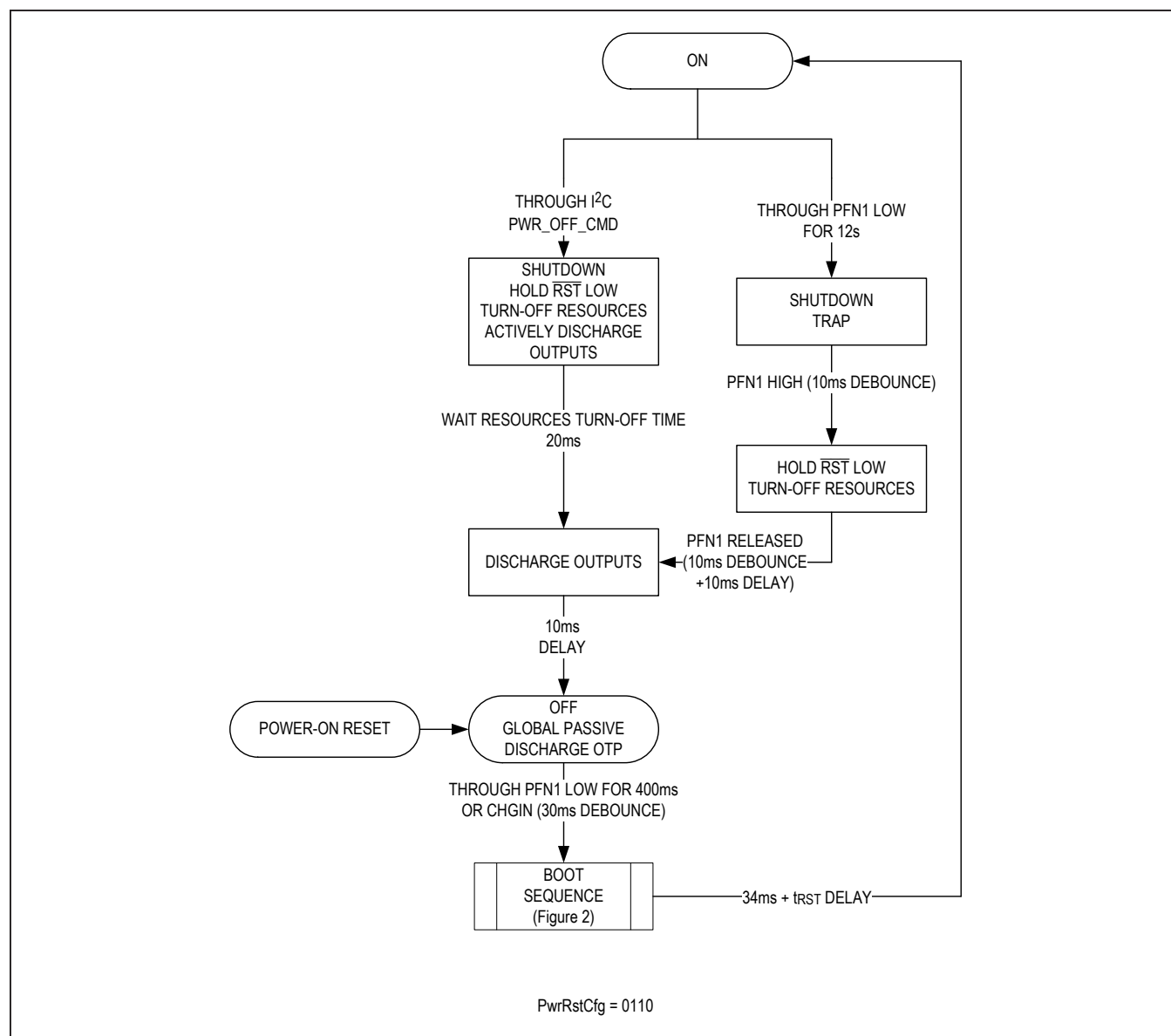
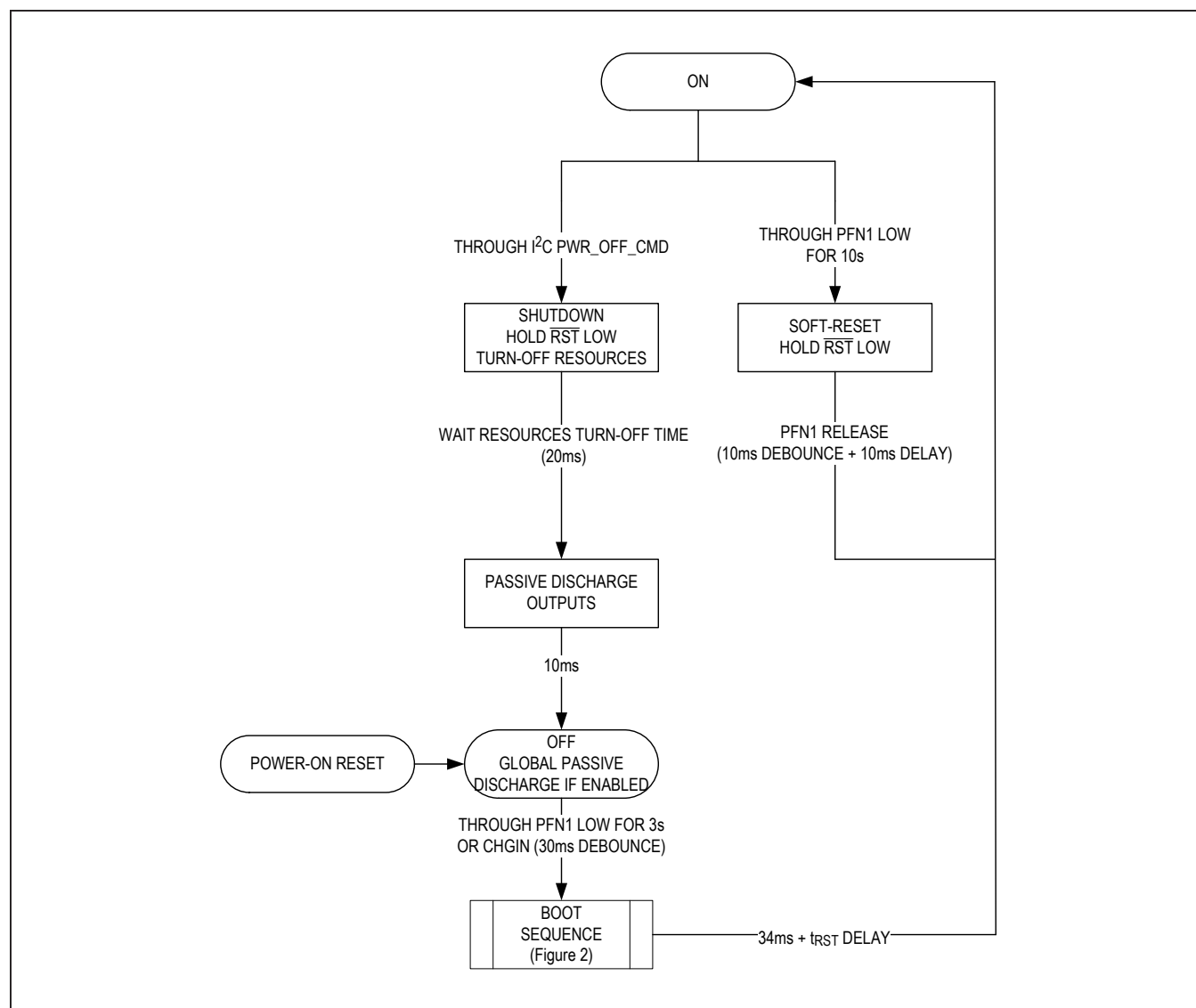
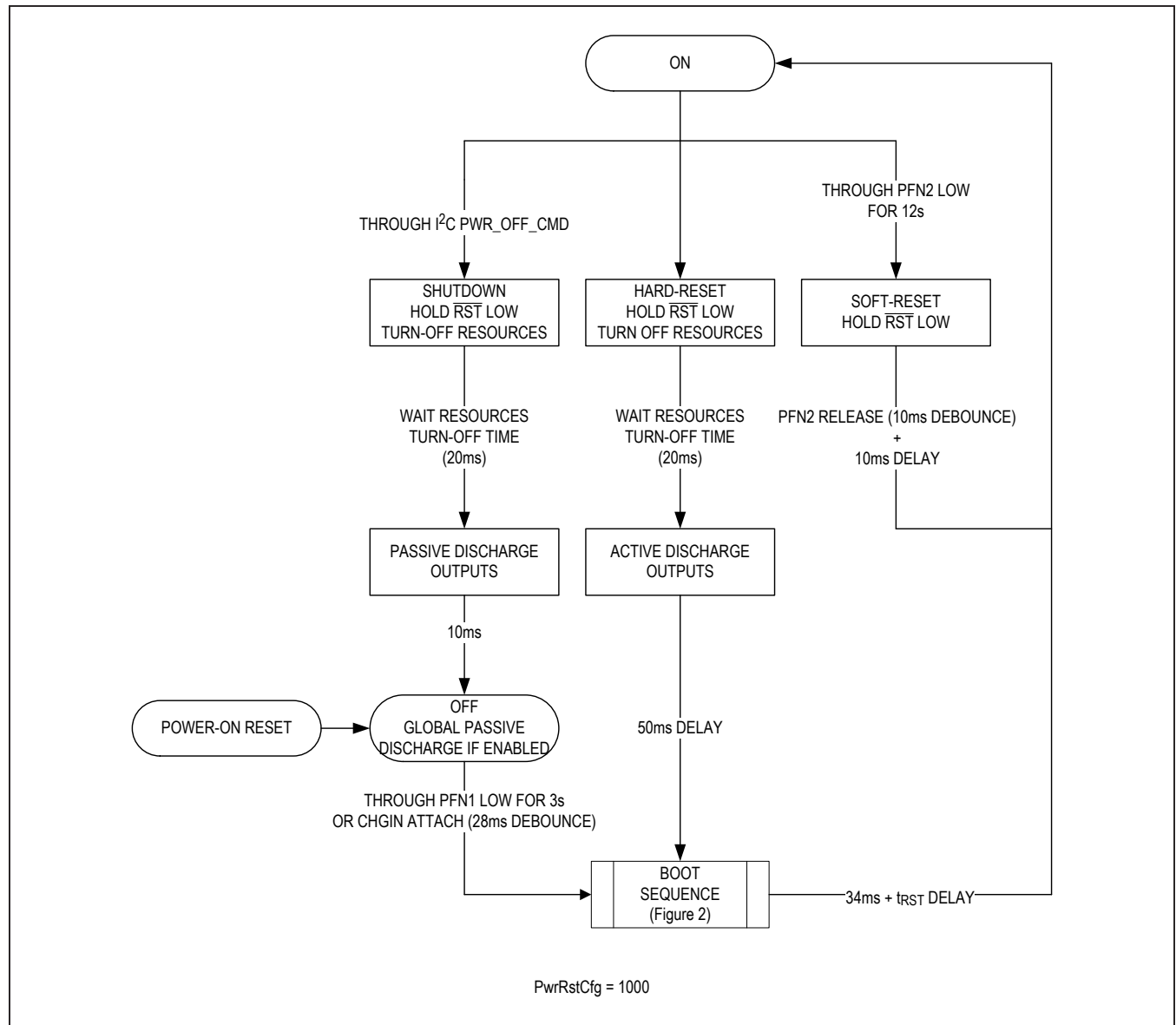


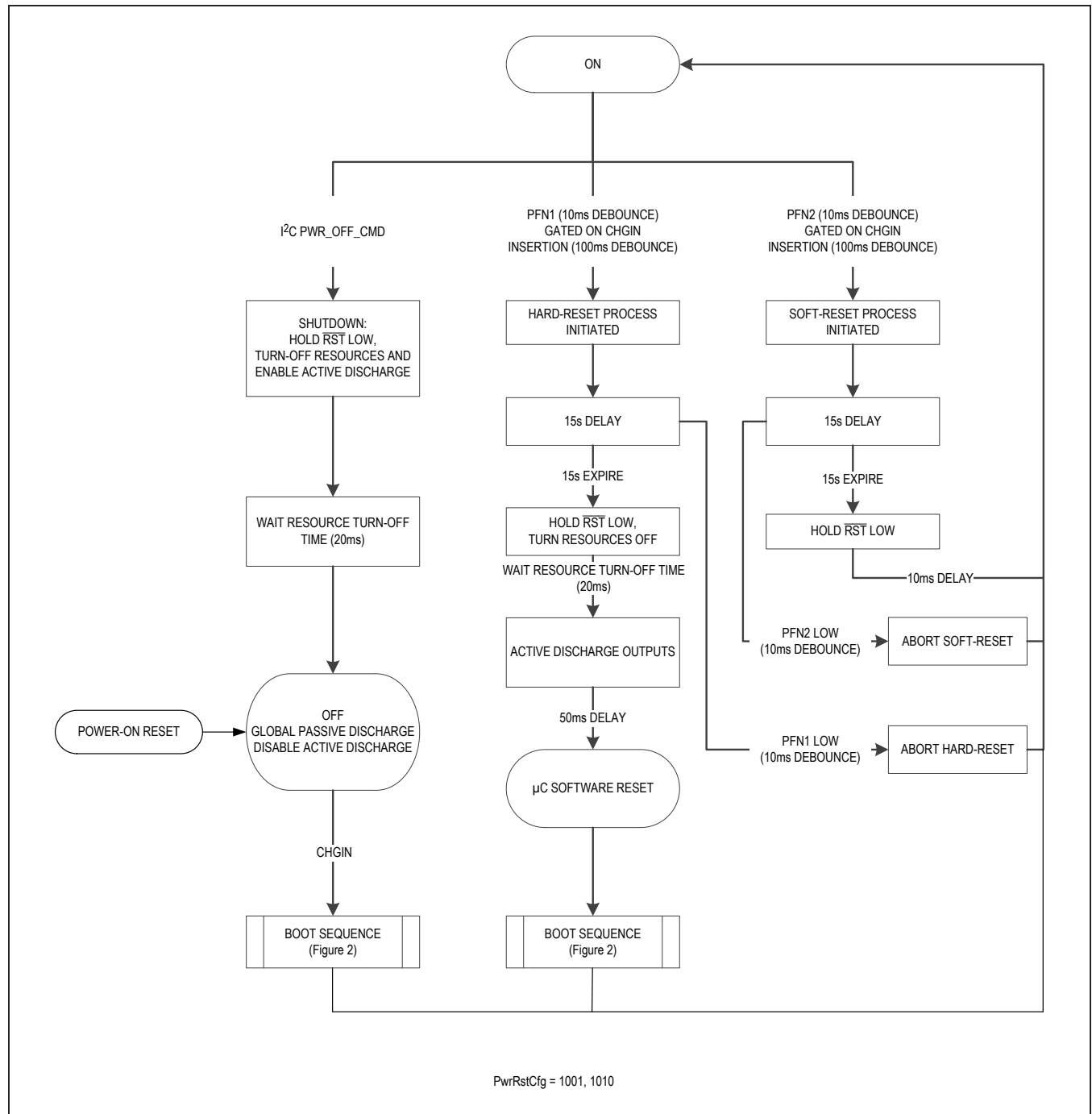
Figure 1b. PwrRstCfg = 0010, 0011

Figure 1c.  $PwrRstCfg = 0100, 0101$

Figure 1d.  $PwrRstCfg = 0110$

Figure 1e.  $PwrRstCfg = 0111$

Figure 1f.  $PwrRstCfg = 1000$

Figure 1g.  $PwrRstCfg = 1001, 1010$

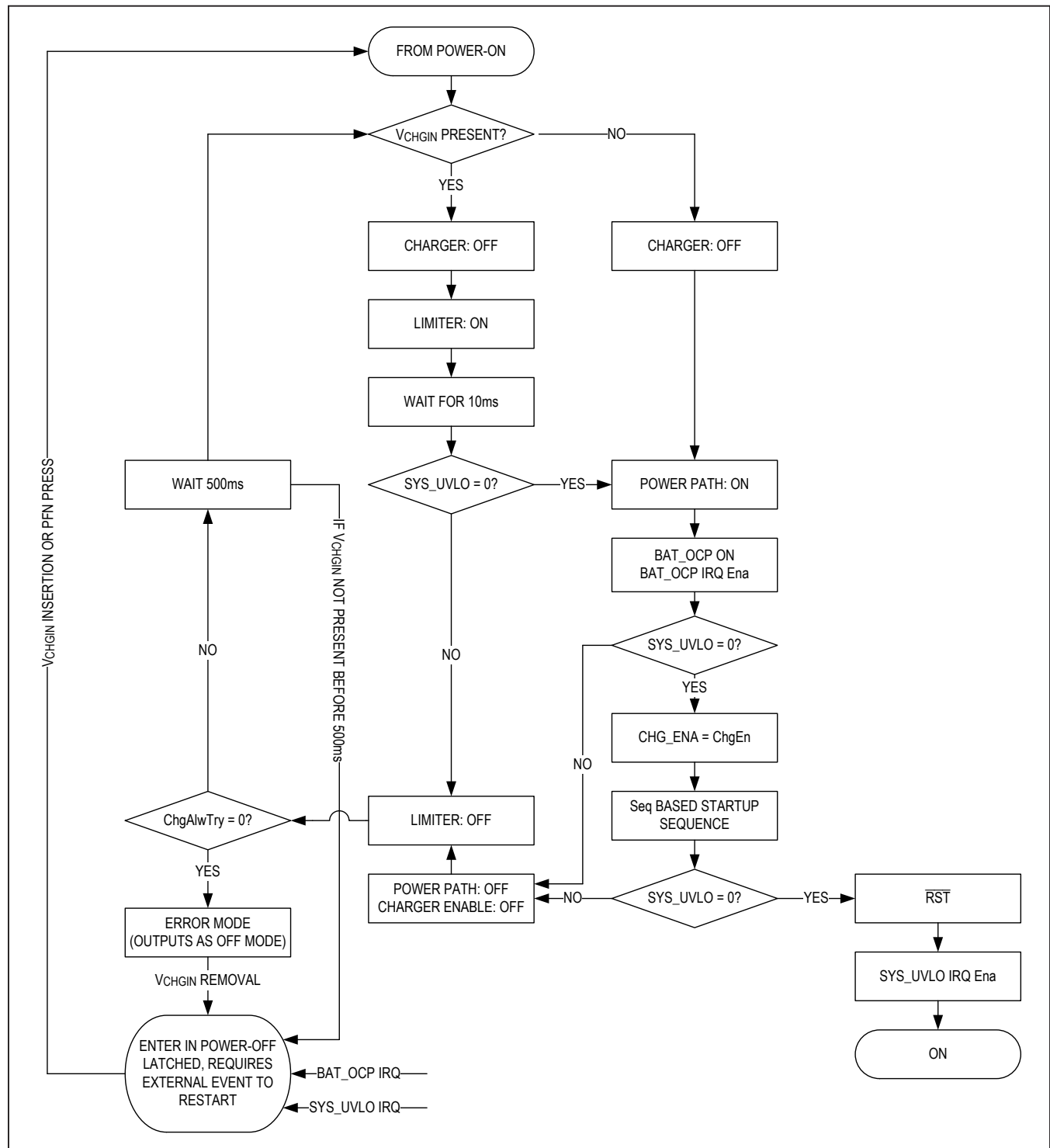
**Boot Sequence**

Figure 2. The MAX20345 Boot Sequence

Power Sequencing

The sequencing of the switching regulators, LDOs, and load switches during power-on is configurable. See each function's sequencing bits for details. Regulators and switches can turn on at one of three points during the power-on process: 45ms after the power-on event, at the time the  $\overline{\text{RST}}$  signal is released, or at two points in between. The two points between the 45ms delay and the  $\overline{\text{RST}}$  rising edge are fixed proportionally to the duration of the power-on reset (POR) process boot delay ( $t_{\text{RST}}$ ). The value of the  $t_{\text{RST}}$  delay ranges from 80ms to 420ms and is stored in the  $\text{BootDly}[1:0]$  bits of register 0x4D. The timing relationship is presented graphically in [Figure 3](#).

Alternatively, the regulators and switches can remain off by default to be turned on manually with an I<sup>2</sup>C command after  $\overline{\text{RST}}$  is released. LDO1 can be configured to be always-on as long as SYS or BAT is present.

The SYS voltage is monitored during the power-on sequence. If  $V_{\text{SYS}}$  falls below  $V_{\text{SYS\_UVLO}}$  during the sequencing process with a valid voltage at CHGIN, the process repeats from the point where SYS was enabled to allow more time for the voltage to stabilize. If there is not a valid voltage at CHGIN, the device returns to the OFF state to avoid draining the battery. Power is also turned off if a current greater than  $\text{IBatOc}$  is sunk from BAT for more than  $t_{\text{BAT\_OC\_D}}$ .

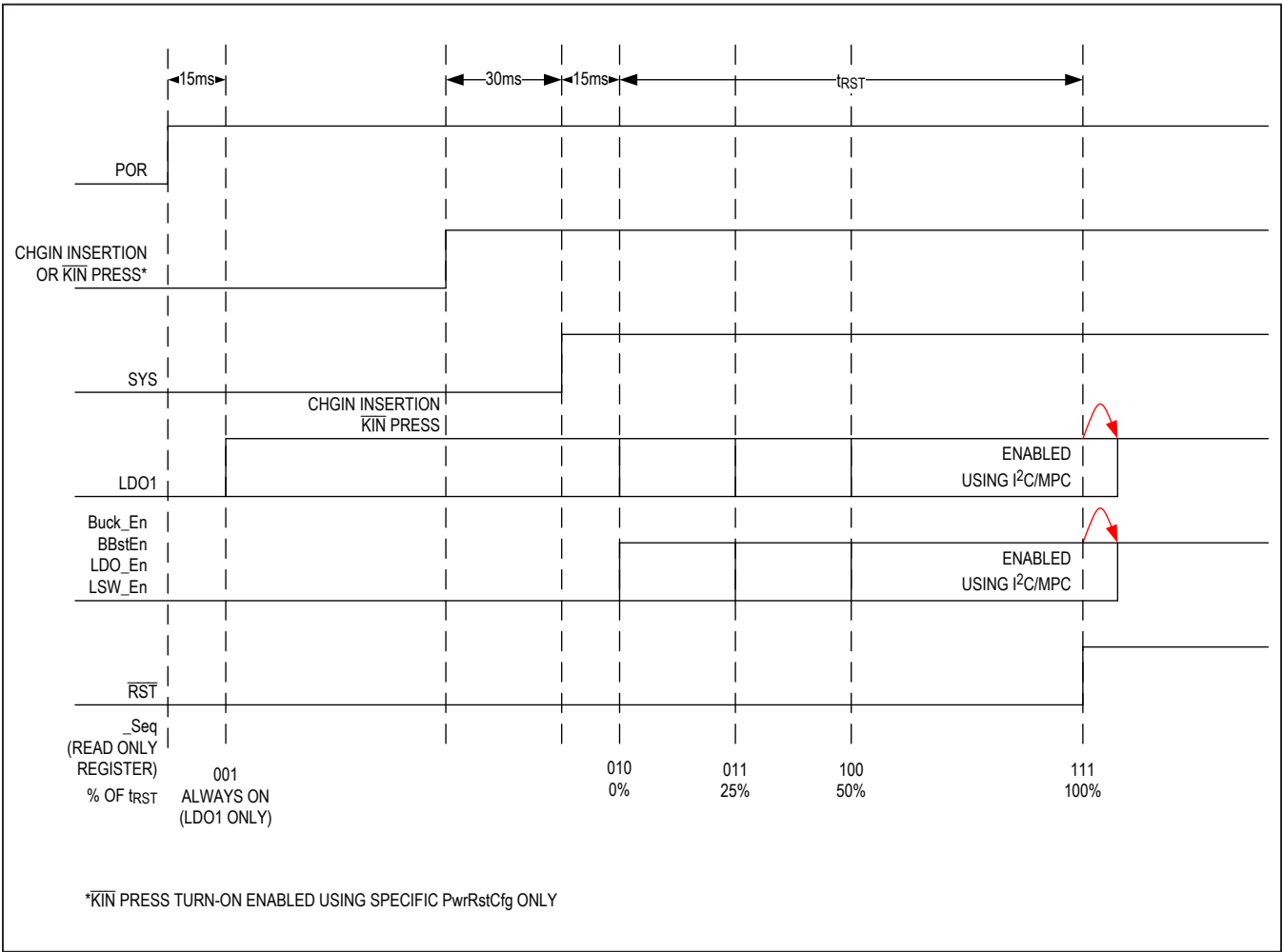


Figure 3. Reset Sequence Programming

### System Load Switch

An internal 80mΩ (typ) MOSFET connects BAT to SYS when no voltage source is available on CHGIN. When an external source is detected at CHGIN, this switch opens and SYS is powered from the input source through the input current limiter. The SYS-to-BAT switch also prevents V<sub>SYS</sub> from falling below V<sub>BAT</sub> when the system load exceeds the input current limit. If V<sub>SYS</sub> drops to V<sub>BAT</sub> due to the current limit, the BAT-SYS switch turns on so the load is supported by the battery. If the system load continuously exceeds the input current limit, the battery is not charged. This is useful for handling loads that are nominally below the input current limit but have high current peaks exceeding the input current limit. During these peaks, battery energy is used, but at all other times the battery charges.

### Smart Power Selector

The smart power selector seamlessly distributes power from the external CHGIN input to the BAT and SYS nodes. With both an external adapter and battery connected, the smart power selector basic functions are:

- When the system load requirements are less than the input current limit, the battery is charged with residual power from the input.
- When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load.
- When the battery is connected and there is no external power input, the system is powered from the battery.

### Input Limiter

The input limiter distributes power from the external adapter to the system load and battery charger. In addition to the input limiter's primary function of passing power to the system load and charger, it performs several additional functions to optimize use of available power.

### Invalid CHGIN Voltage Protection

If CHGIN is above the overvoltage threshold V<sub>CHGIN\_OV</sub>, the device enters overvoltage lockout (OVLO). OVLO protects the MAX20345 and downstream circuitry from high-voltage stress up to +28V. During OVLO, the internal circuit remains powered and an interrupt is sent to the host. The negative voltage protection down to -5.5V disconnects CHGIN and the device is powered only by BAT. The charger turns off and the system load switch closes, allowing the battery to power SYS. CHGIN is also invalid if it is less than V<sub>BAT</sub>, or less than the V<sub>CHGIN\_DET</sub> threshold. With an invalid input voltage, the BAT-SYS load switch closes and allows the battery to power SYS.

### CHGIN Input Current Limit

The CHGIN input current is limited to prevent input overload. The input current limit I<sub>LIM</sub> is I<sup>2</sup>C controlled through parameter ILimCntl[2:0]. To accommodate systems with a high in-rush current, the limiter includes a blanking time t<sub>LIM\_BLANK</sub>, I<sup>2</sup>C programmable through the parameter TLimBlank[1:0], during which the input current limit increases to I<sub>LIM\_MAX</sub>.

### Thermal Limiting

In case the die temperature (T<sub>DIE</sub>) exceeds the T<sub>CHG\_LIM</sub>, the MAX20345 attempts to limit temperature increase by reducing the input current from CHGIN. In particular, the system load has priority over the charger current, so the input current is first reduced by lowering the charge current. If the junction temperature continues to rise and reaches the maximum operating limit T<sub>CHG\_SHDN</sub>, no input current is drawn from CHGIN and the battery powers the entire system load.

### Adaptive Battery Charging

While the system is powered from CHGIN, the charger draws power from SYS to charge the battery. If the total load exceeds the input current limit, an adaptive charger control loop reduces charge current to prevent V<sub>SYS</sub> from collapsing below the maximum between V<sub>SYS\_LIM</sub>, I<sup>2</sup>C programmable through the SysMin[2:0] parameter, and V<sub>SYS\_BAT\_LIM</sub> values. When the charge current is reduced below 50% (IFCHG\_TEXT threshold) due to V<sub>SYS\_LIM</sub>/V<sub>SYS\_BAT\_LIM</sub> or T<sub>CHG\_LIM</sub> limits, the timer clock operates at half speed. When the charge current is reduced below 20% (IFCHG\_TSUS threshold) due to V<sub>SYS\_LIM</sub>/V<sub>SYS\_BAT\_LIM</sub> or T<sub>CHG\_LIM</sub> limits, the timer clock is paused.

### Fast Charge Current Setting

The MAX20345 uses an external resistor connected from ISET to GND to set the fast-charge current I<sub>FCHG</sub>. The precharge, I<sub>PCHG</sub>, and charge-done (I<sub>CHG\_DONE</sub>) currents are I<sup>2</sup>C programmed using IPChg[1:0] and IChgDone[1:0] parameters, respectively, as a percentage of this value. The fast-charge current resistor can be calculated as:

$$R_{ISET} = K_{ISET} \times V_{ISET} / I_{FCHG}$$

where K<sub>ISET</sub> has a typical value of 2000A/A and V<sub>ISET</sub> has a typical value of +1V. The range of acceptable resistors for R<sub>ISET</sub> is 4kΩ to 400kΩ. A capacitive load on ISET can cause instability of the charger if the condition (C<sub>ISET</sub> < 5μs/R<sub>ISET</sub>) pF is violated.

### JEITA Monitoring with Charger Control

To enhance safety when charging Li+ batteries, the MAX20345 includes a JEITA compliant temperature monitoring. A resistive divider is formed on THM by attaching a pullup resistor to TPU and connecting the thermistor of a battery-pack (do not exceed 2mA load on TPU). TPU is internally connected to the internal reference CAP. The divider output is read by internal comparators when JEITA monitoring is enabled and the resulting temperature measurement places the battery into one of five temperature zones: cold, cool, room, warm, and hot. Charging is always inhibited in cold and hot regions or if the thermistor is not detected, while charging behavior is configurable in warm, room, and cool regions using the I<sup>2</sup>C-controlled ThmEn[2:0] parameter. In particular, the battery regulation voltage can be reduced to V<sub>BAT\_REG\_JTA</sub> value using the I<sup>2</sup>C-programmed Cool/Room/WarmBatReg[1:0] parameters, while the fast-charge current can be reduced to I<sub>FCHG\_JTA</sub> value using the I<sup>2</sup>C-programmed Cool/Room/WarmIFChg[2:0] parameters. Charging can also be inhibited in cool and warm regions using ThmEn[2:0].

### THM One-Shot Measurement

Although the MON MUX can route the THM voltage to IVMON with any divider setting, only the 1:1 divider should be used. This ensures the MUX divider impedance does not interfere with the output of the thermistor resistive divider. By default, the thermistor pullup TPU is internally connected to CAP. This does not pose any problem if the application ADC can tolerate the CAP voltage level. If the application ADC requires a lower voltage, however, THM must be sampled using a one-shot measurement procedure.

If a lower voltage reference is needed for thermistor monitoring, an external reference should be connected to TPUEXT and the one-shot THM measurement command should be used to measure the thermistor voltage. When the one-shot is triggered, the MAX20345 performs the following sequence of actions:

- The internal JEITA settings are stored to continue charging in the last sampled temperature region
- The MON MUX is forced into its Hi-Z state
- The internal TPU connection is switched from CAP to TPUEXT
- IVMON is set to output THM at a 1:1 ratio

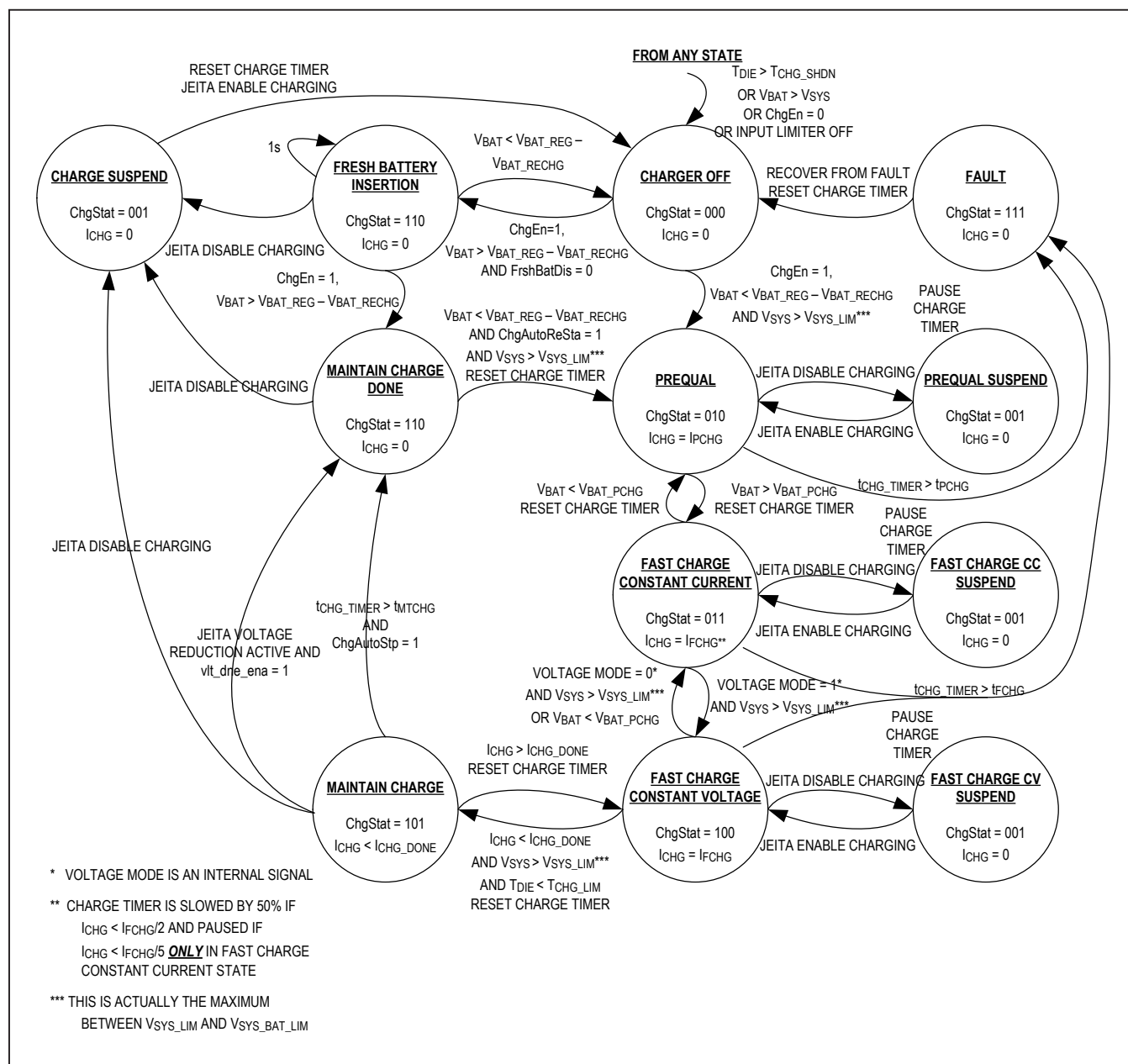
- IVMON passes THM through for 500ms
- The MON MUX is forced into its Hi-Z state
- The internal TPU connection is switched back from TPUEXT to CAP
- The MON MUX returns to its last state before the one-shot

The command is triggered by a rising edge of ThmtoMonEna. The application ADC has 500ms (typ) to take a THM reading before the one-shot expires and the MON MUX returns to its previous state. A rising edge on ThmtoMonAbr aborts the one-shot procedure and returns the TPU reference to CAP.

### Step Charging

Lithium batteries suffer capacity degradation over their lifetimes. One of the primary causes of degradation over the lifetime of a battery is due to an effect called lithium plating which describes the formation of metallic lithium on the anode of the battery. Lithium plating has many causes, but one of the most common is when the battery is charged at high rates relative to the capacity of the battery when the battery is at a high state of charge (SOC). To combat this effect, the MAX20345 includes a step charge function. This function allows the user to select a voltage threshold at which the charge current can be reduced in order to avoid lithium plating and prolong the lifetime of the battery. The settings of this function can be found in the StepChgCfg0 and StepChgCfg1 registers. The ChgStepRise[3:0] field allows the setting of the rising voltage V<sub>BAT\_STPCHG</sub> at which the charge current should be reduced. The ChgIStep[2:0] field sets the percentage I<sub>FCHG\_STPCHG</sub> of the full fast-charge current to which the charger should be set when the battery is above the V<sub>BAT\_STPCHG</sub> value specified with ChgStepRise[3:0]. Lastly, the ChgStepHyst[2:0] field sets the V<sub>BAT\_STPCHG\_H</sub> hysteresis for the step charge function in order to avoid oscillations in case a high battery impedance causes the voltage to fall a large amount upon reduction of the battery current. If this function is not desirable, set the ChgIStep[2:0] field to 100% ("111") to disable it.

In case both JEITA and Step-Charging related fast-charge current reductions are active, the minimum between the two is selected and applied.



## Function Locking

All regulator voltages and the end-of-charge behavior of the charger can be locked. I<sup>2</sup>C writes to a locked bitfield have no effect. To lock a function, its lock mask must be removed in the LockMsk register. To remove the lock mask, set the corresponding function's mask bit to 0. By writing the lock password 0xAA to the LockUnlock register, all unmasked functions are locked. To unlock functions, repeat the mask/unmask process and write the unlock password 0x55 to the LockUnlock register.

## Monitor MUX

In order to simplify system monitoring, the MAX20345 includes a voltage monitor multiplexer (MUX). The MUX, I<sup>2</sup>C controlled using the MONCntl[3:0] parameter, connects the IVMON pin to the scaled value of one of the seven voltage regulators, THM, TPU, BAT, or SYS. A resistive divider scales the selected voltage to one of four ratios determined by MONRatioCfg[1:0]. Because the MUX can only tolerate voltages up to +5.5V, V<sub>CHGIN</sub> is not available to MON.

Additionally, the ISET voltage is available to monitor the charging current according to the following equation:

$$V_{\text{SET}} = I_{\text{CHG}} / (I_{\text{CHG\_PROG}} \times I_{\text{CHG\_RED}}) [V]$$

where:

I<sub>CHG</sub> = Actual charging current flowing into BAT

I<sub>CHG\_PROG</sub> = Either the fast charge or precharge programmed current

I<sub>CHG\_RED</sub> = Eventual reduction factor can be due to JEITA and/or Step-Charging (see ChgIStep[2:0] and Cool/Room/WarmIFChg[2:0] parameters). If neither JEITA nor Step-Charging current reduction is active, I<sub>CHG\_RED</sub> is equal to 1.

## Buck-Boost Regulator

The MAX20345's Buck-Boost regulator provides a low-ripple voltage rail with the ability to boost the battery voltage to 5V. A higher voltage rail eliminates the need for an external regulator to supply systems that cannot otherwise operate from the battery's voltage level. This includes OHR systems with short wavelength LEDs that require large forward voltage drops.

Several controls optimize the efficiency and output noise of the regulator. These include peak current control and automatic peak and valley current adjustment. Additionally, the Buck-Boost regulator can operate in buck-only mode to increase efficiency when V<sub>BBOUT</sub> is much lower than V<sub>SYS</sub>.

The MAX20345 buck-boost is designed to be compatible with small case-size ceramic capacitors. As such, the device has low output capacitance requirements to accommodate the steep voltage derating of 0603 and 0402 (imperial) capacitors. The sample derating curve in Figure 5 presents the minimum capacitance required at OUT for a given maximum set output voltage.

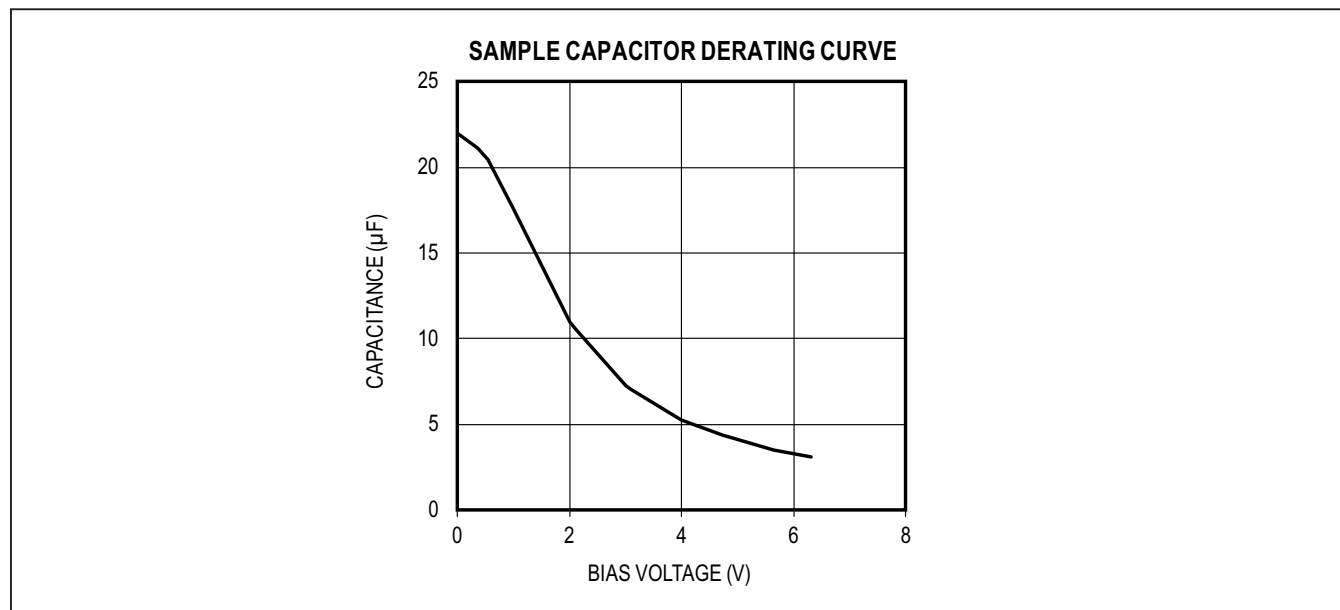


Figure 5. Capacitor Derating for Input and Output Capacitance on Buck-Boost

### Architecture and Switching Phases

The Buck-Boost comprises a typical noninverting Buck-Boost topology. Figure 6 illustrates the regulator's basic structure with arrows depicting the current flow in each switching phase. Depending on the Buck-Boost configurations, the topology enters different sequences of phases to generate the desired output voltage. Only two switches are on in each phase.

- Phase 1: MP1 on, MP2 on. Inductor charges.
- Phase 2: MP1 on, MN2 on. Inductor charges.
- Phase 3: MN1 on, MP2 on. Inductor discharges.
- Phase 4: MN1 on, MN2 on. Freewheeling.

The Buck-Boost features a frequency comparator to monitor its switching frequency. Switching frequency increases as the load current increases. Under low loads, the Buck-Boost optimizes its feedback loop for low quiescent current. When load requirements increase the switching frequency to the  $f_{\text{HIGH}}$  threshold, the low-quiescent current mode is disabled to improve response time. The  $f_{\text{HIGH}}$  threshold is set by the BBFHighSH[1:0] in the BBStCf1 register. Hysteresis prevents the Buck-Boost regulator from resuming the low-quiescent current mode until the switch frequency decreases to  $f_{\text{HIGH}} / 4$ .

### Buck-Boost Mode

When BBStMode (register 0x31[1]) is 0, the regulator operates in Buck-Boost mode. The inductor charges in phase 2 up to BBStIPSet1 (register 0x33[3:0]). The Buck-Boost then transitions to phase 1. If  $V_{\text{SYS}} > V_{\text{BBOU}}$ , the inductor continues charging until either the current reaches BBStIPSet1 + BBStIPSet2 (register 0x33[7:4]) or after a 500ns delay. If  $V_{\text{SYS}} \leq V_{\text{BBOU}}$ , the Buck-Boost waits for the 500ns delay to elapse or until the current drops to the valley limit. Next, the regulator enters phase 3 to discharge the inductor current to the valley limit. When the inductor current reaches the valley-current crossing threshold or falls below 0, the

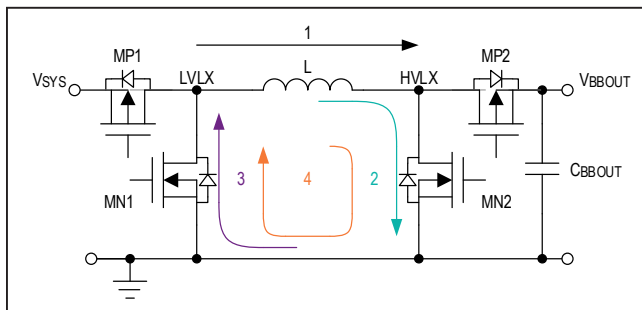


Figure 6. The Buck-Boost Regulator and Switching Phases

regulator freewheels in phase 4 until the next charge phase. When operating in continuous conduction mode (CCM), the Buck-Boost enters phase 4 for approximately 30ns if BBZCCmpEnb = 1. The Buck-Boost skips phase 4 when operating in CCM and BBZCCmpEnb = 0. The valley behavior is determined by BBZCCmpEnb (register 0x34[5]). Figure 7 shows the inductor current in Buck-Boost mode.

### Buck-Only Mode

To maximize efficiency when  $V_{\text{SYS}} > V_{\text{BBOU}}$ , the Buck-Boost regulator has a buck-only mode. When BBStMode = 1, the regulator behaves as a synchronous buck regulator. The inductor charges in phase 1 until the inductor current reaches BBStIPSet1. The regulator then transitions to phase 3 to provide a path to deliver the inductor current to the output. Figure 8 shows the inductor current in buck-only mode.

Buck-only mode reduces switching losses present in Buck-Boost mode. Buck-only mode should be used when  $V_{\text{BBOU}}$  is always less than  $V_{\text{SYS}}$  to maximize efficiency.

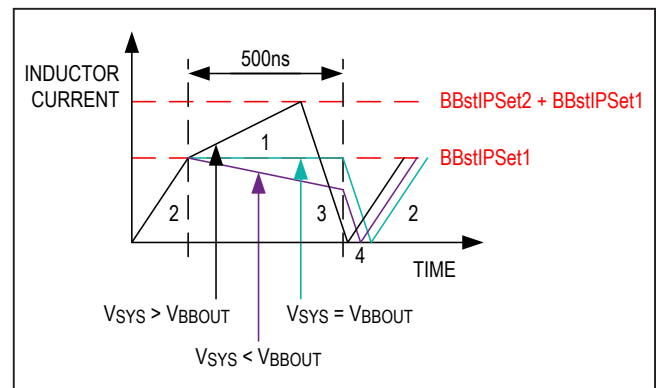


Figure 7. Buck-Boost Inductor Current in Buck-Boost Mode

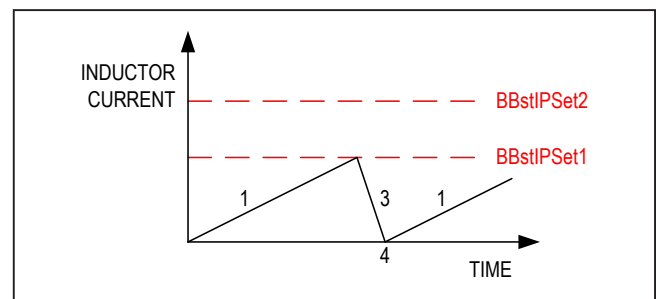


Figure 8. Buck-Boost Inductor Current in Buck-Only Mode

Inductor Peak and Valley Current Limits

The Buck-Boost regulator monitors the maximum and minimum values of the inductor current to control output noise and reduce switching losses. Peak and valley currents can be fixed to the values in BBstIPSet and 0mA, respectively, or allowed to change based on load requirements if BBstIPAdptDis (register 0x34[7]) = 0.

Peak currents are set in the BBstIPSet register. BBstIPSet1 controls the peak current when  $V_{SYS} < V_{BBOU\overline{T}}$  and when the regulator is in buck-only mode. BBstIPSet2 sets a secondary current limit when  $V_{SYS} > V_{BBOU\overline{T}}$

in Buck-Boost mode. The total inductor current limit when  $V_{SYS} > V_{BBOU\overline{T}}$  is BBstIPSet1 + BBstIPSet2. The Buck-Boost regulator transitions to phase 3 if the inductor current reaches BBstIPSet2 before the 500ns timeout has elapsed. Minimizing the difference between BBstIPSet1 and BBstIPSet2 reduces the output ripple, but decreases efficiency. Care must be taken to optimize the peak current settings to keep a low output ripple while maximizing efficiency. Figure 9 presents the safe operating area of BBstIPSet2 with respect to BBstIPSet1. Selecting values lower than those of Figure 9 for a given BBstIPSet1 value may reduce efficiency and increase output ripple.

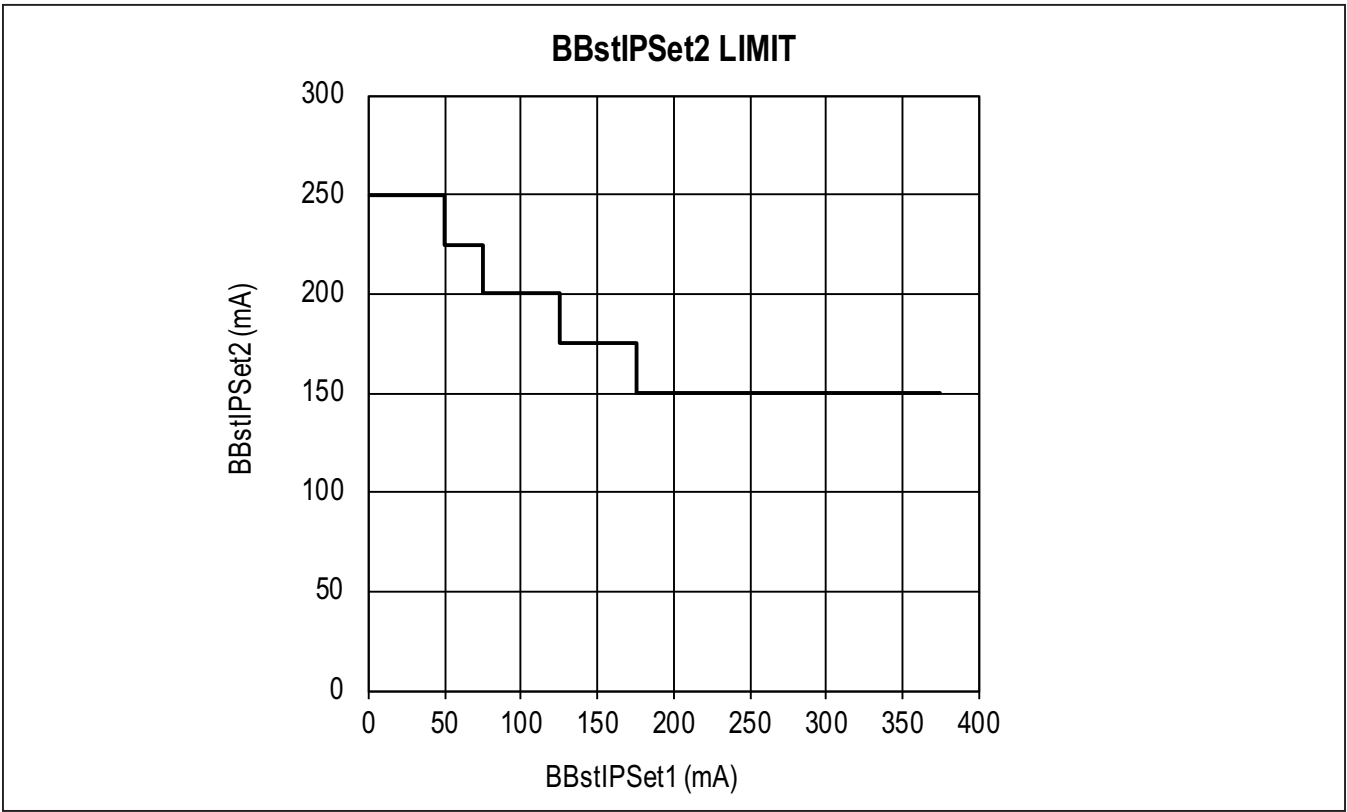


Figure 9. Minimum BBstIPSet2 Limit for a Given BBstIPSet1 Setting

Figure 10 is a graphical guide to selecting combinations of BBstIPSet1 and BBstIPSet2 to maximize efficiency for specific BBstVSet values.

When BBstIPAdptDis = 0, the regulator automatically increases the peak current limits when the load increases to improve load regulation and efficiency at high loads. When BBZCCmpEnb = 1, the Buck-Boost operates with peak and valley current limits. In discontinuous conduction mode (DCM), the valley limit is 0mA and acts as a zero crossing. In CCM mode, the peak and valley limits are automatically adjusted by the voltage loop if BBstIPAdptDis = 0.

When BBZCCmpEnb = 0, the Buck-Boost operates with peak, valley, and zero crossing current limits. The zero crossing limit is fixed at 0mA while the peak and valley limits are adjusted by the voltage loop if BBstIPAdptDis = 0.

In DCM mode, the valley current limit is negative so the end of phase 1 or 3 is determined by the zero-crossing current. In CCM mode, the valley current limit is  $\geq 0$ mA if BBZCCmpEnb = 0. The end of phase 1 or 3 is thus determined by the valley current comparator.

Disabling the zero current crossing comparator reduces the Buck-Boost output ripple. Enabling the comparator improves EMI in CCM mode by removing the phase 4 stage in CCM mode that is otherwise present when BBZCCmpEnb = 1.

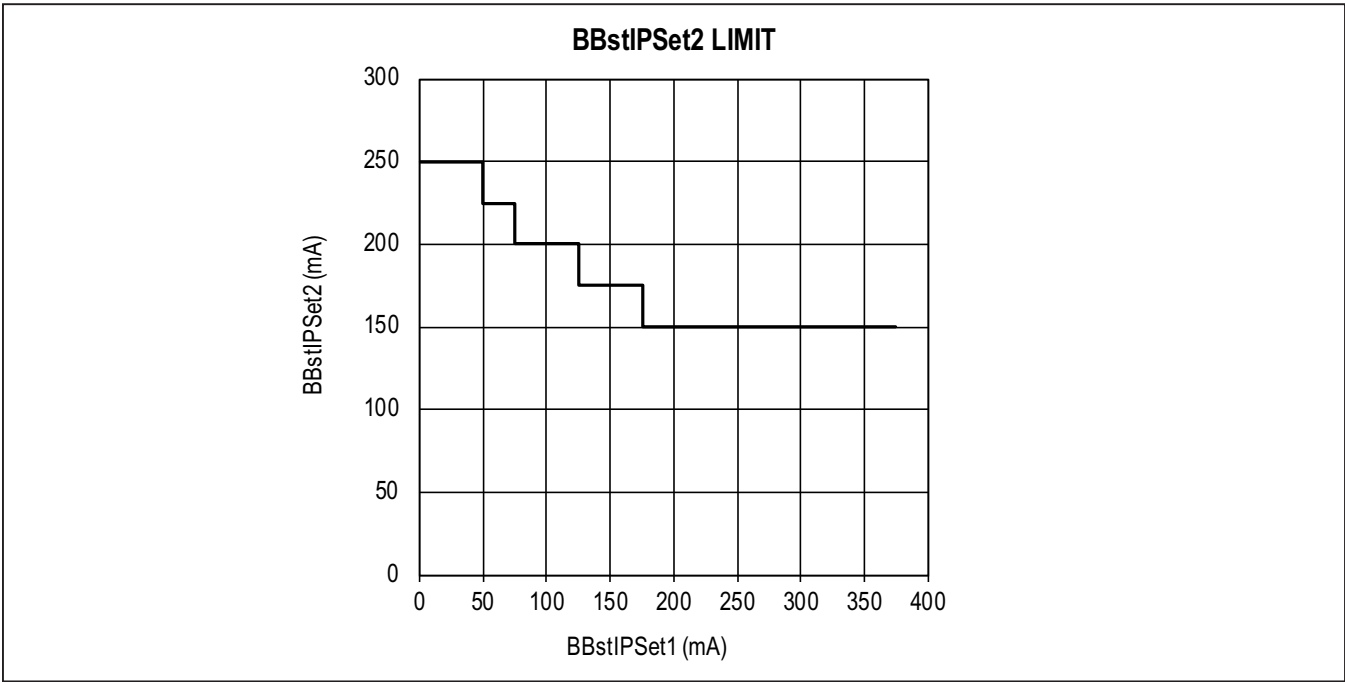


Figure 10. Recommended BBstIPSet1 and BBstIPSet2 Settings

Dynamic Voltage Scaling

All of the MAX20345's switching regulator outputs can be changed without restarting the regulator. This function is called dynamic voltage scaling (DVS). The MAX20345 provides three methods for dynamic voltage scaling of the bucks and Buck-Boost outputs: I<sup>2</sup>C DVS mode, GPIO DVS mode and SPI DVS Mode. The I<sup>2</sup>C mode is the slowest, but requires only simple I<sup>2</sup>C writes to execute. The GPIO control mode offers the fastest control and least complexity. The SPI mode offers a combination of speed and flexibility. Note that the slew-rate of the output voltage scaling is the same in all modes. Only the overhead and delay to initiate the transition changes. DVS modes are selected using the Buck\_DVSCfg and BBstDVSCfg bitfields.

DVS Mode 0 (I<sup>2</sup>C DVS Mode)

DVS Mode 0 configures the regulator outputs to be controlled by I<sup>2</sup>C. If Buck\_DVSCfg or BBstDVSCfg = 000, the output voltage of that regulator is controlled by I<sup>2</sup>C writes to the Buck\_VSet or BBstVSet bitfield. Note, that a regulator in I<sup>2</sup>C mode must be unlocked before modifying the output voltage. Regulators are unlocked by setting their lock mask bit to 0 in LockMsk (register 0x52) and writing the unlock password 0x55 to the LockUnlock register (register 0x53).

DVS Mode 1 (GPIO DVS Mode)

In DVS Mode 1, two MPC inputs select the regulator output from four programmed values. To configure a regulator output for GPIO mode, set the corresponding Buck\_DVSCfg or BBstDVSCfg bits to any value between 001 and 110. Each code selects a different pair of MPC pins to control the regulator. See the DVSCfg register descriptions for details on which MPC inputs are used for a code. In each case, the first MPC listed controls the low bit and the second MPC controls the high bit.

The four voltage levels share the same default value when the MAX20345 first powers on. After the startup process, each 6-bit output voltage level can be programmed using the I<sup>2</sup>C for each converter in the Buck\_DVSVlt\_ and BBstDVSVlt\_ bitfields. As the MPC inputs change, the regulator output adjusts to the newly selected level as illustrated in [Figure 11](#). Voltage levels are selected as shown in [Table 2](#):

Table 2. DVS Mode 1 Voltage Selection

| GPIO1 | GPIO0 | DVS VOLTAGE |
|-------|-------|-------------|
| 0     | 0     | Vlt0        |
| 0     | 1     | Vlt1        |
| 1     | 0     | Vlt2        |
| 1     | 1     | Vlt3        |

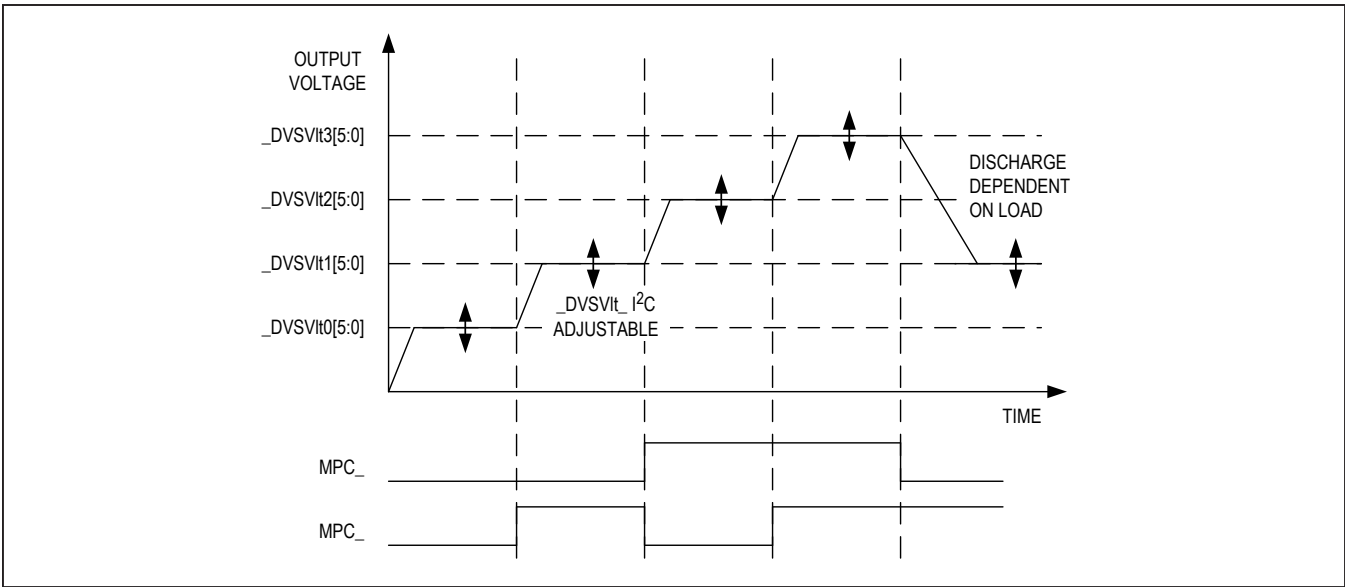


Figure 11. DVS Mode 1, GPIO Control

**SPI DVS Mode (DVS Mode 2)**

In DVS Mode 2, the regulator voltages are changed by writing command bytes to a 3-wire SPI interface. The SPI interface uses MPC0-2. MPC0 becomes the active-low chip select pin  $\overline{CS}$ , MPC1 becomes the clock SCLK, and MPC2 is the data input pin DIN. Data is clocked in on the SCLK rising edge. The maximum SPI clock frequency is 8MHz. A command byte comprises two address bits

ADD[1:0] that select the regulator and six voltage bits VLT[5:0] that set the voltage. [Figure 12](#) shows how data is clocked in SPI mode.

The output voltage is latched on the 8<sup>th</sup> rising edge of the clock. Note that voltages set by the SPI interface are mirrored in the Buck\_VltSet and BBstVltSet bitfields for each converter. [Figure 13](#) shows two regulators controlled in DVS Mode 2.

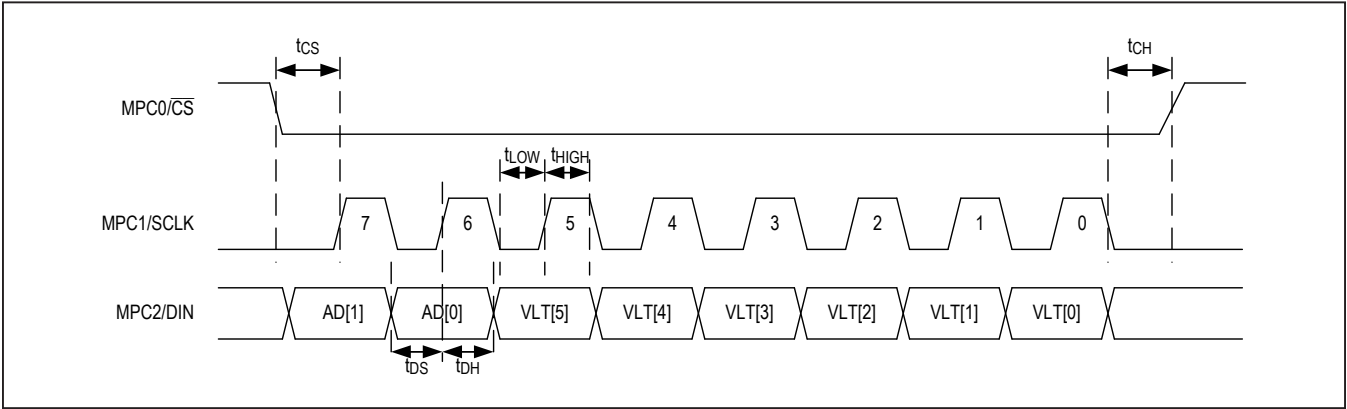


Figure 12. DVS Mode 2 SPI Timing

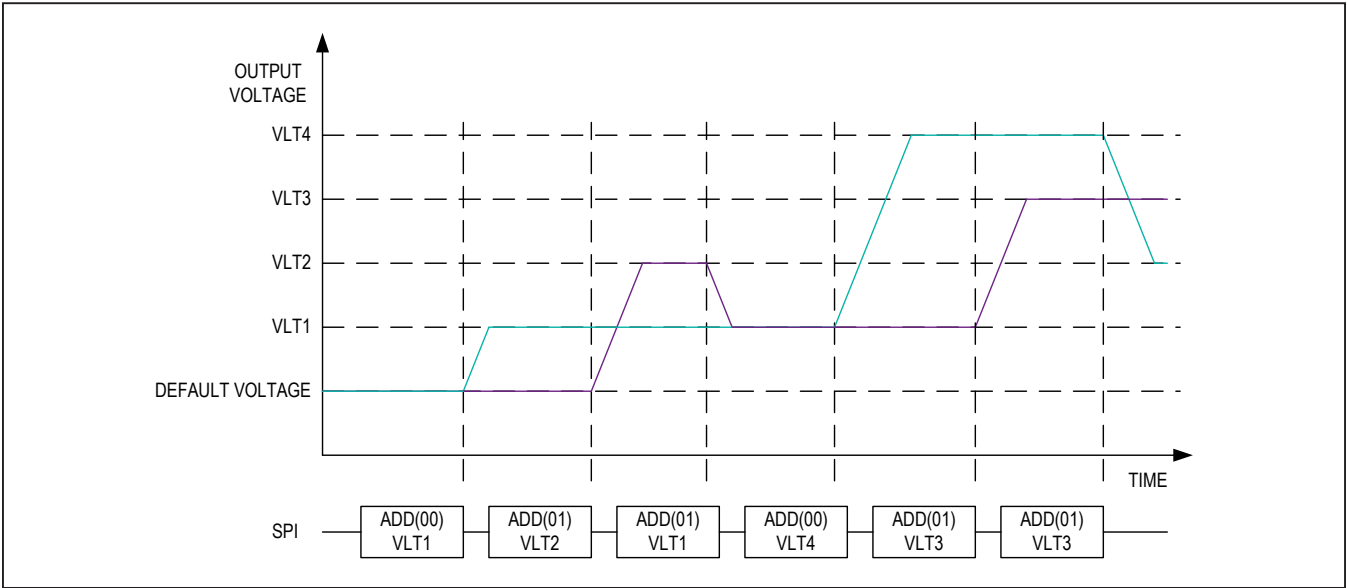


Figure 13. DVS Mode 2, SPI Control

The DVS SPI interface supports single and burst mode data transfer. In single-byte mode,  $\overline{CS}$  goes high after each command byte is transferred. In burst-mode, all command bytes are written to the MAX20345 before  $\overline{CS}$  returns high. [Figure 14](#) shows how data is written in both modes.

**I<sup>2</sup>C Interface Overview**

The MAX20345 uses the two-wire I<sup>2</sup>C interface to communicate with a host microcontroller. The configuration settings and status information provided through this interface are detailed in the register descriptions. The device has the seven-bit slave address 0b0101000 (0x50 for writes, 0x51 for reads). Refer to the [Applications Information](#) section for details on the I<sup>2</sup>C interface.

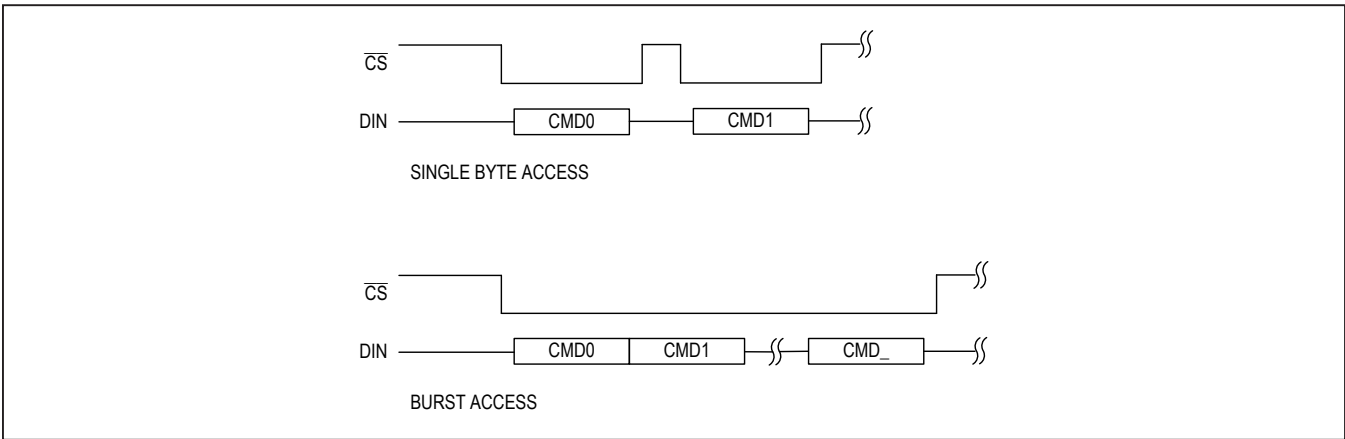


Figure 14. Single-Byte and Burst-Mode SPI Access

## Register Map

| ADDRESS | NAME                  | MSB               |                  |                    |                   |                  |                    |                     | LSB             |
|---------|-----------------------|-------------------|------------------|--------------------|-------------------|------------------|--------------------|---------------------|-----------------|
| User    |                       |                   |                  |                    |                   |                  |                    |                     |                 |
| 0x00    | ChipID[7:0]           | ChipID[7:0]       |                  |                    |                   |                  |                    |                     |                 |
| 0x01    | ChipRev[7:0]          | ChipRev[7:0]      |                  |                    |                   |                  |                    |                     |                 |
| 0x02    | Status0[7:0]          | –                 | –                | ThmStat[2:0]       |                   |                  | ChgStat[2:0]       |                     |                 |
| 0x03    | Status1[7:0]          | –                 | –                | ILim               | UsbOVP            | UsbOk            | ChgJEITA<br>SD     | ChgJEITA<br>Reg     | ChgTmo          |
| 0x04    | Status2[7:0]          | ThmSD             | ThmtoMon         | ThmLDO_<br>LSW     | UVLOL<br>DO2      | –                | –                  | –                   | –               |
| 0x05    | Status3[7:0]          | BBstFault         | BBst<br>UVLO     | Sys<br>BatLim      | ChgSysLim         | StepChg          | ThmBk1             | ThmBk2              | ThmBk3          |
| 0x06    | Int0[7:0]             | Thm<br>StatInt    | ChgStatInt       | ILimInt            | UsbOVPInt         | UsbOkInt         | ChgJEITA<br>SDInt  | ChgJEITA<br>RegInt  | Chg<br>Tmolnt   |
| 0x07    | Int1[7:0]             | ThmSDInt          | ThmtoMon<br>Int  | ThmLDO_<br>LSWInt  | UVLOL<br>DO2Int   | –                | –                  | LSW1<br>Tmolnt      | LSW2<br>Tmolnt  |
| 0x08    | Int2[7:0]             | BBst<br>FaultInt  | BBst<br>UVLOInt  | SYSBat<br>LimInt   | ChgSys<br>LimInt  | Step<br>ChgInt   | Thm<br>Bk1Int      | Thm<br>Bk2Int       | Thm<br>Bk3Int   |
| 0x09    | IntMask0[7:0]         | Thm<br>StatIntM   | Chg<br>StatIntM  | ILimIntM           | Usb<br>OVPIntM    | Usb<br>OkIntM    | ChgJEITA<br>SDIntM | ChgJEITA<br>RegIntM | Chg<br>TmolntM  |
| 0x0A    | IntMask1[7:0]         | Thm<br>SDIntM     | ThmtoMon<br>IntM | ThmLDO_<br>LSWIntM | UVLOL<br>DO2IntM  | –                | –                  | LSW1<br>TmolntM     | LSW2<br>TmolntM |
| 0x0B    | IntMask2[7:0]         | BBstFau<br>ItIntM | BBstUV<br>LOIntM | SysBat<br>LimIntM  | ChgSys<br>LimIntM | Step<br>ChgIntM  | Thm<br>Bk1IntM     | Thm<br>Bk2IntM      | Thm<br>Bk3IntM  |
| 0x0C    | ILimCntl[7:0]         | SysMin[2:0]       |                  |                    | ILimBlank[1:0]    |                  | ILimCntl[2:0]      |                     |                 |
| 0x0D    | ChgCntl0[7:0]         | –                 | BatReChg[1:0]    |                    | BatReg[3:0]       |                  |                    |                     | ChgEn           |
| 0x0E    | ChgCntl1[7:0]         | –                 | VPChg[2:0]       |                    |                   | IPChg[1:0]       |                    | IChgDone[1:0]       |                 |
| 0x0F    | ChgTmr[7:0]           | Chg<br>AutoStp    | ChgAuto<br>ReSta | MtChgTmr[1:0]      |                   | FChgTmr[1:0]     |                    | PChgTmr[1:0]        |                 |
| 0x10    | StepChgCfg0[7:0]      | –                 | ChgStepHyst[2:0] |                    |                   | ChgStepRise[3:0] |                    |                     |                 |
| 0x11    | StepChgCfg1[7:0]      | –                 | –                | –                  | –                 | –                | ChgIStep[2:0]      |                     |                 |
| 0x12    | ThmCfg0[7:0]          | ThmEn[2:0]        |                  |                    | CoolBatReg[1:0]   |                  | CoolIFChg[2:0]     |                     |                 |
| 0x13    | ThmCfg1[7:0]          | –                 | –                | –                  | RoomBatReg[1:0]   |                  | RoomIFChg[2:0]     |                     |                 |
| 0x14    | ThmCfg2[7:0]          | –                 | –                | –                  | WarmBatReg[1:0]   |                  | WarmIFChg[2:0]     |                     |                 |
| 0x15    | MONCfg[7:0]           | –                 | MONRatioCfg[1:0] |                    | MonHiZ            | MONCntl[3:0]     |                    |                     |                 |
| 0x16    | Buck1Cfg[7:0]         | Buck1Seq[2:0]     |                  |                    | Buck1En[1:0]      |                  | Buck1IZCSet[1:0]   |                     | Buck1<br>PsvDsc |
| 0x17    | Buck1VSet[7:0]        | Buck1<br>LowEMI   | Buck1<br>RampEn  | Buck1VSet[5:0]     |                   |                  |                    |                     |                 |
| 0x18    | Buck1Set[7:0]         | Buck1<br>IAdptEn  | Buck1<br>SftStrt | Buck1<br>ActDsc    | Buck1<br>FETScale | Buck1ISet[3:0]   |                    |                     |                 |
| 0x19    | Buck1Ctr(0x19)        | –                 | Buck1DVSCfg[2:0] |                    |                   | Buck1<br>MPC3    | Buck1<br>MPC2      | Buck1<br>MPC1       | Buck1<br>MPC0   |
| 0x1A    | Buck1<br>DVSCfg0[7:0] | –                 | –                | Buck1DVSVIt0[5:0]  |                   |                  |                    |                     |                 |

## Register Map (continued)

| ADDRESS | NAME                                    | MSB              |                  |                   |                   |                |                  |               | LSB             |
|---------|-----------------------------------------|------------------|------------------|-------------------|-------------------|----------------|------------------|---------------|-----------------|
| User    |                                         |                  |                  |                   |                   |                |                  |               |                 |
| 0x1B    | <a href="#">Buck1<br/>DVSCfg1 [7:0]</a> | —                | —                | Buck1DVSVIt1[5:0] |                   |                |                  |               |                 |
| 0x1C    | <a href="#">Buck1<br/>DVSCfg2[7:0]</a>  | —                | —                | Buck1DVSVIt2[5:0] |                   |                |                  |               |                 |
| 0x1D    | <a href="#">Buck1<br/>DVSCfg3[7:0]</a>  | —                | —                | Buck1DVSVIt3[5:0] |                   |                |                  |               |                 |
| 0x1E    | <a href="#">Buck1<br/>DVSSPI[7:0]</a>   | —                | —                | Buck1SPIVIt[5:0]  |                   |                |                  |               |                 |
| 0x1F    | <a href="#">Buck2Cfg[7:0]</a>           | Buck2Seq[2:0]    |                  |                   | Buck2En[1:0]      |                | Buck2IZCSet[1:0] |               | Buck2<br>PsvDsc |
| 0x20    | <a href="#">Buck2VSet[7:0]</a>          | Buck2<br>LowEMI  | Buck2<br>RampEn  | Buck2VSet[5:0]    |                   |                |                  |               |                 |
| 0x21    | <a href="#">Buck2ISet[7:0]</a>          | Buck2<br>IAdptEn | Buck2<br>SftStrt | Buck2<br>ActDsc   | Buck2<br>FETScale | Buck2ISet[3:0] |                  |               |                 |
| 0x22    | <a href="#">Buck2Ctr[7:0]</a>           | —                | Buck2DVSCfg[2:0] |                   |                   | Buck2<br>MPC3  | Buck2<br>MPC2    | Buck2<br>MPC1 | Buck2<br>MPC0   |
| 0x23    | <a href="#">Buck2<br/>DVSCfg0[7:0]</a>  | —                | —                | Buck2DVSVIt0[5:0] |                   |                |                  |               |                 |
| 0x24    | <a href="#">Buck2<br/>DVSCfg1[7:0]</a>  | —                | —                | Buck2DVSVIt1[5:0] |                   |                |                  |               |                 |
| 0x25    | <a href="#">Buck2<br/>DVSCfg2[7:0]</a>  | —                | —                | Buck2DVSVIt2[5:0] |                   |                |                  |               |                 |
| 0x26    | <a href="#">Buck2<br/>DVSCfg3[7:0]</a>  | —                | —                | Buck2DVSVIt3[5:0] |                   |                |                  |               |                 |
| 0x27    | <a href="#">Buck2<br/>DVSSPI[7:0]</a>   | —                | —                | Buck2SPIVIt[5:0]  |                   |                |                  |               |                 |
| 0x28    | <a href="#">Buck3Cfg[7:0]</a>           | Buck3Seq[2:0]    |                  |                   | Buck3En[1:0]      |                | Buck3IZCSet[1:0] |               | Buck3<br>PsvDsc |
| 0x29    | <a href="#">Buck3VSet[7:0]</a>          | Buck3<br>LowEMI  | Buck3<br>RampEn  | Buck3VSet[5:0]    |                   |                |                  |               |                 |
| 0x2A    | <a href="#">Buck3ISet[7:0]</a>          | Buck3<br>IAdptEn | Buck3<br>SftStrt | Buck3<br>ActDsc   | Buck3<br>FETScale | Buck3ISet[3:0] |                  |               |                 |
| 0x2B    | <a href="#">Buck3Ctr[7:0]</a>           | —                | Buck3DVSCfg[2:0] |                   |                   | Buck3<br>MPC3  | Buck3<br>MPC2    | Buck3<br>MPC1 | Buck3<br>MPC0   |
| 0x2C    | <a href="#">Buck3<br/>DVSCfg0[7:0]</a>  | —                | —                | Buck3DVSVIt0[5:0] |                   |                |                  |               |                 |
| 0x2D    | <a href="#">Buck3<br/>DVSCfg1[7:0]</a>  | —                | —                | Buck3DVSVIt1[5:0] |                   |                |                  |               |                 |
| 0x2E    | <a href="#">Buck3<br/>DVSCfg2[7:0]</a>  | —                | —                | Buck3DVSVIt2[5:0] |                   |                |                  |               |                 |
| 0x2F    | <a href="#">Buck3<br/>DVSCfg3[7:0]</a>  | —                | —                | Buck3DVSVIt3[5:0] |                   |                |                  |               |                 |
| 0x30    | <a href="#">Buck3<br/>DVSSPI[7:0]</a>   | —                | —                | Buck3SPIVIt[5:0]  |                   |                |                  |               |                 |

## Register Map (continued)

| ADDRESS | NAME                             | MSB             |                 |                  |               |                 |             |                | LSB         |
|---------|----------------------------------|-----------------|-----------------|------------------|---------------|-----------------|-------------|----------------|-------------|
| User    |                                  |                 |                 |                  |               |                 |             |                |             |
| 0x31    | <a href="#">BBstCfg0[7:0]</a>    | BBstSeq[2:0]    |                 |                  | BBstEn[1:0]   |                 | BBst RampEn | BBstMode       | BBst PsvDsc |
| 0x32    | <a href="#">BBstVSet[7:0]</a>    | BBst LowEMI     | BBstAct Dsc     | BBstVSet[5:0]    |               |                 |             |                |             |
| 0x33    | <a href="#">BBstISet[7:0]</a>    | BBstIPSet2[3:0] |                 |                  |               | BBstIPSet1[3:0] |             |                |             |
| 0x34    | <a href="#">BBstCfg1[7:0]</a>    | BBstI PAcptDis  | BBstFast        | BBZC CmpDis      | BBst FETScale | –               | –           | BBFHighSh[1:0] |             |
| 0x35    | <a href="#">BBstCtr[7:0]</a>     | BBst MPC1FCT    | BBstDVSCfg[2:0] |                  |               | BBst MPC3       | BBst MPC2   | BBst MPC1      | BBst MPC0   |
| 0x36    | <a href="#">BBstDVSCfg0[7:0]</a> | –               | –               | BBstDVSVIt0[5:0] |               |                 |             |                |             |
| 0x37    | <a href="#">BBstDVSCfg1[7:0]</a> | –               | –               | BBstDVSVIt1[5:0] |               |                 |             |                |             |
| 0x38    | <a href="#">BBstDVSCfg2[7:0]</a> | –               | –               | BBstDVSVIt2[5:0] |               |                 |             |                |             |
| 0x39    | <a href="#">BBstDVSCfg3[7:0]</a> | –               | –               | BBstDVSVIt3[5:0] |               |                 |             |                |             |
| 0x3A    | <a href="#">BBstDVSSPI[7:0]</a>  | –               | –               | BBstSPIVIt[5:0]  |               |                 |             |                |             |
| 0x3B    | <a href="#">LDO1Cfg[7:0]</a>     | LDO1Seq[2:0]    |                 |                  | LDO1En[1:0]   |                 | LDO1 ActDsc | LDO1 Mode      | LDO1 PsvDsc |
| 0x3C    | <a href="#">LDO1VSet[7:0]</a>    | –               | –               | –                | LDO1VSet[4:0] |                 |             |                |             |
| 0x3D    | <a href="#">LDO1Ctr[7:0]</a>     | –               | –               | –                | –             | LDO1 MPC3       | LDO1 MPC2   | LDO1 MPC1      | LDO1 MPC0   |
| 0x3E    | <a href="#">LDO2Cfg[7:0]</a>     | LDO2Seq[2:0]    |                 |                  | LDO2En[1:0]   |                 | LDO2 ActDsc | LDO2 Mode      | LDO2 PsvDsc |
| 0x3F    | <a href="#">LDO2VSet[7:0]</a>    | –               | –               | –                | LDO2VSet[4:0] |                 |             |                |             |
| 0x40    | <a href="#">LDO2Ctr[7:0]</a>     | –               | –               | –                | –             | LDO2 MPC3       | LDO2 MPC2   | LDO2 MPC1      | LDO2 MPC0   |
| 0x41    | <a href="#">LDO3Cfg[7:0]</a>     | LDO3Seq[2:0]    |                 |                  | LDO3En[1:0]   |                 | LDO3 ActDsc | LDO3 Mode      | LDO3 PsvDsc |
| 0x42    | <a href="#">LDO3VSet[7:0]</a>    | –               | –               | LDO3VSet[5:0]    |               |                 |             |                |             |
| 0x43    | <a href="#">LDO3Ctr[7:0]</a>     | LDO3_MP C0CNT   | LDO3_MP C0CNF   | –                | –             | LDO3 MPC3       | LDO3 MPC2   | LDO3 MPC1      | LDO3 MPC0   |
| 0x44    | <a href="#">LSW1Cfg[7:0]</a>     | LSW1Seq[2:0]    |                 |                  | LSW1En[1:0]   |                 | LSW1 ActDsc | LSW1 LowIq     | LSW1 PsvDsc |
| 0x45    | <a href="#">LSW1Ctr[7:0]</a>     | –               | –               | –                | –             | LSW1 MPC3       | LSW1 MPC2   | LSW1 MPC1      | LSW1 MPC0   |
| 0x46    | <a href="#">LSW2Cfg[7:0]</a>     | LSW2Seq[2:0]    |                 |                  | LSW2En[1:0]   |                 | LSW2 ActDsc | LSW2 LowIq     | LSW2 PsvDsc |
| 0x47    | <a href="#">LSW2Ctr[7:0]</a>     | –               | –               | –                | –             | LSW2 MPC3       | LSW2 MPC2   | LSW2 MPC1      | LSW2 MPC0   |
| 0x48    | <a href="#">MPC0Cfg[7:0]</a>     | MPC0Pin         | –               | –                | MPC0Out       | MPC0OD          | MPC0 HiZB   | MPC0Res        | MPC0Pup     |
| 0x49    | <a href="#">MPC1Cfg[7:0]</a>     | MPC1Pin         | –               | –                | MPC1Out       | MPC1OD          | MPC1 HiZB   | MPC1Res        | MPC1Pup     |

## Register Map (continued)

| ADDRESS     | NAME                            | MSB               |              |         |         |           |              |         | LSB        |
|-------------|---------------------------------|-------------------|--------------|---------|---------|-----------|--------------|---------|------------|
| <b>User</b> |                                 |                   |              |         |         |           |              |         |            |
| 0x4A        | <a href="#">MPC2Cfg[7:0]</a>    | MPC2Pin           | –            | –       | MPC2Out | MPC2OD    | MPC2 HiZB    | MPC2Res | MPC2Pup    |
| 0x4B        | <a href="#">MPC3Cfg[7:0]</a>    | MPC3Pin           | –            | –       | MPC3Out | MPC3OD    | MPC3 HiZB    | MPC3Res | MPC3Pup    |
| 0x4C        | <a href="#">PFN[7:0]</a>        | –                 | –            | –       | –       | –         | –            | PFN2Pin | PFN1Pin    |
| 0x4D        | <a href="#">BootCfg[7:0]</a>    | PwrRstCfg[3:0]    |              |         |         | SftRstCfg | BootDly[1:0] |         | Chg AlwTry |
| 0x4E        | <a href="#">PwrCfg[7:0]</a>     | ThmtoMon En       | ThmtoMon Abr | –       | –       | –         | –            | –       | StayOn     |
| 0x4F        | <a href="#">PwrCmd[7:0]</a>     | PowerCommand[7:0] |              |         |         |           |              |         |            |
| 0x52        | <a href="#">LockMsk[7:0]</a>    | LDO3Lck           | LDO2Lck      | LDO1Lck | BBstLck | Bk3Lck    | Bk2Lck       | Bk1Lck  | ChgLck     |
| 0x53        | <a href="#">LockUnlock[7:0]</a> | PASSWORD[7:0]     |              |         |         |           |              |         |            |

## Register Descriptions

[ChipID \(0x00\)](#)

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | ChipID[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x07        |   |   |   |   |   |   |   |
| Access Type | Read Only   |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                           |
|----------|------|-------------------------------------------------------|
| ChipID   | 7:0  | ChipID[7:0] indicates the version of MAX20345 in use. |

[ChipRev \(0x01\)](#)

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | ChipRev[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x02         |   |   |   |   |   |   |   |
| Access Type | Read Only    |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                  |
|----------|------|------------------------------------------------------------------------------|
| ChipRev  | 7:0  | ChipRev[7:0] bits show information about the revision of the silicon in use. |

**Status0 (0x02)**

| BIT         | 7 | 6 | 5            | 4 | 3 | 2            | 1 | 0 |
|-------------|---|---|--------------|---|---|--------------|---|---|
| Field       | – | – | ThmStat[2:0] |   |   | ChgStat[2:0] |   |   |
| Reset       | – | – | 000          |   |   | 000          |   |   |
| Access Type | – | – | Read Only    |   |   | Read Only    |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|----------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ThmStat  | 5:3  | Status of Thermistor Monitoring<br>000 = Cold Temperature Region<br>001 = Cool Temperature Region<br>010 = Room Temperature Region<br>011 = Warm Temperature Region<br>100 = Hot Temperature Region<br>101 = No thermistor detected (THM high due to external pullup). Note that if a parallel resistor is used for thermistor monitoring, this status may not function properly.<br>110 = NTC input disable by ThmEn[2:0]<br>111 = Detection disabled because CHGIN is not present. THM can still be measured by IVMON. |
| ChgStat  | 2:0  | Status of Charger Mode<br>000 = Charger off<br>001 = Charging suspended due to temperature (see <a href="#">Figure 4</a> )<br>010 = Pre-charge in progress<br>011 = Fast-charge constant current mode in progress<br>100 = Fast-charge constant voltage mode in progress<br>101 = Maintain charge in progress<br>110 = Maintain charge timer done<br>111 = Charger fault condition (see <a href="#">Figure 4</a> )                                                                                                       |

**Status1 (0x03)**

| BIT         | 7 | 6 | 5         | 4         | 3         | 2          | 1           | 0         |
|-------------|---|---|-----------|-----------|-----------|------------|-------------|-----------|
| Field       | – | – | ILim      | UsbOVP    | UsbOk     | ChgJEITASD | ChgJEITAReg | ChgTmo    |
| Reset       | – | – | 0         | 0         | 0         | 0          | 0           | 0         |
| Access Type | – | – | Read Only | Read Only | Read Only | Read Only  | Read Only   | Read Only |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                  |
|-------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ILim        | 5    | Status of CHGIN Input Current Limit<br>0 = CHGIN input current below limit<br>1 = CHGIN input current limit active                                                                                           |
| UsbOVP      | 4    | Status of CHGIN OVP<br>0 = CHGIN overvoltage not detected<br>1 = CHGIN overvoltage detected                                                                                                                  |
| UsbOk       | 3    | Status of CHGIN Input<br>0 = CHGIN Input not present or outside of valid range<br>1 = CHGIN Input present and valid                                                                                          |
| ChgJEITASD  | 2    | Status of JEITA Thermal Shutdown<br>0 = Charger in normal operating mode, or disabled<br>1 = Charger is in thermal shutdown as set by ThmEn[2:0]                                                             |
| ChgJEITAReg | 1    | Status of Thermal Regulation<br>0 = Charger is in normal operating mode, or disabled<br>1 = Charger is in thermal regulation mode and charging current is being actively reduced according to JEITA settings |
| ChgTmo      | 0    | Status of Charger Time-Out Condition<br>0 = Charger is in normal operating mode, or disabled<br>1 = Charger has reached a time-out condition                                                                 |

**Status2 (0x04)**

| BIT         | 7         | 6         | 5          | 4         | 3 | 2 | 1 | 0 |
|-------------|-----------|-----------|------------|-----------|---|---|---|---|
| Field       | ThmSD     | ThmtoMon  | ThmLDO_LSW | UVLOLDO2  | – | – | – | – |
| Reset       | 0         |           | 0          | 0         | – | – | – | – |
| Access Type | Read Only | Read Only | Read Only  | Read Only | – | – | – | – |

| BITFIELD   | BITS | DESCRIPTION                                                                                                                                                       |
|------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ThmSD      | 7    | Status of Charger and Limiter Thermal Shutdown<br>0 = Charger and Limiter operating normally<br>1 = Charger and Limiter in thermal shutdown                       |
| ThmtoMon   | 6    | Status of the One-Shot THM Monitor<br>0 = MON MUX under manual control<br>1 = MON MUX performing one-shot THM measurement                                         |
| ThmLDO_LSW | 5    | Status of LDO1, LDO2, LDO3, LSW1, LSW2 Thermal Shutdown<br>0 = All the above blocks are operating normally<br>1 = One of the above blocks is in thermal shutdown. |
| UVLOLDO2   | 4    | Status of LDO2 UVLO<br>0 = LDO2 operating normally<br>1 = LDO2 UVLO active                                                                                        |

**Status3 (0x05)**

| BIT         | 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Field       | BBstFault | BBstUVLO  | SysBatLim | ChgSysLim | StepChg   | ThmBk1    | ThmBk2    | ThmBk3    |
| Reset       |           |           | 0         | 0         | 0         | 0         | 0         | 0         |
| Access Type | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only |

| BITFIELD  | BITS | DESCRIPTION                                                                                                                                                                               |
|-----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BBstFault | 7    | Status of Buck-Boost Fault<br>0 = Buck-Boost operating normally<br>1 = Buck-Boost under fault condition                                                                                   |
| BBstUVLO  | 6    | Status of Buck-Boost UVLO<br>0 = Buck-Boost operating normally<br>1 = Buck-Boost UVLO active                                                                                              |
| SysBatLim | 5    | Status of SYS Regulation Current Limit<br>0 = Charge current is not being actively reduced to regulate SYS collapse<br>1 = Charge current actively being reduced to regulate SYS collapse |
| ChgSysLim | 4    | Status of CHGIN Regulation Current Limit<br>0 = Input current limit normal<br>1 = Input current limit being reduced to regulate CHGIN collapse                                            |
| StepChg   | 3    | Status of Charger Step Charge<br>0 = Charger is not in step-charging mode<br>1 = Charger is in step-charging mode (fast-charge current reduction)                                         |
| ThmBk1    | 2    | Status of Buck1 Thermal Shutdown<br>0 = Buck1 operating normally<br>1 = Buck1 in thermal shutdown                                                                                         |
| ThmBk2    | 1    | Status of Buck2 Thermal Shutdown<br>0 = Buck2 operating normally<br>1 = Buck2 in thermal shutdown                                                                                         |
| ThmBk3    | 0    | Status of Buck3 Thermal Shutdown<br>0 = Buck3 operating normally<br>1 = Buck3 in thermal shutdown                                                                                         |

**Int0 (0x06)**

| BIT         | 7                  | 6                  | 5                  | 4                  | 3                  | 2                  | 1                  | 0                  |
|-------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| Field       | ThmStatInt         | ChgStatInt         | ILimInt            | UsbOVPInt          | UsbOkInt           | ChgJEITA<br>SDInt  | ChgJEITA<br>RegInt | ChgTmoInt          |
| Reset       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  |
| Access Type | Read Clears<br>All | Read Clears<br>All | Read Clears<br>All | Read Clears<br>All | Read Clears<br>All | Read Clears<br>All | Read Clears<br>All | Read Clears<br>All |

| BITFIELD       | BITS | DESCRIPTION                               |
|----------------|------|-------------------------------------------|
| ThmStatInt     | 7    | Change in ThmStat caused an interrupt     |
| ChgStatInt     | 6    | Change in ChgStat caused an interrupt     |
| ILimInt        | 5    | Input current limit caused an interrupt   |
| UsbOVPInt      | 4    | Change in UsbOVP caused an interrupt      |
| UsbOkInt       | 3    | Change in UsbOk caused an interrupt       |
| ChgJEITASDInt  | 2    | Change in ChgJEITASD caused an interrupt  |
| ChgJEITARegInt | 1    | Change in ChgJEITAReg caused an interrupt |
| ChgTmoInt      | 0    | Change in ChgTmo caused an interrupt      |

**Int1 (0x07)**

| BIT                | 7               | 6           | 5               | 4               | 3 | 2 | 1               | 0               |
|--------------------|-----------------|-------------|-----------------|-----------------|---|---|-----------------|-----------------|
| <b>Field</b>       | ThmSDInt        | ThmtoMonInt | ThmLDO_ LSWInt  | UVLOL DO2Int    | – | – | LSW1 Tmolnt     | LSW2 Tmolnt     |
| <b>Reset</b>       | 0               |             | 0               | 0               | – | – | 0               | 0               |
| <b>Access Type</b> | Read Clears All | Read Only   | Read Clears All | Read Clears All | – | – | Read Clears All | Read Clears All |

| BITFIELD       | BITS | DESCRIPTION                                  |
|----------------|------|----------------------------------------------|
| ThmSDInt       | 7    | Change in ThmSD caused an interrupt          |
| ThmtoMonInt    | 6    | Change in ThmtoMon caused an interrupt       |
| ThmLDO_ LSWInt | 5    | Change in ThmLDO_ LSW caused an interrupt    |
| UVLOLDO2Int    | 4    | Change in UVLOLDO2 caused an interrupt       |
| LSW1Tmolnt     | 1    | LSW1 failed to startup during timeout period |
| LSW2Tmolnt     | 0    | LSW2 failed to startup during timeout period |

**Int2 (0x08)**

| BIT                | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |
|--------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| <b>Field</b>       | BBstFaultInt    | BBstU VLOInt    | SYSBat LimInt   | ChgSys LimInt   | StepChgInt      | ThmBk1Int       | ThmBk2Int       | ThmBk3Int       |
| <b>Reset</b>       |                 |                 | 0b0             | 0b0             | 0b0             | 0b0             | 0b0             | 0b0             |
| <b>Access Type</b> | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All |

| BITFIELD     | BITS | DESCRIPTION                             |
|--------------|------|-----------------------------------------|
| BBstFaultInt | 7    | Change in BBstFault caused an interrupt |
| BBstUVLOInt  | 6    | Change in BBstUVLO caused an interrupt  |
| SYSBatLimInt | 5    | Change in SysBatLim caused an interrupt |
| ChgSysLimInt | 4    | Change in ChgSysLim caused an interrupt |
| StepChgInt   | 3    | Change in StepChg caused an interrupt   |
| ThmBk1Int    | 2    | Change in ThmBk1 caused an interrupt    |
| ThmBk2Int    | 1    | Change in ThmBk2 caused an interrupt    |
| ThmBk3Int    | 0    | Change in ThmBk3 caused an interrupt    |

**IntMask0 (0x09)**

| BIT         | 7           | 6           | 5           | 4           | 3           | 2              | 1               | 0           |
|-------------|-------------|-------------|-------------|-------------|-------------|----------------|-----------------|-------------|
| Field       | ThmStatIntM | ChgStatIntM | ILimIntM    | UsbOVPIntM  | UsbOkIntM   | ChgJEITASDIntM | ChgJEITARegIntM | ChgTmolIntM |
| Reset       | 0           | 0           | 0           | 0           | 0           | 0              | 0               | 0           |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read    | Write, Read     | Write, Read |

| BITFIELD        | BITS | DESCRIPTION                                                                                                     |
|-----------------|------|-----------------------------------------------------------------------------------------------------------------|
| ThmStatIntM     | 7    | ThmStatIntM masks the ThmStatInt interrupt in the Int0 register (0x06).<br>0 = Masked<br>1 = Not masked         |
| ChgStatIntM     | 6    | ChgStatIntM masks the ChgStatInt interrupt in the Int0 register (0x06).<br>0 = Masked<br>1 = Not masked         |
| ILimIntM        | 5    | ILimIntM masks the ILimInt interrupt in the Int0 register (0x06).<br>0 = Masked<br>1 = Not masked               |
| UsbOVPIntM      | 4    | UsbOVPIntM masks the UsbOVPInt interrupt in the Int0 register (0x06).<br>0 = Masked<br>1 = Not masked           |
| UsbOkIntM       | 3    | UsbOkIntM masks the UsbOkInt interrupt in the Int0 register (0x06).<br>0 = Masked<br>1 = Not masked             |
| ChgJEITASDIntM  | 2    | ChgThmSDIntM masks the ChgThmSDInt interrupt in the Int0 register (0x06).<br>0 = Masked<br>1 = Not masked       |
| ChgJEITARegIntM | 1    | ChgJEITARegIntM masks the ChgJEITARegInt interrupt in the Int0 register (0x06).<br>0 = Masked<br>1 = Not masked |
| ChgTmolIntM     | 0    | ChgTmolIntM masks the ChgTmolInt interrupt in the Int0 register (0x06).<br>0 = Masked<br>1 = Not masked         |

**IntMask1 (0x0A)**

| BIT         | 7           | 6            | 5              | 4            | 3 | 2 | 1           | 0           |
|-------------|-------------|--------------|----------------|--------------|---|---|-------------|-------------|
| Field       | ThmSDIntM   | ThmtoMonIntM | ThmLDO_LSWIntM | UVLOLDO2IntM | – | – | LSW1TmolntM | LSW2TmolntM |
| Reset       | 0           |              | 0              | 0            | – | – | 0           | 0           |
| Access Type | Write, Read | Write, Read  | Write, Read    | Write, Read  | – | – | Write, Read | Write, Read |

| BITFIELD       | BITS | DESCRIPTION                                                                                                   |
|----------------|------|---------------------------------------------------------------------------------------------------------------|
| ThmSDIntM      | 7    | ThmSDIntM masks the ThmSDInt interrupt in the Int1 register (0x07).<br>0 = Masked<br>1 = Not masked           |
| ThmtoMonIntM   | 6    | ThmtoMonIntM masks the ThmtoMonInt interrupt in the Int1 register (0x07).<br>0 = Masked<br>1 = Not masked     |
| ThmLDO_LSWIntM | 5    | ThmLDO_LSWIntM masks the ThmLDO_LSWInt interrupt in the Int1 register (0x07).<br>0 = Masked<br>1 = Not masked |
| UVLOLDO2IntM   | 4    | UVLOLDO2IntM masks the UVLOLDO2Int interrupt in the Int1 register (0x07).<br>0 = Masked<br>1 = Not masked     |
| LSW1TmolntM    | 1    | LSW1TmolntM masks the LSW1Tmolnt interrupt in the Int1 register (0x07).<br>0 = Masked<br>1 = Not masked       |
| LSW2TmolntM    | 0    | LSW2TmolntM masks the LSW2Tmolnt interrupt in the Int1 register (0x07).<br>0 = Masked<br>1 = Not masked       |

**IntMask2 (0x0B)**

| BIT         | 7 | 6 | 5             | 4             | 3           | 2           | 1           | 0           |
|-------------|---|---|---------------|---------------|-------------|-------------|-------------|-------------|
| Field       | – | – | SysBatLimIntM | ChgSysLimIntM | StepChgIntM | ThmBk1IntM  | ThmBk2IntM  | ThmBk3IntM  |
| Reset       | – | – | 0             | 0             | 0           | 0           | 0           | 0           |
| Access Type | – | – | Write, Read   | Write, Read   | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD      | BITS | DESCRIPTION                                                                                                 |
|---------------|------|-------------------------------------------------------------------------------------------------------------|
| SysBatLimIntM | 5    | SysBatLimIntM masks the SysBatLimInt interrupt in the Int2 register (0x08).<br>0 = Masked<br>1 = Not masked |
| ChgSysLimIntM | 4    | ChgSysLimIntM masks the ChgSysLimInt interrupt in the Int2 register (0x08).<br>0 = Masked<br>1 = Not masked |
| StepChgIntM   | 3    | StepChgIntM masks the StepChgInt interrupt in the Int2 register (0x08).<br>0 = Masked<br>1 = Not masked     |
| ThmBk1IntM    | 2    | ThmBk1IntM masks the ThmBk1Int interrupt in the Int2 register (0x08).<br>0 = Masked<br>1 = Not masked       |
| ThmBk2IntM    | 1    | ThmBk2IntM masks the ThmBk2Int interrupt in the Int2 register (0x08).<br>0 = Masked<br>1 = Not masked       |
| ThmBk3IntM    | 0    | ThmBk3IntM masks the ThmBk3Int interrupt in the Int2 register (0x08).<br>0 = Masked<br>1 = Not masked       |

**ILimCntl (0x0C)**

| BIT         | 7           | 6 | 5 | 4              | 3 | 2             | 1 | 0 |
|-------------|-------------|---|---|----------------|---|---------------|---|---|
| Field       | SysMin[2:0] |   |   | ILimBlank[1:0] |   | ILimCntl[2:0] |   |   |
| Reset       |             |   |   |                |   |               |   |   |
| Access Type | Write, Read |   |   | Write, Read    |   | Write, Read   |   |   |

| BITFIELD  | BITS | DESCRIPTION                                                                                                                                                                                                                        |
|-----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SysMin    | 7:5  | System Voltage Minimum Threshold<br>Voltage below which charging current is reduced to prevent SYS from collapsing<br>000 = 3.6V<br>001 = 3.7V<br>010 = 3.8V<br>011 = 3.9V<br>100 = 4.0V<br>101 = 4.1V<br>110 = 4.2V<br>111 = 4.3V |
| ILimBlank | 4:3  | CHGIN Current Limiter Blanking Time<br>00 = No debounce (allow a few clock cycles for resampling)<br>01 = 0.5ms<br>10 = 1ms<br>11 = 10ms                                                                                           |
| ILimCntl  | 2:0  | CHGIN Programmable Input Current Limit<br>000 = 50mA<br>001 = 90mA<br>010 = 150mA<br>011 = 200mA<br>100 = 300mA<br>101 = 400mA<br>110 = 450mA<br>111 = 1000mA                                                                      |

**ChgCntl0 (0x0D)**

| BIT         | 7 | 6             | 5 | 4           | 3 | 2 | 1 | 0           |
|-------------|---|---------------|---|-------------|---|---|---|-------------|
| Field       | – | BatReChg[1:0] |   | BatReg[3:0] |   |   |   | ChgEn       |
| Reset       | – |               |   |             |   |   |   |             |
| Access Type | – | Write, Read   |   | Write, Read |   |   |   | Write, Read |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                |
|----------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BatReChg | 6:5  | Recharge Threshold in Relation to BatReg[3:0]<br>00 = BatReg - 70mV<br>01 = BatReg - 120mV<br>10 = BatReg - 170mV<br>11 = BatReg - 220mV                                                                                   |
| BatReg   | 4:1  | Battery Regulation Voltage<br>0000 = 4.05V<br>0001 = 4.10V<br>0010 = 4.15V<br>0011 = 4.20V<br>0100 = 4.25V<br>0101 = 4.30V<br>0110 = 4.35V<br>0111 = 4.40V<br>1000 = 4.45V<br>1001 = 4.50V<br>1010 = 4.55V<br>1011 = 4.60V |
| ChgEn    | 0    | On/Off Control for Charger<br>Does not affect SYS node<br>0 = Charger Disabled<br>1 = Charger Enabled                                                                                                                      |

**ChgCntl1 (0x0E)**

| BIT         | 7 | 6           | 5 | 4 | 3           | 2 | 1             | 0 |
|-------------|---|-------------|---|---|-------------|---|---------------|---|
| Field       | – | VPChg[2:0]  |   |   | IPChg[1:0]  |   | IChgDone[1:0] |   |
| Reset       | – |             |   |   |             |   |               |   |
| Access Type | – | Write, Read |   |   | Write, Read |   | Write, Read   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                            |
|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VPChg    | 6:4  | Precharge Voltage Threshold Setting<br>000 = 2.10V<br>001 = 2.25V<br>010 = 2.40V<br>011 = 2.55V<br>100 = 2.70V<br>101 = 2.85V<br>110 = 3.00V<br>111 = 3.15V            |
| IPChg    | 3:2  | Precharge Current Setting<br>00 = 0.05 x I <sub>FCHG</sub><br>01 = 0.1 x I <sub>FCHG</sub><br>10 = 0.2 x I <sub>FCHG</sub><br>11 = 0.3 x I <sub>FCHG</sub>             |
| IChgDone | 1:0  | Charge Done Current Threshold Setting<br>00 = 0.05 x I <sub>FCHG</sub><br>01 = 0.1 x I <sub>FCHG</sub><br>10 = 0.2 x I <sub>FCHG</sub><br>11 = 0.3 x I <sub>FCHG</sub> |

**ChgTmr (0x0F)**

| BIT         | 7           | 6            | 5             | 4 | 3            | 2 | 1            | 0 |
|-------------|-------------|--------------|---------------|---|--------------|---|--------------|---|
| Field       | ChgAutoStp  | ChgAutoReSta | MtChgTmr[1:0] |   | FChgTmr[1:0] |   | PChgTmr[1:0] |   |
| Reset       |             |              |               |   |              |   |              |   |
| Access Type | Write, Read | Write, Read  | Write, Read   |   | Write, Read  |   | Write, Read  |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                                                       |
|--------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ChgAutoStp   | 7    | Charger Auto-Stop<br>Controls the Transition from Maintain Charge to Maintain Charge Done. See <a href="#">Figure 4</a> .<br>0 = Auto-Stop Disabled<br>1 = Auto-Stop Enabled                                                                                                      |
| ChgAutoReSta | 6    | Charger Auto-Restart Control<br>See <a href="#">Figure 4</a> .<br>0 = Charger Remains in Maintain Charge Done even when V <sub>BAT</sub> is Less than Charger Restart Threshold<br>1 = Charger Automatically Restarts when V <sub>BAT</sub> Drops Below Charger Restart Threshold |
| MtChgTmr     | 5:4  | Maintain Charge Timer Setting<br>00 = 0min<br>01 = 15min<br>10 = 30min<br>11 = 60min                                                                                                                                                                                              |
| FChgTmr      | 3:2  | Fast Charge Timer Setting<br>00 = 75min<br>01 = 150min<br>10 = 300min<br>11 = 600min                                                                                                                                                                                              |
| PChgTmr      | 1:0  | Precharge Timer Setting<br>00 = 30min<br>01 = 60min<br>10 = 120min<br>11 = 240min                                                                                                                                                                                                 |

**StepChgCfg0 (0x10)**

| BIT         | 7 | 6                | 5 | 4 | 3                | 2 | 1 | 0 |
|-------------|---|------------------|---|---|------------------|---|---|---|
| Field       | – | ChgStepHyst[2:0] |   |   | ChgStepRise[3:0] |   |   |   |
| Reset       | – |                  |   |   |                  |   |   |   |
| Access Type | – | Write, Read      |   |   | Write, Read      |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                   |
|-------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ChgStepHyst | 6:4  | Step Charge Voltage Threshold Hysteresis<br>000 = 100mV<br>001 = 200mV<br>010 = 300mV<br>011 = 400mV<br>100 = 500mV<br>101 = 600mV<br>11x = Reserved                                                                                                                                          |
| ChgStepRise | 3:0  | Step Charge Voltage Threshold<br>0000 = 3.80V<br>0001 = 3.85V<br>0010 = 3.90V<br>0011 = 3.95V<br>0100 = 4.00V<br>0101 = 4.05V<br>0110 = 4.10V<br>0111 = 4.15V<br>1000 = 4.20V<br>1001 = 4.25V<br>1010 = 4.30V<br>1011 = 4.35V<br>1100 = 4.40V<br>1101 = 4.45V<br>1110 = 4.50V<br>1111 = 4.55V |

**StepChgCfg1 (0x11)**

| BIT         | 7 | 6 | 5 | 4 | 3 | 2             | 1 | 0 |
|-------------|---|---|---|---|---|---------------|---|---|
| Field       | – | – | – | – | – | ChgIStep[2:0] |   |   |
| Reset       | – | – | – | – | – |               |   |   |
| Access Type | – | – | – | – | – | Write, Read   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|----------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ChgIStep | 2:0  | Step Charge Current Scaling<br>Sets the modified Fast Charge current once the Step Charge Threshold is exceeded. The Fast Charge current is the minimum of the value set by ChgIStep and the applicable JEITA current scaling register (0x12, 0x13, or 0x14).<br>000 = 0.2 x I <sub>FCHG</sub><br>001 = 0.3 x I <sub>FCHG</sub><br>010 = 0.4 x I <sub>FCHG</sub><br>011 = 0.5 x I <sub>FCHG</sub><br>100 = 0.6 x I <sub>FCHG</sub><br>101 = 0.7 x I <sub>FCHG</sub><br>110 = 0.8 x I <sub>FCHG</sub><br>111 = 1.0 x I <sub>FCHG</sub> |

**ThmCfg0 (0x12)**

| BIT         | 7           | 6 | 5 | 4               | 3 | 2              | 1 | 0 |
|-------------|-------------|---|---|-----------------|---|----------------|---|---|
| Field       | ThmEn[2:0]  |   |   | CoolBatReg[1:0] |   | CoolIFChg[2:0] |   |   |
| Reset       |             |   |   | 11              |   | 111            |   |   |
| Access Type | Write, Read |   |   | Write, Read     |   | Write, Read    |   |   |

| BITFIELD   | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                         |
|------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ThmEn      | 7:5  | Charger Thermal Monitor Control<br>000 = Thermal monitoring disabled<br>001 = Charging enabled in the cool and room temperature regions<br>010 = Charging enabled in the room and warm temperature regions<br>011 = Charging enabled in the cool, room and warm temperature regions<br>1xx = Reserved                                                                               |
| CoolBatReg | 4:3  | Cool Zone Battery Regulation Voltage<br>Sets the modified BatReg[3:0] in the Cool Temperature Zone<br>00 = BatReg - 150mV<br>01 = BatReg - 100mV<br>10 = BatReg - 50mV<br>11 = BatReg                                                                                                                                                                                               |
| CoolIFChg  | 2:0  | Cool Zone Fast Charge Current Scaling<br>Sets the modified Fast Charge current in the Cool Temperature Zone<br>000 = 0.2 x I <sub>FCHG</sub><br>001 = 0.3 x I <sub>FCHG</sub><br>010 = 0.4 x I <sub>FCHG</sub><br>011 = 0.5 x I <sub>FCHG</sub><br>100 = 0.6 x I <sub>FCHG</sub><br>101 = 0.7 x I <sub>FCHG</sub><br>110 = 0.8 x I <sub>FCHG</sub><br>111 = 1.0 x I <sub>FCHG</sub> |

**ThmCfg1 (0x13)**

| BIT         | 7 | 6 | 5 | 4               | 3 | 2              | 1 | 0 |
|-------------|---|---|---|-----------------|---|----------------|---|---|
| Field       | – | – | – | RoomBatReg[1:0] |   | RoomIFChg[2:0] |   |   |
| Reset       | – | – | – | 11              |   | 111            |   |   |
| Access Type | – | – | – | Write, Read     |   | Write, Read    |   |   |

| BITFIELD   | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                         |
|------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RoomBatReg | 4:3  | Room Zone Battery Regulation Voltage<br>Sets the modified BatReg[3:0] in the Room Temperature Zone<br>00 = BatReg - 150mV<br>01 = BatReg - 100mV<br>10 = BatReg - 50mV<br>11 = BatReg                                                                                                                                                                                               |
| RoomIFChg  | 2:0  | Room Zone Fast Charge Current Scaling<br>Sets the modified Fast Charge current in the Room Temperature Zone<br>000 = 0.2 x I <sub>FCHG</sub><br>001 = 0.3 x I <sub>FCHG</sub><br>010 = 0.4 x I <sub>FCHG</sub><br>011 = 0.5 x I <sub>FCHG</sub><br>100 = 0.6 x I <sub>FCHG</sub><br>101 = 0.7 x I <sub>FCHG</sub><br>110 = 0.8 x I <sub>FCHG</sub><br>111 = 1.0 x I <sub>FCHG</sub> |

**ThmCfg2 (0x14)**

| BIT         | 7 | 6 | 5 | 4               | 3 | 2              | 1 | 0 |
|-------------|---|---|---|-----------------|---|----------------|---|---|
| Field       | – | – | – | WarmBatReg[1:0] |   | WarmIFChg[2:0] |   |   |
| Reset       | – | – | – | 11              |   | 111            |   |   |
| Access Type | – | – | – | Write, Read     |   | Write, Read    |   |   |

| BITFIELD   | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                     |
|------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| WarmBatReg | 4:3  | Warm Zone Battery Regulation Voltage<br>Sets the modified BatReg[3:0] in the Warm Temperature Zone<br>00 = BatReg - 150mV<br>01 = BatReg - 100mV<br>10 = BatReg - 50mV<br>11 = BatReg                                                                                                                                                                                           |
| WarmIFChg  | 2:0  | Warm Zone Fast Charge Current Scaling<br>Sets Modified Fast Charge Current in the Warm Temperature Zone<br>000 = 0.2 x I <sub>FCHG</sub><br>001 = 0.3 x I <sub>FCHG</sub><br>010 = 0.4 x I <sub>FCHG</sub><br>011 = 0.5 x I <sub>FCHG</sub><br>100 = 0.6 x I <sub>FCHG</sub><br>101 = 0.7 x I <sub>FCHG</sub><br>110 = 0.8 x I <sub>FCHG</sub><br>111 = 1.0 x I <sub>FCHG</sub> |

**MONCfg (0x15)**

| BIT         | 7 | 6                | 5 | 4           | 3            | 2 | 1 | 0 |
|-------------|---|------------------|---|-------------|--------------|---|---|---|
| Field       | – | MONRatioCfg[1:0] |   | MonHiZ      | MONCntl[3:0] |   |   |   |
| Reset       | – | 00               |   | 1           | 0000         |   |   |   |
| Access Type | – | Write, Read      |   | Write, Read | Write, Read  |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                     |
|-------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MONRatioCfg | 6:5  | IVMON Resistive Partition Selector<br>00 = 1:1<br>01 = 2:1<br>10 = 3:1<br>11 = 4:1                                                                                                                                                                                                                                                              |
| MonHiZ      | 4    | IVMON Pin Off Mode Condition<br>0 = Pulled Low by 59kΩ (typ) pulldown resistor<br>1 = Hi-Z                                                                                                                                                                                                                                                      |
| MONCntl     | 3:0  | IVMON Multiplexer Input Source Selection<br>0000 = Off Mode<br>0001 = Charger Current (buffered version of V <sub>ISET</sub> )<br>0010 = BAT<br>0011 = SYS<br>0100 = BK1OUT<br>0101 = BK2OUT<br>0110 = BK3OUT<br>0111 = L1OUT<br>1000 = L2OUT<br>1001 = L3OUT<br>1010 = BBOUT<br>1011 = THM<br>1100 = TPU<br>1101 = Reserved<br>111x = Reserved |

**Buck1Cfg (0x16)**

| BIT         | 7             | 6 | 5 | 4            | 3 | 2                | 1 | 0           |
|-------------|---------------|---|---|--------------|---|------------------|---|-------------|
| Field       | Buck1Seq[2:0] |   |   | Buck1En[1:0] |   | Buck1IZCSet[1:0] |   | Buck1PsvDsc |
| Reset       |               |   |   |              |   |                  |   | 1           |
| Access Type | Read Only     |   |   | Write, Read  |   | Write, Read      |   | Write, Read |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                       |
|-------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck1Seq    | 7:5  | Buck1 Enable Configuration<br>000 = Disabled<br>001 = Reserved<br>010 = Enabled at 0% of Boot/POR Process Delay Control<br>011 = Enabled at 25% of Boot/POR Process Delay Control<br>100 = Enabled at 50% of Boot/POR Process Delay Control<br>101 = Reserved<br>110 = Reserved<br>111 = Controlled by Buck1En [1:0] after 100% of Boot/POR Process Delay Control |
| Buck1En     | 4:3  | Buck1 Enable Configuration (effective only when Buck1Seq = 111)<br>00 = Disabled: BK1OUT not actively discharged unless Hard-Reset/Shut-down/Off mode<br>01 = Enabled<br>10 = Controlled by MPC_ (See Buck1MPC_ bits in register 0x19)<br>11 = Reserved                                                                                                           |
| Buck1IZCSet | 2:1  | Buck1 Zero Crossing Current Threshold<br>Optimizes Buck1 for a given voltage setting.<br>00 = 10mA, Use for Buck1VSet < 1V<br>01 = 20mA, Use for 1V ≤ Buck1VSet < 1.8V<br>10 = 30mA, Use for 1.8V ≤ Buck1VSet < 3V<br>11 = 40mA, Use for Buck1VSet ≥ 3V                                                                                                           |
| Buck1PsvDsc | 0    | Buck1 Passive Discharge Control<br>0 = Buck1 passively discharged only in Hard-Reset<br>1 = Buck1 passively discharged in Hard-Reset or Enable Low                                                                                                                                                                                                                |

**Buck1VSet (0x17)**

| BIT         | 7           | 6           | 5              | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|----------------|---|---|---|---|---|
| Field       | Buck1LowEMI | Buck1RampEn | Buck1VSet[5:0] |   |   |   |   |   |
| Reset       | 0           | 1           |                |   |   |   |   |   |
| Access Type | Write, Read | Write, Read | Write, Read    |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                         |
|-------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck1LowEMI | 7    | Buck1 Low EMI Mode<br>0 = Normal operation<br>1 = Increase rise/fall time on BK1LX by 3x                                                                                                                            |
| Buck1RampEn | 6    | Buck1 Ramp Enable<br>0 = Voltage setting transition is performed without intermediate steps<br>1 = Voltage setting transition to a higher value is performed with incremental steps every 20μs                      |
| Buck1VSet   | 5:0  | Buck1 Output Voltage Setting<br>0.7V to (63 x Bk1Step), linear scale, increments of Bk1Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk1Step = 10mV:<br>000000 = 0.7V<br>000001 = 0.71V<br>...<br>111111 = 1.33V |

**Buck1ISet (0x18)**

| BIT         | 7            | 6            | 5           | 4             | 3              | 2 | 1 | 0 |
|-------------|--------------|--------------|-------------|---------------|----------------|---|---|---|
| Field       | Buck1IAdptEn | Buck1SftStrt | Buck1ActDsc | Buck1FETScale | Buck1ISet[3:0] |   |   |   |
| Reset       | 1            |              | 0           |               |                |   |   |   |
| Access Type | Write, Read  | Write, Read  | Write, Read | Write, Read   | Write, Read    |   |   |   |

| BITFIELD      | BITS | DESCRIPTION                                                                                                                                                                                                                                         |
|---------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck1IAdptEn  | 7    | Buck1 Adaptive Peak Current Mode<br>0 = Inductor peak current fixed at the programmed value by means of Buck1ISet<br>1 = Inductor peak current automatically increased to provide better load regulation                                            |
| Buck1SftStrt  | 6    | Buck1 Soft-Start Time<br>Buck1 has reduced current capability during soft-start<br>0 = 50ms<br>1 = 5ms                                                                                                                                              |
| Buck1ActDsc   | 5    | Buck1 Active Discharge Control<br>0 = Buck1 actively discharged only in Hard-Reset<br>1 = Buck1 actively discharged in Hard-Reset or Enable Low                                                                                                     |
| Buck1FETScale | 4    | Buck1 Force FET Scaling<br>Reduce the FET size by a factor of two. Used to optimize the efficiency when Buck1ISet must be < 100mA (e.g., to mitigate noise at low frequencies).<br>0 = FET scaling disabled<br>1 = FET scaling enabled              |
| Buck1ISet     | 3:0  | Buck1 Inductor Peak Current Setting<br>For the best efficiency, use = between 150mA and 200mA. Linear scale, 25mA increments, settings below 75mA can be limited by the minimum t <sub>ON</sub><br>0000 = 0mA<br>0001 = 25mA<br>...<br>1111 = 375mA |

**Buck1Ctr (0x19)**

| BIT         | 7 | 6                | 5 | 4 | 3           | 2           | 1           | 0           |
|-------------|---|------------------|---|---|-------------|-------------|-------------|-------------|
| Field       | – | Buck1DVSCfg[2:0] |   |   | Buck1MPC3   | Buck1MPC2   | Buck1MPC1   | Buck1MPC0   |
| Reset       | – | 000              |   |   | 0           | 0           | 0           | 1           |
| Access Type | – | Write, Read      |   |   | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck1DVSCfg | 6:4  | Buck1 DVS Configuration<br>000 = Disabled<br>001 = DVS Mode 1 Enabled, Buck1 DVS controlled by MPC0 and MPC1<br>010 = DVS Mode 1 Enabled, Buck1 DVS controlled by MPC0 and MPC2<br>011 = DVS Mode 1 Enabled, Buck1 DVS controlled by MPC0 and MPC3<br>100 = DVS Mode 1 Enabled, Buck1 DVS controlled by MPC1 and MPC2<br>101 = DVS Mode 1 Enabled, Buck1 DVS controlled by MPC1 and MPC3<br>110 = DVS Mode 1 Enabled, Buck1 DVS controlled by MPC2 and MPC3<br>111 = DVS Mode 2 Enabled (SPI: MPC0 is $\overline{CS}$ , MPC1 is SCLK, MPC2 is DIN.) |
| Buck1MPC3   | 3    | Buck1 MPC3 Enable Control<br>Only valid when Buck1Seq = 111 and Buck1En = 10. If multiple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs.<br>0 = MPC3 does not control Buck1<br>1 = Buck1 controlled by MPC3                                                                                                                                                                                                                                                                                                                  |
| Buck1MPC2   | 2    | Buck1 MPC2 Enable Control<br>Only valid when Buck1Seq = 111 and Buck1En = 10. If multiple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs.<br>0 = MPC2 does not control Buck1<br>1 = Buck1 controlled by MPC2                                                                                                                                                                                                                                                                                                                  |
| Buck1MPC1   | 1    | Buck1 MPC1 Enable Control<br>Only valid when Buck1Seq = 111 and Buck1En = 10. If multiple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs.<br>0 = MPC1 does not control Buck1<br>1 = Buck1 controlled by MPC1                                                                                                                                                                                                                                                                                                                  |
| Buck1MPC0   | 0    | Buck1 MPC0 Enable Control<br>Only valid when Buck1Seq = 111 and Buck1En = 10. If multiple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs.<br>0 = MPC0 does not control Buck1<br>1 = Buck1 controlled by MPC0                                                                                                                                                                                                                                                                                                                  |

**Buck1DVSCfg0 (0x1A)**

| BIT         | 7 | 6 | 5                 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------------|---|---|---|---|---|
| Field       | – | – | Buck1DVSVIt0[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00              |   |   |   |   |   |
| Access Type | – | – | Write, Read       |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                             |
|--------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck1DVSVIt0 | 5:0  | Buck1 Alternate Output Voltage Setting 1 (Controlling MPCs = 00)<br>0.7V to (63 x Bk1Step), linear scale, increments of Bk1Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk1Step = 10mV:<br>000000 = 0.7V<br>000001 = 0.71V<br>...<br>111111 = 1.33V |

**Buck1DVSCfg1 (0x1B)**

| BIT         | 7 | 6 | 5                 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------------|---|---|---|---|---|
| Field       | – | – | Buck1DVSVIt1[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00              |   |   |   |   |   |
| Access Type | – | – | Write, Read       |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                             |
|--------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck1DVSVIt1 | 5:0  | Buck1 Alternate Output Voltage Setting 2 (Controlling MPCs = 01)<br>0.7V to (63 x Bk1Step), linear scale, increments of Bk1Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk1Step = 10mV:<br>000000 = 0.7V<br>000001 = 0.71V<br>...<br>111111 = 1.33V |

**Buck1DVSCfg2 (0x1C)**

| BIT         | 7 | 6 | 5                 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------------|---|---|---|---|---|
| Field       | – | – | Buck1DVSVIt2[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00              |   |   |   |   |   |
| Access Type | – | – | Write, Read       |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                             |
|--------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck1DVSVIt2 | 5:0  | Buck1 Alternate Output Voltage Setting 1 (Controlling MPCs = 10)<br>0.7V to (63 x Bk1Step), linear scale, increments of Bk1Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk1Step = 10mV:<br>000000 = 0.7V<br>000001 = 0.71V<br>...<br>111111 = 1.33V |

**Buck1DVSCfg3 (0x1D)**

| BIT         | 7 | 6 | 5                 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------------|---|---|---|---|---|
| Field       | – | – | Buck1DVSVIt3[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00              |   |   |   |   |   |
| Access Type | – | – | Write, Read       |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                             |
|--------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck1DVSVIt3 | 5:0  | Buck1 Alternate Output Voltage Setting 1 (Controlling MPCs = 11)<br>0.7V to (63 x Bk1Step), linear scale, increments of Bk1Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk1Step = 10mV:<br>000000 = 0.7V<br>000001 = 0.71V<br>...<br>111111 = 1.33V |

**Buck1DVSSPI (0x1E)**

| BIT         | 7 | 6 | 5                | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|------------------|---|---|---|---|---|
| Field       | – | – | Buck1SPIVIt[5:0] |   |   |   |   |   |
| Reset       | – | – |                  |   |   |   |   |   |
| Access Type | – | – | Read Only        |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                   |
|-------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck1SPIVIt | 5:0  | Buck1 SPI DVS Readback<br>0.7V to (63 x Bk1Step), linear scale, increments of Bk1Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk1Step = 10mV:<br>000000 = 0.7V<br>000001 = 0.71V<br>...<br>111111 = 1.33V |

**Buck2Cfg (0x1F)**

| BIT         | 7             | 6 | 5 | 4            | 3 | 2                | 1 | 0           |
|-------------|---------------|---|---|--------------|---|------------------|---|-------------|
| Field       | Buck2Seq[2:0] |   |   | Buck2En[1:0] |   | Buck2IZCSet[1:0] |   | Buck2PsvDsc |
| Reset       |               |   |   |              |   |                  |   | 0b1         |
| Access Type | Read Only     |   |   | Write, Read  |   | Write, Read      |   | Write, Read |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                       |
|-------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck2Seq    | 7:5  | Buck2 Enable Configuration<br>000 = Disabled<br>001 = Reserved<br>010 = Enabled at 0% of Boot/POR Process Delay Control<br>011 = Enabled at 25% of Boot/POR Process Delay Control<br>100 = Enabled at 50% of Boot/POR Process Delay Control<br>101 = Reserved<br>110 = Reserved<br>111 = Controlled by Buck2En [1:0] after 100% of Boot/POR Process Delay Control |
| Buck2En     | 4:3  | Buck2 Enable Configuration (effective only when Buck2Seq = 111)<br>00 = Disabled: BK2OUT not actively discharged unless Hard-Reset/Shut-down/Off mode<br>01 = Enabled<br>10 = Controlled by MPC_ (See Buck2MPC_ bits in register 0x22)<br>11 = Reserved                                                                                                           |
| Buck2IZCSet | 2:1  | Buck2 Zero Crossing Current Threshold<br>Optimizes Buck2 for a given voltage setting.<br>00 = 10mA, Use for Buck2VSet < 1V<br>01 = 20mA, Use for 1V ≤ Buck2VSet < 1.8V<br>10 = 30mA, Use for 1.8V ≤ Buck2VSet < 3V<br>11 = 40mA, Use for Buck2Vset ≥ 3V                                                                                                           |
| Buck2PsvDsc | 0    | Buck2 Passive Discharge Control<br>0 = Buck2 passively discharged only in Hard-Reset<br>1 = Buck2 passively discharged in Hard-Reset or Enable Low                                                                                                                                                                                                                |

**Buck2VSet (0x20)**

| BIT         | 7           | 6           | 5              | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|----------------|---|---|---|---|---|
| Field       | Buck2LowEMI | Buck2RampEn | Buck2VSet[5:0] |   |   |   |   |   |
| Reset       | 0b0         | 0b1         |                |   |   |   |   |   |
| Access Type | Write, Read | Write, Read | Write, Read    |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                           |
|-------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck2LowEMI | 7    | Buck2 Low EMI Mode<br>0 = Normal operation<br>1 = Increase rise/fall time on BK2LX by 3x                                                                                                                              |
| Buck2RampEn | 6    | Buck2 Ramp Enable<br>0 = Voltage setting transition is performed without intermediate steps<br>1 = Voltage setting transition to a higher value is performed with incremental steps every 20μs                        |
| Buck2VSet   | 5:0  | Buck2 Output Voltage Setting<br>0.7V to (63 x Bk2Step), linear scale, increments of Bk2Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk2Step = 25mV:<br>000000 = 0.7V<br>000001 = 0.725V<br>...<br>111111 = 2.275V |

**Buck2ISet (0x21)**

| BIT         | 7            | 6            | 5           | 4                 | 3              | 2 | 1 | 0 |
|-------------|--------------|--------------|-------------|-------------------|----------------|---|---|---|
| Field       | Buck2IAdptEn | Buck2SftStrt | Buck2ActDsc | Buck2<br>FETScale | Buck2ISet[3:0] |   |   |   |
| Reset       | 0b1          |              | 0b0         |                   |                |   |   |   |
| Access Type | Write, Read  | Write, Read  | Write, Read | Write, Read       | Write, Read    |   |   |   |

| BITFIELD      | BITS | DESCRIPTION                                                                                                                                                                                                                                             |
|---------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck2IAdptEn  | 7    | Buck2 Adaptive Peak Current Mode<br>0 = Inductor peak current fixed at the programmed value by means of Buck2ISet<br>1 = Inductor peak current automatically increased to provide better load regulation                                                |
| Buck2SftStrt  | 6    | Buck2 Soft-Start Time<br>Buck2 has reduced current capability during soft-start<br>0 = 50ms<br>1 = 5ms                                                                                                                                                  |
| Buck2ActDsc   | 5    | Buck2 Active Discharge Control<br>0 = Buck2 actively discharged only in Hard-Reset<br>1 = Buck2 actively discharged in Hard-Reset or Enable Low                                                                                                         |
| Buck2FETScale | 4    | Buck2 Force FET Scaling<br>Reduce the FET size by a factor of two. Used to optimize the efficiency when Buck2ISet must be < 100mA (e.g., to mitigate noise at low frequencies).<br>0 = FET scaling disabled<br>1 = FET scaling enabled                  |
| Buck2ISet     | 3:0  | Buck2 Inductor Peak Current Setting<br>For the best efficiency, use Buck2ISet = 150mA and 200mA. Linear scale, 25mA increments, settings below 75mA might be limited by the minimum t <sub>ON</sub><br>0000 = 0mA<br>0001 = 25mA<br>...<br>1111 = 375mA |

**Buck2Ctr (0x22)**

| BIT         | 7 | 6                | 5 | 4 | 3           | 2           | 1           | 0           |
|-------------|---|------------------|---|---|-------------|-------------|-------------|-------------|
| Field       | – | Buck2DVSCfg[2:0] |   |   | Buck2MPC3   | Buck2MPC2   | Buck2MPC1   | Buck2MPC0   |
| Reset       | – | 000              |   |   | 0           | 0           | 1           | 0           |
| Access Type | – | Write, Read      |   |   | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck2DVSCfg | 6:4  | <p>Buck2 DVS Configuration</p> <p>000 = Disabled</p> <p>001 = DVS Mode 1 Enabled, Buck2 DVS controlled by MPC0 and MPC1</p> <p>010 = DVS Mode 1 Enabled, Buck2 DVS controlled by MPC0 and MPC2</p> <p>011 = DVS Mode 1 Enabled, Buck2 DVS controlled by MPC0 and MPC3</p> <p>100 = DVS Mode 1 Enabled, Buck2 DVS controlled by MPC1 and MPC2</p> <p>101 = DVS Mode 1 Enabled, Buck2 DVS controlled by MPC1 and MPC3</p> <p>110 = DVS Mode 1 Enabled, Buck2 DVS controlled by MPC2 and MPC3</p> <p>111 = DVS Mode 2 Enabled (SPI: MPC0 is <math>\overline{CS}</math>, MPC1 is SCLK, MPC2 is DIN.)</p> |
| Buck2MPC3   | 3    | <p>Buck2 MPC3 Enable Control</p> <p>Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs.</p> <p>0 = MPC3 does not control Buck2</p> <p>1 = Buck2 controlled by MPC3</p>                                                                                                                                                                                                                                                                                                                                                |
| Buck2MPC2   | 2    | <p>Buck2 MPC2 Enable Control</p> <p>Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs.</p> <p>0 = MPC2 does not control Buck2</p> <p>1 = Buck2 controlled by MPC2</p>                                                                                                                                                                                                                                                                                                                                                |
| Buck2MPC1   | 1    | <p>Buck2 MPC1 Enable Control</p> <p>Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs.</p> <p>0 = MPC1 does not control Buck2</p> <p>1 = Buck2 controlled by MPC1</p>                                                                                                                                                                                                                                                                                                                                                |
| Buck2MPC0   | 0    | <p>Buck2 MPC0 Enable Control</p> <p>Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs.</p> <p>0 = MPC0 does not control Buck2</p> <p>1 = Buck2 controlled by MPC0</p>                                                                                                                                                                                                                                                                                                                                                |

**Buck2DVSCfg0 (0x23)**

| BIT         | 7 | 6 | 5                 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------------|---|---|---|---|---|
| Field       | – | – | Buck2DVSVIt0[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00              |   |   |   |   |   |
| Access Type | – | – | Write, Read       |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                               |
|--------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck2DVSVIt0 | 5:0  | Buck2 Alternate Output Voltage Setting 1 (Controlling MPCs = 00)<br>0.7V to (63 x Bk2Step), linear scale, increments of Bk2Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk2Step = 25mV:<br>000000 = 0.7V<br>000001 = 0.725V<br>...<br>111111 = 2.275V |

**Buck2DVSCfg1 (0x24)**

| BIT         | 7 | 6 | 5                 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------------|---|---|---|---|---|
| Field       | – | – | Buck2DVSVIt1[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00              |   |   |   |   |   |
| Access Type | – | – | Write, Read       |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                               |
|--------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck2DVSVIt1 | 5:0  | Buck2 Alternate Output Voltage Setting 2 (Controlling MPCs = 01)<br>0.7V to (63 x Bk2Step), linear scale, increments of Bk2Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk2Step = 25mV:<br>000000 = 0.7V<br>000001 = 0.725V<br>...<br>111111 = 2.275V |

**Buck2DVSCfg2 (0x25)**

| BIT         | 7 | 6 | 5                 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------------|---|---|---|---|---|
| Field       | – | – | Buck2DVSVIt2[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00              |   |   |   |   |   |
| Access Type | – | – | Write, Read       |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                               |
|--------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck2DVSVIt2 | 5:0  | Buck2 Alternate Output Voltage Setting 3 (Controlling MPCs = 10)<br>0.7V to (63 x Bk2Step), linear scale, increments of Bk2Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk2Step = 25mV:<br>000000 = 0.7V<br>000001 = 0.725V<br>...<br>111111 = 2.275V |

**Buck2DVSCfg3 (0x26)**

| BIT         | 7 | 6 | 5                 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------------|---|---|---|---|---|
| Field       | – | – | Buck2DVSVIt3[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00              |   |   |   |   |   |
| Access Type | – | – | Write, Read       |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                               |
|--------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck2DVSVIt3 | 5:0  | Buck2 Alternate Output Voltage Setting 4 (Controlling MPCs = 11)<br>0.7V to (63 x Bk2Step), linear scale, increments of Bk2Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk2Step = 25mV:<br>000000 = 0.7V<br>000001 = 0.725V<br>...<br>111111 = 2.275V |

**Buck2DVSSPI (0x27)**

| BIT         | 7 | 6 | 5                | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|------------------|---|---|---|---|---|
| Field       | – | – | Buck2SPIVIt[5:0] |   |   |   |   |   |
| Reset       | – | – |                  |   |   |   |   |   |
| Access Type | – | – | Read Only        |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                     |
|-------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck2SPIVIt | 5:0  | Buck2 SPI DVS Readback<br>0.7V to (63 x Bk2Step), linear scale, increments of Bk2Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk2Step = 25mV:<br>000000 = 0.7V<br>000001 = 0.725V<br>...<br>111111 = 2.275V |

**Buck3Cfg (0x28)**

| BIT         | 7             | 6 | 5 | 4            | 3 | 2                | 1 | 0           |
|-------------|---------------|---|---|--------------|---|------------------|---|-------------|
| Field       | Buck3Seq[2:0] |   |   | Buck3En[1:0] |   | Buck3IZCSet[1:0] |   | Buck3PsvDsc |
| Reset       |               |   |   |              |   |                  |   | 0b1         |
| Access Type | Read Only     |   |   | Write, Read  |   | Write, Read      |   | Write, Read |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                       |
|-------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck3Seq    | 7:5  | Buck3 Enable Configuration<br>000 = Disabled<br>001 = Reserved<br>010 = Enabled at 0% of Boot/POR Process Delay Control<br>011 = Enabled at 25% of Boot/POR Process Delay Control<br>100 = Enabled at 50% of Boot/POR Process Delay Control<br>101 = Reserved<br>110 = Reserved<br>111 = Controlled by Buck3En [1:0] after 100% of Boot/POR Process Delay Control |
| Buck3En     | 4:3  | Buck3 Enable Configuration (effective only when Buck3Seq = 111)<br>00 = Disabled: BK3OUT not actively discharged unless Hard-Reset/Shut-down/Off mode<br>01 = Enabled<br>10 = Controlled by MPC_ (See Buck3MPC_ bits in register 0x2B)<br>11 = Reserved                                                                                                           |
| Buck3IZCSet | 2:1  | Buck3 Zero Crossing Current Threshold<br>Optimizes Buck3 for a given voltage setting.<br>00 = 10mA, Use for Buck3VSet < 1V<br>01 = 20mA, Use for 1V ≤ Buck3VSet < 1.8V<br>10 = 30mA, Use for 1.8V ≤ Buck3VSet < 3V<br>11 = 40mA, Use for Buck3Vset ≥ 3V                                                                                                           |
| Buck3PsvDsc | 0    | Buck3 Passive Discharge Control<br>0 = Buck3 passively discharged only in Hard-Reset<br>1 = Buck3 passively discharged in Hard-Reset or Enable Low                                                                                                                                                                                                                |

**Buck3VSet (0x29)**

| BIT         | 7           | 6           | 5              | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|----------------|---|---|---|---|---|
| Field       | Buck3LowEMI | Buck3RampEn | Buck3VSet[5:0] |   |   |   |   |   |
| Reset       | 0b0         | 0b1         |                |   |   |   |   |   |
| Access Type | Write, Read | Write, Read | Write, Read    |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                         |
|-------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck3LowEMI | 7    | Buck3 Low EMI Mode<br>0 = Normal operation<br>1 = Increase rise/fall time on BK3LX by 3x                                                                                                                            |
| Buck3RampEn | 6    | Buck3 Ramp Enable<br>0 = Voltage setting transition is performed without intermediate steps<br>1 = Voltage setting transition to a higher value is performed with incremental steps every 20μs                      |
| Buck3VSet   | 5:0  | Buck3 Output Voltage Setting<br>0.7V to (63 x Bk3Step), linear scale, increments of Bk3Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk3Step = 50mV:<br>000000 = 0.7V<br>000001 = 0.75V<br>...<br>111111 = 3.85V |

**Buck1Set[7:0]**

| BIT         | 7           | 6            | 5           | 4                 | 3              | 2 | 1 | 0 |
|-------------|-------------|--------------|-------------|-------------------|----------------|---|---|---|
| Field       | Buck3AdptEn | Buck3SftStrt | Buck3ActDsc | Buck3<br>FETScale | Buck3ISet[3:0] |   |   |   |
| Reset       | 0b1         |              | 0b0         |                   |                |   |   |   |
| Access Type | Write, Read | Write, Read  | Write, Read | Write, Read       | Write, Read    |   |   |   |

| BITFIELD      | BITS | DESCRIPTION                                                                                                                                                                                                                                 |
|---------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck3AdptEn   | 7    | Buck3 Adaptive Peak Current Mode<br>0 = Inductor peak current fixed at the programmed value by means of Buck3I-Set<br>1 = Inductor peak current automatically increased to provide better load regulation                                   |
| Buck3SftStrt  | 6    | Buck3 Soft-Start Time<br>Buck3 has reduced current capability during soft-start<br>0 = 50ms<br>1 = 5ms                                                                                                                                      |
| Buck3ActDsc   | 5    | Buck3 Active Discharge Control<br>0 = Buck3 actively discharged only in Hard-Reset<br>1 = Buck3 actively discharged in Hard-Reset or Enable Low                                                                                             |
| Buck3FETScale | 4    | Buck3 Force FET Scaling<br>Reduce the FET size by a factor of two. Used to optimize the efficiency when Buck3ISet must be < 100mA (e.g., to mitigate noise at low frequencies).<br>0 = FET scaling disabled<br>1 = FET scaling enabled      |
| Buck3ISet     | 3:0  | Buck3 Inductor Peak Current Setting<br>For the best efficiency, use Buck3ISet = 150mA. Linear scale, 25mA increments, settings below 75mA may be limited by the minimum t <sub>ON</sub><br>0000 = 0mA<br>0001 = 25mA<br>...<br>1111 = 375mA |

**Buck1Set[7:0]**

| BIT         | 7 | 6                | 5 | 4 | 3           | 2           | 1           | 0           |
|-------------|---|------------------|---|---|-------------|-------------|-------------|-------------|
| Field       | – | Buck3DVSCfg[2:0] |   |   | Buck3MPC3   | Buck3MPC2   | Buck3MPC1   | Buck3MPC0   |
| Reset       | – | 000              |   |   | 0           | 1           | 0           | 0           |
| Access Type | – | Write, Read      |   |   | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck3DVSCfg | 6:4  | Buck3 DVS Configuration<br>000 = Disabled<br>001 = DVS Mode 1 Enabled, Buck3 DVS controlled by MPC0 and MPC1<br>010 = DVS Mode 1 Enabled, Buck3 DVS controlled by MPC0 and MPC2<br>011 = DVS Mode 1 Enabled, Buck3 DVS controlled by MPC0 and MPC3<br>100 = DVS Mode 1 Enabled, Buck3 DVS controlled by MPC1 and MPC2<br>101 = DVS Mode 1 Enabled, Buck3 DVS controlled by MPC1 and MPC3<br>110 = DVS Mode 1 Enabled, Buck3 DVS controlled by MPC2 and MPC3<br>111 = DVS Mode 2 Enabled (SPI: MPC0 is $\overline{CS}$ , MPC1 is SCLK, MPC2 is DIN.) |
| Buck3MPC3   | 3    | Buck3 MPC3 Enable Control<br>Only valid when Buck3Seq = 111 and Buck3En = 10. If multiple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs.<br>0 = MPC3 does not control Buck3<br>1 = Buck3 controlled by MPC3                                                                                                                                                                                                                                                                                                                  |
| Buck3MPC2   | 2    | Buck3 MPC2 Enable Control<br>Only valid when Buck3Seq = 111 and Buck3En = 10. If multiple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs.<br>0 = MPC2 does not control Buck3<br>1 = Buck3 controlled by MPC2                                                                                                                                                                                                                                                                                                                  |
| Buck3MPC1   | 1    | Buck3 MPC1 Enable Control<br>Only valid when Buck3Seq = 111 and Buck3En = 10. If multiple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs.<br>0 = MPC1 does not control Buck3<br>1 = Buck3 controlled by MPC1                                                                                                                                                                                                                                                                                                                  |
| Buck3MPC0   | 0    | Buck3 MPC0 Enable Control<br>Only valid when Buck3Seq = 111 and Buck3En = 10. If multiple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs.<br>0 = MPC0 does not control Buck3<br>1 = Buck3 controlled by MPC0                                                                                                                                                                                                                                                                                                                  |

**Buck3DVSCfg0 (0x2C)**

| BIT         | 7 | 6 | 5                 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------------|---|---|---|---|---|
| Field       | – | – | Buck3DVSVIt0[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00              |   |   |   |   |   |
| Access Type | – | – | Write, Read       |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                             |
|--------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck3DVSVIt0 | 5:0  | Buck3 Alternate Output Voltage Setting 1 (Controlling MPCs = 00)<br>0.7V to (63 x Bk3Step), linear scale, increments of Bk3Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk3Step = 50mV:<br>000000 = 0.7V<br>000001 = 0.75V<br>...<br>111111 = 3.85V |

**Buck3DVSCfg1 (0x2D)**

| BIT         | 7 | 6 | 5                 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------------|---|---|---|---|---|
| Field       | – | – | Buck3DVSVIt1[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00              |   |   |   |   |   |
| Access Type | – | – | Write, Read       |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                             |
|--------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck3DVSVIt1 | 5:0  | Buck3 Alternate Output Voltage Setting 2 (Controlling MPCs = 01)<br>0.7V to (63 x Bk3Step), linear scale, increments of Bk3Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk3Step = 50mV:<br>000000 = 0.7V<br>000001 = 0.75V<br>...<br>111111 = 3.85V |

**Buck3DVSCfg2 (0x2E)**

| BIT         | 7 | 6 | 5                 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------------|---|---|---|---|---|
| Field       | – | – | Buck3DVSVIt2[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00              |   |   |   |   |   |
| Access Type | – | – | Write, Read       |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                             |
|--------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck3DVSVIt2 | 5:0  | Buck3 Alternate Output Voltage Setting 3 (Controlling MPCs = 10)<br>0.7V to (63 x Bk3Step), linear scale, increments of Bk3Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk3Step = 50mV:<br>000000 = 0.7V<br>000001 = 0.75V<br>...<br>111111 = 3.85V |

**Buck3DVSCfg3 (0x2F)**

| BIT         | 7 | 6 | 5                 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------------|---|---|---|---|---|
| Field       | – | – | Buck3DVSVIt3[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00              |   |   |   |   |   |
| Access Type | – | – | Write, Read       |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                             |
|--------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck3DVSVIt3 | 5:0  | Buck3 Alternate Output Voltage Setting 4 (Controlling MPCs = 11)<br>0.7V to (63 x Bk3Step), linear scale, increments of Bk3Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk3Step = 50mV:<br>000000 = 0.7V<br>000001 = 0.75V<br>...<br>111111 = 3.85V |

**Buck3DVSSPI (0x30)**

| BIT         | 7 | 6 | 5                | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|------------------|---|---|---|---|---|
| Field       | – | – | Buck3SPIVIt[5:0] |   |   |   |   |   |
| Reset       | – | – |                  |   |   |   |   |   |
| Access Type | – | – | Read Only        |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                   |
|-------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Buck3SPIVIt | 5:0  | Buck3 SPI DVS Readback<br>0.7V to (63 x Bk3Step), linear scale, increments of Bk3Step. See <a href="#">Table 3</a> ,<br>e.g., for Bk3Step = 50mV:<br>000000 = 0.7V<br>000001 = 0.75V<br>...<br>111111 = 3.85V |

**BBstCfg0 (0x31)**

| BIT         | 7            | 6 | 5 | 4           | 3 | 2           | 1           | 0           |
|-------------|--------------|---|---|-------------|---|-------------|-------------|-------------|
| Field       | BBstSeq[2:0] |   |   | BBstEn[1:0] |   | BBstRampEn  | BBstMode    | BBstPsvDsc  |
| Reset       |              |   |   |             |   |             |             | 1           |
| Access Type | Read Only    |   |   | Write, Read |   | Write, Read | Write, Read | Write, Read |

| BITFIELD   | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                          |
|------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BBstSeq    | 7:5  | Buck-Boost Enable Configuration<br>000 = Disabled<br>001 = Reserved<br>010 = Enabled at 0% of Boot/POR Process Delay Control<br>011 = Enabled at 25% of Boot/POR Process Delay Control<br>100 = Enabled at 50% of Boot/POR Process Delay Control<br>101 = Reserved<br>110 = Reserved<br>111 = Controlled by BBstEn[1:0] after 100% of Boot/POR Process Delay Control |
| BBstEn     | 4:3  | Buck-Boost Enable Configuration (effective only when BBstSeq = 111)<br>00 = Disabled: BBOUT not actively discharged unless Hard-Reset/Shutdown/Off mode<br>01 = Enabled<br>10 = Controlled by MPC_ (See BBstMPC_ bits in register 0x34)<br>11 = Reserved                                                                                                             |
| BBstRampEn | 2    | Buck-Boost Ramp Enable<br>0 = Voltage setting transition is performed without intermediate steps<br>1 = Voltage setting transition to a higher value is performed with incremental steps every 20μs                                                                                                                                                                  |
| BBstMode   | 1    | Buck-Boost Operating Mode<br>0 = Buck-Boost<br>1 = Buck Only                                                                                                                                                                                                                                                                                                         |
| BBstPsvDsc | 0    | Buck-Boost Passive Discharge Control<br>0 = Buck-Boost passively discharged only in Hard-Reset<br>1 = Buck-Boost passively discharged in Hard-Reset or Enable Low                                                                                                                                                                                                    |

**BBstVSet (0x32)**

| BIT         | 7           | 6           | 5             | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|---------------|---|---|---|---|---|
| Field       | BBstLowEMI  | BBstActDsc  | BBstVSet[5:0] |   |   |   |   |   |
| Reset       | 0           | 0           |               |   |   |   |   |   |
| Access Type | Write, Read | Write, Read | Write, Read   |   |   |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                                                                                                                                                                                                                                        |
|------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BBstLowEMI | 7    | Buck-Boost Low EMI Mode<br>0 = Normal operation<br>1 = Increase rise/fall time on HVLX/LVLX by 3x                                                                                                                                                  |
| BBstActDsc | 6    | Buck-Boost Active Discharge Control<br>0 = Buck-Boost actively discharged only in Hard-Reset<br>1 = Buck-Boost actively discharged in Hard-Reset or Enable Low                                                                                     |
| BBstVSet   | 5:0  | Buck-Boost Output Voltage Setting<br>2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V <sub>BBOUT_UVLO</sub> and are not guaranteed<br>000000 = 2.5V<br>000001 = 2.55V<br>...<br>111100 = 5.5V<br>>111100 = N/A |

**BBstIPSet (0x33)**

| BIT         | 7               | 6 | 5 | 4 | 3               | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|-----------------|---|---|---|
| Field       | BBstIPSet2[3:0] |   |   |   | BBstIPSet1[3:0] |   |   |   |
| Reset       |                 |   |   |   |                 |   |   |   |
| Access Type | Write, Read     |   |   |   | Write, Read     |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BBstIPSet2 | 7:4  | <p>Buck-Boost nominal maximum peak current setting.<br/>See Buck-Boost Regulator section for a description of the peak current settings.<br/>0mA to 375mA, linear scale, 25mA increments, settings below 75mA may be limited by the minimum <math>t_{ON}</math>.<br/>0000 = BBstIPSet1 + 0mA<br/>0001 = BBstIPSet1 + 25mA<br/>...<br/>1111 = BBstIPSet1 + 375mA<br/>Recommended settings:<br/><math>V_{BBOUT} \leq 2.65V</math>: 250mA<br/><math>2.7V &lt; V_{BBOUT} \leq 3.05V</math>: 225mA<br/><math>3.1V &lt; V_{BBOUT} \leq 3.6V</math>: 200mA<br/><math>3.65V &lt; V_{BBOUT} \leq 4.35V</math>: 175mA<br/><math>V_{BBOUT} &gt; 4.4V</math>: 150mA</p>                                                                                                                                                                                                                                                                 |
| BBstIPSet1 | 3:0  | <p>Buck-Boost nominal peak current setting.<br/>Nominal peak current when charging inductor between <math>V_{IN}</math> and GND.<br/>See Buck-Boost Regulator section for a description of the peak current settings.<br/>0mA to 375mA, linear scale, 25mA increments, settings below 75mA may be limited by the minimum <math>t_{ON}</math><br/>0000 = 0mA)<br/>0001 = 25mA<br/>...<br/>1111 = 375mA<br/>Recommended settings:<br/><math>V_{BBOUT} \leq 2.65V</math>: 50mA<br/><math>2.7V &lt; V_{BBOUT} \leq 3.05V</math>: 75mA<br/><math>3.1V &lt; V_{BBOUT} \leq 3.4V</math>: 100mA<br/><math>3.45V &lt; V_{BBOUT} \leq 3.8V</math>: 125mA<br/><math>3.85V &lt; V_{BBOUT} \leq 4.15V</math>: 150mA<br/><math>4.2V &lt; V_{BBOUT} \leq 4.55V</math>: 175mA<br/><math>4.6V &lt; V_{BBOUT} \leq 4.9V</math>: 200mA<br/><math>4.95V &lt; V_{BBOUT} \leq 5.3V</math>: 225mA<br/><math>V_{BBOUT} &gt; 5.35V</math>: 250mA</p> |

**BBstCfg1 (0x34)**

| BIT         | 7             | 6           | 5           | 4            | 3 | 2 | 1              | 0 |
|-------------|---------------|-------------|-------------|--------------|---|---|----------------|---|
| Field       | BBstIPAdptDis | BBstFast    | BBZCCmpDis  | BBstFETScale | – | – | BBFHighSh[1:0] |   |
| Reset       | 0             |             |             |              | – | – |                |   |
| Access Type | Write, Read   | Write, Read | Write, Read | Write, Read  | – | – | Write, Read    |   |

| BITFIELD      | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                |
|---------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BBstIPAdptDis | 7    | Adaptive Peak/Valley Current Adjustment Enable<br>0 = Enabled<br>1 = Disabled, peak current fixed and is set by BBstIPSet1,2. Valley current is fixed to 0mA                                                                                                                                                                                                                               |
| BBstFast      | 6    | Buck-Boost Pre-Trigger Mode Setting<br>0 = Normal, low quiescent current operation<br>1 = Increased quiescent mode for fast load transient response. Quiescent current increased to 30μA.                                                                                                                                                                                                  |
| BBZCCmpDis    | 5    | Buck-Boost Zero-Crossing Comparator Disable<br>0 = Enable<br>1 = Disable                                                                                                                                                                                                                                                                                                                   |
| BBstFETScale  | 4    | Buck-Boost Force FET Scaling<br>Reduce the FET size by factor 2 to optimize the efficiency at light loads<br>0 = FET scaling disabled<br>1 = FET scaling enabled                                                                                                                                                                                                                           |
| BBFHighSh     | 1:0  | Buck-Boost f <sub>HIGH</sub> Thresholds<br>Selects the switching frequency threshold f <sub>HIGH</sub> . If f <sub>SW</sub> > f <sub>HIGH</sub> all the blocks are kept ON (I <sub>Q</sub> is higher). A small glitch on V <sub>BBOUT</sub> can be present at the f <sub>HIGH</sub> crossoverover.<br>00 = 25khz/6.125Khz<br>01 = 35Khz/8.25Khz<br>10 = 50khz/12.5Khz<br>11 = 100khz/25khz |

**BBstCtr (0x35)**

| BIT         | 7            | 6               | 5 | 4 | 3           | 2           | 1           | 0           |
|-------------|--------------|-----------------|---|---|-------------|-------------|-------------|-------------|
| Field       | BBstMP-C1FCT | BBstDVSCfg[2:0] |   |   | BBstMPC3    | BBstMPC2    | BBstMPC1    | BBstMPC0    |
| Reset       |              |                 |   |   | 1           | 0           | 0           | 0           |
| Access Type | Write, Read  | Write, Read     |   |   | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BBstMPC1FCT | 7    | Buck-Boost FAST mode enable by MPC1. Improves interoperability with MAX86170/171. Tie MPC1 to INT2 on MAX86170/171 if this mode will be used.<br>0 = FAST status controlled by BBstFast Register<br>1 = FAST mode controlled by MPC1.<br>MPC1 = 0: FAST disabled<br>MPC1 = 1: FAST enabled, I <sub>Q</sub> increased by 30μA                                                                                                                                                                                                                                             |
| BBstDVSCfg  | 6:4  | Buck-Boost DVS Configuration<br>000 = Disabled<br>001 = DVS Mode 1 Enabled, Buck-Boost DVS controlled by MPC0 and MPC1<br>010 = DVS Mode 1 Enabled, Buck-Boost DVS controlled by MPC0 and MPC2<br>011 = DVS Mode 1 Enabled, Buck-Boost DVS controlled by MPC0 and MPC3<br>100 = DVS Mode 1 Enabled, Buck-Boost DVS controlled by MPC1 and MPC2<br>101 = DVS Mode 1 Enabled, Buck-Boost DVS controlled by MPC1 and MPC3<br>110 = DVS Mode 1 Enabled, Buck-Boost DVS controlled by MPC2 and MPC3<br>111 = DVS Mode 2 Enabled (SPI: MPC0 is CS, MPC1 is SCLK, MPC2 is DIN.) |
| BBstMPC3    | 3    | Buck-Boost MPC3 Enable Control<br>Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs.<br>0 = MPC3 does not control Buck-Boost<br>1 = Buck-Boost controlled by MPC3                                                                                                                                                                                                                                                                                                                     |
| BBstMPC2    | 2    | Buck-Boost MPC2 Enable Control<br>Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs.<br>0 = MPC2 does not control Buck-Boost<br>1 = Buck-Boost controlled by MPC2                                                                                                                                                                                                                                                                                                                     |
| BBstMPC1    | 1    | Buck-Boost MPC1 Enable Control<br>Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs.<br>0 = MPC1 does not control Buck-Boost<br>1 = Buck-Boost controlled by MPC1                                                                                                                                                                                                                                                                                                                     |
| BBstMPC0    | 0    | Buck-Boost MPC0 Enable Control<br>Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, Buck-Boost is controlled by the logical OR of the MPCs.<br>0 = MPC0 does not control Buck-Boost<br>1 = Buck-Boost controlled by MPC0                                                                                                                                                                                                                                                                                                                     |

**BBstDVSCfg0 (0x36)**

| BIT         | 7 | 6 | 5                | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|------------------|---|---|---|---|---|
| Field       | – | – | BBstDVSVIt0[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00             |   |   |   |   |   |
| Access Type | – | – | Write, Read      |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                                                                                            |
|-------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BBstDVSVIt0 | 5:0  | Buck-Boost Alternate Output Voltage Setting 1 (Controlling MPCs = 00)<br>2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V <sub>BBOUT_UVLO</sub> and are not guaranteed<br>000000 = 2.5V<br>000001 = 2.55V<br>...<br>111100 = 5.5V<br>>111100 = N/A |

**BBstDVSCfg1 (0x37)**

| BIT         | 7 | 6 | 5                | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|------------------|---|---|---|---|---|
| Field       | – | – | BBstDVSVIt1[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00             |   |   |   |   |   |
| Access Type | – | – | Write, Read      |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                                                                                            |
|-------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BBstDVSVIt1 | 5:0  | Buck-Boost Alternate Output Voltage Setting 2 (Controlling MPCs = 01)<br>2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V <sub>BBOUT_UVLO</sub> and are not guaranteed<br>000000 = 2.5V<br>000001 = 2.55V<br>...<br>111100 = 5.5V<br>>111100 = N/A |

**BBstDVSCfg2 (0x38)**

| BIT         | 7 | 6 | 5                | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|------------------|---|---|---|---|---|
| Field       | – | – | BBstDVSVIt2[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00             |   |   |   |   |   |
| Access Type | – | – | Write, Read      |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                                                                                            |
|-------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BBstDVSVIt2 | 5:0  | Buck-Boost Alternate Output Voltage Setting 3 (Controlling MPCs = 10)<br>2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V <sub>BBOUT_UVLO</sub> and are not guaranteed<br>000000 = 2.5V<br>000001 = 2.55V<br>...<br>111100 = 5.5V<br>>111100 = N/A |

**BBstDVSCfg3 (0x39)**

| BIT         | 7 | 6 | 5                | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|------------------|---|---|---|---|---|
| Field       | – | – | BBstDVSVIt3[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x00             |   |   |   |   |   |
| Access Type | – | – | Write, Read      |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                                                                                            |
|-------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BBstDVSVIt3 | 5:0  | Buck-Boost Alternate Output Voltage Setting 4 (Controlling MPCs = 11)<br>2.6V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V <sub>BBOUT_UVLO</sub> and are not guaranteed<br>000000 = 2.5V<br>000001 = 2.55V<br>...<br>111100 = 5.5V<br>>111100 = N/A |

**BBstDVSSPI (0x3A)**

| BIT         | 7 | 6 | 5               | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-----------------|---|---|---|---|---|
| Field       | – | – | BBstSPIVIt[5:0] |   |   |   |   |   |
| Reset       | – | – |                 |   |   |   |   |   |
| Access Type | – | – | Read Only       |   |   |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                                                                                                                                                                                                                                  |
|------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BBstSPIVIt | 5:0  | Buck-Boost SPI DVS Readback<br>2.5V to 5.5V, Linear Scale, 50mV increments, codes below 000010 can interfere with V <sub>BBOUT_UVLO</sub> and are not guaranteed<br>000000 = 2.5V<br>000001 = 2.55V<br>...<br>111100 = 5.5V<br>>111100 = N/A |

**LDO1Cfg (0x3B)**

| BIT         | 7            | 6 | 5 | 4           | 3 | 2           | 1           | 0           |
|-------------|--------------|---|---|-------------|---|-------------|-------------|-------------|
| Field       | LDO1Seq[2:0] |   |   | LDO1En[1:0] |   | LDO1ActDsc  | LDO1Mode    | LDO1PsvDsc  |
| Reset       |              |   |   |             |   | 0           |             | 1           |
| Access Type | Read Only    |   |   | Write, Read |   | Write, Read | Write, Read | Write, Read |

| BITFIELD   | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDO1Seq    | 7:5  | LDO1 Enable Configuration (Read only)<br>000 = Disabled<br>001 = Enabled always when BAT/SYS is present<br>010 = Enabled at 0% of Boot/ POR Process Delay Control<br>011 = Enabled at 25% of Boot/ POR Process Delay Control<br>100 = Enabled at 50% of Boot/ POR Process Delay Control<br>101 = Reserved<br>110 = Reserved<br>111 = Controlled by LDO1En [1:0] after 100% of Boot/POR Process Delay Control |
| LDO1En     | 4:3  | LDO1 Enable Configuration (effective only when LDO1Seq = 111)<br>00 = Disabled<br>01 = Enabled<br>10 = Controlled by MPC_ (See LDO1MPC_ bits in register 0x3D)<br>11 = Reserved                                                                                                                                                                                                                              |
| LDO1ActDsc | 2    | LDO1 Active Discharge Control<br>0 = LDO1 output will be actively discharged only in Hard-Reset mode<br>1 = LDO1 output will be actively discharged in Hard-Reset mode and also when its Enable goes Low                                                                                                                                                                                                     |
| LDO1Mode   | 1    | LDO1 Mode Control<br>When FET is On, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled.<br>0 = Normal LDO operating mode<br>1 = Load switch mode. FET is either fully On or Off depending on state of LDO1En.                                                                                                                                       |
| LDO1PsvDsc | 0    | LDO1 Passive Discharge Control<br>0 = LDO1 output will be discharged only entering Off and Hard-Reset modes.<br>1 = LDO1 output will be discharged only entering Off and Hard-Reset modes and when the enable is Low                                                                                                                                                                                         |

**LDO1VSet (0x3C)**

| BIT         | 7 | 6 | 5 | 4             | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---------------|---|---|---|---|
| Field       | – | – | – | LDO1VSet[4:0] |   |   |   |   |
| Reset       | – | – | – |               |   |   |   |   |
| Access Type | – | – | – | Write, Read   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                    |
|----------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDO1VSet | 4:0  | LDO1 Output Voltage Setting<br>Limited by input supply.<br>0.8V to 3.6V, Linear Scale, 100mV increments<br>00000 = 0.8V<br>00001 = 0.9V<br>...<br>11100 = 3.6V<br>>11101 = N/A |

**LDO1Ctr (0x3D)**

| BIT         | 7 | 6 | 5 | 4 | 3           | 2           | 1           | 0           |
|-------------|---|---|---|---|-------------|-------------|-------------|-------------|
| Field       | – | – | – | – | LDO1MPC3    | LDO1MPC2    | LDO1MPC1    | LDO1MPC0    |
| Reset       | – | – | – | – | 0           | 0           | 0           | 1           |
| Access Type | – | – | – | – | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                  |
|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDO1MPC3 | 3    | LDO1 MPC3 Enable Control<br>Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs.<br>0 = MPC3 does not control LDO1<br>1 = LDO1 controlled by MPC3 |
| LDO1MPC2 | 2    | LDO1 MPC2 Enable Control<br>Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs.<br>0 = MPC2 does not control LDO1<br>1 = LDO1 controlled by MPC2 |
| LDO1MPC1 | 1    | LDO1 MPC1 Enable Control<br>Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs.<br>0 = MPC1 does not control LDO1<br>1 = LDO1 controlled by MPC1 |
| LDO1MPC0 | 0    | LDO1 MPC0 Enable Control<br>Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs.<br>0 = MPC0 does not control LDO1<br>1 = LDO1 controlled by MPC0 |

**LDO2Cfg (0x3E)**

| BIT         | 7            | 6 | 5 | 4           | 3 | 2           | 1           | 0           |
|-------------|--------------|---|---|-------------|---|-------------|-------------|-------------|
| Field       | LDO2Seq[2:0] |   |   | LDO2En[1:0] |   | LDO2ActDsc  | LDO2Mode    | LDO2PsvDsc  |
| Reset       |              |   |   |             |   | 0           |             | 1           |
| Access Type | Read Only    |   |   | Write, Read |   | Write, Read | Write, Read | Write, Read |

| BITFIELD   | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                    |
|------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDO2Seq    | 7:5  | LDO2 Enable Configuration (Read only)<br>000 = Disabled<br>001 = Reserved<br>010 = Enabled at 0% of Boot/ POR Process Delay Control<br>011 = Enabled at 25% of Boot/ POR Process Delay Control<br>100 = Enabled at 50% of Boot/ POR Process Delay Control<br>101 = Reserved<br>110 = Reserved<br>111 = Controlled by LDO2En [1:0] after 100% of Boot/POR Process Delay Control |
| LDO2En     | 4:3  | LDO2 Enable Configuration (effective only when LDO2Seq = 111)<br>00 = Disabled<br>01 = Enabled<br>10 = Controlled by MPC_ (See LDO2MPC_ bits in register 0x40)<br>11 = Reserved                                                                                                                                                                                                |
| LDO2ActDsc | 2    | LDO2 Active Discharge Control<br>0 = LDO2 output will be actively discharged only in Hard-Reset mode<br>1 = LDO2 output will be actively discharged in Hard-Reset mode and also when its Enable goes Low                                                                                                                                                                       |
| LDO2Mode   | 1    | LDO2 Mode Control<br>When FET is On, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled.<br>0 = Normal LDO operating mode<br>1 = Load switch mode. FET is either fully On or Off depending on state of LDO2En.                                                                                                         |
| LDO2PsvDsc | 0    | LDO2 Passive Discharge Control<br>0 = LDO2 output will be discharged only entering Off and Hard-Reset modes.<br>1 = LDO2 output will be discharged only entering Off and Hard-Reset modes and when the enable is Low                                                                                                                                                           |

**LDO2VSet (0x3F)**

| BIT         | 7 | 6 | 5 | 4             | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---------------|---|---|---|---|
| Field       | – | – | – | LDO2VSet[4:0] |   |   |   |   |
| Reset       | – | – | – |               |   |   |   |   |
| Access Type | – | – | – | Write, Read   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                |
|----------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDO2VSet | 4:0  | LDO2 Output Voltage Setting<br>Limited by input supply.<br>0.9V to 4V, Linear Scale, 100mV increments<br>000000 = 0.9V<br>000001 = 1V<br>...<br>11110 = 3.9V<br>11111 = 4V |

**LDO2Ctr (0x40)**

| BIT         | 7 | 6 | 5 | 4 | 3           | 2           | 1           | 0           |
|-------------|---|---|---|---|-------------|-------------|-------------|-------------|
| Field       | – | – | – | – | LDO2MPC3    | LDO2MPC2    | LDO2MPC1    | LDO2MPC0    |
| Reset       | – | – | – | – | 0           | 0           | 1           | 0           |
| Access Type | – | – | – | – | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                  |
|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDO2MPC3 | 3    | LDO2 MPC3 Enable Control<br>Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs.<br>0 = MPC3 does not control LDO2<br>1 = LDO2 controlled by MPC3 |
| LDO2MPC2 | 2    | LDO2 MPC2 Enable Control<br>Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs.<br>0 = MPC2 does not control LDO2<br>1 = LDO2 controlled by MPC2 |
| LDO2MPC1 | 1    | LDO2 MPC1 Enable Control<br>Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs.<br>0 = MPC1 does not control LDO2<br>1 = LDO2 controlled by MPC1 |
| LDO2MPC0 | 0    | LDO2 MPC0 Enable Control<br>Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs.<br>0 = MPC0 does not control LDO2<br>1 = LDO2 controlled by MPC0 |

**LDO3Cfg (0x41)**

| BIT         | 7            | 6 | 5 | 4           | 3 | 2           | 1           | 0           |
|-------------|--------------|---|---|-------------|---|-------------|-------------|-------------|
| Field       | LDO3Seq[2:0] |   |   | LDO3En[1:0] |   | LDO3ActDsc  | LDO3Mode    | LDO3PsvDsc  |
| Reset       |              |   |   |             |   | 0           |             | 1           |
| Access Type | Read Only    |   |   | Write, Read |   | Write, Read | Write, Read | Write, Read |

| BITFIELD   | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                    |
|------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDO3Seq    | 7:5  | LDO3 Enable Configuration (Read only)<br>000 = Disabled<br>001 = Reserved<br>010 = Enabled at 0% of Boot/ POR Process Delay Control<br>011 = Enabled at 25% of Boot/ POR Process Delay Control<br>100 = Enabled at 50% of Boot/ POR Process Delay Control<br>101 = Reserved<br>110 = Reserved<br>111 = Controlled by LDO3En [1:0] after 100% of Boot/POR Process Delay Control |
| LDO3En     | 4:3  | LDO3 Enable Configuration (effective only when LDO3Seq = 111)<br>00 = Disabled<br>01 = Enabled<br>10 = Controlled by MPC_ (See LDO3MPC_ bits in register 0x43)<br>11 = Reserved                                                                                                                                                                                                |
| LDO3ActDsc | 2    | LDO3 Active Discharge Control<br>0 = LDO3 output will be actively discharged only in Hard-Reset mode<br>1 = LDO3 output will be actively discharged in Hard-Reset mode and also when its Enable goes Low                                                                                                                                                                       |
| LDO3Mode   | 1    | LDO3 Mode Control<br>When FET is On, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled.<br>0 = Normal LDO operating mode<br>1 = Load switch mode. FET is either fully On or Off depending on state of LDO3En.                                                                                                         |
| LDO3PsvDsc | 0    | LDO3 Passive Discharge Control<br>0 = LDO3 output will be discharged only entering Off and Hard-Reset modes.<br>1 = LDO3 output will be discharged only entering Off and Hard-Reset modes and when the enable is Low                                                                                                                                                           |

**LDO3VSet (0x42)**

| BIT         | 7 | 6 | 5             | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---------------|---|---|---|---|---|
| Field       | – | – | LDO3VSet[5:0] |   |   |   |   |   |
| Reset       | – | – |               |   |   |   |   |   |
| Access Type | – | – | Write, Read   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                               |
|----------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDO3VSet | 5:0  | LDO3 Output Voltage Setting<br>Limited by input supply.<br>0.5V to 1.95V, Linear Scale, 25mV increments<br>000000 = 0.5V<br>000001 = 0.525V<br>...<br>111010 = 1.95V<br>>111010 = Limited by input supply |

**LDO3Ctr (0x43)**

| BIT         | 7            | 6            | 5 | 4 | 3           | 2           | 1           | 0           |
|-------------|--------------|--------------|---|---|-------------|-------------|-------------|-------------|
| Field       | LDO3_MPC0CNT | LDO3_MPC0CNF | – | – | LDO3MPC3    | LDO3MPC2    | LDO3MPC1    | LDO3MPC0    |
| Reset       | 0x0          | 0x0          | – | – | 0           | 1           | 0           | 0           |
| Access Type | Write, Read  | Write, Read  | – | – | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                  |
|--------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDO3_MPC0CNT | 7    | LDO3/MPC0 Control Bit<br>0 = MPC0 has no effect on the LDO3<br>1 = LDO3_MPC0CNF is valid and MPC0 function is enabled.                                                                                                       |
| LDO3_MPC0CNF | 6    | MPC0 configuration bit<br>0 = MPC0 controls LDO/SW mode of LDO3 (MPC0 = 0 ldo mode, MPC0 = 1 sw mode)<br>1 = MPC0 controls Enable of LDO3 (MPC0 = 0 disabled, MPC0 = 1 enabled in sw mode)                                   |
| LDO3MPC3     | 3    | LDO3 MPC3 Enable Control<br>Only valid when LDO3Seq = 111 and LDO3En = 10. If multiple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs.<br>0 = MPC3 does not control LDO3<br>1 = LDO3 controlled by MPC3 |
| LDO3MPC2     | 2    | LDO3 MPC2 Enable Control<br>Only valid when LDO3Seq = 111 and LDO3En = 10. If multiple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs.<br>0 = MPC2 does not control LDO3<br>1 = LDO3 controlled by MPC2 |
| LDO3MPC1     | 1    | LDO3 MPC1 Enable Control<br>Only valid when LDO3Seq = 111 and LDO3En = 10. If multiple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs.<br>0 = MPC1 does not control LDO3<br>1 = LDO3 controlled by MPC1 |
| LDO3MPC0     | 0    | LDO3 MPC0 Enable Control<br>Only valid when LDO3Seq = 111 and LDO3En = 10. If multiple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs.<br>0 = MPC0 does not control LDO3<br>1 = LDO3 controlled by MPC0 |

**LSW1Cfg (0x44)**

| BIT         | 7            | 6 | 5 | 4           | 3 | 2           | 1           | 0           |
|-------------|--------------|---|---|-------------|---|-------------|-------------|-------------|
| Field       | LSW1Seq[2:0] |   |   | LSW1En[1:0] |   | LSW1ActDsc  | LSW1Lowlq   | LSW1PsvDsc  |
| Reset       |              |   |   |             |   | 0           |             | 1           |
| Access Type | Read Only    |   |   | Write, Read |   | Write, Read | Write, Read | Write, Read |

| BITFIELD   | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                    |
|------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LSW1Seq    | 7:5  | LSW1 Enable Configuration (Read only)<br>000 = Disabled<br>001 = Reserved<br>010 = Enabled at 0% of Boot/ POR Process Delay Control<br>011 = Enabled at 25% of Boot/ POR Process Delay Control<br>100 = Enabled at 50% of Boot/ POR Process Delay Control<br>101 = Reserved<br>110 = Reserved<br>111 = Controlled by LSW1En [1:0] after 100% of Boot/POR Process Delay Control |
| LSW1En     | 4:3  | LSW1 Enable Configuration (effective only when LSW1Seq = 111)<br>00 = Disabled<br>01 = Enabled<br>10 = Controlled by MPC_ (See LSW1MPC_ bits in register 0x45)<br>11 = Reserved                                                                                                                                                                                                |
| LSW1ActDsc | 2    | LSW1 Active Discharge Control<br>0 = LSW1 output will be actively discharged only in Hard-Reset mode<br>1 = LSW1 output will be actively discharged in Hard-Reset mode and also when its Enable goes Low                                                                                                                                                                       |
| LSW1Lowlq  | 1    | LSW1 Low Quiescent<br>Low quiescent mode is achieved by disabling the voltage protection of LSW1.<br>0 = Voltage Protection Enabled<br>1 = Voltage Protection Disabled and quiescent is reduced                                                                                                                                                                                |
| LSW1PsvDsc | 0    | LSW1 Passive Discharge Control<br>0 = LSW1 output will be discharged only entering Off and Hard-Reset modes.<br>1 = LSW1 output will be discharged only entering Off and Hard-Reset modes and when the enable is Low                                                                                                                                                           |

**LSW1Ctr (0x45)**

| BIT         | 7 | 6 | 5 | 4 | 3           | 2           | 1           | 0           |
|-------------|---|---|---|---|-------------|-------------|-------------|-------------|
| Field       | – | – | – | – | LSW1MPC3    | LSW1MPC2    | LSW1MPC1    | LSW1MPC0    |
| Reset       | – | – | – | – |             |             |             |             |
| Access Type | – | – | – | – | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                  |
|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LSW1MPC3 | 3    | LSW1 MPC3 Enable Control<br>Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs.<br>0 = MPC3 does not control LSW1<br>1 = LSW1 controlled by MPC3 |
| LSW1MPC2 | 2    | LSW1 MPC2 Enable Control<br>Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs.<br>0 = MPC2 does not control LSW1<br>1 = LSW1 controlled by MPC2 |
| LSW1MPC1 | 1    | LSW1 MPC1 Enable Control<br>Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs.<br>0 = MPC1 does not control LSW1<br>1 = LSW1 controlled by MPC1 |
| LSW1MPC0 | 0    | LSW1 MPC0 Enable Control<br>Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs.<br>0 = MPC0 does not control LSW1<br>1 = LSW1 controlled by MPC0 |

**LSW2Cfg (0x46)**

| BIT         | 7            | 6 | 5 | 4           | 3 | 2           | 1           | 0           |
|-------------|--------------|---|---|-------------|---|-------------|-------------|-------------|
| Field       | LSW2Seq[2:0] |   |   | LSW2En[1:0] |   | LSW2ActDsc  | LSW2Lowlq   | LSW2PsvDsc  |
| Reset       |              |   |   |             |   | 0           |             | 1           |
| Access Type | Read Only    |   |   | Write, Read |   | Write, Read | Write, Read | Write, Read |

| BITFIELD   | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                    |
|------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LSW2Seq    | 7:5  | LSW2 Enable Configuration (Read only)<br>000 = Disabled<br>001 = Reserved<br>010 = Enabled at 0% of Boot/ POR Process Delay Control<br>011 = Enabled at 25% of Boot/ POR Process Delay Control<br>100 = Enabled at 50% of Boot/ POR Process Delay Control<br>101 = Reserved<br>110 = Reserved<br>111 = Controlled by LSW2En [1:0] after 100% of Boot/POR Process Delay Control |
| LSW2En     | 4:3  | LSW2 Enable Configuration (effective only when LSW2Seq = 111)<br>00 = Disabled<br>01 = Enabled<br>10 = Controlled by MPC_ (See LSW2MPC_ bits in register 0x47)<br>11 = Reserved                                                                                                                                                                                                |
| LSW2ActDsc | 2    | LSW2 Active Discharge Control<br>0 = LSW2 output will be actively discharged only in Hard-Reset mode<br>1 = LSW2 output will be actively discharged in Hard-Reset mode and also when its Enable goes Low                                                                                                                                                                       |
| LSW2Lowlq  | 1    | LSW2 Low Quiescent<br>Low quiescent mode is achieved by disabling the voltage protection of LSW2.<br>0 = Voltage Protection Enabled<br>1 = Voltage Protection Disabled and quiescent is reduced                                                                                                                                                                                |
| LSW2PsvDsc | 0    | LSW2 Passive Discharge Control<br>0 = LSW2 output will be discharged only entering Off and Hard-Reset modes.<br>1 = LSW2 output will be discharged only entering Off and Hard-Reset modes and when the enable is Low                                                                                                                                                           |

**LSW2Ctr (0x47)**

| BIT         | 7 | 6 | 5 | 4 | 3           | 2           | 1           | 0           |
|-------------|---|---|---|---|-------------|-------------|-------------|-------------|
| Field       | – | – | – | – | LSW2MPC3    | LSW2MPC2    | LSW2MPC1    | LSW2MPC0    |
| Reset       | – | – | – | – |             |             |             |             |
| Access Type | – | – | – | – | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                  |
|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LSW2MPC3 | 3    | LSW2 MPC3 Enable Control<br>Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs.<br>0 = MPC3 does not control LSW2<br>1 = LSW2 controlled by MPC3 |
| LSW2MPC2 | 2    | LSW2 MPC2 Enable Control<br>Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs.<br>0 = MPC2 does not control LSW2<br>1 = LSW2 controlled by MPC2 |
| LSW2MPC1 | 1    | LSW2 MPC1 Enable Control<br>Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs.<br>0 = MPC1 does not control LSW2<br>1 = LSW2 controlled by MPC1 |
| LSW2MPC0 | 0    | LSW2 MPC0 Enable Control<br>Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs.<br>0 = MPC0 does not control LSW2<br>1 = LSW2 controlled by MPC0 |

**MPC0Cfg (0x48)**

| BIT         | 7         | 6 | 5 | 4           | 3           | 2           | 1           | 0           |
|-------------|-----------|---|---|-------------|-------------|-------------|-------------|-------------|
| Field       | MPC0Pin   | – | – | MPC0Out     | MPC0OD      | MPC0HiZB    | MPC0Res     | MPC0Pup     |
| Reset       | 0         | – | – |             |             |             |             |             |
| Access Type | Read Only | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                            |
|----------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MPC0Pin  | 7    | MPC0 State<br>0 = MPC0 LOW<br>1 = MPC0 HIGH (if MPC0OD = 0) / Hi-Z (if MPC0OD = 1)                                                                                                     |
| MPC0Out  | 4    | MPC0 Output value<br>Valid only if MPC0 is configured as output (MPC0HiZB = 1)<br>0 = MPC0 connected to GND<br>1 = MPC0 open drain off (MPC0OD = 1) / connected to BK3OUT (MPC0OD = 0) |
| MPC0OD   | 3    | MPC0 Output Configuration<br>Valid only if MPC0 is configured as output (MPC0HiZB = 1)<br>0 = MPC0 is push-pull connected to BK3OUT<br>1 = MPC0 is open drain                          |
| MPC0HiZB | 2    | MPC0 Direction<br>0 = MPC0 is Hi-Z. Input buffer enabled<br>1 = MPC0 is not Hi-Z. Output buffer enabled                                                                                |
| MPC0Res  | 1    | MPC0 Resistor Presence<br>Valid only if MPC0 is configured as input (MPC0HiZB = 0)<br>0 = Resistor not connected to MPC0<br>1 = Resistor connected to MPC0                             |
| MPC0Pup  | 0    | MPC0 Resistor Configuration<br>Valid only if there is a resistor on MPC0 (MPC0Res = 1)<br>0 = Pulldown connected to MPC0<br>1 = Pullup to VCCINT connected MCP0                        |

**MPC1Cfg (0x49)**

| BIT         | 7         | 6 | 5 | 4           | 3           | 2           | 1           | 0           |
|-------------|-----------|---|---|-------------|-------------|-------------|-------------|-------------|
| Field       | MPC1Pin   | – | – | MPC1Out     | MPC1OD      | MPC1HiZB    | MPC1Res     | MPC1Pup     |
| Reset       | 0         | – | – |             |             |             |             |             |
| Access Type | Read Only | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                            |
|----------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MPC1Pin  | 7    | MPC1 State<br>0 = MPC1 LOW<br>1 = MPC1 HIGH (if MPC1OD = 0) / Hi-Z (if MPC1OD = 1)                                                                                                     |
| MPC1Out  | 4    | MPC1 Output value<br>Valid only if MPC1 is configured as output (MPC1HiZB = 1)<br>0 = MPC1 connected to GND<br>1 = MPC1 open drain off (MPC1OD = 1) / connected to BK3OUT (MPC1OD = 0) |
| MPC1OD   | 3    | MPC1 Output Configuration<br>Valid only if MPC1 is configured as output (MPC1HiZB = 1)<br>0 = MPC1 is push-pull connected to BK3OUT<br>1 = MPC1 is open drain                          |
| MPC1HiZB | 2    | MPC1 Direction<br>0 = MPC1 is Hi-Z. Input buffer enabled<br>1 = MPC1 is not Hi-Z. Output buffer enabled                                                                                |
| MPC1Res  | 1    | MPC1 Resistor Presence<br>Valid only if MPC1 is configured as input (MPC1HiZB = 0)<br>0 = Resistor not connected to MPC1<br>1 = Resistor connected to MPC1                             |
| MPC1Pup  | 0    | MPC1 Resistor Configuration<br>Valid only if there is a resistor on MPC1 (MPC1Res = 1)<br>0 = Pulldown connected to MPC1<br>1 = Pullup to VCCINT connected MCP1                        |

**MPC2Cfg (0x4A)**

| BIT         | 7         | 6 | 5 | 4           | 3           | 2           | 1           | 0           |
|-------------|-----------|---|---|-------------|-------------|-------------|-------------|-------------|
| Field       | MPC2Pin   | – | – | MPC2Out     | MPC2OD      | MPC2HiZB    | MPC2Res     | MPC2Pup     |
| Reset       | 0         | – | – |             |             |             |             |             |
| Access Type | Read Only | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                            |
|----------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MPC2Pin  | 7    | MPC2 State<br>0 = MPC2 LOW<br>1 = MPC2 HIGH (if MPC2OD = 0) / Hi-Z (if MPC2OD = 1)                                                                                                     |
| MPC2Out  | 4    | MPC2 Output value<br>Valid only if MPC2 is configured as output (MPC2HiZB = 1)<br>0 = MPC2 connected to GND<br>1 = MPC2 open drain off (MPC2OD = 1) / connected to BK3OUT (MPC2OD = 0) |
| MPC2OD   | 3    | MPC2 Output Configuration<br>Valid only if MPC2 is configured as output (MPC2HiZB = 1)<br>0 = MPC2 is push-pull connected to BK3OUT<br>1 = MPC2 is open drain                          |
| MPC2HiZB | 2    | MPC2 Direction<br>0 = MPC2 is Hi-Z. Input buffer enabled<br>1 = MPC2 is not Hi-Z. Output buffer enabled                                                                                |
| MPC2Res  | 1    | MPC2 Resistor Presence<br>Valid only if MPC2 is configured as input (MPC2HiZB = 0)<br>0 = Resistor not connected to MPC2<br>1 = Resistor connected to MPC2                             |
| MPC2Pup  | 0    | MPC2 Resistor Configuration<br>Valid only if there is a resistor on MPC2 (MPC2Res = 1)<br>0 = Pulldown connected to MPC2<br>1 = Pullup to VCCINT connected MCP2                        |

**MPC3Cfg (0x4B)**

| BIT         | 7         | 6 | 5 | 4           | 3           | 2           | 1           | 0           |
|-------------|-----------|---|---|-------------|-------------|-------------|-------------|-------------|
| Field       | MPC3Pin   | – | – | MPC3Out     | MPC3OD      | MPC3HiZB    | MPC3Res     | MPC3Pup     |
| Reset       | 0         | – | – |             |             |             |             |             |
| Access Type | Read Only | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                            |
|----------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MPC3Pin  | 7    | MPC3 State<br>0 = MPC3 LOW<br>1 = MPC3 HIGH (if MPC3OD = 0) / Hi-Z (if MPC3OD = 1)                                                                                                     |
| MPC3Out  | 4    | MPC3 Output value<br>Valid only if MPC3 is configured as output (MPC3HiZB = 1)<br>0 = MPC3 connected to GND<br>1 = MPC3 open drain off (MPC3OD = 1) / connected to BK3OUT (MPC3OD = 0) |
| MPC3OD   | 3    | MPC3 Output Configuration<br>Valid only if MPC3 is configured as output (MPC3HiZB = 1)<br>0 = MPC3 is push-pull connected to BK3OUT<br>1 = MPC3 is open drain                          |
| MPC3HiZB | 2    | MPC Direction<br>0 = MPC3 is Hi-Z. Input buffer enabled<br>1 = MPC3 is not Hi-Z. Output buffer enabled                                                                                 |
| MPC3Res  | 1    | MPC3 Resistor Presence<br>Valid only if MPC3 is configured as input (MPC3HiZB = 0)<br>0 = Resistor not connected to MPC3<br>1 = Resistor connected to MPC3                             |
| MPC3Pup  | 0    | MPC3 Resistor Configuration<br>Valid only if there is a resistor on MPC3 (MPC3Res = 1)<br>0 = Pulldown connected to MPC3<br>1 = Pullup to VCCINT connected MCP3                        |

**PFN (0x4C)**

| BIT         | 7 | 6 | 5 | 4 | 3 | 2 | 1         | 0         |
|-------------|---|---|---|---|---|---|-----------|-----------|
| Field       | – | – | – | – | – | – | PFN2Pin   | PFN1Pin   |
| Reset       | – | – | – | – | – | – |           |           |
| Access Type | – | – | – | – | – | – | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION                                              |
|----------|------|----------------------------------------------------------|
| PFN2Pin  | 1    | Status of PFN2<br>0 = PFN2 not active<br>1 = PFN2 active |
| PFN1Pin  | 0    | Status of PFN1<br>0 = PFN1 not active<br>1 = PFN1 active |

**BootCfg (0x4D)**

| BIT         | 7              | 6 | 5 | 4 | 3         | 2            | 1 | 0         |
|-------------|----------------|---|---|---|-----------|--------------|---|-----------|
| Field       | PwrRstCfg[3:0] |   |   |   | SftRstCfg | BootDly[1:0] |   | ChgAlwTry |
| Reset       |                |   |   |   |           |              |   |           |
| Access Type | Read Only      |   |   |   | Read Only | Read Only    |   | Read Only |

| BITFIELD  | BITS | DESCRIPTION                                                                                                                                                                        |
|-----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PwrRstCfg | 7:4  | Power Reset Configuration<br>Determines how the device turns on, off, and enters hard/soft reset. See Table 1 for PwrRstCfg values and their associated behaviors.                 |
| SftRstCfg | 3    | Soft-Reset Configuration<br>Indicates whether registers are held or reset to default during a soft-reset.<br>0 = Hold register contents<br>1 = Reset registers to default          |
| BootDly   | 2:1  | Boot Delay<br>The boot period when the sequencing engine turns on features with sequence bits 010, 011, and 100.<br>00 = 80ms<br>01 = 120ms<br>10 = 220ms<br>11 = 420ms            |
| ChgAlwTry | 0    | UVLO Automatic Retry<br>If a SYS UVLO condition occurs during the boot process<br>0 = Part latches off until CHGIN is removed and replaced<br>1 = Part retries to boot after delay |

**PwrCfg (0x4E)**

| BIT         | 7           | 6           | 5 | 4 | 3 | 2 | 1 | 0           |
|-------------|-------------|-------------|---|---|---|---|---|-------------|
| Field       | ThmtoMonEn  | ThmtoMonAbr | – | – | – | – | – | StayOn      |
| Reset       |             |             | – | – | – | – | – |             |
| Access Type | Write, Read | Write, Read | – | – | – | – | – | Write, Read |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                     |
|-------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ThmtoMonEn  | 7    | One-Shot THM Monitor Enable<br>Writing 1 triggers a one-shot measurement sequence to measure THM on IV-MON using the TPUEXT reference (see THM One-Shot Measurement section in Detailed Description). This bit must be manually cleared before triggering a new measurement.                    |
| ThmtoMonAbr | 6    | One-Shot THM Monitor Abort<br>Writing 1 aborts a one-shot THM measurement sequence. This bit must be manually cleared.                                                                                                                                                                          |
| StayOn      | 0    | StayOn<br>This bit is used to ensure that the processor booted correctly. This bit must be set within 5s of power-on to prevent the part from shutting down and returning to the power-off condition. This bit has no effect after being set.<br>0 = Shut down 5s after power-on<br>1 = Stay on |

**PwrCmd (0x4F)**

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field       | PowerCommand[7:0] |   |   |   |   |   |   |   |
| Reset       |                   |   |   |   |   |   |   |   |
| Access Type | Write, Read       |   |   |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PowerCommand | 7:0  | Power Command Register<br>Writing the following values issues the command listed:<br>0xB2 = places the part in off mode<br>0xC3 = issues a hard-reset (power cycle)<br>0xD4 = issues a soft-reset (reset pulse only)<br>After the written value has been validated by the internal logic, this register is cleared automatically. Any other commands are ignored. See <a href="#">Table 1</a> for the available PwrCmd for each PwrRstCfg value. |

**LockMsk (0x52)**

| BIT         | 7           | 6           | 5           | 4           | 3           | 2           | 1           | 0           |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Field       | LDO3Lck     | LDO2Lck     | LDO1Lck     | BBstLck     | Bk3Lck      | Bk2Lck      | Bk1Lck      | ChgLck      |
| Reset       |             |             |             |             |             |             |             |             |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                |
|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDO3Lck  | 7    | Lock Mask for LDO3 Registers<br>0 = LDO3 Registers not masked from locking/unlocking<br>1 = LDO3 Registers masked from locking/unlocking                   |
| LDO2Lck  | 6    | Lock Mask for LDO2 Registers<br>0 = LDO2 Registers not masked from locking/unlocking<br>1 = LDO2 Registers masked from locking/unlocking                   |
| LDO1Lck  | 5    | Lock Mask for LDO1 Registers<br>0 = LDO1 Registers not masked from locking/unlocking<br>1 = LDO1 Registers masked from locking/unlocking                   |
| BBstLck  | 4    | Lock Mask for Buck-Boost Registers<br>0 = Buck-Boost Registers not masked from locking/unlocking<br>1 = Buck-Boost Registers masked from locking/unlocking |
| Bk3Lck   | 3    | Lock Mask for Buck3 Registers<br>0 = Buck3 Registers not masked from locking/unlocking<br>1 = Buck3 Registers masked from locking/unlocking                |
| Bk2Lck   | 2    | Lock Mask for Buck2 Registers<br>0 = Buck2 Registers not masked from locking/unlocking<br>1 = Buck2 Registers masked from locking/unlocking                |
| Bk1Lck   | 1    | Lock Mask for Buck1 Registers<br>0 = Buck1 Registers not masked from locking/unlocking<br>1 = Buck1 Registers masked from locking/unlocking                |
| ChgLck   | 0    | Lock Mask for Charger Registers<br>0 = Charger Registers not masked from locking/unlocking<br>1 = Charger Registers masked from locking/unlocking          |

**LockUnlock (0x53)**

| BIT         | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------|---|---|---|---|---|---|---|
| Field       | PASSWORD[7:0] |   |   |   |   |   |   |   |
| Reset       |               |   |   |   |   |   |   |   |
| Access Type | Write, Read   |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PASSWORD | 7:0  | Lock/Unlock Password<br>Locks or unlocks all unmasked functions set in the Lock Mask register 0x52 when the correct password is written. Reading this register returns the current lock state of the functions. Locked functions return 1 and unlocked functions return 0. Functions are organized in the same order as register 0x52.<br>0x55 = Unlock unmasked functions<br>0xAA = Lock unmasked functions<br>All other codes = No effect |

## Applications Information

### I<sup>2</sup>C Interface

The MAX20345 contains an I<sup>2</sup>C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

#### Start, Stop, and Repeated Start Conditions

When writing to the MAX20345 using I<sup>2</sup>C, the master sends a START condition (S) followed by the MAX20345 I<sup>2</sup>C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I<sup>2</sup>C slave. See [Figure 15](#).

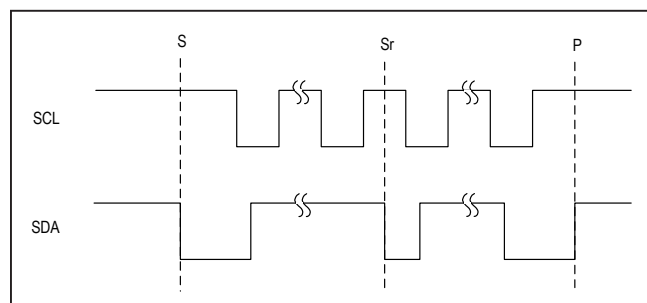


Figure 15. I<sup>2</sup>C START, STOP, and REPEATED START Conditions

### Slave Address

Set the Read/Write bit high to configure the MAX20345 to read mode. Set the Read/Write bit low to configure the MAX20345 to write mode. The address is the first byte of information sent to the MAX20345 after the START condition.

### Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the [Start, Stop, and Repeated Start Conditions](#) section). Both SDA and SCL remain high when the bus is not active.

### Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device ([Figure 16](#)). The following procedure describes the single byte write operation:

- The master sends a START condition
- The master sends the 7-bit slave address plus a write bit (low)
- The addressed slave asserts an ACK on the data line
- The master sends the 8-bit register address
- The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- The master sends 8 data bits
- The slave asserts an ACK on the data line
- The master generates a STOP condition

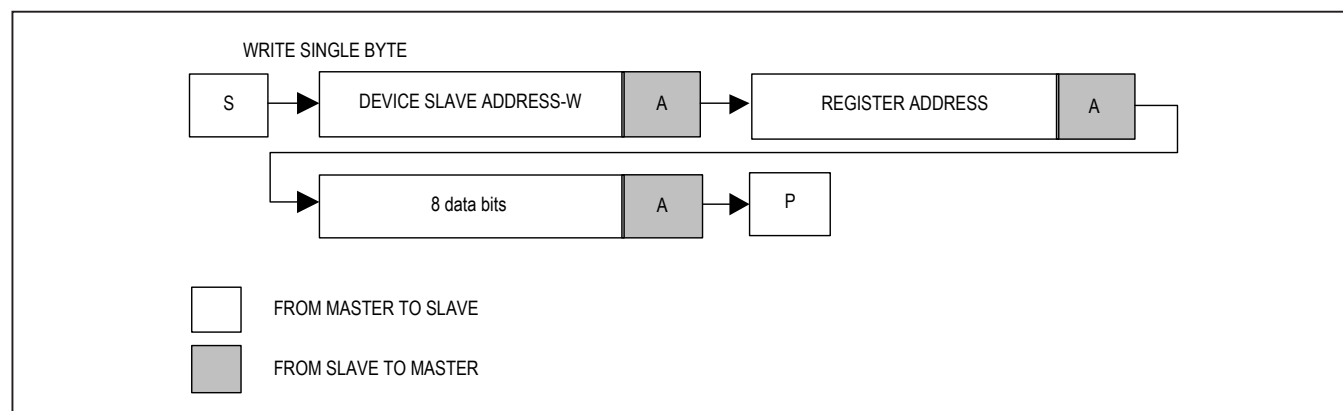


Figure 16. Write Byte Sequence

**Burst Write**

In this operation, the master sends an address and multiple data bytes to the slave device (Figure 17). The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

- The master sends a START condition
- The master sends the 7-bit slave address plus a write bit (low)
- The addressed slave asserts an ACK on the data line
- The master sends the 8-bit register address
- The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- The master sends 8 data bits
- The slave asserts an ACK on the data line
- Repeat 6 and 7 N-1 times
- The master generates a STOP condition

**Single Byte Read**

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (Figure 18). The following procedure describes the single byte read operation:

- The master sends a START condition
- The master sends the 7-bit slave address plus a write bit (low)
- The addressed slave asserts an ACK on the data line
- The master sends the 8-bit register address
- The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- The master sends a REPEATED START condition
- The master sends the 7-bit slave address plus a read bit (high)
- The addressed slave asserts an ACK on the data line
- The slave sends 8 data bits
- The master asserts a NACK on the data line
- The master generates a STOP condition

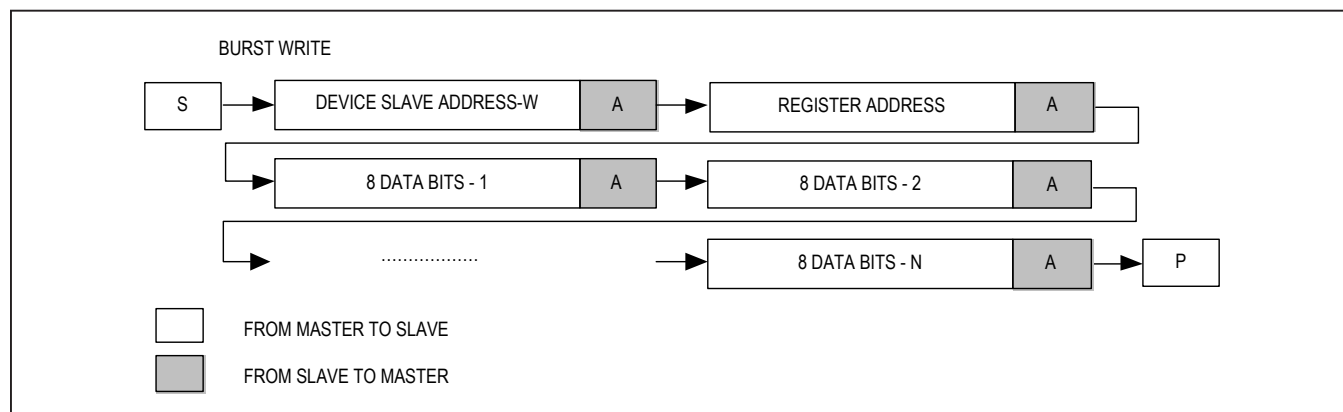


Figure 17. Burst Write Sequence

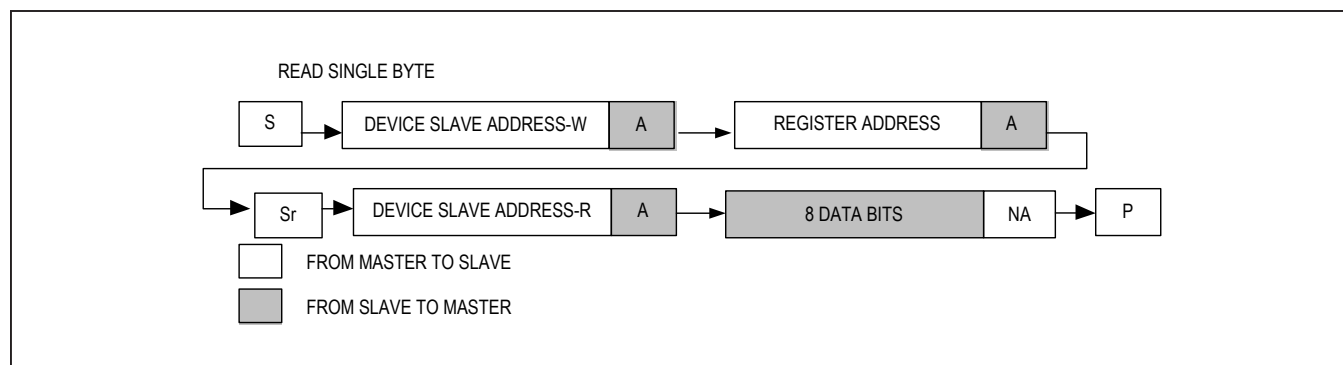


Figure 18. Read Byte Sequence

**Burst Read**

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (Figure 19). The following procedure describes the burst byte read operation:

- The master sends a START condition
- The master sends the 7-bit slave address plus a write bit (low)
- The addressed slave asserts an ACK on the data line
- The master sends the 8-bit register address
- The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- The master sends a REPEATED START condition
- The master sends the 7-bit slave address plus a read bit (high)
- The slave asserts an ACK on the data line

- The slave sends 8 data bits
- The master asserts an ACK on the data line
- Repeat 9 and 10 N-2 times
- The slave sends the last 8 data bits
- The master asserts a NACK on the data line
- The master generates a STOP condition

**Acknowledge Bits**

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NAK). Both the master and the MAX20345 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (see Figure 20). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

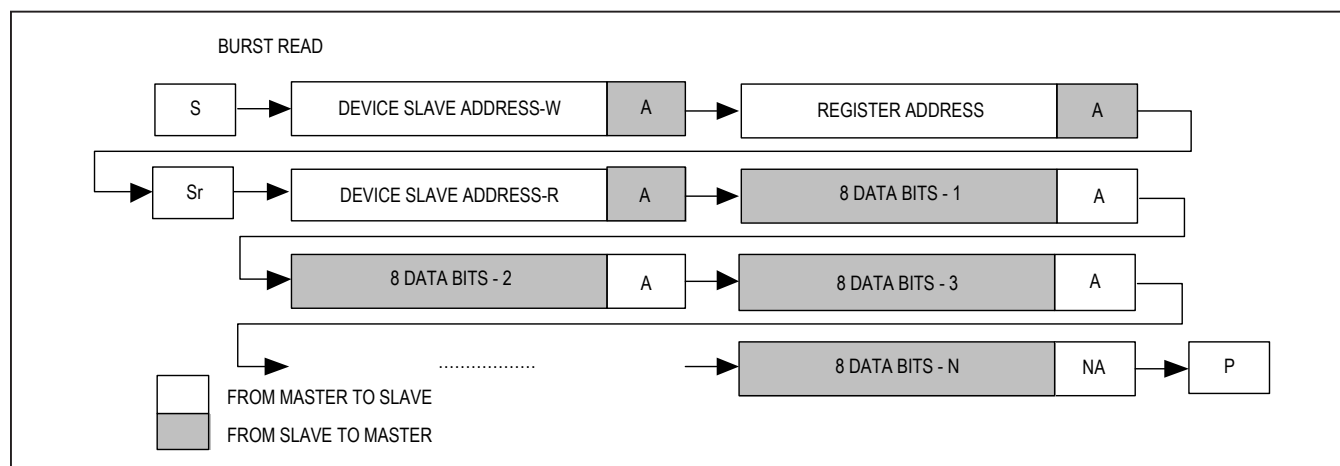


Figure 19. Burst Read Sequence

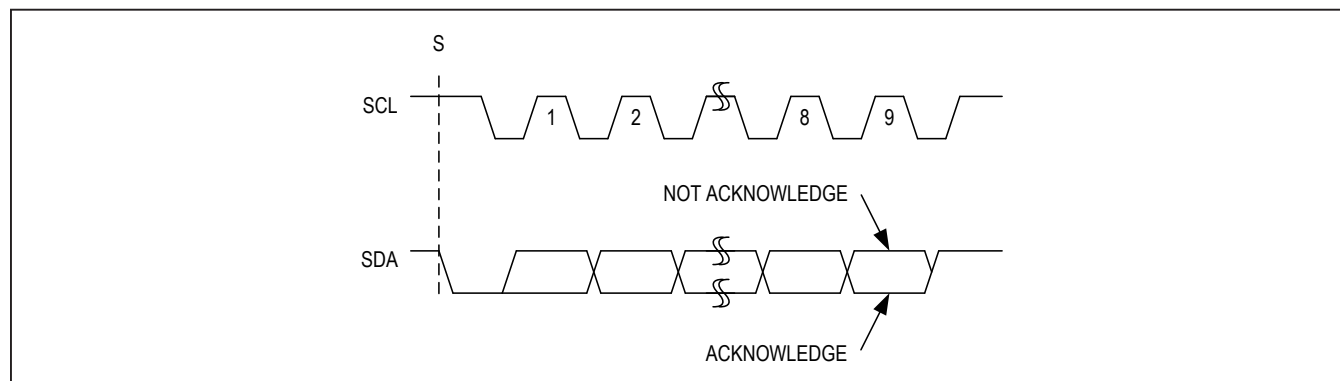


Figure 20. Acknowledge Bits

## Default Bits

Table 3. Register Bit Default Values

| REGISTER BITS | MAX20345A                       |
|---------------|---------------------------------|
| SysMinVlt     | 4.0V                            |
| ILimBlank     | Disabled, minimum response time |
| ILimCntl      | 450mA                           |
| IChgDone      | 30% I <sub>FCHG</sub>           |
| BatReChg      | BatReg - 70mV                   |
| BatReg        | 4.20V                           |
| ChgEn         | Enabled                         |
| PChgTmr       | 240min                          |
| VPChg         | 3.00V                           |
| IPChg         | 5% I <sub>FCHG</sub>            |
| ChgStepRise   | 4.00V                           |
| ChgAutoStp    | Enabled                         |
| ChgAutoReSta  | Enabled                         |
| MtChgTmr      | 60min                           |
| FChgTmr       | 300min                          |
| ChgIStep      | 30% I <sub>FCHG</sub>           |
| ChgStepHyst   | 400mV                           |
| Buck1VSet     | 1.200V                          |
| Buck1En       | Disabled                        |
| Buck1IZCSet   | 20mA                            |
| ThmEn         | Disabled                        |
| Buck1ISet     | 150mA                           |
| Buck2VSet     | 1.800V                          |
| Buck2En       | Enabled                         |
| Buck2IZCSet   | 20mA                            |
| Buck1SftStrt  | 50ms soft-start                 |
| Buck1FETScale | Disabled                        |
| Buck2ISet     | 150mA                           |
| Buck3VSet     | 3.100V                          |
| Buck3En       | Enabled                         |
| Buck3IZCSet   | 40mA                            |
| Buck2SftStrt  | 50ms soft-start                 |
| Buck2FETScale | Disabled                        |
| Buck3ISet     | 150mA                           |
| BBstVSet      | 3.30V                           |
| BBstEn        | Enabled                         |

| REGISTER BITS | MAX20345A             |
|---------------|-----------------------|
| BBstMode      | Buck-Boost            |
| Buck3SftStrt  | 50ms soft-start       |
| Buck3FETScale | Disabled              |
| BBstIPSet2    | BBstIPSet1 + 200mA    |
| BBstIPSet1    | 100mA                 |
| LDO1Mode      | Load Switch           |
| BBstFETScale  | Disabled              |
| LDO2Mode      | LDO                   |
| LDO1VSet      | 1.8V                  |
| LDO1En        | Enabled               |
| LDO3Mode      | LDO                   |
| LDO2VSet      | 3.1V                  |
| LDO2En        | Disabled              |
| LDO3VSet      | 1.2V                  |
| LDO3En        | Disabled              |
| BootDly       | 80ms                  |
| ChgAlwTry     | Retry                 |
| SW2En         | Disabled              |
| LSW2Lowlq     | No voltage protection |
| LSW1En        | Disabled              |
| LSW1Lowlq     | No voltage protection |
| UsbOkselect   | CHGIN Rise            |
| PwrRstCfg     | 0b0110                |
| SftRstCfg     | Reset Registers       |
| IBatOc        | 1600mA                |
| FrshBatDis    | 1                     |
| Bk2Step       | 25mV                  |
| Buck1Seq      | Buck1En After 100%    |
| Bk1Step       | 10mV                  |
| Bk3Step       | 50mV                  |
| Buck2Seq      | Buck2En After 100%    |
| LDO1Seq       | LDO1En After 100%     |
| BBstSeq       | 0%                    |
| Buck3Seq      | Buck3En After 100%    |
| LSW1Seq       | LSW1En After 100%     |
| LDO3Seq       | LDO3En After 100%     |

**Table 3. Register Bit Default Values (continued)**

| REGISTER BITS | MAX20345A          |
|---------------|--------------------|
| LDO2Seq       | LDO2En After 100%  |
| PFN1RInt      | Resistor connected |
| PFN2RInt      | No Resistor        |
| GlbPsvDsc     | Enabled            |
| LSW2Seq       | LSW2En After 100%  |
| BBstlAdptDis  | Adaptive IPEAK     |

| REGISTER BITS | MAX20345A                |
|---------------|--------------------------|
| PFN1PUD       | Pullup                   |
| PFN2PUD       | N/A                      |
| JEITASet      | T4 = 25.53%, T3 = 32.94% |
| ILimMax       | 1000mA                   |
| TShdn         | 120°C                    |

**Register Defaults****Table 4. Register Default Values**

| REGISTER | NAME         | MAX20345A |
|----------|--------------|-----------|
| 0x00     | ChipID       | 0x07      |
| 0x01     | ChipRev      | 0x01      |
| 0x09     | IntMask0     | 0x00      |
| 0x0A     | IntMask1     | 0x00      |
| 0x0B     | IntMask2     | 0x00      |
| 0x0C     | ILimCntl     | 0x86      |
| 0x0D     | ChgCntl0     | 0x07      |
| 0x0E     | ChgCntl1     | 0x63      |
| 0x0F     | ChgTmr       | 0xFB      |
| 0x10     | StepChgCfg0  | 0x34      |
| 0x11     | StepChgCfg1  | 0x01      |
| 0x12     | ThmCfg0      | 0x1F      |
| 0x13     | ThmCfg1      | 0x1F      |
| 0x14     | ThmCfg2      | 0x1F      |
| 0x15     | MONCfg       | 0x10      |
| 0x16     | Buck1Cfg     | 0xE3      |
| 0x17     | Buck1VSet    | 0x70      |
| 0x18     | Buck1ISet    | 0xC6      |
| 0x19     | Buck1Ctr     | 0x01      |
| 0x1A     | Buck1DVSCfg0 | 0x00      |
| 0x1B     | Buck1DVSCfg1 | 0x00      |
| 0x1C     | Buck1DVSCfg2 | 0x00      |
| 0x1D     | Buck1DVSCfg3 | 0x00      |
| 0x1E     | Buck1DVSSPI  | 0x00      |
| 0x1F     | Buck2Cfg     | 0xED      |
| 0x20     | Buck2VSet    | 0x6C      |
| 0x21     | Buck2ISet    | 0xC6      |

| REGISTER | NAME         | MAX20345A |
|----------|--------------|-----------|
| 0x22     | Buck2Ctr     | 0x02      |
| 0x23     | Buck2DVSCfg0 | 0x00      |
| 0x24     | Buck2DVSCfg1 | 0x00      |
| 0x25     | Buck2DVSCfg2 | 0x00      |
| 0x26     | Buck2DVSCfg3 | 0x00      |
| 0x27     | Buck2DVSSPI  | 0x00      |
| 0x28     | Buck3Cfg     | 0xEF      |
| 0x29     | Buck3VSet    | 0x70      |
| 0x2A     | Buck3ISet    | 0xC6      |
| 0x2B     | Buck3Ctr     | 0x04      |
| 0x2C     | Buck3DVSCfg0 | 0x00      |
| 0x2D     | Buck3DVSCfg1 | 0x00      |
| 0x2E     | Buck3DVSCfg2 | 0x00      |
| 0x2F     | Buck3DVSCfg3 | 0x00      |
| 0x30     | Buck3DVSSPI  | 0x00      |
| 0x31     | BBstCfg0     | 0x4D      |
| 0x32     | BBstVSet     | 0x10      |
| 0x33     | BBstISet     | 0x84      |
| 0x34     | BBstCfg1     | 0x23      |
| 0x35     | BBstCtr      | 0x08      |
| 0x36     | BBstDVSCfg0  | 0x00      |
| 0x37     | BBstDVSCfg1  | 0x00      |
| 0x38     | BBstDVSCfg2  | 0x00      |
| 0x39     | BBstDVSCfg3  | 0x00      |
| 0x3A     | BBstDVSSPI   | 0x00      |
| 0x3B     | LDO1Cfg      | 0xEC      |
| 0x3C     | LDO1VSet     | 0x0A      |

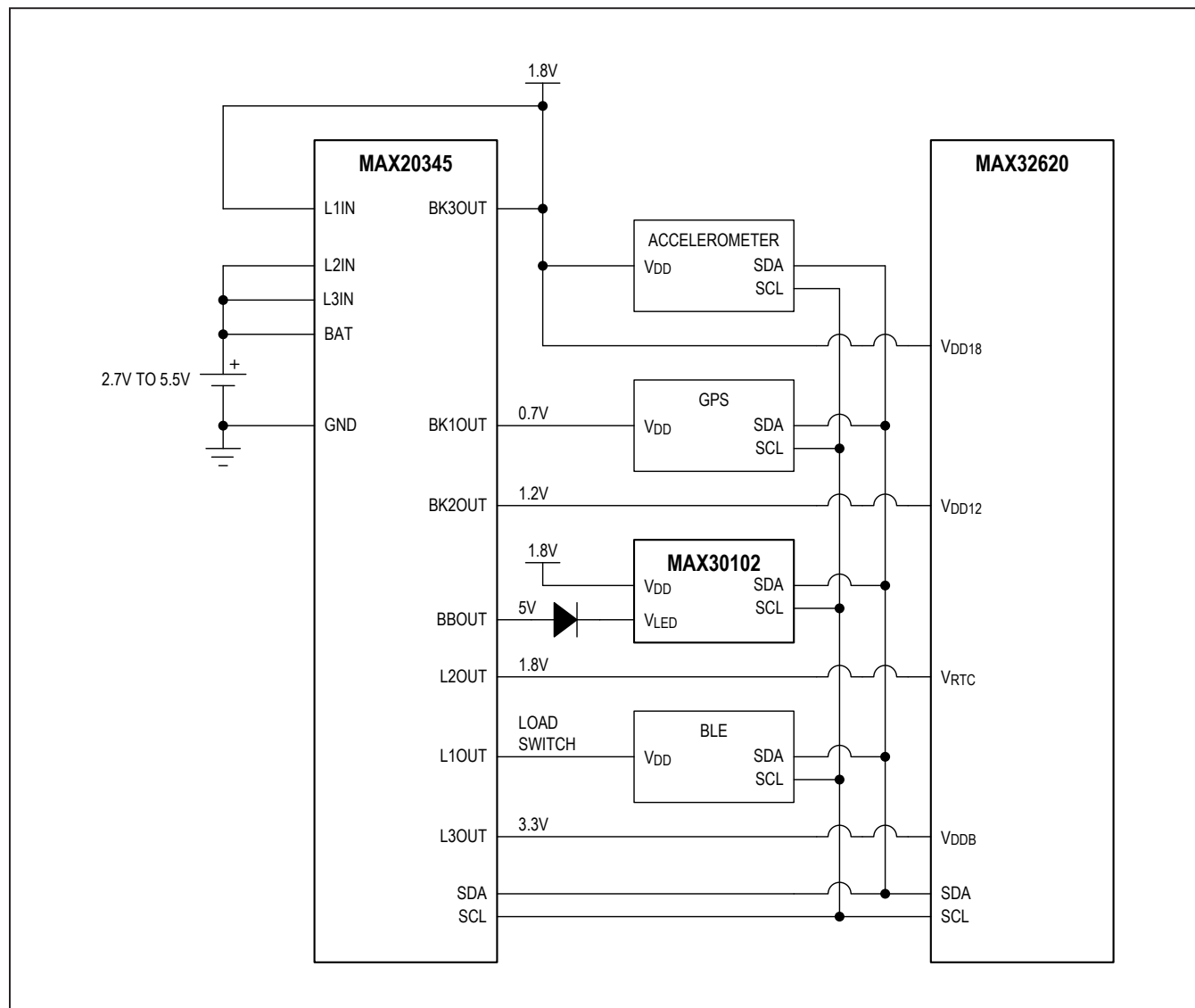
**Table 4. Register Default Values (continued)**

| REGISTER | NAME     | MAX20345A |
|----------|----------|-----------|
| 0x3D     | LDO1Ctr  | 0x01      |
| 0x3E     | LDO2Cfg  | 0xE1      |
| 0x3F     | LDO2VSet | 0x16      |
| 0x40     | LDO2Ctr  | 0x02      |
| 0x41     | LDO3Cfg  | 0xE1      |
| 0x42     | LDO3VSet | 0x1C      |
| 0x43     | LDO3Ctr  | 0x04      |
| 0x44     | LSW1Cfg  | 0xE3      |
| 0x45     | LSW1Ctr  | 0x00      |
| 0x46     | LSW2Cfg  | 0xE3      |

| REGISTER | NAME       | MAX20345A |
|----------|------------|-----------|
| 0x47     | LSW2Ctr    | 0x00      |
| 0x48     | MPC0Cfg    | 0x00      |
| 0x49     | MPC1Cfg    | 0x00      |
| 0x4A     | MPC2Cfg    | 0x00      |
| 0x4B     | MPC3Cfg    | 0x00      |
| 0x4D     | BootCfg    | 0x6A      |
| 0x4E     | PwrCfg     | 0x01      |
| 0x52     | LockMsk    | 0x00      |
| 0x53     | LockUnlock | 0xFF      |

## Typical Application Circuits

## Sports Watch with Heart Rate Monitoring



## Ordering Information

| PART NUMBER    | TEMP RANGE     | PIN-PACKAGE |
|----------------|----------------|-------------|
| MAX20345AEWN+  | -40°C to +85°C | 56-WLP      |
| MAX20345AEWN+T | -40°C to +85°C | 56-WLP      |

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

## Revision History

| REVISION<br>NUMBER | REVISION<br>DATE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                       | PAGES<br>CHANGED                                          |
|--------------------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------|
| 0                  | 6/18             | Initial release                                                                                                                                                                                                                                                                                                                                                                                                                   | —                                                         |
| 1                  | 11/18            | Updated the title, <i>General Description</i> section; replaced all <i>Typical Operating Characteristics</i> and corrected bit names; corrected typos                                                                                                                                                                                                                                                                             | 1–126                                                     |
| 2                  | 12/18            | Added new TOC06–TOC09 and renumbered subsequent and renumbered remaining TOCs; corrected some typos in TOCs and added the <i>I<sup>2</sup>C Interface Overview</i> section                                                                                                                                                                                                                                                        | 27–33, 57                                                 |
| 3                  | 2/20             | Updated the <i>Electrical Characteristics</i> , <i>Pin Description</i> , and <i>Buck-Boost Regulator</i> sections; updated the <i>Register Map</i> , <i>Register 0x18</i> , and bit 3 information for Registers 0x04, 0x07, and 0x0A; corrected Reset information for Registers 0x00 and 0x01, and Description for Bit 6 for Registers 0x18, 0x21, and 0x2A; added new Figure 5 and renumbered subsequent figures; corrected typo | 9, 20–22, 35,<br>51, 58, 61, 63,<br>65, 67, 79,<br>85, 91 |

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