

## MAX20734

## Integrated, Step-Down Switching Regulator with PMBus

### General Description

The MAX20734 is a fully integrated, highly efficient switching regulator with PMBus™ for applications operating from 4.5V to 16V and requiring up to 40A (max) load. This single-chip regulator provides extremely compact, high-efficiency power-delivery solutions with high-precision output voltages and excellent transient response for networking, datacom, and telecom equipment.

The IC offers a broad range of programmable features through either the PMBus or a capacitor and resistor connected to a dedicated programming pin. Using this feature, the operation can be optimized for a specific application, reducing the component count and/or setting appropriate trade-offs between the regulator's performance and system cost. Ease of programming enables using the same design for multiple applications.

The IC includes protection and telemetry features. Positive and negative cycle-by-cycle overcurrent protection and overtemperature protection ensure a rugged design. Input undervoltage lockout shuts down the device to prevent operation when the input voltage is out of specification. A status pin provides an output signal to show that the output voltage is within range and the system is regulating.

### Applications

- Communications Equipment
- Networking Equipment
- Servers and Storage Equipment
- Point-of-Load Voltage Regulators
- $\mu$ P Chipsets
- Memory  $V_{DDQ}$
- I/O

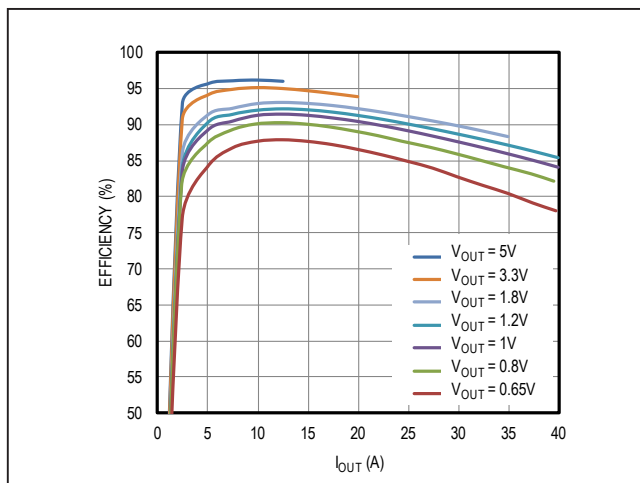
DESCRIPTION	CURRENT RATING*	INPUT VOLTAGE	OUTPUT VOLTAGE
Electrical rating	40A	4.5V to 16V	0.6V to 5.5V
Thermal rating, $T_A = 55^\circ\text{C}$ , 200LFM	35A	12V	1V
Thermal rating, $T_A = 85^\circ\text{C}$ , 0LFM	22A	12V	1V

\*For specific operating conditions, refer to the SOA curves in the [Typical Operating Characteristics](#) section.

### Benefits and Features

- High Power Density and Low Component Count
  - Overall Solution Size 509mm<sup>2</sup> Including Inductor and Output Capacitors
  - 90.7% Peak Efficiency with  $V_{DDH} = 12\text{V}$  and  $V_{OUT} = 1\text{V}$
  - Fast Transient Response: Supports Up to 300A/ $\mu$ s Load-Step Transients
- Optimized Component Performance and Efficiency with Reduced Design-In Time
  - PMBus-Compliant Interface for Telemetry and Power Management
  - Voltage, Current, and Temperature Reporting through the Digital Bus
- Increased Power-Supply Reliability with System and IC Self-Protection Features
  - Differential Remote Sense with Open-Circuit Detection
  - Hiccup Overcurrent Protection
  - Programmable Thermal Shutdown

### Typical System Efficiency vs. Load Current ( $V_{DDH} = 12\text{V}$ )



[Order Information](#) appears at end of data sheet.

PMBus is a trademark of SMIF, Inc.

## Absolute Maximum Ratings

Input Pin Voltage ( $V_{DDH}$ ) (Note 1).....	-0.3V to +18V	Switching Node Voltage (VX) DC.....	-0.3V to +18V
$V_{CC}$ .....	-0.3V to +2V	Switching Node Voltage (VX) 25ns (Note 2).....	-10V to +23V
STAT, OE, CLK, DATA, and SMALERT Pin Voltages.....	-0.3V to +4V	(BST - VX) Pin Differential .....	-0.3V to +2.5V
PGMA, PGMB, $V_{SENSE+}$ and $V_{SENSE-}$ Pin Voltages .....	-0.3V to +2V	Junction Temperature ( $T_J$ ).....	+150°C
		Storage Temperature Range .....	-65°C to +150°C
		Peak Reflow Temperature Lead-Free .....	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Operating Ratings

Input Voltage ( $V_{DDH}$ ).....	4.5V to 16V	Maximum Average Input Current ( $V_{DDH\_MAX}$ ) (Note 3).....	6A
Junction Temperature ( $T_J$ ).....	-40°C to +125°C	Maximum Average Output Current ( $I_{MAX}$ ) .....	40A
		Peak Output Current ( $I_{PK}$ ).....	90A

## Package Information

<b>PACKAGE TYPE: 15 FCQFN</b>	
Package Code	P154A9F+1
Outline Number	<a href="#">21-100027</a>
Land Pattern Number	<a href="#">90-100025</a>
<b>THERMAL RESISTANCE</b>	
Junction to Ambient ( $\theta_{JA}$ ) (Note 4; Still Air, No Heatsink)	12°C/W
Junction to Case ( $\theta_{JC}$ )	0.42°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

**Note 1:** As measured at the  $V_{DDH}$  pin referenced to GND pin immediately adjacent using a high-frequency scope probe with  $I_{LOAD}$  at  $I_{MAX}$ . A high-frequency input bypass capacitor must be located less than 60 mils from the  $V_{DDH}$  pin per our design guidelines.

**Note 2:** The 25ns rating is the allowable voltage on the VX node in excess of the -0.3V to +18V DC ratings. The VX voltage may exceed the DC rating in either the positive or negative direction for up to 25ns per cycle.

**Note 3:** See the [Average Input Current Limit](#) section.

**Note 4:** Data taken using Maxim's evaluation kit (MAX20734EVKIT#). The PCB has four layers of 2oz copper.

## Electrical Characteristics

(Circuit of [Figure 6](#),  $V_{DDH} = 4.5V$  to  $16V$ ,  $T_A = +25^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All devices 100% tested at  $T_A = +25^\circ C$ . Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE						
Supply-Voltage Range	V <sub>DDH</sub>	T <sub>J</sub> = -40°C to +125°C	4.5		16	V
OUTPUT VOLTAGE (Note 5)						
Output-Voltage Range	V <sub>OUT</sub>	(Note 6)	0.6		5.5	V
Programmable V <sub>OUT</sub> Slew Rates		Default is 1mV/μs; other values are set through PMBus; measured at V <sub>SENSE</sub> +/- pins		1		mV/μs
				2		
				4		
V <sub>REF</sub>						
V <sub>BOOT</sub> Values	V <sub>REF</sub>	Selected by C_SELA (Note 7)		0.6484		V
				0.8984		
				1.0		
V <sub>REF</sub> Tolerance		V <sub>REF</sub> = 0.6484V, 0.8984V, and 1.0V (Notes 6, 8), referred to V <sub>SENSE</sub> +/- pins	-1.0		+1.0	%
Programmable V <sub>REF</sub> Range		See Table 8 for accuracy vs. V <sub>REF</sub> (Note 7)	0.6016		1.0	V
FEEDBACK LOOP						
Integrator Recovery Time Constant	t <sub>REC</sub>			20		μs
Gain (see the <i>Control Loop Stability</i> section for details)	R <sub>GAIN</sub>	Selected by R_SELB or PMBus (Notes 6, 7, 8, 9)		0.8		mV/A
				1.6		
				3.2		
Gain Accuracy		(Notes 6, 8, 9)	-20		+20	%
SWITCHING FREQUENCY						
Switching Frequency	f <sub>SW</sub>	400kHz/600kHz/800kHz selected by C_SEL_B; other values are set through PMBus (Note 7)		400		kHz
				500		
				600		
				700		
				800		
				900		
Switching Frequency Accuracy		(Notes 6, 8, 9)	-20		+20	%
INPUT PROTECTION						
Rising V <sub>DDH</sub> UVLO Threshold	V <sub>DDH</sub> UVLO	(Note 6)		4.25	4.47	V
Falling V <sub>DDH</sub> UVLO Threshold			3.7	3.9		
Hysteresis						350

**Electrical Characteristics (continued)**

(Circuit of [Figure 6](#),  $V_{DDH} = 4.5V$  to  $16V$ ,  $T_A = +25^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All devices 100% tested at  $T_A = +25^\circ C$ . Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT-VOLTAGE PROTECTION (OVP)							
Overshoot-Protection, Rising Threshold	OVP	Relative to programmed V <sub>OUT</sub>		9.5	13	16.5	%
OVP Deglitch Filter Time				8			μs
Power-Good Protection, Falling Threshold	PWRGD	Relative to programmed V <sub>OUT</sub>		6	9	12	%
Power-Good Protection Rising Threshold				3	6	9	%
Power-Good Deglitch Filter Time				8			μs
OVERCURRENT PROTECTION (OCP)							
Positive OCP Inception Threshold (Inductor Valley Current)	OCP	Selected by R_SELB or PMBus (Notes 6, 7, 8, 9)	OCP Setting 0	16.3	21	26.1	A
			OCP Setting 1	20.8	27	33.0	
			OCP Setting 2	24.6	32	39.9	
			OCP Setting 3	30.6	38	45.5	
Negative OCP Inception Threshold (Inductor Valley Current)		Selected by R_SELB or PMBus	OCP Setting 0	-28			A
			OCP Setting 1	-33			
			OCP Setting 2	-39			
			OCP Setting 3	-44			
Hysteresis	Hysteresis applies only to positive OCP		15			%	
OVERTEMPERATURE PROTECTION (OTP)							
OTP Inception Threshold	OTP	Default is 150, 130 is set through PMBus (Notes 7, 8, 9)	120	130	140	°C	
Hysteresis			140	150	160		
OE MAXIMUM VOLTAGE							
OE Maximum Voltage	OE	Full V <sub>CC</sub> supply range; measured at the OE pin (Note 6)	V <sub>DDH</sub> - 2.5			V	
Rising Threshold			0.83	0.9	0.97		
Hysteresis			0.2				
OE Pin Input Resistance			200	275	350	kΩ	
OE Deglitch Filter Time		(Note 9)	0.9	2.2		μs	
STARTUP TIMING							
Enable Time from OE Rise to Start of BST Charge	t <sub>OE</sub>	After t <sub>INIT</sub>		16			μs
Soft-Start Ramp Time	t <sub>SS</sub>	3 or 1.5 can be bet by R_SELA; any value can be set by PMBus (Note 7)		0.75			ms
				1.5			
				3			
				6			
BST Charging Time	t <sub>BST</sub>			8			μs

## Electrical Characteristics (continued)

(Circuit of Figure 6,  $V_{DDH} = 4.5V$  to  $16V$ ,  $T_A = +25^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All devices 100% tested at  $T_A = +25^\circ C$ . Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STAT PIN						
Allowable Pullup Voltage	VOH <sub>STAT</sub>				3.6	V
Status Output Low	VOL <sub>STAT</sub>	I <sub>STAT</sub> = 2.5mA			0.4	V
		I <sub>STAT</sub> = 0.2mA, 0V < V <sub>CC</sub> < UVLO and 0V < V <sub>DDH</sub> < UVLO (Note 6)			0.65	
		I <sub>STAT</sub> = 1.3mA, 0V < V <sub>CC</sub> < UVLO and 0V < V <sub>DDH</sub> < UVLO (Note 6)			0.75	
Status Output High Leakage Current	I <sub>STAT</sub>	STAT pulled up to 3.3V through 20kΩ (Note 6)			7	μA
Time from V <sub>OUT</sub> Ramp Completion to STAT Pin Released	t <sub>STAT</sub>	STAT output low to high, default is 125; 2000 can be set through PMBus (Note 7)		125		μs
				2000		
PGMA AND PGMB PINS (see Tables 2–5)						
Allowable R_SEL Resistor Range		12 resistor values detected	1.78		162	kΩ
R_SEL Resistor Required Accuracy		EIA standard resistor values only		±1		%
Allowable C_SEL Capacitor Range		3 options (0pF, 220pF, or 1000pF)	0		1000	pF
C_SEL Capacitor Required Accuracy		Use X7R or better		±20		%
Allowable External Capacitance		Load and stray capacitance in addition to C_SELA/B			20	pF
PMBus TELEMETRY						
Reading Range	V <sub>DDH</sub> Readback		4.5		16	V
Reading Update Interval				5		ms
Reading Averaging Interval				1		ms
Reading Error		T <sub>A</sub> = -40°C to T <sub>J</sub> = +125°C (Notes 8, 9, 10, 11)	-3		+3	%
Reading Resolution				28		mV
Reading Range	V <sub>SENSE</sub> Readback		0		1.25	V
Reading Update Interval				5		ms
Reading Averaging Interval				1		ms
Referred to SENSE Pins (V <sub>OUT</sub> may be scaled by divider in feedback)		T <sub>A</sub> = -40°C to T <sub>J</sub> = +125°C (Notes 8, 9, 10, 11)	-25		+25	mV
Reading Resolution				1.95		mV
Reading Range	I <sub>OUT</sub> Readback		0		25	A
Reading Update Interval				5		ms
Reading Averaging Interval				1		ms
Reading Error		T <sub>A</sub> = -40°C to T <sub>J</sub> = +125°C (Notes 8, 9, 10, 11)		±3		A
Reading Resolution				0.07		A

**Electrical Characteristics (continued)**

(Circuit of [Figure 6](#),  $V_{DDH} = 4.5V$  to  $16V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ . All devices 100% tested at  $T_A = +25^{\circ}C$ . Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reading Range	Temperature Readback		-40		+125	°C
Reading Update Interval				5		ms
Reading Averaging Interval				1		ms
Reading Error		(Notes 6, 8, 9)		±8		°C
Reading Resolution				0.52		°C
PMBus PINS (CLK, DATA, SMALERT)						
Input Rising Threshold	V <sub>T</sub> RISE		0.83	0.9	0.97	V
Input Falling Threshold	V <sub>T</sub> FALL		0.62	0.7	0.79	V
Hysteresis	V <sub>HYS</sub>			0.2		V
Output Low Voltage	V <sub>OL</sub>	Sinking 4mA			0.4	V
PMBus Clock Frequency	f <sub>PM</sub> CLK				400	kHz
SYSTEM SPECIFICATIONS (Note 10)						
Line Regulation	V <sub>OUT</sub>			±0.2		%
Load Regulation (Static)		I <sub>OUT</sub> = 0 - I <sub>MAX</sub>		±0.7		
Efficiency (V <sub>DDH</sub> = 12V, V <sub>OUT</sub> = 1V)	η	Peak		90.7		%
		Full load (40A)		84.3		

**Note 5:** For proper regulation, it is required that  $V_{DDH} > (V_{OUT} + 2V)$ . If  $V_{OUT}$  is set  $> (UVLO - 2V)$ , the IC may come out of UVLO, but regulation is not guaranteed while  $V_{DDH}$  is below  $(V_{OUT} + 2V)$ . To avoid this condition, OE can be held low until  $V_{DDH} > (V_{OUT} + 2V)$ .

**Note 6:** Denotes specifications that apply over the temperature range of  $T_J = -40$  to  $+125^{\circ}C$ .

**Note 7:** Denotes parameters that are programmable.

**Note 8:** Min/Max limits are  $\geq 4\sigma$  about the mean.

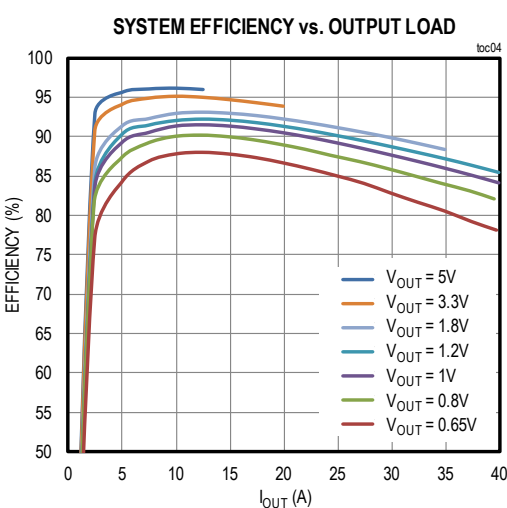
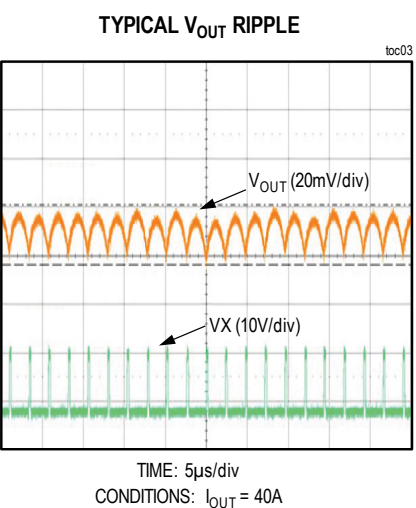
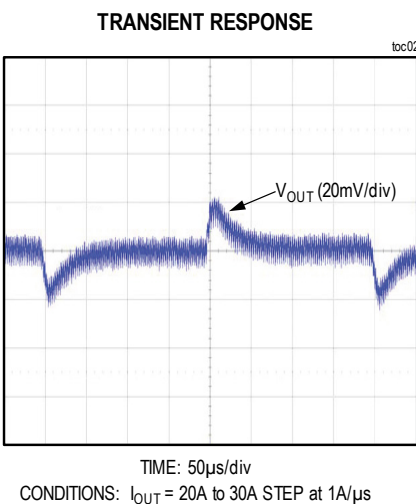
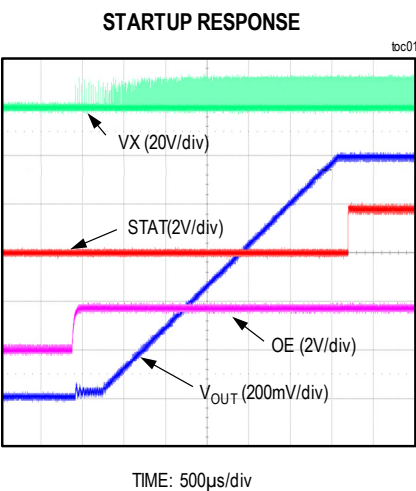
**Note 9:** Guaranteed by design; not production tested.

**Note 10:** These specifications refer to the operation of the system and are based on the circuit shown in the reference schematic. Tolerance of external components may affect these parameters. System performance numbers are measured using the Maxim evaluation board for this product with BOM, as shown on the MAX20734 EV kit data sheet. If a different PCB layout and different external components are used, these values may change.

**Note 11:** A  $-40^{\circ}C$  test condition is specified at a  $T_A$  test condition, instead of  $T_J$ , to allow for self-heating.

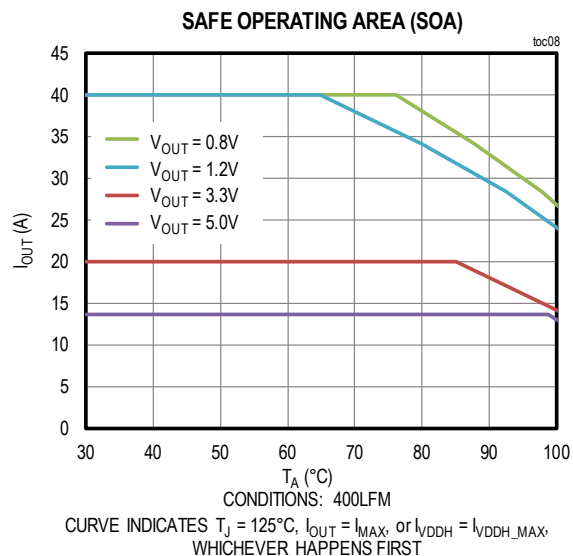
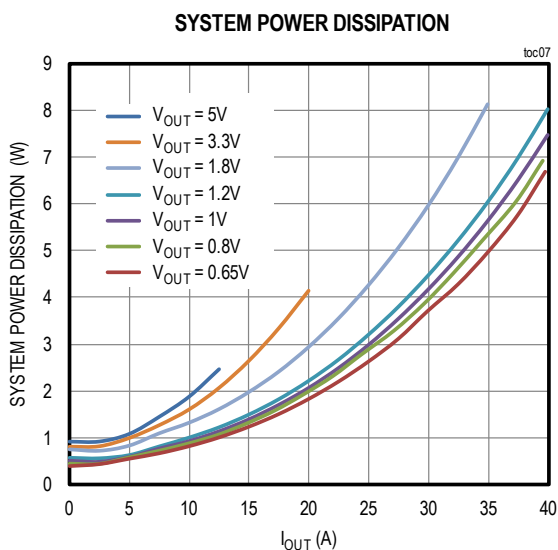
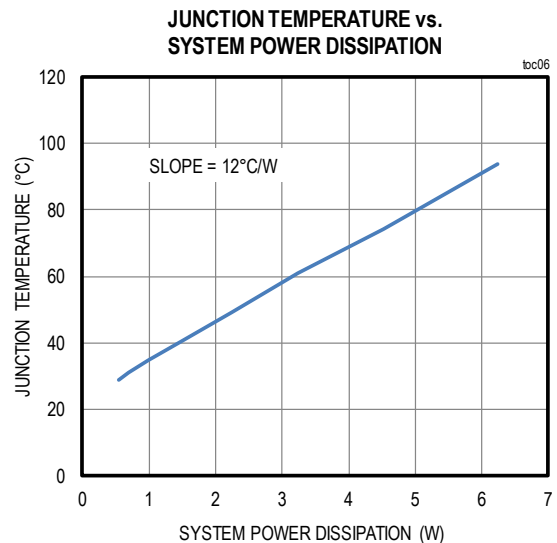
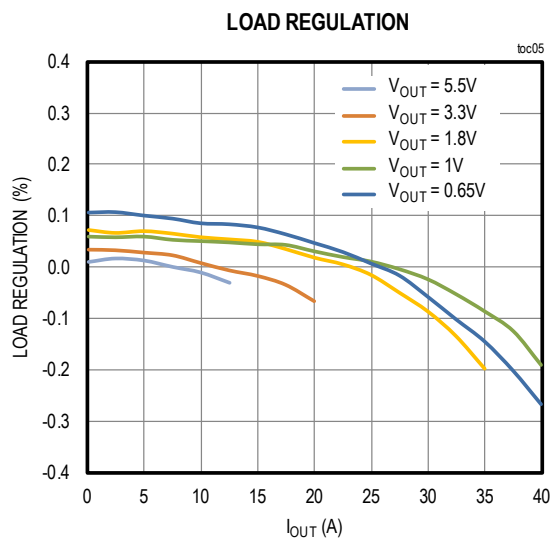
Typical Operating Characteristics

(Unless otherwise stated: Tested on the MAX20734EVKIT# EV kit with component values per Table 7,  $V_{DDH} = 12V$ ,  $V_{OUT} = 1V$ ,  $f_{SW} = 400kHz$ ,  $T_A = 25^{\circ}C$ , Still Air, and No Heatsink.)



## Typical Operating Characteristics (continued)

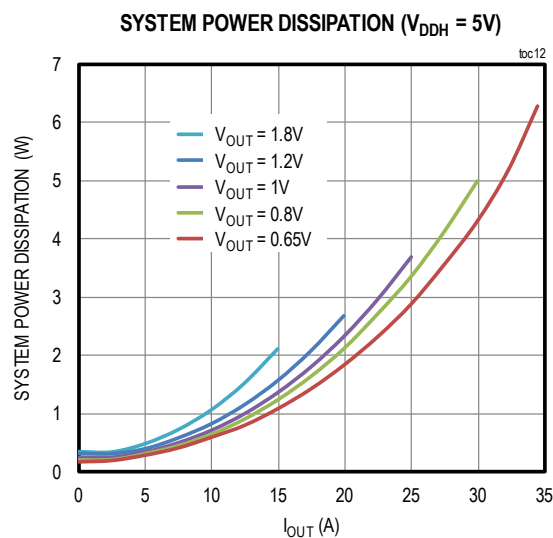
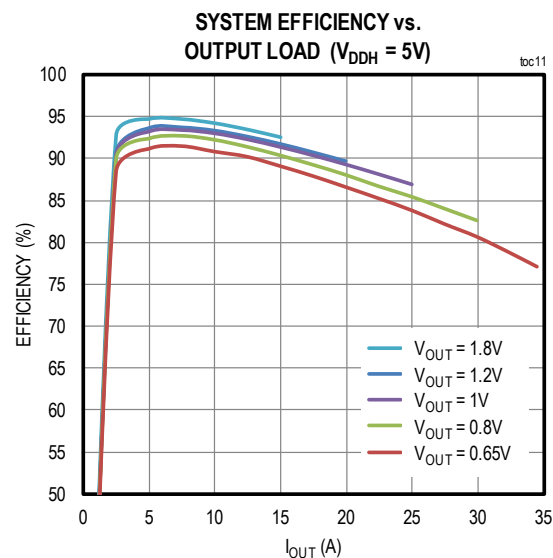
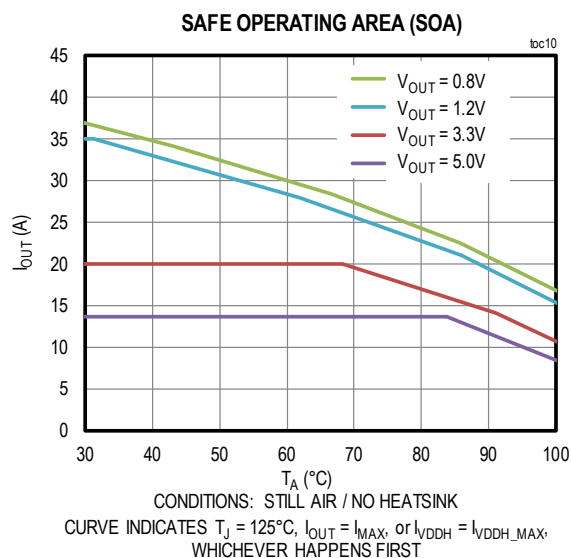
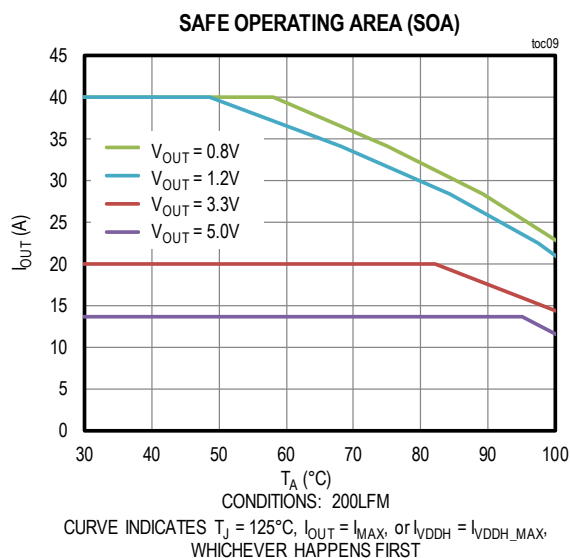
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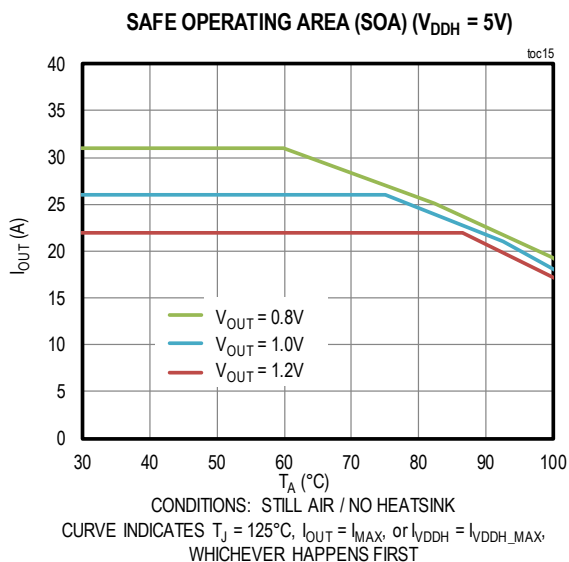
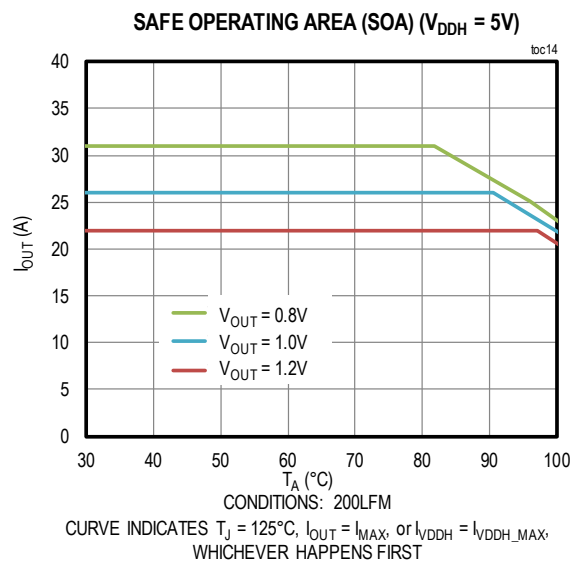
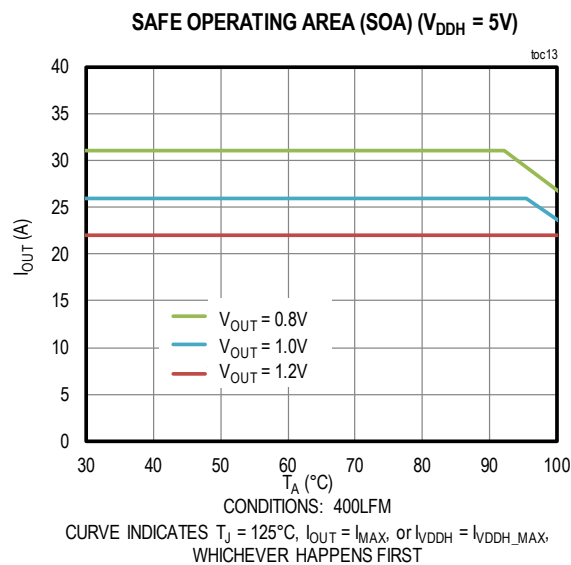
**Typical Operating Characteristics (continued)**

(Unless otherwise stated: Tested on the MAX20734EVKIT# EV kit with component values per [Table 7](#),  $V_{DDH} = 12V$ ,  $V_{OUT} = 1V$ ,  $f_{SW} = 400kHz$ ,  $T_A = 25^\circ C$ , Still Air, and No Heatsink.)

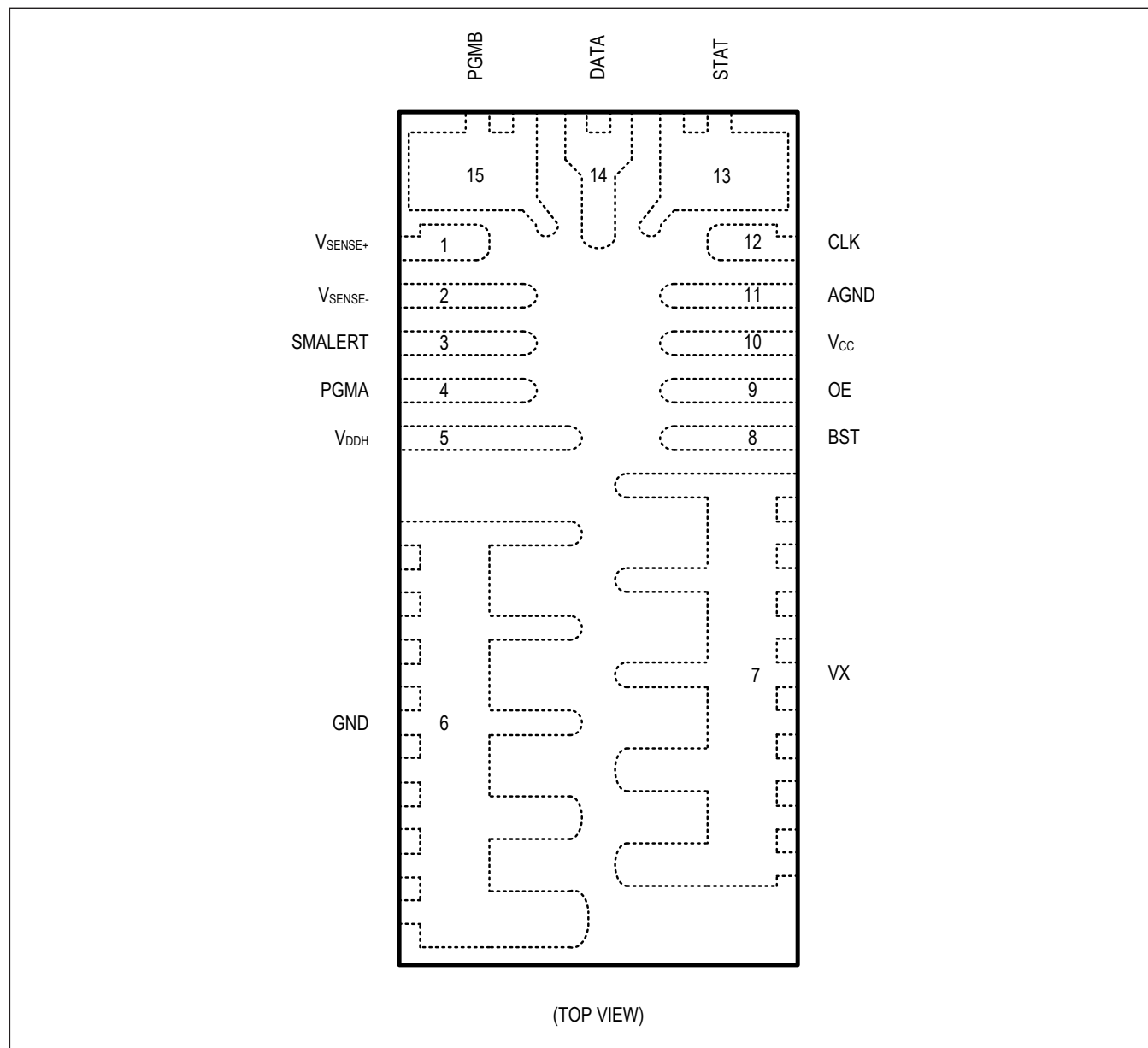


Typical Operating Characteristics (continued)

(Unless otherwise stated: Tested on the MAX20734EVKIT# EV kit with component values per Table 7,  $V_{DDH} = 12V$ ,  $V_{OUT} = 1V$ ,  $f_{SW} = 400kHz$ ,  $T_A = 25^{\circ}C$ , Still Air, and No Heatsink.)



## Pin Configuration



## Pin Description

PIN	NAME	FUNCTION
1	V <sub>SENSE+</sub>	Remote-Sense Positive Node. Connect this node to V <sub>OUT</sub> at the load. A resistive voltage-divider can be used to regulate the output above the reference voltage.
2	V <sub>SENSE-</sub>	Remote-Sense Negative Node. Connect this node to ground at the load using a Kelvin connection.
3	SMALERT	SMALERT Pin
4	PGMA	Program Node. Connect this node to ground through a programming resistor and capacitor.
5	V <sub>DDH</sub>	Power Input Voltage. The high-side MOSFET switch is connected to this node. See the <i>Input Capacitor Selection</i> section for decoupling requirements.
6	GND	Power Ground Node. The low-side MOSFET switch is connected to this node.
7	VX	Power Switching Node. Connect this node to the inductor.
8	BST	Bootstrap for High-Side Switch. Connect a 0.22μF ceramic capacitor between BST and VX.
9	OE	Output Enable Node. This node is used to enable the regulator and has a precise threshold to allow sequencing of multiple regulators. There is an internal 275kΩ (typ) pulldown on this node.
10	V <sub>CC</sub>	Analog/Gate-Drive Supply for the IC from Internal 1.85V (typ) LDO. This node <b>must</b> be connected to three 10μF X5R or better decoupling capacitors with very short, wide traces. V <sub>CC</sub> can be connected to 20kΩ pullups for STAT and OE, as shown in Figure 6. Do not connect V <sub>CC</sub> to other external loads. Do not overdrive V <sub>CC</sub> from an external source.
11	AGND	Analog/Signal Ground. See the <i>PCB Layout</i> section for layout information.
12	CLK	PMBus Clock
13	STAT	Open-Drain Power-Good/Fault-Status Indication. Connect a pullup resistor to 1.8V or 3.3V.
14	DATA	PMBus Data
15	PGMB	Program Node. Connect this node to ground through a programming resistor and capacitor.

The block diagram illustrates the control system for the DC-DC converter. Key components and their interconnections include:

- Inputs:** STAT, OE, PGMA, PGMB, CLK, DATA, SMALERT,  $V_{CC}$ , and AGND.
- Control Logic:** A **DIGITAL CONTROL** block receives inputs from STAT, OE, PGMA, PGMB, CLK, DATA, and SMALERT. It is also connected to a **TELEMETRY** block and a **PMBus INTERFACE** block.
- Timing and Logic:** The **DIGITAL CONTROL** block is connected to a  **$t_{ON}$  TIMER** and an **R-S flip-flop** (labeled R, S, Q). The Q output of the flip-flop is connected to an inverter and the **POWER SWITCHING** block.
- Power Regulation:** The **DIGITAL CONTROL** block is connected to an **OCP** (Over-Current Protection) block and a **PWM** (Pulse Width Modulation) block. The OCP block is connected to a **CURRENT SENSE** block. The PWM block is connected to an **ERROR AMP** (Error Amplifier).
- Power Stages:** The **POWER SWITCHING** block is connected to the **POWER MOSFET** and the **POWER DIODE**. The **POWER MOSFET** is connected to the **POWER DIODE** and the **POWER INDUCTOR**. The **POWER DIODE** is connected to the **POWER INDUCTOR** and the **POWER CAPACITOR**.
- Feedback and Reference:** The **POWER INDUCTOR** is connected to the **POWER CAPACITOR** and the **POWER OUTPUT**. The **POWER CAPACITOR** is connected to the **POWER OUTPUT** and the **POWER GND**. The **POWER OUTPUT** is connected to the **POWER GND** and the **POWER SENSE** block. The **POWER SENSE** block is connected to the **POWER GND** and the **POWER SENSE** block. The **POWER SENSE** block is connected to the **POWER SENSE** block and the **POWER SENSE** block.
- Reference and Soft-Start:** A **CURRENT DAC** block is connected to the **POWER SENSE** block and the **POWER SENSE** block. The **CURRENT DAC** block is connected to the **POWER SENSE** block and the **POWER SENSE** block.

## Control Architecture

The IC implements an advanced valley current-mode control algorithm that supports all multi-layer ceramic chip (MLCC) output capacitors and fast transient response. In steady state, it operates at a fixed switching frequency. When loading transients, the switching frequency speeds up to minimize the output voltage undershoot. Likewise, when unloading transients, the switching frequency slows down to minimize the output voltage overshoot.

Voltage regulation is achieved by modulating the low-side on-time, comparing the difference between the feedback and reference voltages with the low-side current-sense signal using Maxim's proprietary integrated current-sense technology. Once the PWM modulator forces a low-to-high transition, the high-side switch is enabled for a fixed time, after which the low-side switch is turned on again. An error amplifier with an integrator is used to maintain zero-droop operation. The integrator has a transient recovery time constant of 20 $\mu$ s (typ).

The switching frequency is determined by the high-side on-time, as shown in Equation 1.

**Equation 1:**

$$f_{SW} = \frac{1}{t_{H\_ON}} \times \frac{V_{OUT}}{V_{DDH}}$$

where:

$f_{SW}$  = Switching frequency (MHz)

$t_{H\_ON}$  = On-period for high-side switch ( $\mu$ s)

$V_{OUT}$  = Output voltage (V)

$V_{DDH}$  = Input voltage (V)

The  $t_{H\_ON}$  high-side on-time is controlled by the IC to be proportional to the duty cycle so that the resulting switching frequency is independent of supply voltage and output voltage.

**Equation 2:**

$$t_{H\_ON} \propto \frac{V_{OUT}}{V_{DDH}}$$

The  $t_{H\_ON}$  pulse width is clamped to a minimum of 50ns (after  $t_{SS}$ ) and a maximum of 2 $\mu$ s to prevent any unexpected operation during extreme  $V_{OUT}$  conditions.

**Voltage-Regulator Enable and Turn-On Sequencing**

The startup timing is shown in [Figure 1](#). After  $V_{DDH}$  is applied, the IC goes through an initialization time ( $t_{INIT}$ ) that takes up to 308 $\mu$ s. After initialization, OE is read. Once OE is high for more than the 16 $\mu$ s OE filter time ( $t_{OE}$ ), BST charging starts and is performed for 8 $\mu$ s ( $t_{BST}$ ), and then the soft-start ramp begins. The soft-start ramp time ( $t_{SS}$ ) can be 0.75ms, 1.5ms, 3ms, or 6ms depending on the user's programmed value.  $V_{OUT}$  ramps up linearly during the soft-start ramp time. If there are no faults, the STAT pin is released from being held low after the

completion of the soft-start ramp time plus the user-programmable STAT blanking time ( $t_{STAT}$ ) of 125 $\mu$ s or 2ms. If OE is pulled low, the IC shuts down.

Alternatively, the IC can be enabled by sending a PMBus Operate command. This raises the internal Operation signal, which is OR'd with the OE pin to create an internal OE signal. Therefore, when either the OE pin or the internal Operate signal go high, startup is initiated, but it takes both to be low to shut the part down.

**Soft-Start Control**

The initial output voltage behavior is determined by a linear ramp of the internal reference voltage from zero to the final value ( $t_{SS}$  in [Figure 1](#)). The ramp time ( $t_{SS}$ ) is programmable from 0.75ms to 6ms.

If the regulator is enabled when the output voltage has a residual voltage, the system will not regulate until the reference voltage ramps above this residual value. In this case, the  $t_{OE}$  (OE valid to onset of regulation) specification is extended by the time required for the desired voltage start-up ramp to reach the actual residual output voltage, but the time to reach the steady-state output voltage is unchanged.

If the residual voltage is higher than the set output voltage, neither the high-side or low-side switch is turned on by the end of  $t_{SS}$ . Under these conditions, switching begins after  $t_{SS}$ .

The MAX20734 exhibits a non-linearity during startup. This behavior is normal and does not have an adverse effect on system operation. With the circuit of [Figure 6](#), the typical nonlinearity is 55mV with  $R_{GAIN} = 0.8\text{mV/A}$  or 1.6mV/A, 330mV with  $R_{GAIN} = 3.2\text{mV/A}$ , and 480mV with  $R_{GAIN} = 6.4\text{mV/A}$ . The nonlinearity gets proportionately smaller as  $C_{OUT}$  increases.

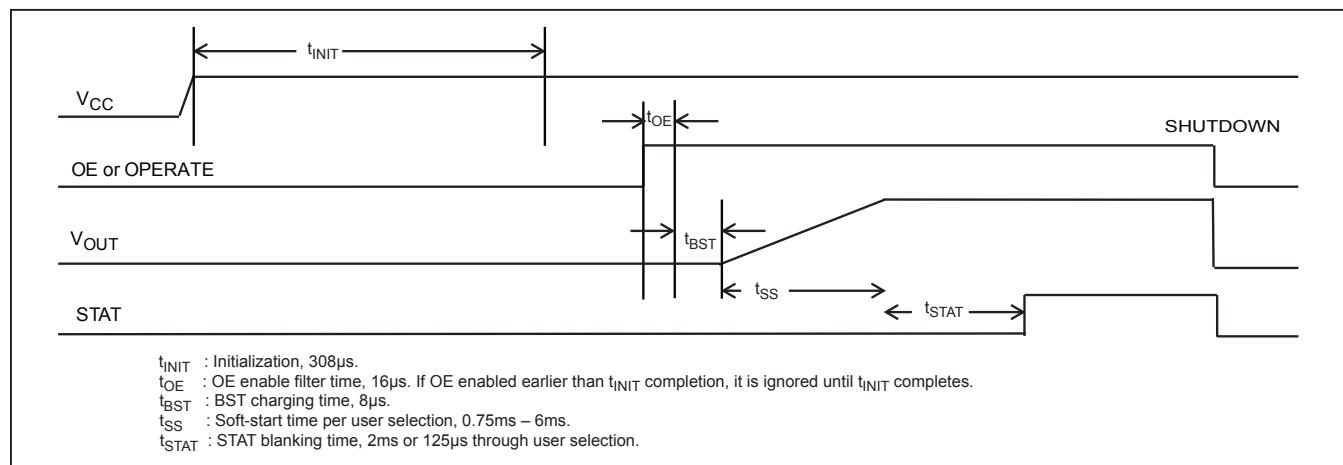


Figure 1. Startup Timing

Remote Output-Voltage Sensing

To ensure the most accurate sensing of the output voltage, a differential voltage-sense topology is used, with a negative remote-sense pin provided. Point-of-load (PoL) sensing compensates for voltage drops between the output of the regulator and its load and provides the highest regulation accuracy. The voltage-sensing circuit features excellent common-mode rejection to further improve load voltage regulation.

Protection and Status Operation

Output-Voltage Protection

The feedback voltage is continuously monitored for both undervoltage and overvoltage conditions. The typical fault-detection threshold is 13% above and 9% below the reference voltage (see the [Electrical Characteristics](#) table). If the output voltage falls below the power-good protection (PWRGD) threshold beyond the filter time, the STAT output goes low, but the system continues to operate, attempting to maintain regulation.

If the output voltage rises above the overvoltage protection (OVP) threshold beyond the filter time, the STAT pin is lowered and the system shuts down until the output voltage falls within the valid range.

Current Limiting and Short-Circuit Protection

The regulator’s valley current-mode control architecture provides inherent current limiting and short-circuit protection. The bottom switch’s instantaneous current is monitored using integrated current sensing and is controlled on a cycle-by-cycle basis within the control block.

Current clamping occurs when the minimum instantaneous (“valley”) low-side switch current level exceeds

the OCP threshold current, as shown in [Figure 2](#). In this situation, turn-on of the high-side switch is prevented until the current falls below the threshold level. Since the inductor valley current is the controlled parameter, the average current delivered during positive current clamping remains a function of several system-level parameters. Note that  $I_{OCP}$  has hysteresis and the value drops down to  $I_{OCP2}$  once it has been triggered (see [Figure 2](#)).

Undervoltage Lockout (UVLO)

The regulator internally monitors  $V_{DDH}$  with a UVLO circuit. When the input supply voltage is below the UVLO threshold, the regulator stops switching, and the STAT pin is driven low. For UVLO levels, see the [Electrical Characteristics](#) table.

Overtemperature Protection (OTP)

The OTP-level default is 150°C and can be set to 130°C over PMBus. If the die temperature reaches the OTP level during operation, the regulator is disabled and the STAT pin is driven low. Overtemperature is a nonlatching fault, with the hysteresis shown in the [Electrical Characteristics](#) table.

Table 1. Summary of Fault Actions

FAULT	ACTION
Power Good (Output Undervoltage)	STAT LOW
Output OVP	STAT LOW, Shutdown and Restart
Overtemperature	STAT LOW, Shutdown and Restart
Supply Fault ( $V_{DDH\_UVLO}$ , $V_{CC\_UVLO}$ )	STAT LOW, Shutdown and Restart
BST Fault	STAT LOW, Shutdown and Restart

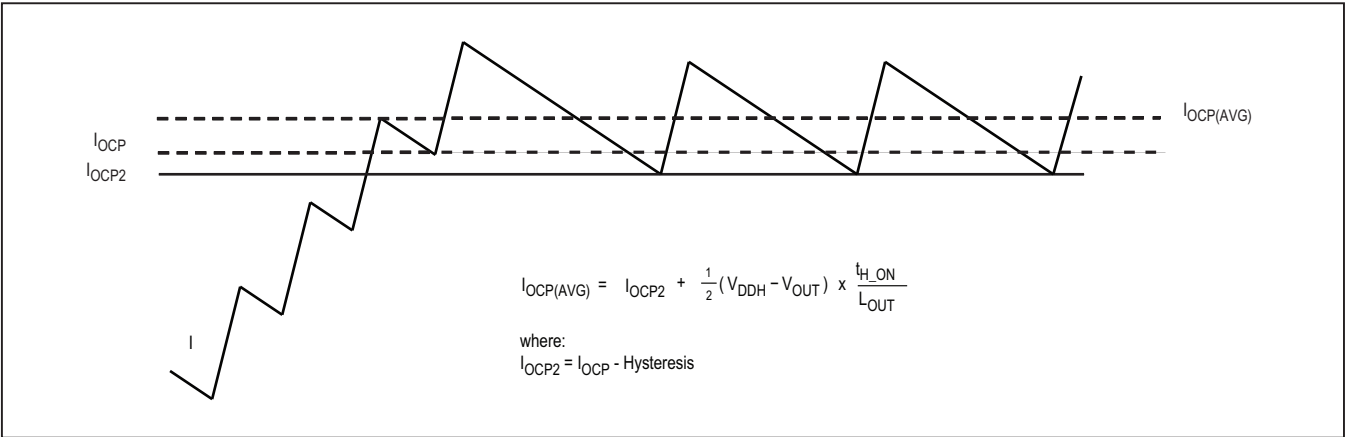


Figure 2. Inductor Current During Current Limiting

**Regulator Status (STAT)**

The STAT signal provides an open-drain output consistent with CMOS logic levels, which indicates whether the regulator is functioning properly. An external pullup resistor is required for connecting STAT to  $V_{CC}$  or another 1.8V or 3.3V supply.

The STAT pin is low while the regulator is disabled and goes high after the startup ramp is completed, plus the programmed  $t_{STAT}$  blanking interval if the output voltage is within the PWRGD/OVP regulation window. The STAT pin is an open-drain output and is 3.3V tolerant. The pin remains low when  $V_{DDH}$  is not present.

The STAT pin is driven low when one or more of the following conditions occurs:

- PWRGD fault (see the [Output-Voltage Protection](#) section)
- $V_{SENSE}$ - pin is left unconnected or shorted to  $V_{DDH}$
- Die temperature exceeds the temperature shutdown threshold shown in the [Electrical Characteristics](#) table
- OVP circuit detects that the output voltage is above the tolerance limit
- Supply voltage drops below the UVLO threshold
- Fault detected on the BST node, such as shorted or open bootstrap capacitor

The ensuing startup follows the same timing shown in [Figure 1](#).

**Table 2. PGMA Pin R\_SELA Values**

NO.	R (k $\Omega$ ) $\pm 1\%$	SOFT-START TIME (mS)	PMBus SLAVE ADDRESS (1010_xxx)
1	1.78	3	1010 000b
2	2.67	3	1010 001b
3	4.02	3	1010 010b
4	6.04	3	1010 011b
5	9.09	3	1010 100b
6	13.3	3	1010 101b
7	20	3	1010 110b
8	30.9	3	1010 111b
9	46.4	1.5	1010 000b
10	71.5	1.5	1010 001b
11	107	1.5	1010 010b
12	162	1.5	1010 011b

**PGMA and PGMB Pin Functionality**

The PGMA and PGMB pins are used to set up some of the key programmable features of the regulator IC. A resistor and capacitor are connected to the PGMA/B pins and their values are read during power-up initialization (e.g., power must be cycled to re-read the values).

The parasitic loading on the PGMA and PGMB pins must be limited to less than 20pF and greater than 20m $\Omega$  to avoid interfering with the R\_SEL and C\_SEL decoding.

**Table 3. PGMA Pin C\_SELA Capacitor Values**

NO.	C (pF) $\pm 20\%$	$V_{BOOT}$ (V)
1	Open	0.6484
2	220	0.8984
3	1000	1

**Table 4. PGMB Pin R\_SELB Values**

NO.	R (k $\Omega$ ) $\pm 1\%$	R <sub>GAIN</sub> (m $\Omega$ )	OCP SETTING*
1	1.78	0.8	0
2	2.67	0.8	1
3	4.02	0.8	2
4	6.04	0.8	3
5	9.09	3.2	0
6	13.3	3.2	1
7	20	3.2	2
8	30.9	3.2	3
9	46.4	1.6	0
10	71.5	1.6	1
11	107	1.6	2
12	162	1.6	3

\*See the [Electrical Characteristics](#) table for values.

**Table 5. PGMB Pin C\_SELB Capacitor Values**

NO.	C (pF) $\pm 20\%$	$f_{SW}$ FREQUENCY (kHz)
1	Open	400
2	220	600
3	1000	800



**PMBus Commands**

A summary of PMBus commands is shown in [Table 6](#). PMBus communication can be initiated as soon as  $V_{CC}$  is valid (after  $t_{INIT}$ , [Figure 1](#)), regardless of the state of the OE and STAT pins. For more information, refer to AN6209: *MAX20734 PMBus Application Note*.

**Table 6. Summary of PMBus Commands**

COMMAND CODE	COMMAND NAME	TYPE*	NO. OF DATA BYTES
01h	OPERATION	RW	1
02h	ON_OFF_CONFIG	RO	1
03h	CLEAR_FAULTS	WO	0
10h	WRITE_PROTECT	RW	1
1Bh	PMBALERT_MASK	RW	2
20h	VOUT_MODE	RO	1
21h	VOUT_COMMAND	RW	2
24h	VOUT_MAX	RW	2
78h	STATUS_BYTE	RO	1
79h	STATUS_WORD	RO	2
7Ah	STATUS_VOUT	RO	1
7Bh	STATUS_IOUT	RO	1
7Ch	STATUS_INPUT	RO	1

**PMBus Telemetry**

The IC provides input and output voltage, output current, and junction-temperature telemetry. Output voltage is measured at the  $V_{SENSE+/-}$  pins. Therefore, if there is a divider in the feedback, the measurement is scaled by the divide ratio. For range and accuracy specifications, see the [Electrical Characteristics](#) table. For data format, refer to AN6209: *MAX20734 PMBus Application Note*.

COMMAND CODE	COMMAND NAME	TYPE*	NO. OF DATA BYTES
7Dh	STATUS_TEMPERATURE	RO	1
7Eh	STATUS_CML	RO	1
80h	STATUS_MFR_SPECIFIC	RO	1
88h	READ_VIN	RO	2
8Bh	READ_VOUT	RO	2
8Ch	READ_IOUT	RO	2
8Dh	READ_TEMPERATURE_1	RO	2
99h	MFR_ID	BLK	4
9Bh	MFR_REVISION	BLK	1
D1h	MFR_VOUT_MIN	RW	2
D2h	MFR_DEVSET1	RW	2
D3h	MFR_DEVSET2	RW	2

\*RW = Read/Write, WO = Write Only, RO = Read Only, and BLK = Block.

## Reference Design

A typical application schematic is shown in [Figure 3](#), and optimum component values for common output voltages are shown in [Table 7](#).

## Output-Voltage Setting

If an output voltage not listed in [Table 7](#) is required, calculate new values for  $R_{FB1}$  and  $R_{FB2}$  (as discussed below) and use the other circuit values of the closest output voltage in [Table 7](#), or calculate them as shown below.

## Average Input Current Limit

The input current of  $V_{DDH}$  is given by Equation 3.  $V_{OUT}$ ,  $I_{OUT}$ , and  $V_{DDH}$  should be properly chosen so that the average input current does not exceed 6A ( $I_{VDDH\_MAX}$ ).

## Equation 3:

where:

$$I_{VDDH} = \frac{V_{OUT} \times I_{OUT}}{V_{DDH} \times \eta}$$

$V_{OUT}$  = Output voltage

$I_{OUT}$  = Output current

$V_{DDH}$  = Input voltage

$\eta$  = Efficiency (refer to the [Typical Operating Characteristics](#) section)

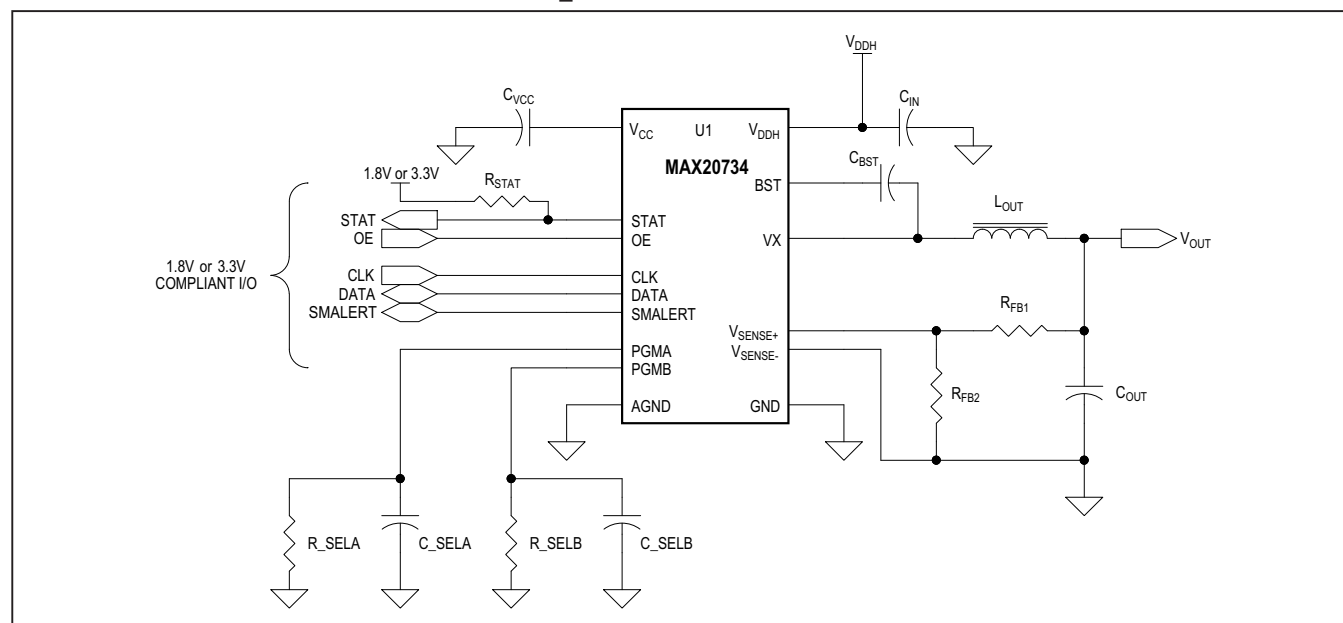


Figure 3. Typical Application Circuit

Table 7. Reference Design Component Values

$V_{OUT}$ (V)	$R_{FB1}$ (k $\Omega$ )	$R_{FB2}$ (k $\Omega$ )	$R_{SELA}$ (k $\Omega$ )	$C_{SELA}$ (pF)	$R_{SELB}$ (k $\Omega$ )	$C_{SELB}$ (pF)	$R_{GAIN}$ (m $\Omega$ )	$V_{REF}$ (V)	$f_{sw}$ (kHz)	$L_{OUT}$ (nH)	$C_{OUT}$
0.6484	1	Open	1.78	Open	107	Open	1.6	0.6484	400	170	12 x 100 $\mu$ F + 1 x 22 $\mu$ F
0.8	1.37	5.9	1.78	Open	71.5	Open	1.6	0.6484	400	170	10 x 100 $\mu$ F + 1 x 22 $\mu$ F
1	1.87	3.48	1.78	Open	71.5	Open	1.6	0.6484	400	170	9 x 100 $\mu$ F + 1 x 22 $\mu$ F
1.2	1.74	2.05	1.78	Open	71.5	Open	1.6	0.6484	400	170	9 x 100 $\mu$ F + 1 x 22 $\mu$ F
1.8	3.09	1.74	1.78	Open	71.5	220	1.6	0.6484	600	170	9 x 100 $\mu$ F + 1 x 22 $\mu$ F
3.3	5.62	1.37	1.78	Open	162	220	1.6	0.6484	600	210	9 x 100 $\mu$ F + 1 x 22 $\mu$ F
5.0	7.15	1.07	1.78	Open	107	220	1.6	0.6484	600	210	9 x 100 $\mu$ F + 1 x 22 $\mu$ F

**Note:** For input caps, see the [Input Capacitor Selection](#) section.

The output voltage is set by the  $V_{REF}$  DAC and divider ratio of resistors  $R_{FB1}$  and  $R_{FB2}$  per Equation 4. The IC regulates the  $V_{SENSE+}$  pin to the reference voltage ( $V_{REF}$ ) set by the DAC. Upon power-up, the DAC voltage initializes to one of the user-selectable  $V_{BOOT}$  voltages. Using PMBus, the DAC can also be set to any voltage from 0.6016V to 1V with 3.9mV resolution, as shown in Table 8. The divider resistors are chosen to give the correct output voltage and to have an approximate parallel resistance of  $R_{PAR} = 1k\Omega$  for best common-mode rejection of the error amplifier. In applications requiring less than 10mV peak-to-peak output voltage ripple, setting a lower DAC reference voltage such as 0.6484V or less is recommended because the part will have less DAC voltage noise.

**Equation 4:**

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where  $V_{REF} = 0.6016V$  to  $1V$  (set by DAC).

The divider resistors are then given by Equation 5.

**Equation 5:**

$$R_{FB1} = V_{OUT} \times \left(\frac{R_{PAR}}{V_{REF}}\right)$$

$$R_{FB2} = R_{FB1} \times \left(\frac{R_{PAR}}{R_{FB1} - R_{PAR}}\right)$$

where:

$R_{FB1}$  = Top divider resistor

$R_{FB2}$  = Bottom divider resistor

$R_{PAR}$  = Desired parallel resistance of  $R_{FB1}$  and  $R_{FB2}$

$V_{OUT}$  = Output voltage

$V_{REF}$  = Reference voltage = 0.6016V to 1V (set by DAC)

**Table 8. Voltage vs. PMBus VOUT\_COMMAND**

VOUT COMMAND [9:0] (decimal)	VOLTAGE (V)	ACCURACY (+/-)	VOUT COMMAND [9:0] (decimal)	VOLTAGE (V)	ACCURACY (+/-)	VOUT COMMAND [9:0] (decimal)	VOLTAGE (V)	ACCURACY (+/-)
307	0.6016	1.2%	325	0.6367	1.1%	343	0.6719	1.0%
308	0.6016	1.2%	326	0.6367	1.1%	344	0.6719	1.0%
309	0.6055	1.2%	327	0.6406	1.0%	345	0.6758	1.0%
310	0.6055	1.2%	328	0.6406	1.0%	346	0.6758	1.0%
311	0.6094	1.2%	329	0.6445	1.0%	347	0.6797	1.0%
312	0.6094	1.2%	330	0.6445	1.0%	348	0.6797	1.0%
313	0.6133	1.2%	331	0.6484	1.0%	349	0.6836	1.0%
314	0.6133	1.2%	332	0.6484	1.0%	350	0.6836	1.0%
315	0.6172	1.1%	333	0.6523	1.0%	351	0.6875	1.0%
316	0.6172	1.1%	334	0.6523	1.0%	352	0.6875	1.0%
317	0.6211	1.1%	335	0.6563	1.0%	353	0.6914	1.0%
318	0.6211	1.1%	336	0.6563	1.0%	354	0.6914	1.0%
319	0.6250	1.1%	337	0.6602	1.0%	355	0.6953	1.0%
320	0.6250	1.1%	338	0.6602	1.0%	356	0.6953	1.0%
321	0.6289	1.1%	339	0.6641	1.0%	357	0.6992	1.0%
322	0.6289	1.1%	340	0.6641	1.0%	358	0.6992	1.0%
323	0.6328	1.1%	341	0.6680	1.0%	359	0.7031	1.0%
324	0.6328	1.1%	342	0.6680	1.0%	360	0.7031	1.0%

Table 8. Voltage vs. PMBus VOUT\_COMMAND (continued)

VOUT COMMAND [9:0] (decimal)	VOLTAGE (V)	ACCURACY (+/-)	VOUT COMMAND [9:0] (decimal)	VOLTAGE (V)	ACCURACY (+/-)	VOUT COMMAND [9:0] (decimal)	VOLTAGE (V)	ACCURACY (+/-)
361	0.7070	1.0%	396	0.7734	1.0%	431	0.8438	1.0%
362	0.7070	1.0%	397	0.7773	1.0%	432	0.8438	1.0%
363	0.7109	1.0%	398	0.7773	1.0%	433	0.8477	1.0%
364	0.7109	1.0%	399	0.7813	1.0%	434	0.8477	1.0%
365	0.7148	1.0%	400	0.7813	1.0%	435	0.8516	1.0%
366	0.7148	1.0%	401	0.7852	1.0%	436	0.8516	1.0%
367	0.7188	1.0%	402	0.7852	1.0%	437	0.8555	1.0%
368	0.7188	1.0%	403	0.7891	1.0%	438	0.8555	1.0%
369	0.7227	1.0%	404	0.7891	1.0%	439	0.8594	1.0%
370	0.7227	1.0%	405	0.7930	1.0%	440	0.8594	1.0%
371	0.7266	1.0%	406	0.7930	1.0%	441	0.8633	1.0%
372	0.7266	1.0%	407	0.7969	1.0%	442	0.8633	1.0%
373	0.7305	1.0%	408	0.7969	1.0%	443	0.8672	1.0%
374	0.7305	1.0%	409	0.8008	1.0%	444	0.8672	1.0%
375	0.7344	1.0%	410	0.8008	1.0%	445	0.8711	1.0%
376	0.7344	1.0%	411	0.8047	1.0%	446	0.8711	1.0%
377	0.7383	1.0%	412	0.8047	1.0%	447	0.8750	1.0%
378	0.7383	1.0%	413	0.8086	1.0%	448	0.8750	1.0%
379	0.7422	1.0%	414	0.8086	1.0%	449	0.8789	1.0%
380	0.7422	1.0%	415	0.8125	1.0%	450	0.8789	1.0%
381	0.7461	1.0%	416	0.8125	1.0%	451	0.8828	1.0%
382	0.7461	1.0%	417	0.8164	1.0%	452	0.8828	1.0%
383	0.7500	1.0%	418	0.8164	1.0%	453	0.8867	1.0%
384	0.7500	1.0%	419	0.8203	1.0%	454	0.8867	1.0%
385	0.7539	1.0%	420	0.8203	1.0%	455	0.8906	1.0%
386	0.7539	1.0%	421	0.8242	1.0%	456	0.8906	1.0%
387	0.7578	1.0%	422	0.8242	1.0%	457	0.8945	1.0%
388	0.7578	1.0%	423	0.8281	1.0%	458	0.8945	1.0%
389	0.7617	1.0%	424	0.8281	1.0%	459	0.8984	1.0%
390	0.7617	1.0%	425	0.8320	1.0%	460	0.8984	1.0%
391	0.7656	1.0%	426	0.8320	1.0%	461	0.9023	1.0%
392	0.7656	1.0%	427	0.8359	1.0%	462	0.9023	1.0%
393	0.7695	1.0%	428	0.8359	1.0%	463	0.9063	1.0%
394	0.7695	1.0%	429	0.8398	1.0%	464	0.9063	1.0%
395	0.7734	1.0%	430	0.8398	1.0%	465	0.9102	1.0%

Table 8. Voltage vs. PMBus VOUT\_COMMAND (continued)

VOUT COMMAND [9:0] (decimal)	VOLTAGE (V)	ACCURACY (+/-)	VOUT COMMAND [9:0] (decimal)	VOLTAGE (V)	ACCURACY (+/-)	VOUT COMMAND [9:0] (decimal)	VOLTAGE (V)	ACCURACY (+/-)
466	0.9102	1.0%	482	0.9414	1.0%	498	0.9727	1.0%
467	0.9141	1.0%	483	0.9453	1.0%	499	0.9766	1.0%
468	0.9141	1.0%	484	0.9453	1.0%	500	0.9766	1.0%
469	0.9180	1.0%	485	0.9492	1.0%	501	0.9805	1.0%
470	0.9180	1.0%	486	0.9492	1.0%	502	0.9805	1.0%
471	0.9219	1.0%	487	0.9531	1.0%	503	0.9844	1.0%
472	0.9219	1.0%	488	0.9531	1.0%	504	0.9844	1.0%
473	0.9258	1.0%	489	0.9570	1.0%	505	0.9883	1.0%
474	0.9258	1.0%	490	0.9570	1.0%	506	0.9883	1.0%
475	0.9297	1.0%	491	0.9609	1.0%	507	0.9922	1.0%
476	0.9297	1.0%	492	0.9609	1.0%	508	0.9922	1.0%
477	0.9336	1.0%	493	0.9648	1.0%	509	0.9961	1.0%
478	0.9336	1.0%	494	0.9648	1.0%	510	0.9961	1.0%
479	0.9375	1.0%	495	0.9688	1.0%	511	1.0000	1.0%
480	0.9375	1.0%	496	0.9688	1.0%	512	1.0000	1.0%
481	0.9414	1.0%	497	0.9727	1.0%	—	—	—

**Notes:** The repeated voltage values in the table are due to ignoring the LSB in hardware. The available  $V_{BOOT}$  values are highlighted in gray. Voltages shown are referenced to the sense pins. Actual  $V_{OUT}$  can be scaled by a voltage-divider in the feedback.

### Control-Loop Stability

The IC uses valley current-mode control which is stabilized by selecting appropriate values of  $C_{OUT}$  and  $R_{GAIN}$ . No compensation network is required. For stability, the loop bandwidth (BW) should be 100kHz or less. Consider the case of using MLCC output capacitors that have nearly ideal impedance characteristics in the frequency range of interest with negligible ESR and ESL. The loop bandwidth can be approximated by breaking the loop into gain terms as outlined below.

- 1) The IC's valley current-mode control scheme has an effective transconductance gain of  $1/R_{GAIN}$ .
- 2) For MLCC capacitors, the output capacitors contribute an impedance gain of  $1/(2 \times \pi \times C_{OUT} \times f)$ .
- 3) The feedback-divider contributes an attenuation of  $K_{DIV} = R_{FB2}/(R_{FB1} + R_{FB2})$ .
- 4) An inherent high-frequency pole located at 150kHz.

When the BW is 100kHz or less, the high-frequency pole can be ignored and the approximate loop gain and BW are given by Equation 6.

Equation 6:

$$|LOOP\_GAIN(f)| = \frac{K_{DIV}}{2 \times \pi \times R_{GAIN} \times C_{OUT} \times f}$$

$$BW = \frac{K_{DIV}}{2 \times \pi \times R_{GAIN} \times C_{OUT}}$$

OR

$$BW = \frac{1}{2 \times \pi \times R_{GAIN\_EFF} \times C_{OUT}}$$

where:

$$R_{GAIN\_EFF} = R_{GAIN}/K_{DIV}$$

For stability,  $R_{GAIN}$  and  $C_{OUT}$  should be chosen so that  $BW < 100\text{kHz}$ .

The available  $R_{GAIN}$  settings are shown in Table 4. When choosing which  $R_{GAIN}$  setting to use, one should consider that while higher  $R_{GAIN}$  allows the loop to be stabilized with less  $C_{OUT}$ , less  $C_{OUT}$  generally results in higher ripple and larger transient overshoot and undershoot, so there needs to be a balance.

### Integrator

The IC has an integrator included in its error amplifier, which was ignored in the above equations for simplicity. The integrator only adds gain at low frequencies, so it does not really effect the loop BW calculation. The purpose of the integrator is to improve load regulation. The integrator adds a factor of  $(1/t_{REC} + s)/s$  to the loop gain.

### Step Response

$R_{GAIN\_EFF}$  is important because it determines the small-signal transient response of the regulator. When a load step is applied that does not exceed the slew-rate capability of the inductor current, the regulator responds linearly and  $V_{OUT}$  temporarily changes by the amount of  $V_{OUT\_ERROR}$  (see Equation 7).

Equation 7:

$$V_{OUT\_ERROR} = I_{STEP} \times R_{GAIN\_EFF}$$

The integrator causes  $V_{OUT}$  to recover to the nominal value with a time constant of  $t_{REC} = 20\mu\text{s}$ . The regulator can be modeled to a first-order by the averaged small-signal equivalent circuit shown in Figure 4. Here,  $V_{EQ}$  is an ideal voltage source,  $R_{EQ}$  is an equivalent lossless resistance created by the control-loop action, and  $L_{EQ}$  is an equivalent inductance. Note that  $L_{EQ}$  is not the same as the actual  $L_{OUT}$  inductor that has been absorbed into the model.  $C_{OUT}$  is the actual output capacitance.

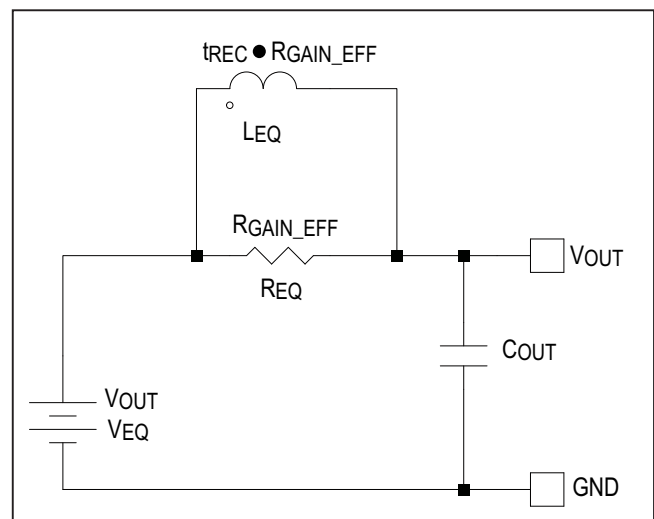


Figure 4. Averaged Small-Signal Equivalent Circuit of Regulator

**Note:** The large-signal transient response is approximately the larger between the  $V_{OUT\_ERROR}$  and the unloading transient.

**Output-Capacitor ESR**

In the above control-loop discussion, the case of MLCC output capacitors has been considered. Another case worth mentioning is the use of output capacitors with more significant ESR. This can be considered as long as the capacitors are rated to handle the inductor current ripple and expected surge currents. Thus far, it has been assumed that  $C_{OUT}$  is comprised of MLCCs and the net ESR is negligible compared to  $R_{GAIN}/K_{DIV}$ . If the net ESR of the  $C_{OUT}$  bank is not negligible compared to  $R_{GAIN}/K_{DIV}$ , the inductor current ripple is effectively sensed by the ESR and adds to the  $R_{GAIN\_EFF}$ , as shown in Equation 8.

**Equation 8:**

$$R_{GAIN\_EFF} = \frac{R_{GAIN}}{K_{DIV}} + ESR$$

The capacitor's ESR also introduces a zero into the loop gain. The inherent high-frequency pole helps to compensate this zero. For a more in-depth view of the effect of circuit values on regulator performance, the Maxim Simplis model and MAX20734 evaluation kit can be used. It is recommended to simulate and/or test regulator performance when using values other than the recommended component values.

The performance data shown in the [Typical Operating Characteristics](#) section was taken using the MAX20734 evaluation kit and component values in [Table 7](#). For most applications, these are the optimum values to use. [Table 9](#), [Table 10](#), and [Table 11](#) show suitable part numbers for input and output capacitors and the inductor.

**Table 9. Recommended Inductors**

COMPANY	VALUE (nH)	I <sub>SAT</sub> (A)	R <sub>DC</sub> (mΩ)	FOOTPRINT (mm)	HEIGHT (mm)	PART NUMBER	WEBSITE
Cooper	170	60	0.29	10.4 x 8.0	7.5	FP1007R3-R17-R	www.cooperindustries.com
Pulse	215	41	0.29	10.4 x 7.9	7.3	PA2607.211NL	www.pulseelectronics.com
Pulse	270	34	0.29	10.4 x 7.9	7.3	PA2607.271NL	www.pulseelectronics.com
Pulse	320	45	0.32	13.5 x 13.0	8.0	PA0513.321NLT	www.pulseelectronics.com
Pulse	440	30	0.32	13.5 x 13.0	8.0	PA0513.441NLT	www.pulseelectronics.com

**Table 10. MLCC Input Capacitors**

CASE SIZE	VALUE (μF)	TEMPERATURE RATING	VOLTAGE RATING	T (mm) (NOTE 1)	COMPANY	PART NUMBER
0603	1	X7S X7R	16V	0.8 (Note 2)	Murata TDK	GRM188C71C105KA12D C1608X7R1C105K
0805	2.2	X7R	25V 16V 16V	1.25 1.25 1.25	Murata TDK AVX	GRM21BR71E225KA73L C2012X7R1C225M 0805YC225MAT
0805	4.7	X7R	16V	1.25	Murata	GRM21BR71C475K
1206	4.7	X7R	16V	1.65	AVX Murata	1206YC475MAT GRM31CR71C475KA01L
1206	10	X7R	16V	1.65	Murata TDK AVX	GRM31CR71C106KAC7L C3216X7R1C106M 1206YC106MAT
1210	10	X7R	16V 25V	2.0 2.5	Murata TDK	GRM32DR71C106KA01L C3225X7R1E106M
1210	22	X7R	16V	2.45 2.5 2.5	AVX Murata TDK	1210YC226MAT GRM32ER71A476K C3225X7R1C226M

**Note 1:** T indicates nominal thickness.

**Note 2:** Indicates capacitors with nominal thickness smaller than the minimum FCQFN package thickness.

**Table 11. Recommended Output Capacitors**

COMPANY	VALUE (μF)	PART NUMBER	TEMPERATURE RATING	VOLTAGE RATING	CASE SIZE	T (mm) (Note 1)	WEBSITE
AVX Corp.	22	08054D226MAT2A	X5R	4V	0805	1.3	www.avxcorp.com
	22	12066D226MAT2A	X5R	6.3V	1206	1.65	
Murata	22	GRM21BR60J226ME39L	X5R	6.3V	0805	1.25	www.murata.co.jp
	22	GRM31CR60J226KE19L	X5R	6.3V	1206	1.6	
	22	GRM32DR60J226KA01L	X5R	6.3V	1210	2.0	
Panasonic	22	ECJ3YB0J226M	X5R	6.3V	1206	1.6	www.panasonic.com
	22	ECJHVB0J226M	X5R	6.3V	1206	0.85	
	22	ECJ3Y70J226M	X7R	6.3V	1206	1.65	
Taiyo Yuden	22	AMK212BJ226MG	X5R	4V	0805	1.25	www.taiyo-yuden.com
	22	JMK316BJ226ML	X5R	6.3V	1206	1.6	
	22	JMK325BJ226MY	X5R	6.3V	1210	1.9	
TDK Corp.	22	C2012X5R0J226M	X5R	6.3V	0805	1.25	www.component.tdk.com
	22	C3216X5R0J226M	X5R	6.3V	1206	1.6	
	22	C3225X5R0J226M	X5R	6.3V	1210	1.6	
	22	C3216X6S0J226M	X6S	6.3V	1206	1.6	

**Note 1:** T indicates nominal thickness.

## Inductor Selection

The output inductor has an important influence on the overall size, cost, and efficiency of the voltage regulator. Since the inductor is typically one of the larger components in the system, a minimum inductor value is particularly important in space-constrained applications. Smaller inductor values also permit faster transient response, reducing the amount of output cap needed to maintain transient tolerances.

For any buck regulator, the maximum current slew rate through the output inductor is given by Equation 9.

**Equation 9:**

$$\text{SlewRate} = \frac{dI_L}{dt} = \frac{V_L}{L_{OUT}}$$

where:

$I_L$  = Inductor current

$L_{OUT}$  = Output inductance

$V_L = V_{DDH} - V_{OUT}$  during high-side FET conduction and  $-V_{OUT}$  during low-side FET conduction

Equation 9 shows that larger inductor values limit the regulator's ability to slew current through the output inductor in response to step-load transients. Consequently, more output capacitors are required to supply (or store) sufficient charge to maintain regulation while the inductor current ramps up to supply the load.

In contrast, smaller inductor values increase the regulator's maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current. The peak-to-peak ripple current is given by Equation 10.

**Equation 10:**

$$I_{OUTRIPPLE} = \frac{t_{H\_ON} \times (V_{DDH} - V_{OUT})}{L_{OUT}}$$

where:

$t_{H\_ON}$  = High-side switch on-time (based on nominal  $V_{OUT}$ ) (see Equation 1)

$L_{OUT}$  = Output inductance

$V_{DDH}$  = Input voltage

$V_{OUT}$  = Output voltage

From Equation 10, for the same switching frequency and ripple current increases as  $L$  decreases. This increased ripple current results in increased AC losses, larger peak current, and for the same output capacitance, results in increased output voltage ripple.



$I_{OUTRIPPLE}$  should be set to 25% to 50% of the IC's rated output current. A suitable inductor value can then be found by solving Equation 10 for inductance as in Equation 11 and Equation 12.

**Equation 11:**

$$L_{OUT} = \frac{V_{OUT}(V_{DDH} - V_{OUT})}{V_{DDH} \times I_{OUTRIPPLE} \times f_{SW}}$$

Assuming  $I_{OUTRIPPLE} = 0.5 \times I_{OUT}$  for a typical inductor value, see Equation 12.

**Equation 12:**

$$L_{OUT} = \frac{V_{OUT}(V_{DDH} - V_{OUT})}{V_{DDH} \times (0.5 \times I_{OUT}) \times f_{SW}}$$

For a 25A regulator running at 400kHz, with  $V_{DDH} = 12V$  and  $V_{OUT} = 1V$ , Equation 13 shows the target value for the inductor.

**Equation 13:**

$$L_{OUT} = \frac{1 \times (12 - 1)}{12 \times 0.5 \times 25 \times 400000} \\ = 183nH$$

The saturation current rating of the inductor is another important consideration. At current limit, the peak inductor current is given in Equation 14.

**Equation 14:**

$$I_{PK} = I_{OCP} + I_{OUTRIPPLE}$$

where:

$I_{OCP}$  = Overcurrent protection trip point (see the [Electrical Characteristics](#) table and the [Current Limiting and Short-Circuit Protection](#) section)

$I_{OUTRIPPLE}$  = Peak-to-peak inductor current ripple, as defined above

For proper OCP operation of the regulator, it is important that  $I_{PK}$  never exceeds the saturation current rating of the inductor ( $I_{SAT}$ ). It is recommended that a margin of at least 20% is included between  $I_{PK}$  and  $I_{SAT}$ , as shown in Equation 15.

**Equation 15:**

$$I_{SAT} > 1.2 \times I_{PK}$$

Also, note that during a hard  $V_{OUT}$  short circuit,  $I_{OUTRIPPLE}$  increases due to  $V_{OUT}$  going to zero in Equation 10.

Finally, the power dissipation of the inductor influences the regulation efficiency. Losses in the inductor include core loss, DC resistance loss, and AC resistance loss. For the best efficiency, use inductors with core material exhibiting low loss in the range of 0.5MHz to 2MHz, and low-winding resistance.

[Table 9](#) provides a summary of the recommended inductor suppliers and part numbers.

### Output Capacitor Selection

The minimum recommended output capacitance for stability is described in the [Control-Loop Stability](#) section and is normally implemented using several 100μF 1206 (or similar) MLCCs. For low slew-rate transient loads,  $R_{GAIN\_EFF}$  determines the  $V_{OUT\_ERROR}$  for a given load step per the small-signal model, as discussed above. In this case,  $C_{OUT}$  has no effect on the  $V_{OUT\_ERROR}$ .

However, in the event that the slew rate of the load transient greatly exceeds the slew rate of the inductor current, the transient  $V_{OUT\_ERROR}$  may be larger than predicted by the small-signal model. In this case, the  $V_{OUT}$  loading and unloading transients can be approximated by taking the larger result between Equation 7 and Equation 16.

**Equation 16:**

$$LOADINGTRANSIENT(V) = \frac{L_{OUT} \times \left( I_{STEP} + \frac{I_{OUTRIPPLE}}{2} \right)^2}{2 \times C_{OUT} \times (V_{DDH} - V_{OUT})}$$

$$UNLOADINGTRANSIENT(V) = \frac{L_{OUT} \times \left( I_{STEP} + \frac{I_{OUTRIPPLE}}{2} \right)^2}{2 \times C_{OUT} \times V_{OUT}} \\ + I_{STEP} \times \frac{t_{H\_ON}}{C_{OUT}}$$

In order to meet an aggressive transient specification,  $C_{OUT}$  may have to be increased and/or  $L_{OUT}$  decreased; however, note that decreasing  $L_{OUT}$  results in larger inductor ripple current; thus, decreased efficiency and increased output ripple.

Output voltage ripple is another important consideration in the selection of output capacitors. For a buck regulator operating in CCM, the total voltage ripple across the output capacitor bank can be approximated as the sum of three voltage waveforms: 1) the triangle wave that results from multiplying the AC ripple current by the ESR, 2) the square wave that results from multiplying the ripple current slew rate by the ESL, and 3) the piecewise quadratic waveform that results from charging/discharging the output capacitor. Although the phasing of these three components impacts the total output ripple, a common approximation is to ignore the phasing and to find the upper bound of the peak-to-peak ripple by summing all three components, as shown in Equation 17.

**Equation 17:**

$$V_{P-P} = ESR(I_{OUTRIPPLE}) + ESL \left( \frac{V_{DDH}}{L_{OUT}} \right) + \left( \frac{I_{OUTRIPPLE}}{8 \times f_{SW} \times C_{OUT}} \right)$$

where:

ESR = Equivalent series resistance at the output

$I_{OUTRIPPLE}$  = Peak-to-peak inductor current ripple

ESL = High-frequency equivalent series inductance at output

$V_{DDH}$  = Input voltage

$L_{OUT}$  = Output inductance

$f_{SW}$  = Switching frequency

$C_{OUT}$  = Output capacitance

In a typical MAX20734 application with a bank of 0805, X5R, 6.3V, 22 $\mu$ F output capacitors, these three components are roughly equal.

The ESL effect of an output capacitor on output voltage ripple cannot be easily estimated from the resonant frequency so the high-frequency (10MHz or above) impedance of that capacitor should be used instead. PCB traces and vias in the  $V_{OUT}/GND$  loop contribute additional parasitic inductance.

The final considerations in the selection of output capacitors are ripple-current rating and power dissipation. Using a conservative design approach, the output capacitors should be designed to handle the maximum peak-to-peak AC ripple current experienced in the worst-case scenario. Because the recommended output capacitors have extremely low ESR values, they are typically rated well above the current and power stresses seen here. For

the triangular AC ripple current at the output, the total RMS current and power is given by Equation 18 and Equation 19.

**Equation 18:**

$$I_{RMS\_COUT} = \frac{I_{OUTRIPPLE}}{\sqrt{12}}$$

where:

$I_{OUTRIPPLE}$  = Peak-to-peak ripple current value

**Equation 19:**

$$P_{COUT} = I_{RMS\_COUT}^2 \times ESR$$

where:

ESR = Equivalent series resistance of the entire output capacitor bank

**Input Capacitor Selection**

The selection and placement of input capacitors are important considerations. High-frequency input capacitors serve to control switching noise. Bulk input capacitors are designed to filter the pulsed DC current that is drawn by the regulator. For the best performance, lowest cost, and smallest size of the MAX20734 systems, MLCC capacitors with 1210 or smaller case sizes, capacitance values of 47 $\mu$ F or smaller, 16V or 25V voltage ratings, and X5R or better temperature characteristics are recommended as bulk. The minimum recommended value of capacitance are 2 x 47 $\mu$ F (bulk) and 1.0 $\mu$ F + 0.1 $\mu$ F (high frequency). Smaller values of bulk capacitance can be used in direct proportion to the maximum load current.

It is recommended to choose the main MLCC input capacitance to control the peak-to-peak input-voltage ripple to 2% to 3% of its DC value in accordance with Equation 20.

**Equation 20:**

$$C_{IN} = \frac{I_{MAX} \times V_{OUT} \times (V_{DDH} - V_{OUT})}{(f_{SW} \times V_{DDH}^2 \times V_{INPP})}$$

where:

$C_{IN}$  = Input capacitance (MLCC)

$I_{MAX}$  = Maximum load current

$V_{DDH}$  = DC input voltage

$V_{OUT}$  = DC output voltage

$f_{SW}$  = Switching frequency

$V_{INPP}$  = Target peak-to-peak input-voltage ripple

Because the bulk input capacitors must source the pulsed DC input current of the regulator, the power dissipation and ripple current rating for these capacitors are far more important than that for the output capacitors. The RMS current that the input capacitor must withstand can be approximated using Equation 21.

**Equation 21:**

$$I_{\text{RMS\_CIN}} = \frac{I_{\text{LOAD}} \sqrt{V_{\text{OUT}} (V_{\text{DDH}} - V_{\text{OUT}})}}{V_{\text{DDH}}}$$

where:

$I_{\text{LOAD}}$  = Output DC load current

With an equivalent series resistance of the bulk input capacitor bank ( $\text{ESR}_{\text{CIN}}$ ), the total power dissipation in the input capacitors is given by Equation 22.

**Equation 22:**

$$P_{\text{CIN}} = I_{\text{RMS\_CIN}}^2 \times \text{ESR}_{\text{CIN}}$$

### Resistor Selection and its Effect on DC Output-Voltage Accuracy

$R_{\text{FB1}}$  and  $R_{\text{FB2}}$  set the output voltage, as described in Equation 4. The tolerance of these resistors affects the

accuracy of the set output voltage. Due to the form of Equation 4, the effect is higher at higher output voltages.

Figure 5 shows the effect of 0.1% tolerance resistors over a range of output voltages. For different tolerance resistors, multiply the output voltage error by the resistors' tolerances divided by 0.1% (e.g., for 0.5% tolerance resistors, multiply the output error shown by 5). To obtain accuracy over temperature, for a worst-case scenario, the temperature coefficients multiplied by the temperature range should be added to the tolerance (i.e., for 25ppm/°C resistors over a 50°C excursion, add 0.125% to the 25°C tolerance).

The error due to the voltage feedback resistors' tolerance ( $R_{\text{FB1}}$  and  $R_{\text{FB2}}$ ) should be added to the output-voltage tolerance due to the IC's feedback-voltage accuracy shown in the [Electrical Characteristics](#) table.

### Voltage Margining

Voltage margining can be achieved by changing the  $V_{\text{OUT}}$  setting through PMBus.  $V_{\text{OUT}}$  changes occur with a default linear slew rate of 1V/ms. The slew rate can be set to 1, 2, or 4mV/μs using the  $V_{\text{RATE}}$  bits. Refer to the AN6140: MAX20734 PMBus Application Note for details. If a voltage-divider is present in the feedback loop, the  $V_{\text{OUT}}$  slew rate will be scaled accordingly.

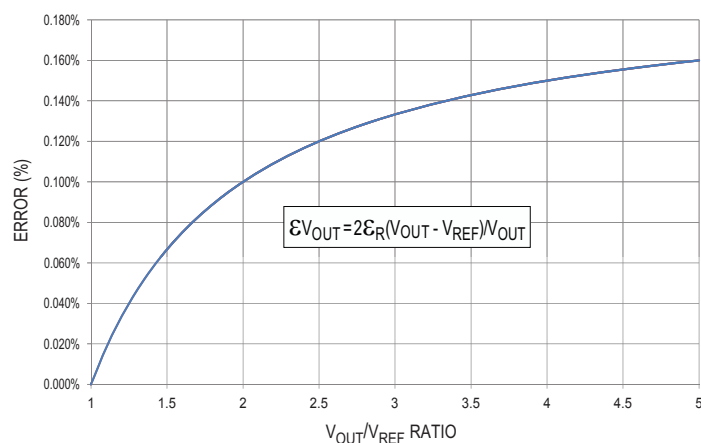


Figure 5. DC Accuracy Impact Showing Effect of 0.1% Tolerance for  $R_{\text{FB1}}$  and  $R_{\text{FB2}}$

### PCB Layout Guidelines

PCB layout can dramatically affect the performance of the regulator. A poorly designed board can degrade efficiency, noise performance, and even control-loop stability. At higher switching frequencies, layout issues are especially critical.

As a general guideline, the input capacitors and the output inductor should be placed in close proximity to the regulator IC, while the output capacitors should be lumped together as close as possible to the load. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance. Traces connecting the input capacitors and  $V_{DDH}$  (power input node) on the IC require particular attention since they carry currents with the largest RMS values and fastest slew rates. According to best practice, the input capacitors should be placed as close as possible to the input supply pins, with the smallest package high-frequency capacitor being the closest to the IC and no more than 60 mils from the IC pins. Preferably, there should be an uninterrupted ground plane located immediately underneath these high-frequency current paths, with the ground plane located no more than 8 mils below the top layer. By keeping the flow of this high-frequency AC current localized to a tight loop at the regulator, electro-magnetic interference (EMI) can be minimized.

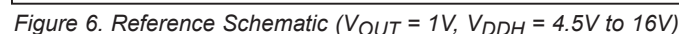
Voltage-sense lines should be routed differentially directly from the load points. The ground plane can be used as a shield for these or other sensitive signals to protect them from capacitive or magnetic coupling of high-frequency noise.

For remote-sense applications where the load and regulator IC are separated by a significant distance or impedance, it is important to place the majority of the output capacitors directly at the load. Ideally, for system stability, all the output capacitors should be placed as close as possible to the load. In remote-sense applications, common-mode filtering is necessary to filter high-frequency noise in the sense lines.

The following layout recommendations should be used for optimal performance:

- It is essential to have a low-impedance and uninterrupted ground plane under the IC and extended out underneath the inductor and output capacitor bank.
- Multiple vias are recommended for all paths that carry high currents (i.e., GND,  $V_{DDH}$ , VX). Vias should be placed close to the chip to create the shortest possible current loops. Via placement must not obstruct the flow of currents or mirror currents in the ground plane.
- A single via in close proximity to the chip should be used to tie the top layer AGND trace to the second layer ground plane, it must not be connected to the top power ground area.
- The feedback-divider and compensation network should be close to the IC to minimize the noise on the IC side of the divider.

Gerber files with layout information and complete reference designs can be obtained by contacting a Maxim account representative.



## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20734EPL+	-40°C to +125°C	15 FCQFN
MAX20734EPL+T	-40°C to +125°C	15 FCQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/17	Initial release	—

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