# MAX22194

# Quad Industrial Sink/Source Digital Input

## Product Highlights

- Software Configurable
  - Four Inputs Individually Configurable as Sink or Source
  - Type 1/3, Type 2, TTL, and Hi-Z (HTL) Modes
  - Wide Resistor-Settable Accurate Input Current Ranging from 0.5mA to 6.75mA
  - Programmable Glitch Filters
  - Extensive Diagnostics (Supply Voltage Monitoring, Temperature Alarms, PCB Fault Alarms, Thermal Shutdown)
  - Addressable or Daisy-Chain SPI to Reduce Isolation Channels
- Robust Solution
  - IEC 61000-4-2 ESD Airgap ±15kV and Contact ±8kV with Minimum 680Ω Pulse Resistor at Field Inputs
  - IEC 61000-4-5 Surge ±1.2kV/42Ω with Minimum 680Ω Pulse Resistor at Field Inputs
  - CRC Error Detection on SPI
  - -40°C to +125°C Operating Temperature
- Low-Power Dissipation
  - Operates from 8V to 36V Field Supply
  - Low-Supply Current 2mA Maximum
- Compact Solution
  - Integrated 5V, 20mA Linear Regulator
  - 2.5V to 5.5V Logic Interface
  - LED Driver Matrix or GPO Outputs
  - 5mm x 5mm 32-Pin TQFN Package

## Key Applications

- Programmable Logic Controllers
- Factory Automation
- Process Control

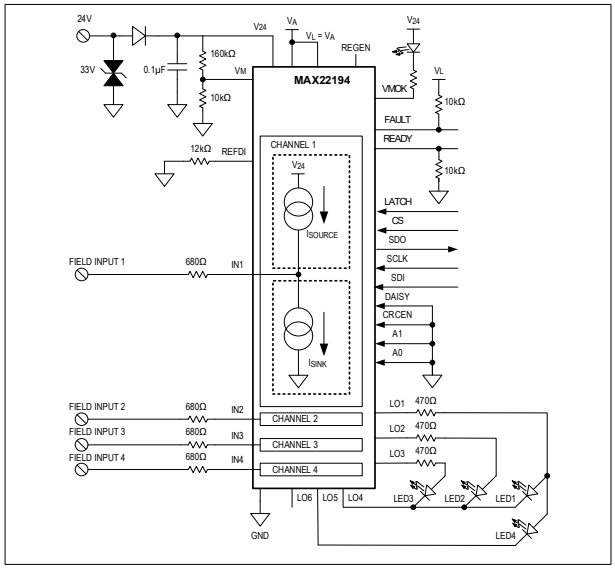
The MAX22194 is an industrial quad digital input that translates four industrial 24V or TTL level inputs to logic level outputs. The device has a serial interface allowing configuration and reading of serialized data through SPI.

The input channels are individually configurable as sinking (p-type) or sourcing (n-type) inputs. Current limiters on each digital input minimize power dissipation while ensuring compliance with the IEC 61131-2 standard. With a single current-setting resistor, the inputs are individually configurable for Type 1/3, Type 2, TTL, or HTL (high-impedance 24V levels). The current sinks or sources can be individually disabled.

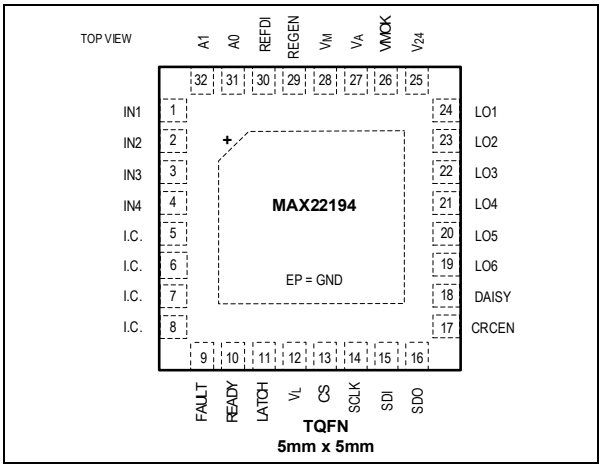
Every input channel has a programmable glitch/debounce filter.

The MAX22194 can be powered from a field supply from 8V up to 36V for sink/source operation and has an integrated 5V linear regulator that can provide up to 20mA of load current.

## Simplified Application Diagram




## Pin Description




***Ordering Information* appears at end of data sheet.**

*19-101861B; Rev 0; 3/24*

## Absolute Maximum Ratings

$V_{24}$ to GND ..... -0.3V to +70V

IN_ to GND..... -40V to +40V

($V_{24}$ – IN_) to GND ..... -40V to +70V

$\overline{VMOK}$ to GND.....-0.3V to ($V_{24}$ + 0.3)V

$V_A$, $V_L$ to GND..... -0.3V to +6V

**$V_M$ to GND**

$V_A \geq V_{A\_UVLO}$..... -0.3V to ($V_A$ + 0.3)V

$V_A < V_{A\_UVLO}$.....-0.3V to (Min(3.3, $V_{24}$) + 0.3)V

**REGEN to GND**

$V_A \geq V_{A\_UVLO}$..... -0.3V to ($V_A$ + 0.3)V

$V_A < V_{A\_UVLO}$.....-0.3V to (Min(3.3, $V_{24}$) + 0.3)V

**Digital Pins**

$\overline{CS}$, SCLK, SDI, $\overline{LATCH}$ to GND..... -0.3V to +6V

A1, A0 to GND ..... -0.3V to ($V_A$ + 0.3)V

DAISY, CRCEN to GND ..... -0.3V to +6V

$\overline{FAULT}$ to GND .....-0.3V to +6V

$\overline{READY}$, SDO to GND .....-0.3V to ($V_L$ + 0.3)V

**Analog Pins**

REFDI to GND .....-0.3V to ($V_A$ + 0.3)V

LO1–LO6 to GND .....-0.3V to ($V_A$ + 0.3)V

**Continuous Power Dissipation ($T_A$ = +70°C)**

Single-Layer Board (Derate 21.3°C/mW above +70°C) ..... 1702.1mW

Four-Layer Board (Derate 34.5°C/mW above +70°C) ..... 2758.6mW

**Temperature Ratings**

Operating Temperature Range..... -40°C to +125°C

Maximum Junction Temperature.....+150°C

Storage Temperature Range..... -60°C to +150°C

Lead Temperature (Soldering, 10s) .....+300°C

Soldering Temperature (Reflow) .....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

| PACKAGE TYPE | 32 TQFN |
|---|---|
| Package Code | T3255+8C |
| Outline Number | 21-0140 |
| Land Pattern Number | 90-0013 |
| **THERMAL RESISTANCE, SINGLE-LAYER BOARD** | |
| Junction-to-Ambient ($\theta_{JA}$) | 47°C/W |
| Junction-to-Case Thermal Resistance ($\theta_{JC}$) | 1.7°C/W |
| **THERMAL RESISTANCE, FOUR-LAYER BOARD** | |
| Junction-to-Ambient ($\theta_{JA}$) | 29°C/W |
| Junction-to-Case Thermal Resistance ($\theta_{JC}$) | 1.7°C/W |

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html.

For the latest package outline information and land patterns (footprints), go to https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

## Electrical Characteristics

($V_{24}$ = +8V to +36V, $V_L$ = +2.5V to +5.5V, $V_A$ = +3.0V to +5.5V, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $V_{24}$ = +24V, $V_L$ = +3.3V, $V_A$ = +5V, $T_A$ = +25°C) (*Note 1*)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **$V_{24}$ Power Supply (Device Powered by $V_{24}$ Pin)** | | | | | | |
| $V_{24}$ Supply Voltage | $V_{24}$ | Sink and TTL configuration | 8 | | 65 | V |
| | | Source configuration | 8 | | 36 | V |
| $V_{24}$ Undervoltage Lockout Threshold | $V_{24\_UVLO}$ | REGEN shorted to GND, $V_A$ = $V_L$ = 5V; $V_{24}$ rising | 7 | 7.45 | 7.75 | V |
| | | REGEN shorted to GND, $V_A$ = $V_L$ = 5V; $V_{24}$ falling | 6.5 | 7 | 7.5 | V |
| $V_{24}$ UVLO Threshold Hysteresis | $V_{24\_UVHYS}$ | | | 0.5 | | V |
| $V_{24}$ Supply Current | $I_{24SNK\_V24PWR}$ | $V_{24}$ = 36V, REGEN open, GPO bit in the GLOBLCFG register = 1, all logic outputs unloaded, all IN_ floating and in sink 1x DI mode | | 1.4 | 2 | mA |
| | $I_{24SNK\_VAPWR}$ | $V_{24}$ = 36V, $V_A$ = 5.5V, REGEN shorted to GND, GPO bit in the GLOBLCFG register = 1, all logic outputs unloaded, all IN_ floating and in sink 1x DI mode | | 0.1 | 0.2 | |
| | $I_{24SRC\_V24PWR}$ | $V_{24}$ = 36V, REGEN open, GPO bit in the GLOBLCFG register = 1, all logic outputs unloaded, all IN_ floating and in source 1x DI mode | | 2 | 4 | |
| | $I_{24SRC\_VAPWR}$ | $V_{24}$ = 36V, $V_A$ = 5.5V, REGEN shorted to GND, GPO bit in the GLOBLCFG register = 1, all logic outputs unloaded, all IN_ floating and in source 1x DI mode | | 0.7 | 2 | |
| **$V_A$ Linear Regulator (REGEN Open)** | | | | | | |
| $V_A$ Output Voltage | $V_A$ | $I_{A\_LOAD}$ = 1mA, 8V ≤ $V_{24}$ ≤ 65V | 4.7 | 5 | 5.3 | V |
| $V_A$ Line Regulation | $\Delta V_{A\_LNR}$ | $I_{A\_LOAD}$ = 1mA, $V_{24}$ = 12V to 24V | | 1 | | mV |
| $V_A$ Load Regulation | $\Delta V_{A\_LD}$ | $V_{24}$ = 12V, $I_{A\_LOAD}$ = 1mA to 10mA | | 4 | | mV |
| $V_A$ Short-Circuit Current | $I_{A\_SC}$ | $V_{24}$ = 12V, $V_A$ shorted to GND | 20 | 28 | 45 | mA |
| **$V_A$ Power Supply (REGEN Shorted to GND, Device Powered by $V_A$ Pin, $V_{24}$ = $V_A$ to 65V)** | | | | | | |
| $V_A$ Supply Voltage | $V_A$ | | 3 | | 5.5 | V |
| $V_A$ Supply Current | $I_{A\_SNK}$ | $V_A$ = 5.5V, $V_{24}$ = 36V, GPO bit in the GLOBLCFG register = 1, all logic outputs unloaded, all IN_ floating and in sink 1x DI mode | | 1.3 | 2 | mA |
| | $I_{A\_SRC}$ | $V_A$ = 5.5V, $V_{24}$ = 36V, GPO bit in the GLOBLCFG register = 1, all logic outputs unloaded, all IN_ floating and in source 1x DI mode | | 1.3 | 2 | |
| $V_A$ UVLO Threshold | $V_{A\_UVLO}$ | $V_A$ rising | 2.3 | | 2.9 | V |
| | | $V_A$ falling | 2.1 | | 2.85 | |
| $V_A$ UVLO Threshold Hysteresis | $V_{A\_UVHYS}$ | | | 0.074 | | V |
| REGEN Threshold | $V_{TH\_REGEN}$ | | 0.3 | | 3.3 | V |
| REGEN Pullup Resistor | $R_{LK\_REGEN}$ | $V_A$ = 5.5V | | 200 | | kΩ |
| **$V_L$ Power Supply** | | | | | | |

($V_{24}$ = +8V to +36V, $V_L$ = +2.5V to +5.5V, $V_A$ = +3.0V to +5.5V, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $V_{24}$ = +24V, $V_L$ = +3.3V, $V_A$ = +5V, $T_A$ = +25°C) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_L$ Supply Voltage | $V_L$ | | 2.5 | | 5.5 | V |
| $V_L$ Supply Current | $I_L$ | No switching, logic inputs static, $V_L$ = 5.5V, $\overline{CS}$ = $\overline{LATCH}$ = $V_L$ | | 15 | 30 | µA |
| $V_L$ UVLO Threshold | $V_{L\_UVLO}$ | $V_A$ = 5V, REGEN shorted to GND; $V_L$ rising | 0.9 | | 1.8 | V |
| | | $V_L$ falling | 0.9 | | 1.75 | |
| $V_L$ UVLO Threshold Hysteresis | $V_{L\_UVHYS}$ | | | 0.061 | | V |
| **$\overline{READY}$ Timing** | | | | | | |
| $\overline{READY}$ Delay | $t_{DRDY\_VARISE}$ | Delay from $V_A$ rising above UVLO to $\overline{READY}$ low, REGEN shorted to GND, $V_L$ = 5V, pulldown current 5mA | | 1 | | ms |
| | $t_{DRDY\_VLRISE}$ | Delay from $V_L$ rising above UVLO to $\overline{READY}$ low, REGEN shorted to GND, $V_A$ = 5V, pulldown current 5mA | | 1 | | |
| **$V_M$ Monitoring Comparator** | | | | | | |
| External $V_M$ Monitor Alarm, On to Off | $V_{EXTVMOFF}$ | $V_M$ pin rising, bit VMLOW in the FAULT1 register goes to 0 and $\overline{VMOK}$ goes to low | 0.778 | 0.81 | 0.842 | V |
| External $V_M$ Monitor Alarm, Off to On | $V_{EXTVMON}$ | $V_M$ pin falling, bit VMLOW in the FAULT1 register goes to 1 and $\overline{VMOK}$ goes to high | 0.751 | 0.78 | 0.814 | V |
| $V_M$ Glitch Filter | $t_{FILTER\_VM}$ | $V_M$ glitch length that is filtered | | 3 | | µs |
| $V_M$ Leakage Current | $I_{LEAK\_VM}$ | $V_M$ = 5.5V, $V_A$ = 5.5V | -1 | | 1 | µA |
| $\overline{VMOK}$ Leakage Current | $I_{LEAK\_\overline{VMOK}}$ | $\overline{VMOK}$ = 36V, $V_{24}$ = 36V, REGEN open | -1 | | 1 | µA |
| $\overline{VMOK}$ Output Logic-Low Voltage | $V_{\overline{VMOK}\_OL}$ | $I_{LOAD}$ = 5mA (Note 2) | | | 0.4 | V |
| **Thermal Management** | | | | | | |
| Temperature Alarm | $T_{ALRM}$ | Temperature rising until TEMPALM bit in the FAULT1 register is 1, REGEN shorted to GND, $V_A$ = 5V, $V_{24}$ = 8V | | 115 | | °C |
| Temperature Alarm Hysteresis | $T_{ALRM\_HYS}$ | Temperature falling until TEMPALM bit in the FAULT1 register is 0 | | 10 | | °C |
| Thermal Shutdown | $T_{OTSHDN1}$ | Temperature rising until OTSHDN1 bit in the FAULT1 register is 1, REGEN shorted to GND, $V_A$ = 5V, $V_{24}$ = 8V | | 150 | | °C |
| Thermal Shutdown Hysteresis | $T_{OTSHDN1\_HYS}$ | Temperature falling until OTSHDN1 bit in the FAULT1 register is 0 | | 10 | | °C |
| System Thermal Shutdown Threshold | $T_{OTSHDN2}$ | Temperature rising until OTSHDN2 bit in the FAULT2 register is 1, REGEN shorted to GND, $V_A$ = 5V, $V_{24}$ = 8V | | 165 | | °C |
| System Thermal Shutdown Hysteresis | $T_{OTSHDN2\_HYS}$ | Temperature falling until OTSHDN2 bit in the FAULT2 register is 0 | | 10 | | °C |
| **PCB Fault Detection** | | | | | | |
| REFDI Pin Short Alarm | $I_{RFDIS}$ | Increasing current at pin REFDI until bit RFDIS in the FAULT2 register is 1 | 106 | 147 | 180 | µA |
| | | Decreasing current at pin REFDI until bit RFDIS in the FAULT2 register is 0 | 100 | 132 | 170 | |
| REFDI Pin Short Hysteresis | $I_{RFDIS\_HYS}$ | | | 15 | | µA |

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| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| REFDI Pin Open Alarm | $I_{RFDIO}$ | Decreasing current at pin REFDI until bit RFDIO in the FAULT2 register is 1 | 1.8 | 3 | 4 | µA |
| | | Increasing current at pin REFDI until bit RFDIO in the FAULT2 register is 0 | 2.5 | 4 | 5 | |
| REFDI Pin Open Hysteresis | $I_{RFDIO\_HYS}$ | | | 1 | | µA |
| **REFDI Current Setting** | | | | | | |
| REFDI Pin Voltage | $V_{REFDI}$ | | 0.585 | 0.61 | 0.635 | V |
| REFDI Resistor Range | $R_{REFDI}$ | | 12 | | 55 | kΩ |
| Input Current Set Range Min | $I_{IN\_TY1/3\_MIN}$ | $R_{REFDI}$ = 55kΩ, Sink 1x DI mode and Source 1x DI mode | 0.43 | 0.5 | 0.59 | mA |
| Input Current Set Range Max | $I_{IN\_TY1/3\_MAX}$ | $R_{REFDI}$ = 12kΩ, Sink 1x DI mode and Source 1x DI mode | | 2.25 | | mA |
| Input Current 3x Scale Factor | SCLF | $R_{REFDI}$ = 12kΩ, Sink 3x DI mode and Source 3x DI mode | | 3.0 | | |
| **Inputs (IN1–IN4)** | | | | | | |
| **Type 1/3 Digital Input** | | | | | | |
| On-State Input Current in Sink Mode (Type 1/3) | $I_{IN\_TY1/3SK}$ | Sink 1x DI mode, $R_{REFDI}$ = 12kΩ, 6V ≤ $V_{IN\_}$ ≤ 36V | 2.1 | 2.25 | 2.65 | mA |
| On-State Input Current in Source Mode (Type 1/3) | $I_{IN\_TY1/3SR}$ | Source 1x DI mode, $R_{REFDI}$ = 12kΩ, $V_{24}$ = 36V, ($V_{24}$ - 36V) ≤ $V_{IN\_}$ ≤ ($V_{24}$ - 6V) (Note 2) | -2.65 | -2.25 | -2.1 | mA |
| **Type 2 Digital Input** | | | | | | |
| On-State Input Current in Sink Mode (Type 2) | $I_{IN\_TY2SK}$ | Sink 3x DI mode, $R_{REFDI}$ = 12kΩ, HITHR_ = 0, 3V ≤ $V_{IN\_}$ ≤ 36V | 6.25 | 6.7 | 7.7 | mA |
| On-State Input Current in Source Mode (Type 2) | $I_{IN\_TY2SR}$ | Source 3x DI mode, $R_{REFDI}$ = 12kΩ, $V_{24}$ = 36V, HITHR_ = 0, ($V_{24}$ - 36V) ≤ $V_{IN\_}$ ≤ ($V_{24}$ - 3V) (Note 2) | -7.7 | -7 | -6.4 | mA |
| **High-Impedance Mode** | | | | | | |
| Input Current Hi-Z Mode | $I_{IN\_HIZ}$ | Sink off DI mode, $V_{IN\_}$ = 36V, $V_{24}$ = 36V, REGEN open; HITHR_ = 1 | 10 | 45 | 70 | µA |
| | | Sink off DI mode, $V_{IN\_}$ = 36V, $V_{24}$ = 36V, REGEN open; HITHR_ = 0 | | | 40 | |
| | | Source off DI mode, $V_{IN\_}$ = 0V, HITHR_ = 1, $V_{24}$ = 36V, REGEN open (Note 2) | -70 | | -10 | |
| | | TTL off mode, $V_{IN\_}$ = 5.5V, $V_{24}$ = 3V, REGEN shorted to GND, $V_A$ = 3V | | 2.6 | 15 | |
| **Threshold Voltages** | | | | | | |
| On Threshold Voltage in Sink Mode | $V_{TONSK\_L}$ | Sink mode, HITHR_ = 0, $V_{IN\_}$ rising | 3.5 | 4 | 4.3 | V |
| | $V_{TONSK\_H}$ | Sink mode, HITHR_ = 1, $V_{IN\_}$ rising | 6.6 | 7 | 7.6 | |
| Off Threshold Voltage in Sink Mode | $V_{TOFFSK\_L}$ | Sink mode, HITHR_ = 0, $V_{IN\_}$ falling | 2.7 | 3 | 3.3 | V |
| | $V_{TOFFSK\_H}$ | Sink mode, HITHR_ = 1, $V_{IN\_}$ falling | 5.6 | 6 | 6.5 | |
| On Threshold Voltage in Source Mode | $V_{TONSC\_L}$ | Source mode, HITHR_ = 0, $V_{24}$ = 8V to 36V, $V_{IN\_}$ falling | $V_{24}$ - 4.3 | $V_{24}$ - 4 | $V_{24}$ - 3.5 | V |
| | $V_{TONSC\_H}$ | Source mode, HITHR_ = 1, $V_{24}$ = 8V to 36V, $V_{IN\_}$ falling | $V_{24}$ - 7.4 | $V_{24}$ - 7 | $V_{24}$ - 6.4 | |
| Off Threshold Voltage in Source Mode | $V_{TOFFSC\_L}$ | Source mode, HITHR_ = 0, $V_{24}$ = 8V to 36V, $V_{IN\_}$ rising | $V_{24}$ - 3.15 | $V_{24}$ - 2.9 | $V_{24}$ - 2.55 | V |

($V_{24}$ = +8V to +36V, $V_L$ = +2.5V to +5.5V, $V_A$ = +3.0V to +5.5V, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $V_{24}$ = +24V, $V_L$ = +3.3V, $V_A$ = +5V, $T_A$ = +25°C) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| | $V_{TOFFSC\_H}$ | Source mode, HITHR_ = 1, $V_{24}$ = 8V to 36V, $V_{IN\_}$ rising | $V_{24}$ - 6.3 | $V_{24}$ - 6 | $V_{24}$ - 5.4 | |
| $V_{IN\_}$ Threshold Hysteresis | $V_{IN\_HYS}$ | HITHR_ don't care | | 0.8 | | V |
| Input High in TTL Mode | $V_{IH\_TTL}$ | TTL mode, REGEN shorted to GND, $V_{24}$ = $V_A$ | 1.5 | | 1.8 | V |
| Input Low in TTL Mode | $V_{IL\_TTL}$ | TTL mode, REGEN shorted to GND, $V_{24}$ = $V_A$ | 1 | | 1.3 | V |
| Input Threshold Hysteresis in TTL Mode | $V_{TTL\_HYS}$ | TTL mode | | 0.5 | | V |
| **Input Filters** | | | | | | |
| $V_{IN\_}$ Sampling Rate | $f_{OSC}$ | $V_{24}$ = $V_A$, REGEN shorted to GND | | 1 | | MHz |
| Minimum Detectable Field Input Pulse Width | $t_{PW}$ | Filter bypass, no external capacitors on pins IN1–IN4 | | 3 | | µs |
| Input Filter Delay | $t_{FLT\_DELAY}$ | Bypass, FLTEN_ is 0 in the CNFG_ register | | 2 | | µs |
| | | DELAY_[2:0] = 0 | | 50 | | |
| | | DELAY_[2:0] = 1 | | 0.1 | | ms |
| | | DELAY_[2:0] = 2 | | 0.4 | | |
| | | DELAY_[2:0] = 3 | | 0.8 | | |
| | | DELAY_[2:0] = 4 | | 1.6 | | |
| | | DELAY_[2:0] = 5 | | 3.2 | | |
| | | DELAY_[2:0] = 6 | | 12.8 | | |
| | | DELAY_[2:0] = 7 | | 20 | | |
| Input Filter Delay Tolerance | | Filters and sampling clock tolerance for DELAY_[2:0] | -10.16 | | +10.16 | % |
| **LED Matrix/GPO Pins (LO_)** | | | | | | |
| Output Logic-High Voltage | $V_{OH\_LED}$ | $I_{LOAD}$ = -5mA (Note 2) | $V_A$ – 0.4 | | | V |
| Output Logic-Low Voltage | $V_{OL\_LED}$ | $I_{LOAD}$ = 5mA (Note 2) | | | 0.4 | V |
| Output Off Leakage | $I_{LEAK\_LED}$ | $V_A$ = 5.5V | -1 | | +1 | µA |
| LED Matrix Scan Rate | $f_{LED}$ | | | 0.33 | | kHz |
| **Logic Pins (LATCH, CS, SCLK, SDI, SDO, READY, FAULT, CRCEN, DAISY, A0, A1)** | | | | | | |
| Input Logic-High Voltage | $V_{IH}$ | | 0.7 x $V_L$ | | | V |
| Input Logic-Low Voltage | $V_{IL}$ | | | | 0.3 x $V_L$ | V |
| Input Hysteresis | $V_{HYS}$ | | | 0.5 | | mV |
| Input Logic Leakage Current | $I_{IL}$ | $V_L$ = $V_A$ = 5.5V | -1 | | 1 | µA |
| Input Pullup Resistance | $R_{PU}$ | $\overline{CS}$ = $\overline{LATCH}$ = 0V, $V_L$ = $V_A$ = 5.5V, REGEN shorted to GND | | 195 | | kΩ |
| Input Pulldown Resistance | $R_{PD}$ | A0, A1, CRCEN, DAISY, SDI, SCLK, $V_L$ = $V_A$ = 5.5V, REGEN shorted to GND | | 195 | | kΩ |
| Output Logic-High Voltage | $V_{OH}$ | SDO, $\overline{READY}$, $I_{LOAD}$ = -5mA, $V_L$ = 2.5V to 5.5V, $V_A$ = 5V, REGEN shorted to GND (Note 2) | $V_L$ - 0.4 | | | V |

($V_{24}$ = +8V to +36V, $V_L$ = +2.5V to +5.5V, $V_A$ = +3.0V to +5.5V, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $V_{24}$ = +24V, $V_L$ = +3.3V, $V_A$ = +5V, $T_A$ = +25°C) (*Note 1*)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Output Logic-Low Voltage | $V_{OL}$ | $I_{LOAD}$ = 5mA, REGEN shorted to GND (*Note 2*) | $V_L$ = 2.5V to 5.5V, $V_A$ = 5V for SDO | | | 0.4 | V |
| | | | $V_A$ = 3V to 5.5V for $\overline{FAULT}$ | | | 0.4 | |
| Output Open-Drain Off Leakage Current | $I_{OLEAK}$ | | | -1 | | 1 | µA |
| **Dynamic Characteristics** | | | | | | | |
| IN_ Sampling Rate | $f_S$ | $V_{24}$ = $V_A$ = 5V, REGEN shorted to GND | | | 1 | | MHz |
| IN_ Latching Delay | $t_{\overline{LATCH}}$ | From $\overline{LATCH}$ or $\overline{CS}$ falling until input data is frozen | | | 40 | | ns |
| **SPI Timing Characteristics** | | | | | | | |
| SCLK Frequency | $f_{SCLK}$ | | | | | 12 | MHz |
| SCLK Pulse Duration | $t_{SCLK}$ | (*Figure 1*) | | 38 | | | ns |
| $\overline{CS}$ High Pulse Duration | $t_{CSBPW}$ | (*Figure 1*) | | 1.11 | | | µs |
| Minimum Data Setup Time | $t_{DINSU}$ | (*Figure 1*) | | 10 | | | ns |
| Minimum Data Hold Time | $t_{DINH}$ | (*Figure 1*) | | 10 | | | ns |
| Minimum $\overline{CS}$ Hold Time | $t_{CSBH}$ | (*Figure 1*) | | 38 | | | ns |
| $\overline{CS}$ Falling Edge to First Rising SCLK Edge | $t_{SCLK\_SU}$ | (*Figure 1*) | | 40 | | | ns |
| Maximum SCLK to SDO Output Valid Time | $t_{DO}$ | (*Figure 1*) | | | | 30 | ns |
| Maximum $\overline{CS}$ to SDO Output Valid Time | $t_{CSB\_SDOVALID}$ | (*Figure 1*) | | | | 40 | ns |
| SDO Rise/Fall Time | $t_{R/F}$ | | | | 3.5 | | ns |

**Note 1:** All devices are 100% production tested at $T_A$ = +25°C. Specifications over temperature are guaranteed by design and characterization.

**Note 2:** All currents into the device are positive. All currents out of the device are negative.

## Timing Diagram

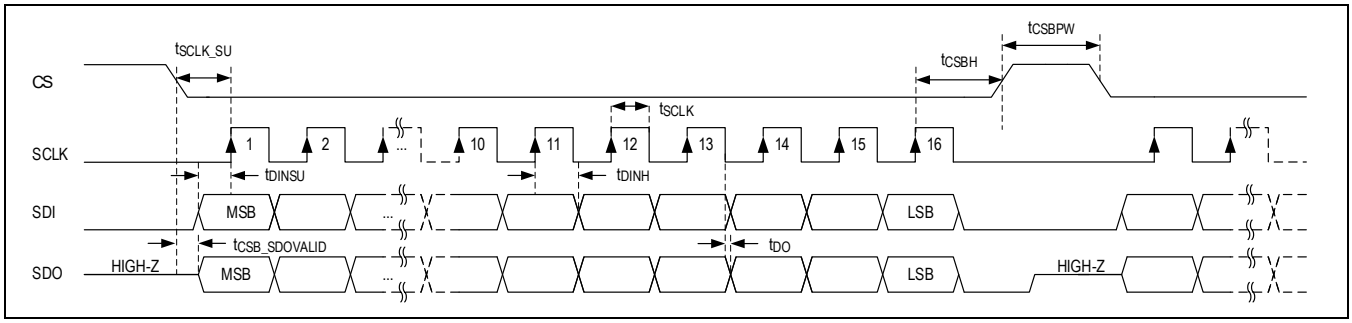



*Figure 1. SPI Timing Diagram*

## ESD Protection

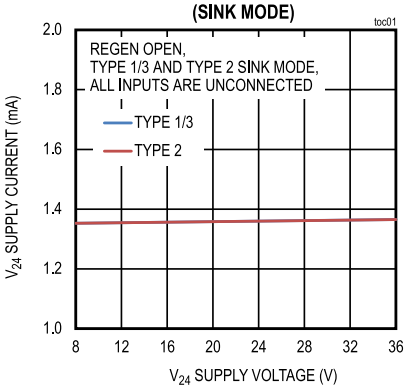
($T_A$ = +25°C)

| PARAMETER | SYMBOL | CONDITIONS | VALUE | UNITS |
|---|---|---|---|---|
| ESD | | Human Body Model, All Pins | ±2 | kV |

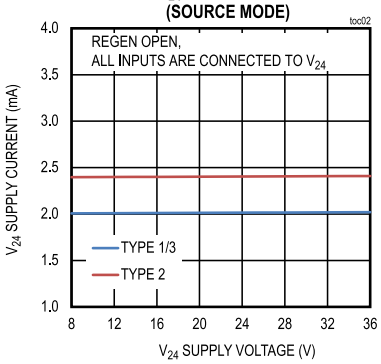
## Typical Operating Characteristics

($V_{24}$ = +24V, REGEN = GND, $V_A$ = +5V, $V_L$ = +3.3V, $R_{REFDI}$ = 12kΩ, $R_{IN\_}$ = 680Ω, $V_{FIN\_}$ = voltage measured at the field side, $V_{IN\_}$ = voltage measured at the pin, $T_A$ = +25°C, unless otherwise noted.)

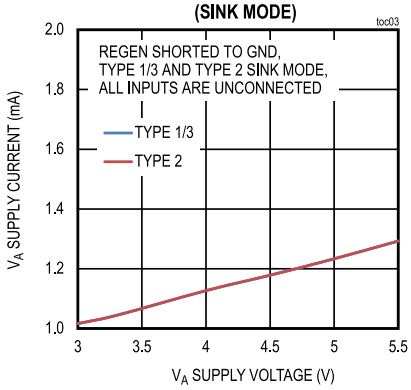
$V_{24}$ SUPPLY CURRENT vs. $V_{24}$ SUPPLY VOLTAGE (SINK MODE)



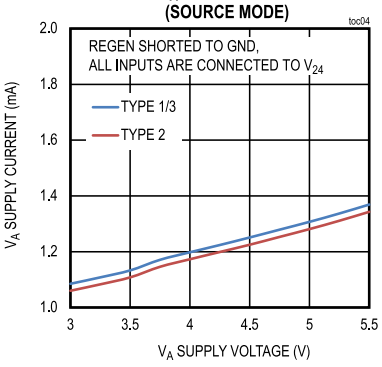

$V_{24}$ SUPPLY CURRENT vs. $V_{24}$ SUPPLY VOLTAGE (SOURCE MODE)



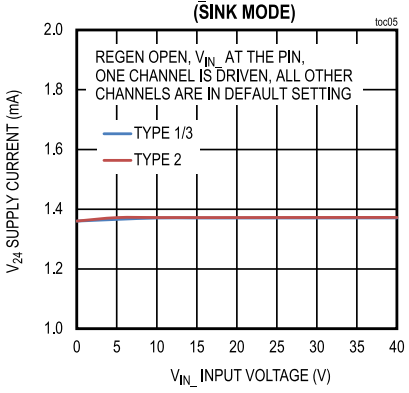

$V_A$ SUPPLY CURRENT vs. $V_A$ SUPPLY VOLTAGE (SINK MODE)



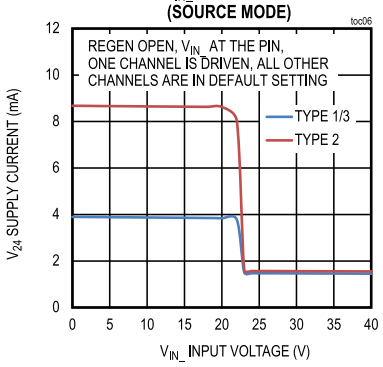

$V_A$ SUPPLY CURRENT vs. $V_A$ SUPPLY VOLTAGE (SOURCE MODE)



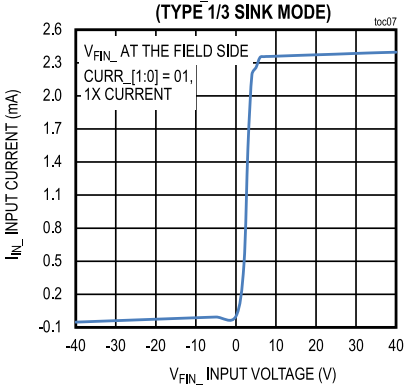

$V_{24}$ SUPPLY CURRENT vs. $V_{IN\_}$ INPUT VOLTAGE (SINK MODE)



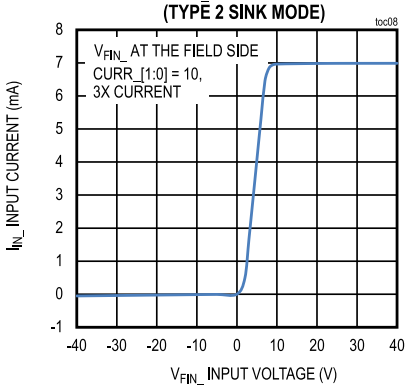

$V_{24}$ SUPPLY CURRENT vs. $V_{IN\_}$ INPUT VOLTAGE (SOURCE MODE)



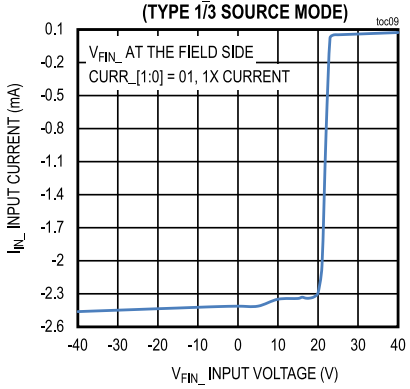

$I_{IN\_}$ INPUT CURRENT vs. $V_{FIN\_}$ INPUT VOLTAGE (TYPE 1/3 SINK MODE)




$I_{IN\_}$ INPUT CURRENT vs. $V_{FIN\_}$ INPUT VOLTAGE (TYPE 2 SINK MODE)

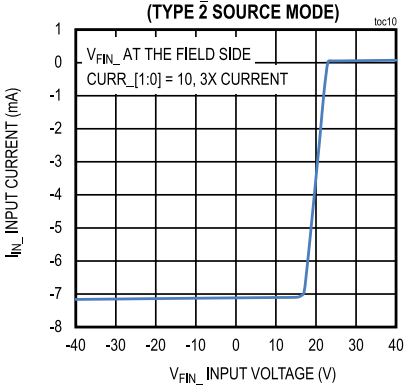



$I_{IN\_}$ INPUT CURRENT vs. $V_{FIN\_}$ INPUT VOLTAGE (TYPE 1/3 SOURCE MODE)

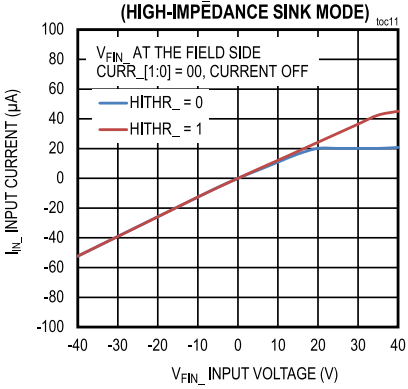


($V_{24}$ = +24V, REGEN = GND, $V_A$ = +5V, $V_L$ = +3.3V, $R_{REFDI}$ = 12kΩ, $R_{IN\_}$ = 680Ω, $V_{FIN\_}$ = voltage measured at the field side, $V_{IN\_}$ = voltage measured at the pin, $T_A$ = +25°C, unless otherwise noted.)

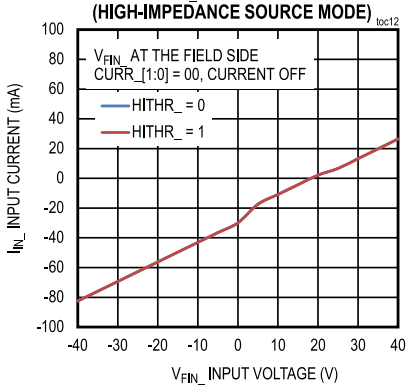
$I_{IN\_}$ INPUT CURRENT vs. $V_{FIN\_}$ INPUT VOLTAGE (TYPE 2 SOURCE MODE)



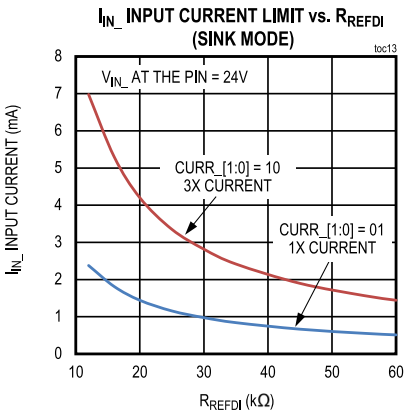

$I_{IN\_}$ INPUT CURRENT vs. $V_{FIN\_}$ INPUT VOLTAGE (HIGH-IMPEDANCE SINK MODE)



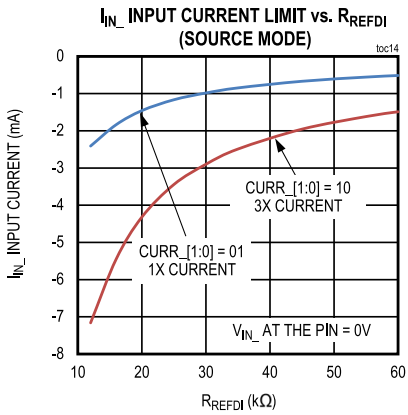

$I_{IN\_}$ INPUT CURRENT vs. $V_{FIN\_}$ INPUT VOLTAGE (HIGH-IMPEDANCE SOURCE MODE)



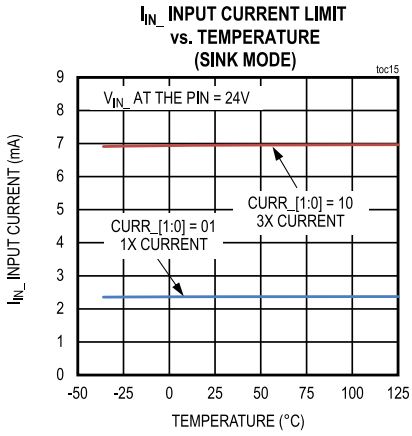

$I_{IN\_}$ INPUT CURRENT LIMIT vs. $R_{REFDI}$ (SINK MODE)



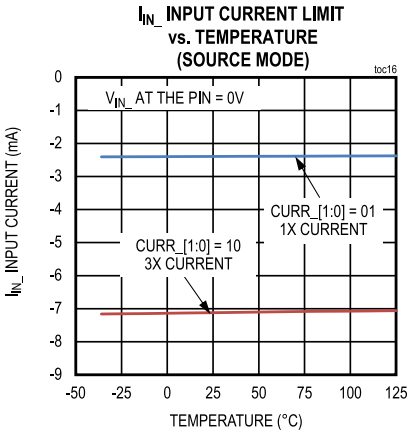

$I_{IN\_}$ INPUT CURRENT LIMIT vs. $R_{REFDI}$ (SOURCE MODE)



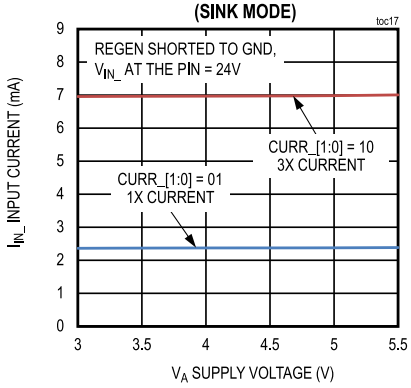

$I_{IN\_}$ INPUT CURRENT LIMIT vs. TEMPERATURE (SINK MODE)



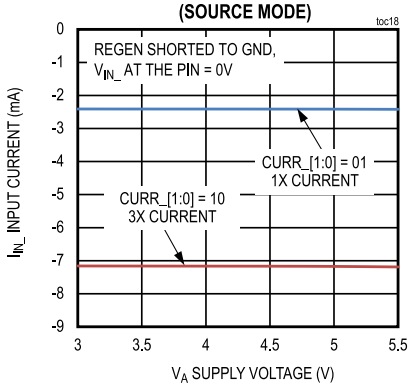

$I_{IN\_}$ INPUT CURRENT LIMIT vs. TEMPERATURE (SOURCE MODE)



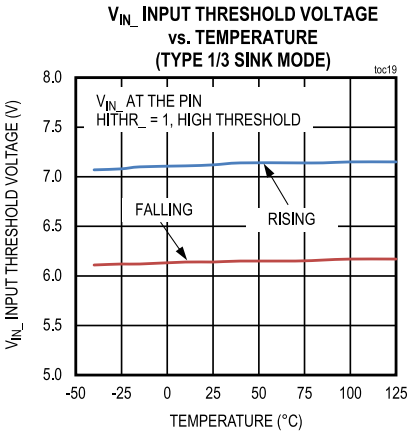

$I_{IN\_}$ INPUT CURRENT LIMIT vs. $V_A$ SUPPLY VOLTAGE (SINK MODE)

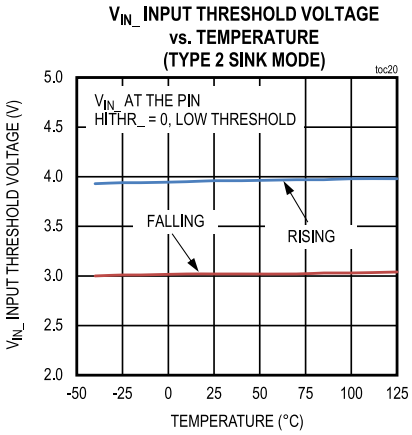


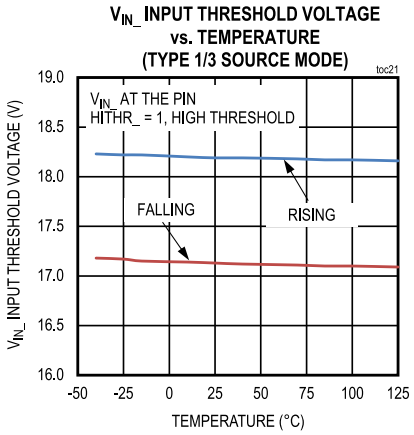

$I_{IN\_}$ INPUT CURRENT LIMIT vs. $V_A$ SUPPLY VOLTAGE (SOURCE MODE)

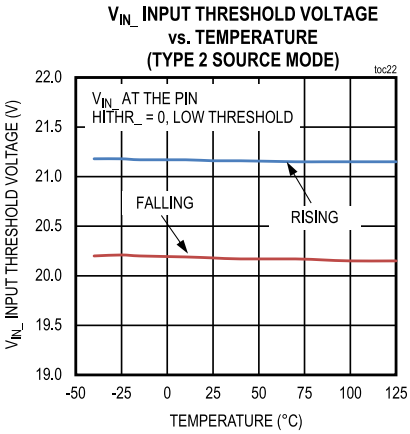


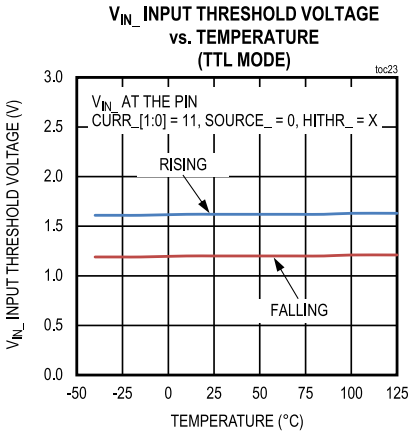
($V_{24}$ = +24V, REGEN = GND, $V_A$ = +5V, $V_L$ = +3.3V, $R_{REFDI}$ = 12kΩ, $R_{IN\_}$ = 680Ω, $V_{FIN\_}$ = voltage measured at the field side, $V_{IN\_}$ = voltage measured at the pin, $T_A$ = +25°C, unless otherwise noted.)

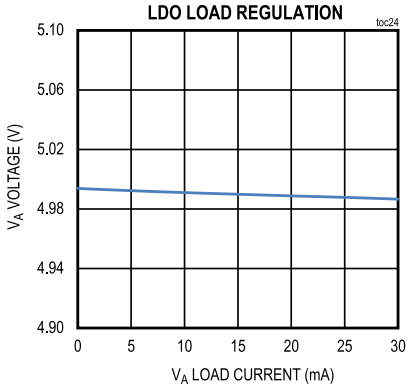


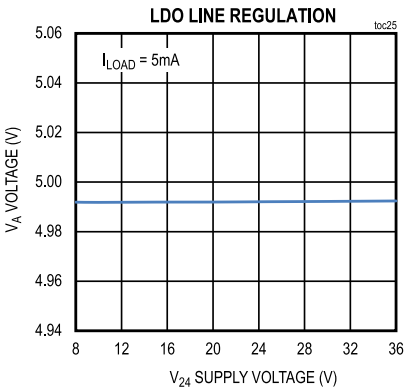



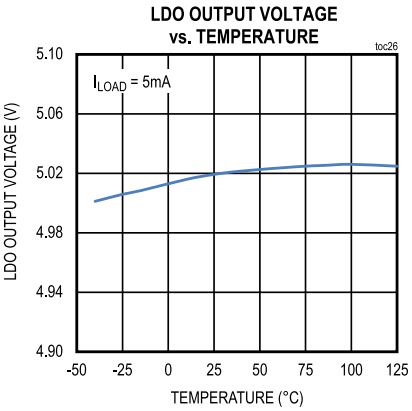



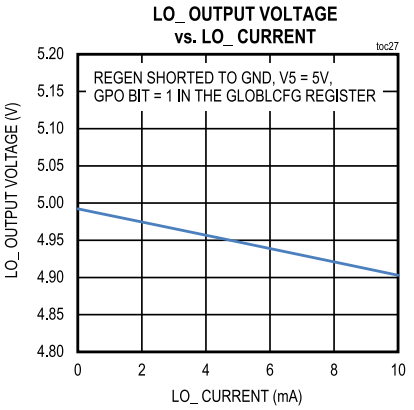



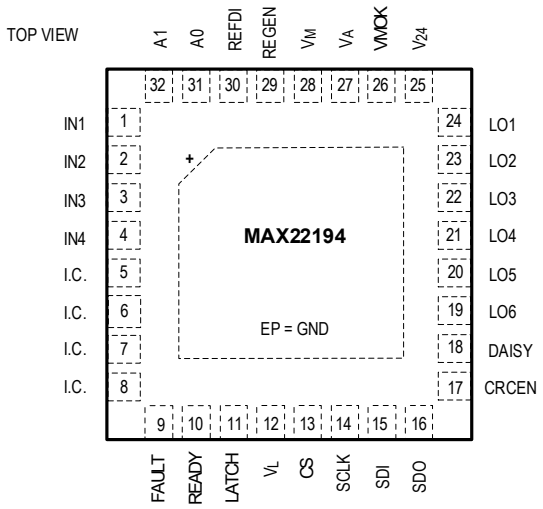



## Pin Configurations




**TQFN**
**5mm x 5mm**

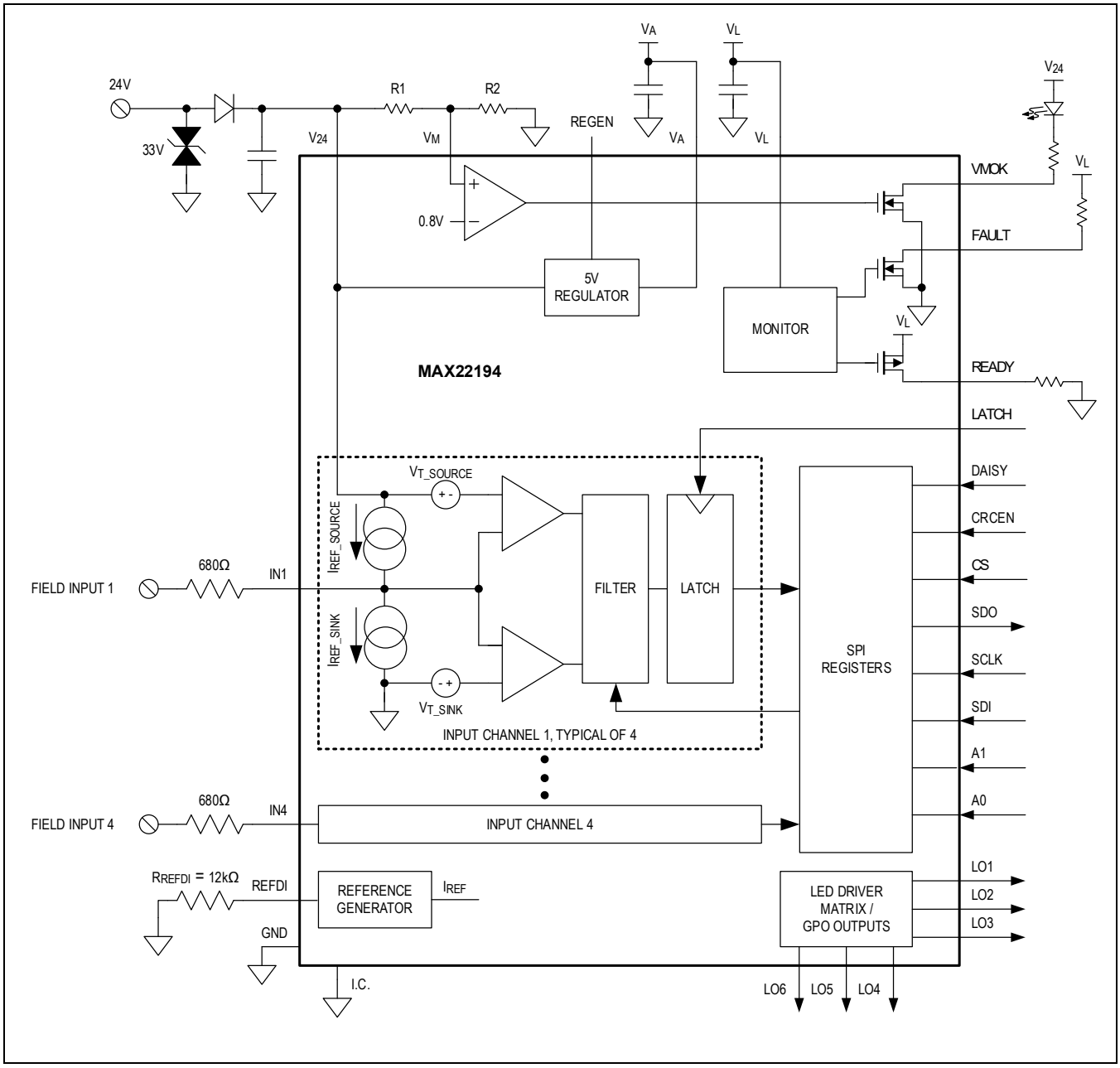
## Pin Descriptions

| PIN | NAME | FUNCTION | REF SUPPLY | Type |
|---|---|---|---|---|
| **POWER SUPPLIES** | | | | |
| 25 | $V_{24}$ | 24V field supply. Bypass to GND with a 1µF capacitor. In sink and TTL modes, external 24V field supply is not necessary. See *Power Supply* section for details. | | Power |
| 27 | $V_A$ | 5V linear regulator output (REGEN pin unconnected) or 3V to 5.5V supply input (REGEN pin shorted to GND). The MAX22194 can optionally be powered only from $V_A$ in sink and TTL modes ($V_{24}$ shorted to $V_A$). Bypass $V_A$ to GND with 1µF capacitor. | | Power |
| 29 | REGEN | $V_A$ Regulator Enable Input. Connect REGEN to GND to disable $V_A$ regulator. Leave REGEN open (internally pulled up) to enable $V_A$ regulator. | VA | Digital Input |
| 12 | $V_L$ | 2.5V to 5.5V Logic Interface Supply. Bypass $V_L$ to GND with a 0.1µF capacitor. Make sure $V_L$ is always lower than or equal to $V_A$. | | Power |
| 28 | $V_M$ | $V_M$ is the input voltage to a comparator that can be used for supervising $V_{24}$ or other supply voltage. The $V_M$ comparator trip voltage is 0.81V (rising, typical) or 0.78V (falling, typical), and voltage scaling can be achieved using an external resistor-divider. | VA | Analog Input |
| 26 | $\overline{VMOK}$ | Active-Low, Low-Side, Open-Drain Output. $\overline{VMOK}$ goes low when the $V_M$ input voltage rises to exceed 0.81V (typical), and goes high when the $V_M$ input voltage falls below 0.78V (typical). Connect a pullup resistor from $\overline{VMOK}$ to a supply voltage of up to $V_{24}$. An LED can be used in series to indicate a good field supply condition. | V24 | Digital Output |
| 5, 6, 7, 8 | I.C. | Internally Connected. Leave I.C. unconnected or connect to GND. | | |
| EP | GND | Ground return for all field inputs and all power supplies. | GND | |
| **DIGITAL INPUT PINS** | | | | |
| 1, 2, 3, 4 | IN1 to IN4 | Field Inputs. Place a 680Ω resistor between the field input and IN_ pin. See the *Detailed Description* section for details. | V24 | Sink or Source Inputs |
| **SPI** | | | | |

| | | | | |
|---|---|---|---|---|
| 9 | $\overline{FAULT}$ | Active-Low, Low-Side, Open-Drain Fault Indicator. $\overline{FAULT}$ goes low to indicate that one or more of the flags in the FAULT registers are set. Connect a pullup resistor from $\overline{FAULT}$ to $V_L$. | VL | Digital Output |
| 10 | $\overline{READY}$ | Active-Low, High-Side, Open-Drain Output. $\overline{READY}$ goes low when $V_A$ and $V_L$ are both above their respective UVLO thresholds, indicating that the MAX22194 is powered up and ready for operation. Connect a pulldown resistor from $\overline{READY}$ to GND. | VL | Digital Output |
| 11 | $\overline{LATCH}$ | Both $\overline{LATCH}$ and $\overline{CS}$ control data latching at the input of the serializer (after the inputs). The latch is transparent when both $\overline{CS}$ and $\overline{LATCH}$ are high. The data at the input of the serializer is frozen on the falling edge of either $\overline{LATCH}$ or $\overline{CS}$. $\overline{LATCH}$ is typically used to synchronize input channel sampling across multiple MAX22194 devices. $\overline{LATCH}$ has a weak internal pullup. | VL | Digital Input |
| 13 | $\overline{CS}$ | Chip Select Input. Assert low to latch input states and enable the SPI. $\overline{CS}$ has a weak internal pullup. | VL | Digital Input |
| 14 | SCLK | Serial Clock Input. SCLK has a weak internal pulldown. | VL | Digital Input |
| 15 | SDI | Serial Data Input. Data is clocked into SDI on the rising edge of SCLK. SDI has a weak internal pulldown. | VL | Digital Input |
| 16 | SDO | Serial Data Output. Data is updated on the falling edge of SCLK. When $\overline{CS}$ is high, SDO is high impedance. | VL | Digital Output |
| **CONFIGURATION PINS** | | | | |
| 17 | CRCEN | CRC Enable Pin. Drive CRCEN pin high to enable CRC generation and error detection on the SPI. Drive CRCEN pin low if CRC is not used. CRCEN has a weak internal pulldown. | VL | Digital Input |
| 18 | DAISY | Daisy-Chain Enable Pin. Drive DAISY pin high to enable daisy-chained SPI mode. Drive DAISY pin low if daisy-chain mode is not used. DAISY has a weak internal pulldown. | VL | Digital Input |
| 30 | REFDI | Digital Input Current-Limit Reference Resistor. For Type 1 and Type 3 inputs, place a 12kΩ resistor from REFDI to GND. See the *Detailed Description* section for details. | VA | Analog Input |
| 31 | A0 | Chip Address LSB for Addressable SPI. See *Table 4*. | VL | Digital Input |
| 32 | A1 | Chip Address MSB for Addressable SPI. See *Table 4*. | VL | Digital Input |
| **LED MATRIX/GPO OUTPUTS** | | | | |
| 21 | LO4 | Channel 4 LED Common Cathode Connection (Open-Drain Low-Side) when GPO bit in the GLOBLCFG register is 0, or General-Purpose Logic Output 4 (Push-Pull) when GPO bit in the GLOBLCFG register is 1. Connect a resistor in series when configured as an LED output to set the LED current. Leave unconnected, if not used. See the *LED Matrix* section for connection/details. | VA | Digital Output |
| 20 | LO5 | Channel 5 LED Common Cathode Connection (Open-Drain Low-Side) when GPO bit in the GLOBLCFG register is 0, or General-Purpose Logic Output 5 (Push-Pull) when GPO bit in the GLOBLCFG register is 1. Connect a resistor in series when configured as an LED output to set the LED current. Leave unconnected, if not used. See the *LED Matrix* section for connection/details. | VA | Digital Output |
| 19 | LO6 | Channel 6 General-Purpose Logic Output 6 (Push-Pull) when GPO bit in the GLOBLCFG register is 1. Leave unconnected, if not used, or when GPO bit in the GLOBLCFG register is 0. | VA | Digital Output |
| 24 | LO1 | Channel 1 LED Common Anode Connection (Open-Drain High-Side) when GPO bit in the GLOBLCFG register is 0, or General-Purpose Logic Output 1 (Push-Pull) when GPO bit in the GLOBLCFG register is 1. Connect a resistor in series when configured as an LED output to set the LED current. Leave unconnected, if not used. See the *LED Matrix* section for connection/details. | VA | Digital Output |
| 23 | LO2 | Channel 2 LED Common Anode Connection (Open-Drain High-Side) when GPO bit in the GLOBLCFG register is 0, or General-Purpose Logic Output 2 (Push-Pull) when GPO bit in the GLOBLCFG register is 1. Connect a resistor | VA | Digital Output |

| | | | | |
|---|---|---|---|---|
| | | in series when configured as an LED output to set the LED current. Leave unconnected, if not used. See the *LED Matrix* section for connection/details. | | |
| 22 | LO3 | Channel 3 LED Common Anode Connection (Open-Drain High-Side) when GPO bit in the GLOBLCFG register is 0, or General-Purpose Logic Output 3 (Push-Pull) when GPO bit in the GLOBLCFG register is 1. Connect a resistor in series when configured as an LED output to set the LED current. Leave unconnected, if not used. See the *LED Matrix* section for connection/details. | VA | Digital Output |

## Functional Diagrams



## Detailed Description

The MAX22194 senses the logic state of four digital inputs. The voltages at the IN1 to IN4 input pins are compared against internal references to determine whether the field binary-output sensor is on (logic 1) or off (logic 0). All four inputs are simultaneously latched by the assertion of either $\overline{LATCH}$ or $\overline{CS}$, and the data made available in a serialized form through the SPI.

Each input can be individually configured for current sinking or sourcing, DI (high or low thresholds), or TTL thresholds. Digital input in source mode can supply current while in sink mode it can receive current. The ON state is a high voltage when the input channel is configured as a sinking input (SOURCE_ bit in the CNFG_ register = 0) or a low voltage when the input is configured as a sourcing input (SOURCE_ bit in the CNFG_ register = 1). The OFF state is a low voltage when the input channel is configured as a sinking input or a high voltage when the input is configured as a sourcing input.

The current sinks and sources can be turned off while the input comparator continues normal operation allowing 5V TTL operation, or 24V HTL operation with high-impedance inputs.

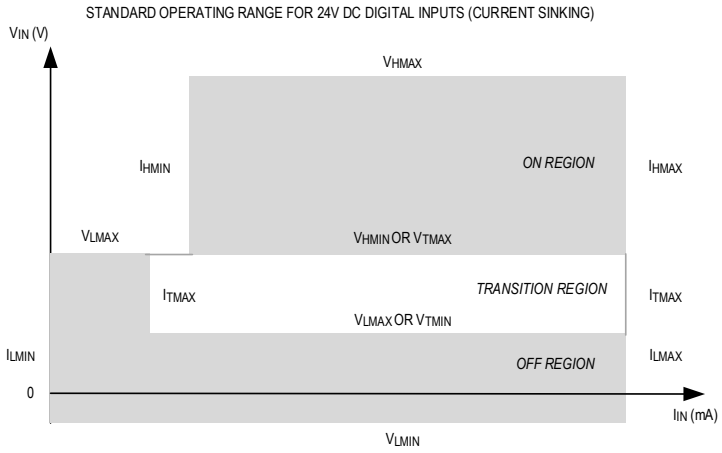
Placing a 12kΩ resistor between REFDI and GND and a 680Ω resistor between each field input and the corresponding IN_ pin ensures that the current at the ON and OFF trip points as well as the voltage at the trip points satisfy the requirements of IEC 61131-2 Type 1/3 or Type 2 digital inputs. The current sunk (or sourced) by each input pin rises linearly with input voltage until the level set by the current limiter is reached; any voltage increase beyond this point does not increase the input current. Current limiting ensures compliance with the IEC 61131-2 while significantly reducing power dissipation compared to traditional resistive inputs. *Figure 2* shows the IEC 61131-2 digital input current and voltage requirements.

Type 1/Type 3 digital input can be selected on a per-channel basis by setting the two CURR_[1:0] bits in the CNFG_ register to 0b01 to select the 1x factor for the current set by the REFDI resistor, and setting HITHR_ bit in the CNFG_ register to 1 to select the higher voltage threshold at the input pin. Type 2 digital input can be selected on a per-channel basis by setting the two CURR_[1:0] bits in the CNFG_ register to 0b10. This configuration selects the 3x factor for the current set by the REFDI resistor. Hence, the HITHR_ bit in the CNFG_ register is set to 0 to select the lower voltage threshold as the 3x factor gives a higher input current causing a bigger voltage-drop across the input series resistor. See *Table 1* for input mode configuration.

The current-setting resistor REFDI can be calculated using the following simplified equation:

$$R_{REFDI} = \frac{M \times V_{REFDI}}{I_{IN\_}}$$

where, $V_{REFDI}$ = 0.61V (typical). Constant M is different based on the input mode configuration, as shown in *Table 2*. The minimum allowed REFDI resistor value is 12kΩ. If REFDI resistor is less than 12kΩ, the RFDIS bit in the FAULT2 register is asserted to indicate a short-circuit fault on the REFDI pin.




| TYPE OF LIMIT | TYPE 1 LIMITS | | | | | | TYPE 2 LIMITS | | | | | | TYPE 3 LIMITS | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | OFF REGION | | TRANSITION | | ON REGION | | OFF REGION | | TRANSITION | | ON REGION | | OFF REGION | | TRANSITION | | ON REGION | |
| | $V_L$ (V) | $I_L$ (mA) | $V_T$ (V) | $I_T$ (mA) | $V_H$ (V) | $I_H$ (mA) | $V_L$ (V) | $I_L$ (mA) | $V_T$ (V) | $I_T$ (mA) | $V_H$ (V) | $I_H$ (mA) | $V_L$ (V) | $I_L$ (mA) | $V_T$ (V) | $I_T$ (mA) | $V_H$ (V) | $I_H$ (mA) |
| **MAX** | 15/5 | 15 | 15 | 15 | 30 | 15 | 11/5 | 30 | 11 | 30 | 30 | 30 | 11/5 | 15 | 11 | 15 | 30 | 15 |
| **MIN** | -3 | ND | 5 | 0.5 | 15 | 2 | -3 | ND | 5 | 2 | 11 | 6 | -3 | ND | 5 | 1.5 | 11 | 2 |

ND = NOT DEFINED

*Figure 2. Switching Characteristics for IEC 61131-2 Type 1, 2, and 3 24VDC Digital Inputs*

## Table 1. Input Mode Configurations

| INPUT TYPE | CNFG_ REGISTER | | |
|---|---|---|---|
| | CURR_[1:0] | SOURCE_ | HITHR_ |
| HTL Mode/High-Impedance Mode | 00 | 0 | X |
| Digital Input Type 1/3 Sink Mode | 01 | 0 | 1 |
| Digital Input Type 2 Sink Mode | 10 | 0 | 0 |
| TTL Mode | 11 | 0 | X |
| High-Impedance Mode | 00 | 1 | X |
| Digital Input Type 1/3 Source Mode | 01 | 1 | 1 |
| Digital Input Type 2 Source Mode | 10 | 1 | 0 |
| High-Impedance Mode | 11 | 1 | X |

*X = Don't care.*

## Table 2. Simplified Scaling Factor of REFDI in Input Current Equation

| INPUT TYPE | M VALUE | INPUT CURRENT LIMIT (mA) WHEN REFDI = 12kΩ |
|---|---|---|
| Digital Input Type 1/3 Sink Mode (1x) | 46 | 2.34 |
| Digital Input Type 2 Sink Mode (3x) | 136 | 6.91 |
| Digital Input Type 1/3 Source Mode (1x) | 43 | 2.19 |
| Digital Input Type 2 Source Mode (3x) | 133 | 6.76 |

### Input Filters

The MAX22194 features a digital filter per-channel to reduce glitches and noise at the input, making an analog RC filter unnecessary. Capacitors should not be connected to the IN_ pins for filtering. Each input (IN1 to IN4) has a programmable digital filter; input data can be filtered, or it can be bypassed for high-speed sampling. The input is sampled, and the data is latched at 1MHz (typ). Bit FLTEN_ in the corresponding CNFG_ register is used to bypass the filter or enable the filter. One of the eight filter delays (50µs, 100µs, 400µs, 800µs, 1.6ms, 3.2ms, 12.8ms, 20ms) can be independently selected for each channel.

Noise rejection is accomplished through a no-rollover up-down counter, where the state of the field input controls the counting direction (up or down). The filter uses an up-down counter fed by a 1MHz clock. If the input is high, it counts up; if the input is low, it counts down. The filter output is updated when the counter hits the upper or lower limit, with the upper limit depending on the selected filter delay and the lower limit being zero regardless of the filter delay. The low-to-high transition of the filter occurs when the counter reaches the upper limit. The high-to-low transition occurs when the counter reaches the lower limit. There is no rollover; counting simply stops when the upper or lower limit is hit. The filter delay is the time it takes to reach the upper/lower limit in response to a step input when the counter starts from the lower/upper limit. If the input is not a step function, but is bouncing, as shown in *Figure 3*, the output changes state after a total delay of:

$$t_{DELAY} = t_{FLT\_DELAY} + 2 \times t_{OLD\_STATE}$$

In the example in *Figure 3*, the filter has a nominal delay of 1.6ms, and the input returns high for two 0.2ms periods after the first transition from high to low. These transitions back to the high state extend the time before the output of the filter switches.

$$t_{DELAY} = 1.6ms + 2 \times (0.2ms + 0.2ms) = 2.4ms$$

The channel input to data output (at SPI) delay is formed by the delay due to the input comparator ($t_{CMPDELAY}$), the sampling delay ($t_{SMPLDELAY}$), filter delay configured in the CNFG_ register, and SPI read delay, as illustrated in *Figure 4*.

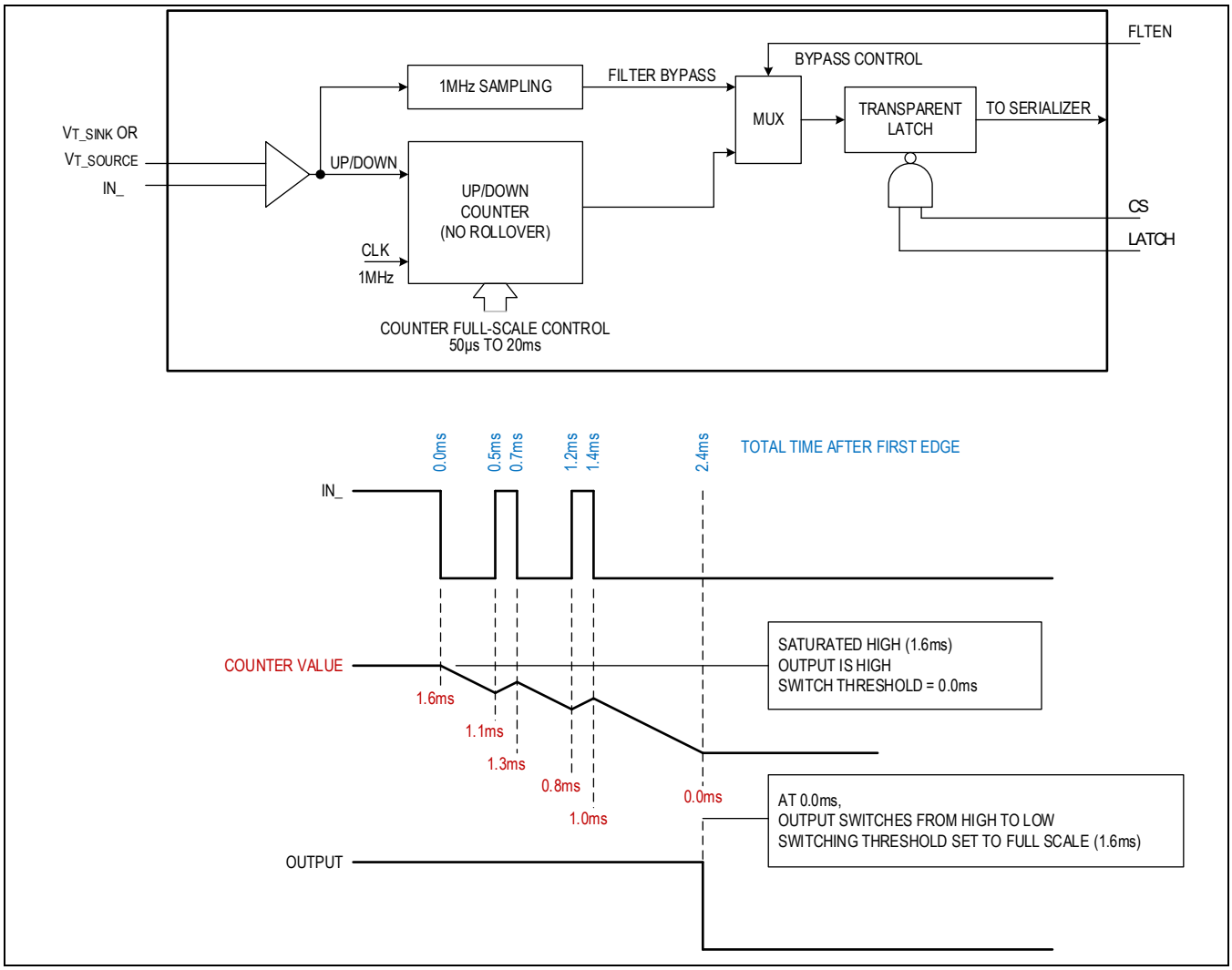



*Figure 3. MAX22194 Digital Filter*

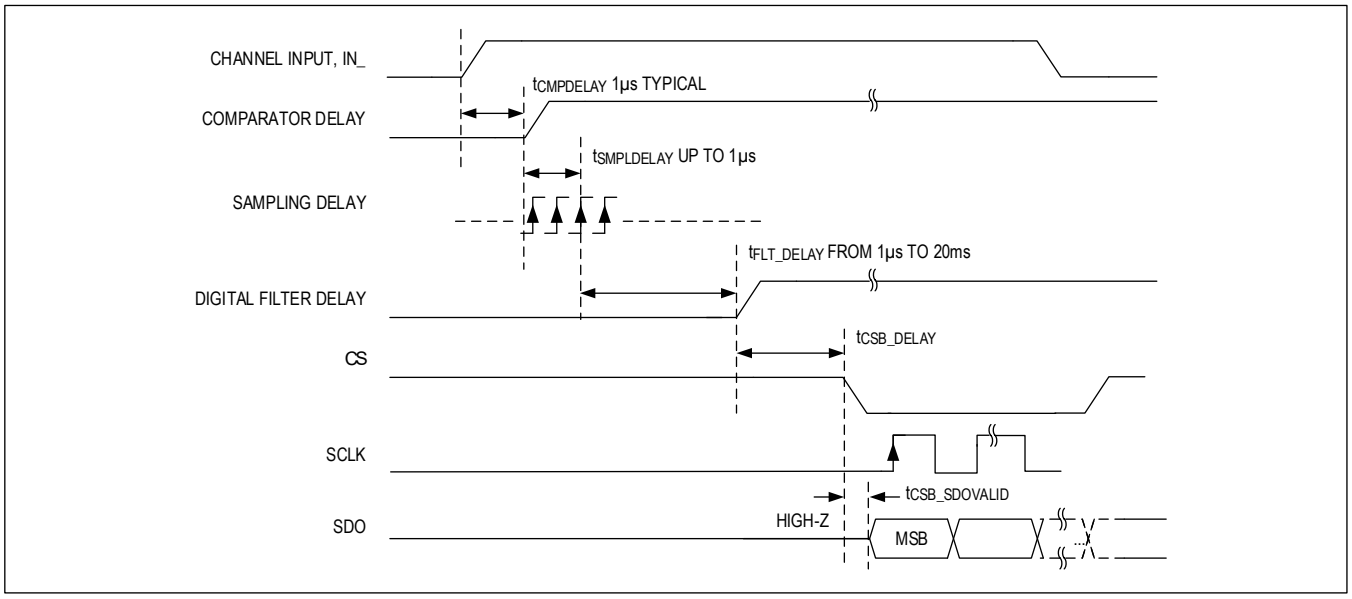



*Figure 4. Channel Input to Output Delay*

## Sampling the IN_ Data

All four inputs of the MAX22194 are simultaneously latched on the falling edge of either $\overline{\text{LATCH}}$ or $\overline{\text{CS}}$, and the data is made available for SPI reading out of the DISTATE register (address 0x00). When the digital filter is disabled by setting the FLTEN_ bit in the corresponding CNFG_ register to 0, the IN_ signals are sampled at a 1MHz sampling rate and the time resolution is ±1µs relative to the $\overline{\text{LATCH}}$ or $\overline{\text{CS}}$ falling edge.

## Power Supply

For normal operation, the MAX22194 needs to be powered by the $V_{24}$ field supply, $V_A$ analog supply, and $V_L$ logic I/O supply. The $V_A$ can be supplied by the internal linear regulator, or by an external supply. The integrated 5V linear regulator generates the $V_A$ supply when the REGEN pin is open. The REGEN pin should be connected to GND when supplying $V_A$ from an external supply in the range of 3.0V to 5.5V.

When powering the MAX22194 from an external 3.3V or 5V supply on $V_A$, $V_{24}$ must be powered by the external 24V supply. If the MAX22194 is only operated in sink or TTL configurations, $V_{24}$ can be powered by the external $V_A$ supply, and a 24V supply is not needed.

The advantage of powering the MAX22194 from an external 5V supply on $V_A$ is to remove the LDO power dissipation from the 24V field supply. The advantage of powering the MAX22194 from the $V_{24}$ field supply is that if the system thermal shutdown (OTSHDN2 bit in the FAULT2 register) occurs, register contents are not lost. See the *SPI Power Status* section for details.

The $V_L$ supply is the logic interface supply in the range of 2.5V to 5.5V. Make sure $V_L$ is always lower than or equal to $V_A$.

## $\overline{\text{READY}}$ Logic

The MAX22194 features a $\overline{\text{READY}}$ signal to indicate that the MAX22194 is powered properly and is ready for normal operation. $\overline{\text{READY}}$ asserts low when both $V_A$ analog supply and $V_L$ logic I/O supply are both above their respective UVLO

thresholds. $\overline{\text{READY}}$ is an open-drain high-side output that needs a pulldown resistor. Note that $\overline{\text{READY}}$ is not associated with the $V_M$ comparator.

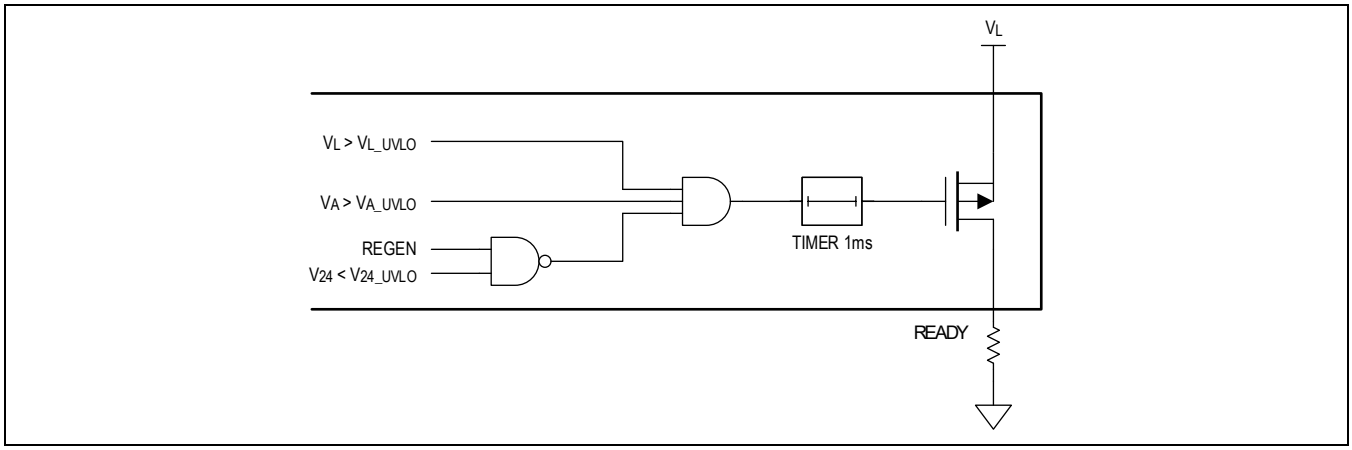



*Figure 5. $\overline{\text{READY}}$ Logic*

## $\overline{\text{VMOK}}$ Supply Monitoring

The MAX22194 features a comparator that can be used to monitor and provide visual indication of the state of a power supply or other voltage. Connecting $V_M$ to an external resistor-divider defines the threshold voltage. $\overline{\text{VMOK}}$ is a high-voltage open-drain output that can drive an LED through a current-limiting resistor. The $V_M$ comparator generates two outputs, the $\overline{\text{VMOK}}$ signal and the VMLOW bit in the FAULT1 register.

The $\overline{\text{VMOK}}$ signal is not used with the $\overline{\text{READY}}$ indication. This allows the $\overline{\text{VMOK}}$ threshold to be set differently from the internal $V_{24\_UVLO}$ thresholds.

## Fault Detection and Monitoring

$\overline{\text{FAULT}}$ is a low-side open-drain output that can be wire ORed with other open-drain outputs and be used to notify the host processor of a fault. When enabled, $\overline{\text{FAULT}}$ goes low to indicate that one or more of the flags in the FAULT1 register are set. These faults are as follows: $V_M$ comparator trip (VMLOW), $V_{24}$ undervoltage alarm (V24UV), overtemperature alarm (TEMPALM), thermal shutdown (OTSHDN1), CRC error detected on the previous SPI frame (CRCERR), a POR occurred, or an unmasked bit in the FAULT2 register is set.

Mask bits in the F1MASK and F2MASK registers select which flags in the FAULT1 and FAULT2 registers assert the $\overline{\text{FAULT}}$ pin. The mask bits do not affect the flags in the FAULT1 register; they only affect the $\overline{\text{FAULT}}$ pin. All bits in the FAULT1 register, except FAULT2, are latched. They remain set until read even if the faults go away. If the fault persists, the fault bit stays as 1 after the read.

The FAULT2 bit in the FAULT1 register is the logic OR of all unmasked bits in the FAULT2 register. It goes to 0 as soon as every unmasked fault bit in the FAULT2 register is cleared. The FAULT2 register can only be cleared by reading it. If the fault persists, the fault bit stays as 1 after the read.

The fault bits can only be cleared on reading the FAULT1 register if the FSPICLR bit in the GLOBLCFG register is 1. If the FSPICLR bit is 0, the fault bits in the FAULT1 register can also be cleared with a successful SPI read or write command except the OTSHDN1 bit.

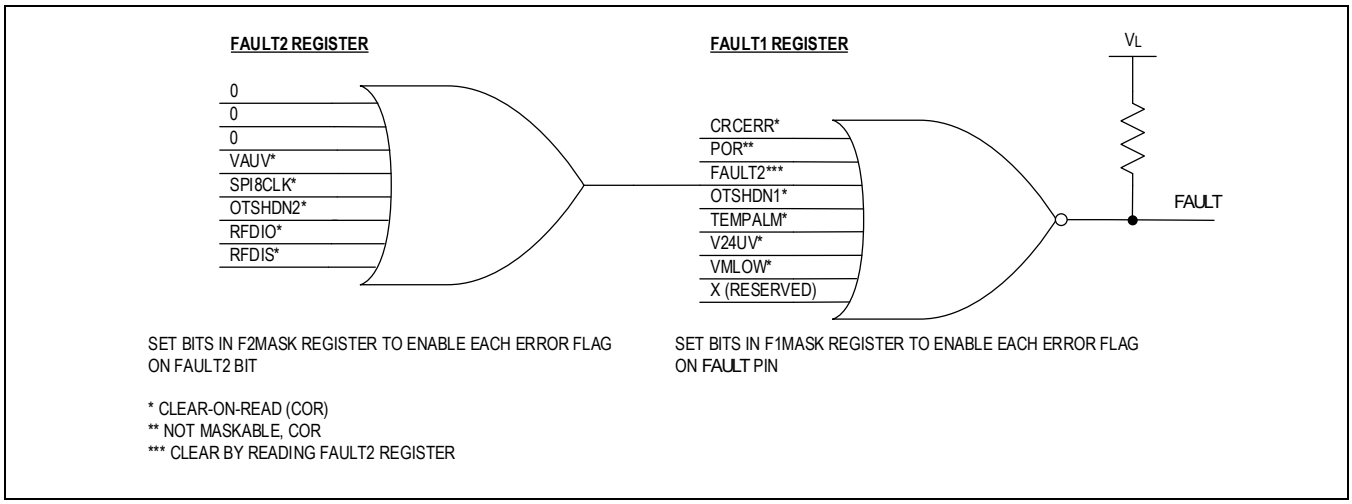



*Figure 6. $\overline{FAULT}$ Output Sources*

## Thermal Considerations

The MAX22194 operates at an ambient air temperature up to +125°C on a properly designed PC board under the following listed conditions. Operating at higher voltages, higher input currents, or with external loads on the internal linear regulator increases power dissipation and reduces the maximum allowable ambient temperature. See *Package Information* and *Absolute Maximum Ratings* sections for thermal specifications.

The 125°C ambient temperature operating conditions include the following:

- Multilayer board (four or more)
- $V_{24}$ = +28.8V max
- 680Ω resistor in series with each IN_ input
- All field input voltage = +30V max
- All logic outputs driving CMOS loads
- Resistor from REFDI to GND = 12kΩ

The MAX22194 has three levels of thermal protection: temperature alarm (TEMPALM bit in the FAULT1 register), thermal shutdown (OTSHDN1 bit in the FAULT1 register), and system thermal shutdown (OTSHDN2 bit in the FAULT2 register).

- Temperature Alarm: If the junction temperature rises to 115°C (typical), the TEMPALM bit in the FAULT1 register is set to 1. The MAX22194 operation is normal when TEMPALM is set to 1.
- Thermal Shutdown: If the temperature rises to 150°C (typical), the OTSHDN1 bit in the FAULT1 register is set to 1. All input channels are forced into high-impedance mode.
- System Thermal Shutdown: If the temperature rises to 165°C (typical), the OTSHDN2 bit in the FAULT2 register is set to 1. All input channels are forced into high-impedance mode. The internal LDO is turned off.

If $V_A$ and $V_L$ are supplied externally and a system thermal shutdown (OTSHDN2) happens, the SPI communication is operational and register access is available. If the external supply is present at $V_A$, the thermal shutdown is less probable, but it could happen if too much current flows through input channels.

If the MAX22194 is powered by $V_{24}$, internal LDO is enabled, and $V_L$ is powered by the internal LDO output $V_A$, when a system thermal shutdown (OTSHDN2) happens, $V_A$ and $V_L$ are powered off, SPI buffers are off, SPI circuitry is powered by a supplementary internal 3.3V voltage, and register values are retained, but it is not feasible to read or write the registers since both $V_A$ and $V_L$ are off.

If the MAX22194 is powered by $V_{24}$, internal LDO is enabled, and $V_L$ is independent from $V_A$, when a system thermal shutdown (OTSHDN2) happens, $V_A$ is powered off, SPI buffers are off, SPI circuitry is powered by a supplementary internal 3.3V voltage, and register values are retained, but it is not feasible to read or write the registers since $V_A$ is off and SPI logic interface is not operational. See *Table 3* for internal circuitry power-up status during different thermal events.

## Table 3. Internal Circuits Power-Up Status During Thermal Events

| THERMAL EVENTS | INTERNAL CIRCUITS | POWER-UP STATUS | |
|---|---|---|---|
| | | Internal LDO Enabled, $V_A$ Generated by $V_{24}$ | Internal LDO Disabled, $V_A$ Supplied Externally |
| TEMPALM | Internal Regulator | ON | OFF |
| | Input Channels | ON | ON |
| | REFDI | ON | ON |
| | Registers | ON | ON |
| | SPI | ON | ON |
| OTSHDN1 | Internal Regulator | ON | OFF |
| | Input Channels | OFF | OFF |
| | REFDI | OFF | OFF |
| | Registers | ON | ON |
| | SPI | ON | ON |
| OTSHDN2 | Internal Regulator | OFF | OFF |
| | Input Channels | OFF | OFF |
| | REFDI | OFF | OFF |
| | Registers | ON | ON |
| | SPI | OFF | ON |

### LED Matrix

The MAX22194 features six logic output pins (LO1 to LO6) that can be configured as six general-purpose push-pull logic outputs (GPO) or as a 4 LED driver matrix. This is achieved by setting the GPO bit in the GLOBLCFG register to 0 for LED matrix mode, or to 1 for GPO mode. In the LED matrix mode, if the LEDs are controlled by the MAX22194 autonomously by setting the LEDINT bit in the GLOBLCFG register to 1, LED1 to LED4 indicate the state of the digital inputs (IN1 to IN4).

#### GPO Bit = 0: LED Matrix Mode

To select the LED matrix mode, bit GPO in the GLOBLCFG register is set to 0. LED1 to LED4 can either be turned on or off by the LED register providing that the LEDINT bit in the GLOBLCFG register is 0 or controlled by the MAX22194 autonomously to indicate per-input channel status. If the LED matrix is controlled autonomously by setting the LEDINT bit to 1, the status LED is automatically turned on when current flows into or out of the corresponding IN_ channel in sink or source modes, or when the input is high in TTL mode. In low-leakage high-impedance (HTL) mode, the status LEDs are always off. When the LEDINT bit is set to 0, LED1 to LED4 are controlled by the LED register.

The LEDs in the ON state are driven with a 33% duty cycle square wave from the $V_A$ supply. The LED current is set through the current-limiting resistor in series from LO1 to LO3 output. Each row (LO4 and LO5) is alternatively kept low for 1ms over a 3ms period. A common column (LO1 to LO3) is high when the corresponding LED is turned on. Current from each resistor flows through only one LED at a time. To get the same brightness as an LED that is turned on permanently, increase the LED current by a factor of three to get the equivalent brightness. Note that the LED matrix is turned off during a thermal shutdown event (OTSHDN1).

#### GPO Bit = 1: GPO Mode

To select the GPO mode, set the GPO bit to 1 in the GLOBLCFG register. The six GPO pins (LO1 to LO6) are then controlled by writing a 0, to set GPO pin low, or a 1, to set GPO pin high, to the corresponding LED1 to LED4, GPO5, and GPO6 bits in the LED register. Note that the GPO drivers are disabled during a system thermal shutdown event (OTSHDN2).

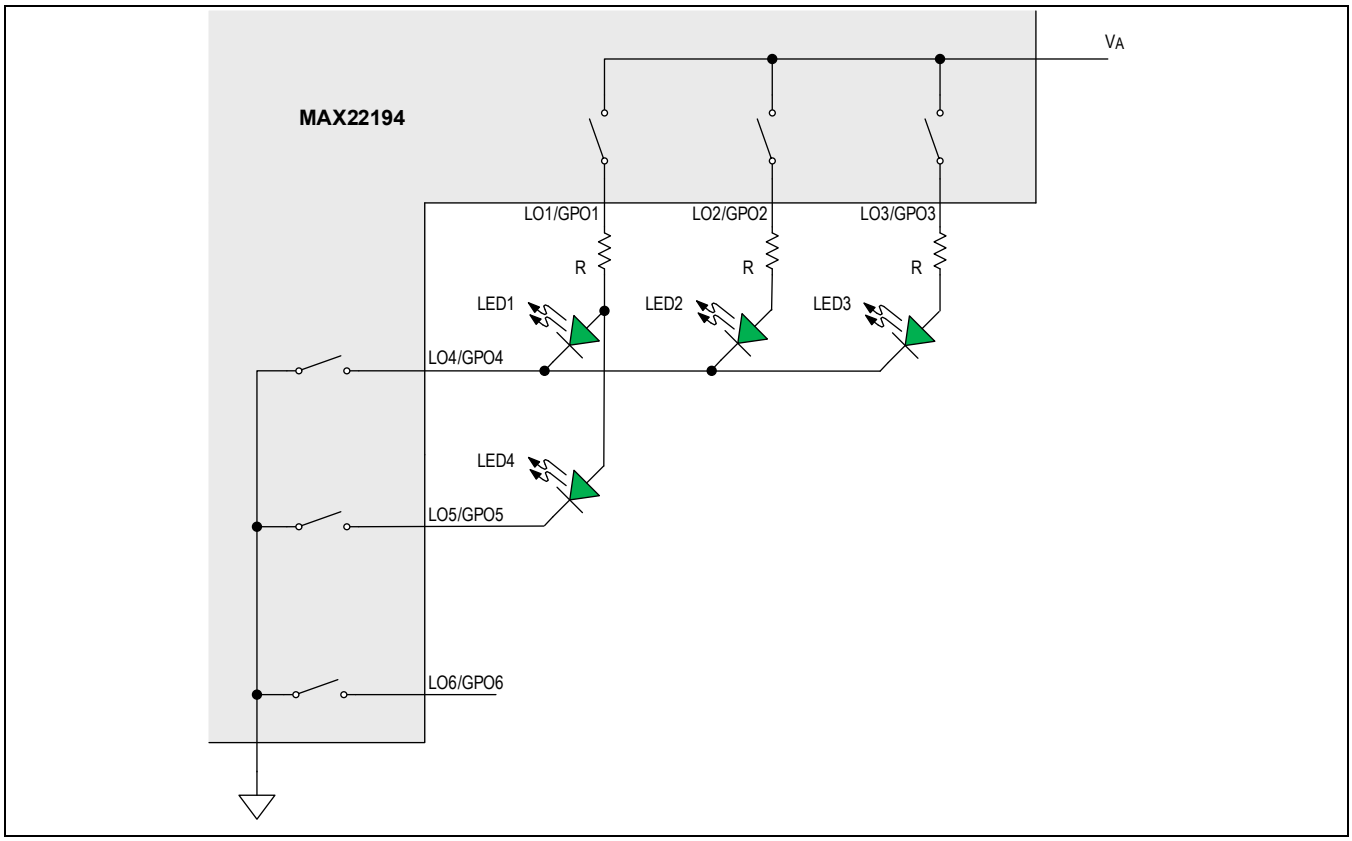



*Figure 7. LED Matrix or GPO Driver Scheme*

## Serial Peripheral Interface

The MAX22194 has an SPI-compatible interface to read input data, read diagnostic data, and configure all the registers. Each configuration register can be read back to ensure proper configuration. The interface can be operated as addressable SPI or daisy-chain mode as selected by the DAISY pin. In addressable SPI mode, it supports direct communication with up to four MAX22194 devices on a shared SPI using a single $\overline{CS}$ signal. Data at the SDI input is sampled on the rising edge of SCLK and data at SDO is updated on the falling edge of SCLK. Transitions of SCLK while $\overline{CS}$ is deasserted (high) are ignored. SCLK must idle low when $\overline{CS}$ is asserted. SDO is three-stated when $\overline{CS}$ is high, allowing multiple SPI devices to share a common SPI. The maximum SPI SCLK rate is 12MHz.

The MAX22194 has a $\overline{LATCH}$ input to allow synchronous sampling of all input channels from multiple modules not controlled by the same $\overline{CS}$. When $\overline{LATCH}$ goes low, digital input data are frozen in the digital input state register DISTATE (address = 0x00) and are clocked out onto SDO when $\overline{CS}$ is driven low. If $\overline{LATCH}$ is high, input data are sampled and frozen at the falling edge of $\overline{CS}$.

### SPI Protocol

The serial output of the device adheres to the SPI protocol, running with CPHA = 0 and CPOL = 0. For addressable SPI mode (DAISY pin held low), the first two MSB bits clocked in on SDI are for A1 and A0 to define the chip address so the MAX22194 device can immediately identify if it is being communicated with. For daisy-chain SPI mode (DAISY pin held high), the first two MSB bits clocked in on SDI are “don’t care” values. See *Figure 8* and *Figure 9* for SPI diagrams in addressable SPI mode. *Figure 12* to *Figure 15* demonstrate the SPI diagrams in daisy-chain mode.

### Addressable SPI Mode

The MAX22194 features an addressable SPI allowing direct SPI access to any of up to four MAX22194 devices on a shared SPI using a common $\overline{CS}$ chip-select signal. This is achieved by assigning a device address to each MAX22194 using the A0 and A1 logic inputs, as listed in *Table 4*. The SPI controller starts off every SPI command by sending the two device address bits so that the MAX22194 immediately identifies if it is being communicated with. Upon identifying

that it is being addressed, the MAX22194 starts clocking out six fault bits from the FAULT1 register, including CRCERR, POR, FAULT2, TEMPALM, V24UV, and VMLOW, on SDO indicating the status of the MAX22194. The SPI write cycle provides the state of four digital inputs on SDO, following the six fault bits and four “don’t care” bits, while the SPI read cycle provides the register value.

If the FSPICLR bit in the GLOBLCFG register is 0, any of the fault bits set in the FAULT1 register, except OTSHDN1, are automatically cleared by a successful SPI command. In contrast, if the FSPICLR bit in the GLOBLCFG register is 1, any of the fault bits set in the FAULT1 register are only reset if the FAULT1 register is read.

## Table 4. SPI Device Address Selection

| A1 | A0 | DEVICE ADDRESS |
|---|---|---|
| Low | Low | 00 |
| Low | High | 01 |
| High | Low | 10 |
| High | High | 11 |

*Figure 8* shows the SPI write command in SPI addressable mode. Every SPI write cycle provides the state of the four digital inputs as data bits DI4 to DI1 on the SDO pin.

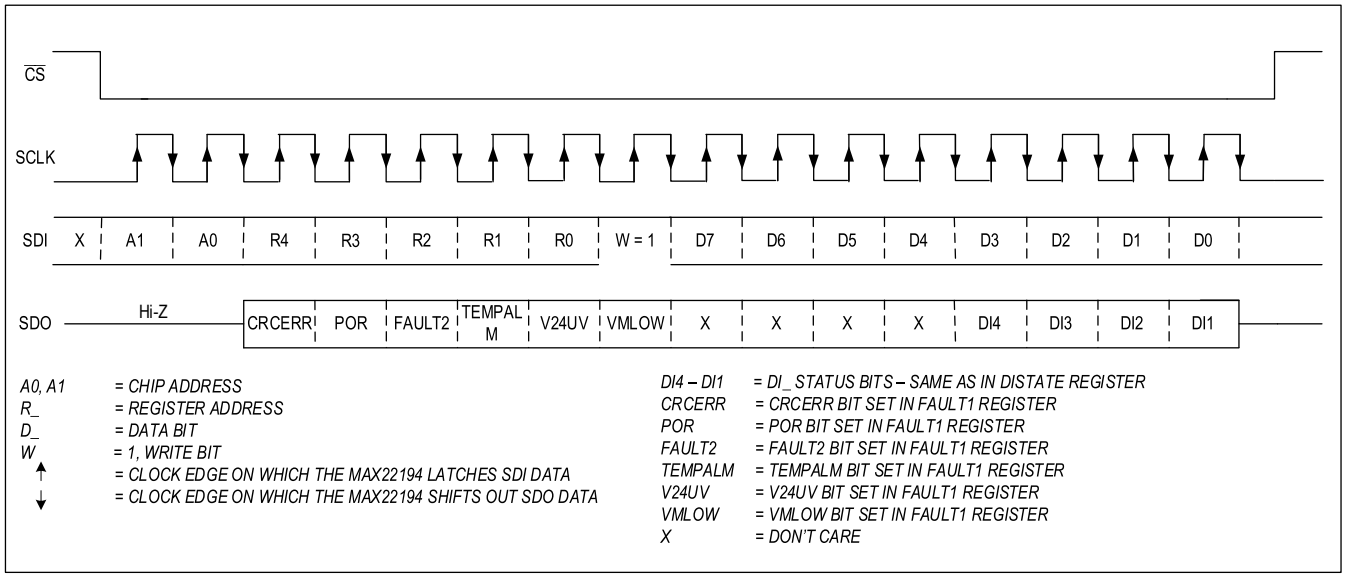



*Figure 8. Write Command in SPI Addressable Mode*

*Figure 9* shows the SPI read command in the SPI addressable mode.

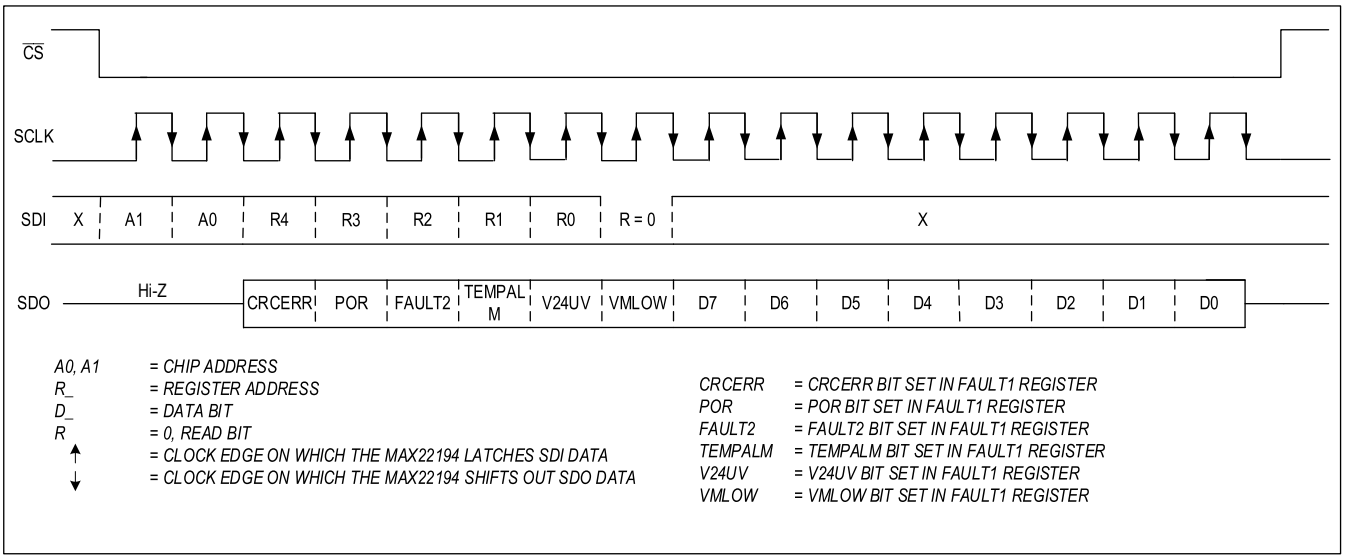



*Figure 9. Read Command in SPI Addressable Mode*

### Daisy-Chain SPI Mode

For systems with more than four sensor inputs, multiple devices can be daisy-chained to allow access to all data inputs through a single serial interface. The MAX22194 can be operated in daisy-chain SPI mode by setting the DAISY pin high. When using a daisy-chain configuration, connect MOSI to SDI of the first device in the chain. Connect MISO to SDO of the last device in the chain. For all middle links, connect SDI to SDO of the previous device and SDO to SDI of the next device. $\overline{CS}$ and SCLK of all devices in the chain should be connected together in parallel. See *Figure 10*, which illustrates a 12-input application with a MAX22194 and a MAX22196 in the daisy-chain mode, and *Figure 11*, which shows the SPI command frames with two devices in the chain. The MAX22194 and the MAX22196 have the same SPI. *Figure 12* to *Figure 15* show different MAX22194 SPI timing diagrams for read and write cycles in daisy-chain mode. Note, in daisy-chain SPI mode, the feature of clearing fault bits by SPI read or write command is disabled, regardless of FSPICLR bit setting.

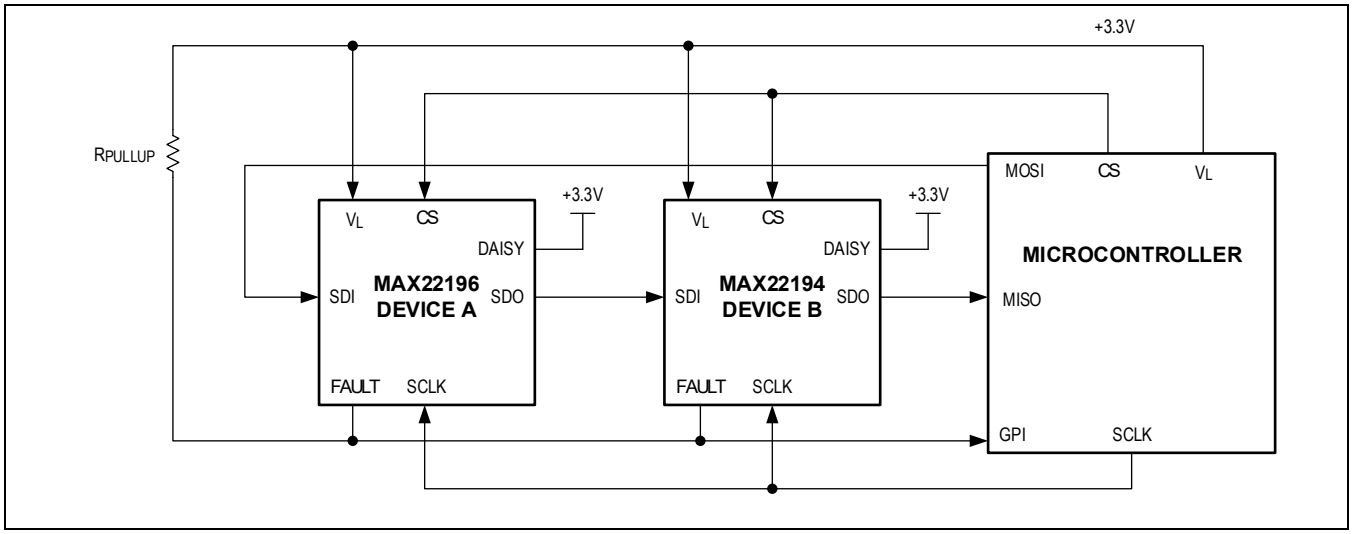



*Figure 10. Daisy-Chain SPI Operation in a 12-Channel Application*

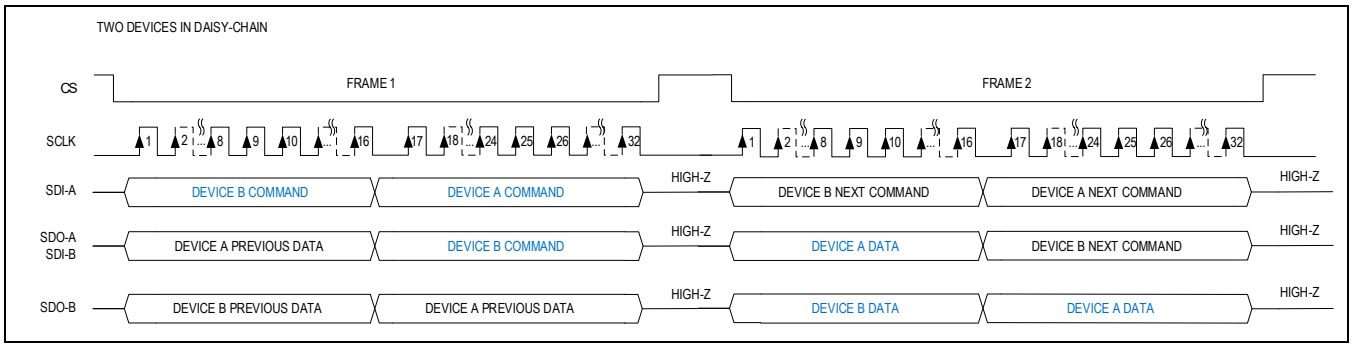



*Figure 11. Daisy-Chain SPI Command Diagram*

*Figure 12* shows the daisy-chain SPI diagram for a write command followed by a prior write cycle. The device provides the status of four digital input channels (DI4 to DI1) and fault bits from the FAULT1 register (F7 to F0) in the first and second byte sent on SDO.

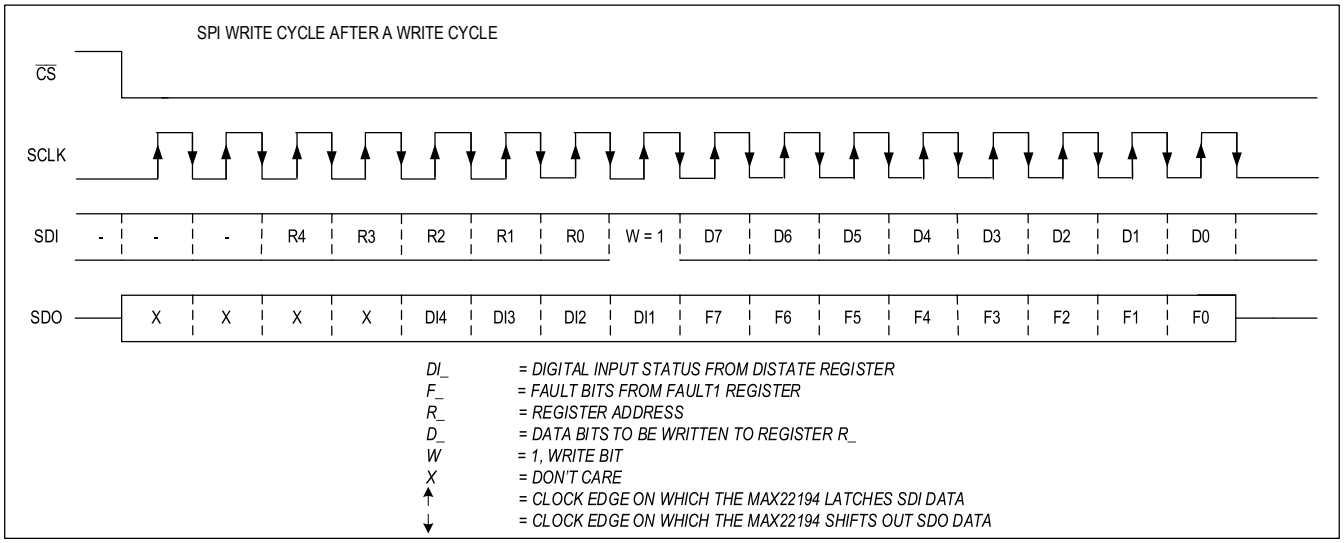



*Figure 12. SPI Write Cycle After a Prior Write Cycle in Daisy-Chain Mode*

Figure 13 shows the daisy-chain SPI diagram for a write command followed by a prior read cycle. The device provides the status of four digital input channels (DI4 to DI1) as the first byte sent on SDO. The second byte on SDO is the register value from the prior read command.

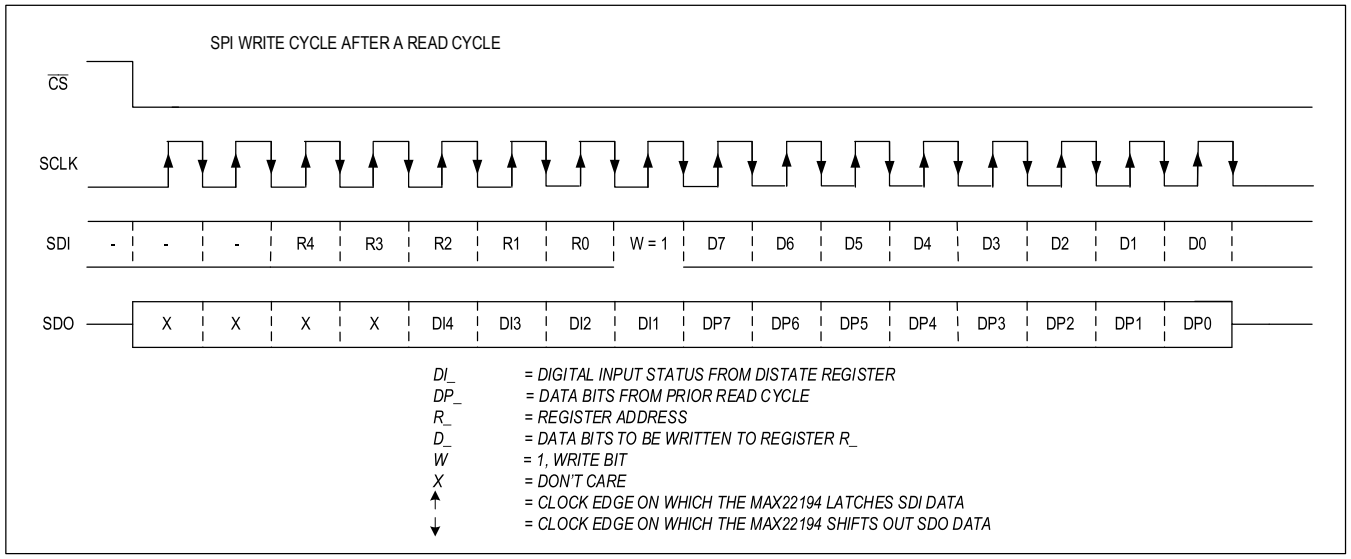



*Figure 13. SPI Write Cycle After a Prior Read Cycle in Daisy-Chain Mode*

Figure 14 shows the daisy-chain SPI diagram for a read command followed by a prior read cycle. The device provides the status of four digital input channels (DI4 to DI1) as the first byte sent on SDO. The second byte on SDO is the register value from the prior read command.

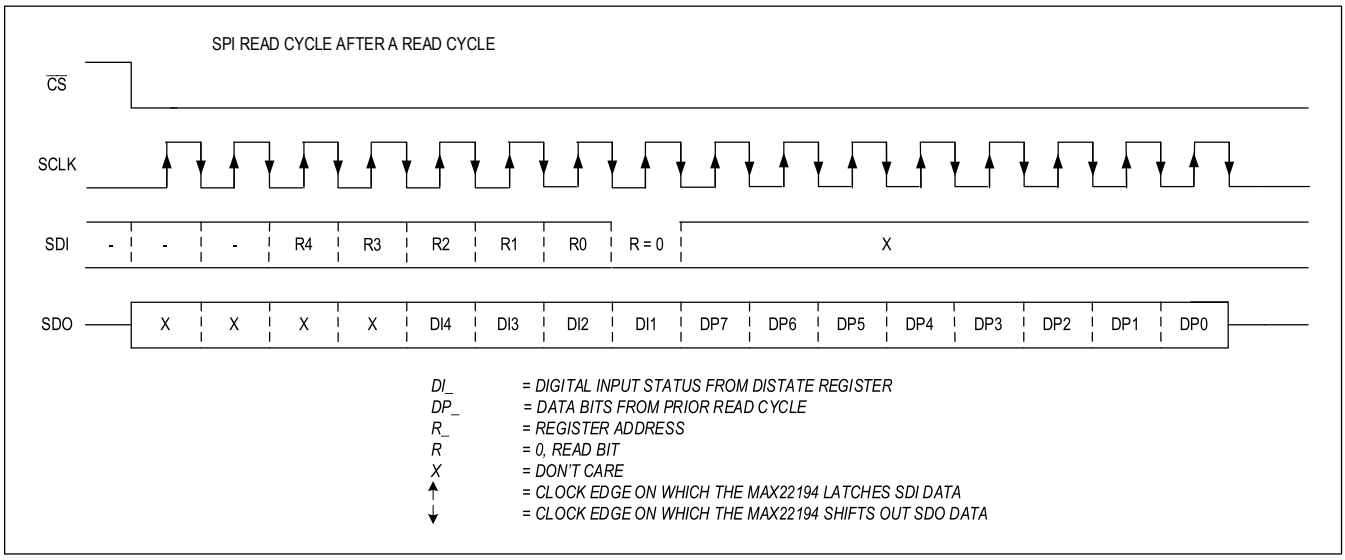



*Figure 14. SPI Read Cycle After a Prior Read Cycle in Daisy-Chain Mode*

Figure 15 shows the daisy-chain SPI diagram for a read command followed by a prior write cycle. The device provides the status of four digital input channels (DI4 to DI1) and fault bits from the FAULT1 register (F7 to F0) in the first and second byte sent on SDO.

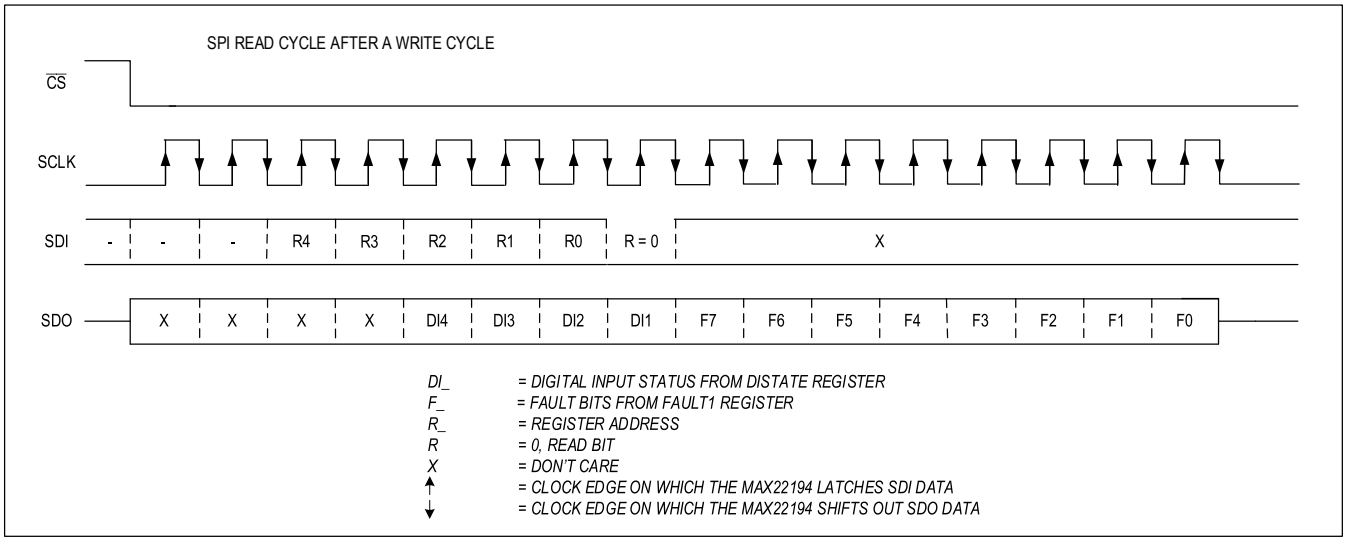



*Figure 15. SPI Read Cycle After a Prior Write Cycle in Daisy-Chain Mode*

### SPI Power Status

Only the SPI I/O buffers are powered from the $V_L$ supply; internal SPI circuits are powered from the $V_A$ supply. Both $V_A$ and $V_L$ must be valid for SPI communication to take place. In addition to powering the SPI circuits, $V_A$ also sustains the SPI memory (configuration and status registers). If power is being supplied through $V_{24}$, then an auxiliary supply for the memory is also available. The auxiliary supply only sustains memory; it does not allow SPI communication. The auxiliary supply takes over if $V_A$ is lost due to external loading or due to a thermal shutdown event. When the event is over, the device configuration is maintained and fault information is available in the FAULT registers. See Table 5 for power requirement for SPI communication and register configuration.

## Table 5. SPI Power Status

| $V_{24}$ | $V_A$ | $V_L$ | REGISTER CONTENTS | SPI COMMUNICATION |
|---|---|---|---|---|
| Valid | Valid | Valid | Data Maintained | Normal Operation |
| Not Valid | Valid | Valid | Data Maintained | Normal Operation |
| Valid | Not Valid | X | Data Maintained | $\overline{CS}$ ignored, SDO is High-Z |
| X | Valid | Not Valid | Data Maintained | $\overline{CS}$ ignored, SDO is High-Z |
| Not Valid | Not Valid | X | Data Lost | $\overline{CS}$ ignored, SDO is High-Z |

*X = Don't Care.*

### CRC Generation

The MAX22194 has an optional CRC error detection on the SPI for both addressable and daisy-chain modes of operation, lengthening the SPI frame by 8 bits, as shown in Table 6. Five CRC bits are used to check data integrity during transfer between the device and an external microcontroller. In applications where the integrity of data transferred is not of concern, the CRC bits can be disabled by holding CRCEN pin low and operating in CRC-disabled mode.

When CRC error detection is enabled by setting the CRCEN pin high, the MAX22194:

1. Performs error detection on the SDI data that it receives from the controller, and
2. Calculates the CRC on the SDO data and appends a check byte at the end of the SDO data stream that it sends to the controller.

This ensures that both the data it receives from the controller and the data it sends to the controller maintains data integrity.

Once enabled, the CRC value is sent with each SPI command. The 5-bit CRC (CR[4:0]) is based on the generator polynomial $P(x) = x^5 + x^4 + x^2 + 1$ with CRC starting value = 0b11111. When CRC is enabled, the MAX22194 expects a check byte appended to the SDI data stream that it receives. The check byte format (CR[4:0]) can be seen in *Figure 16* and *Figure 17*. Refer to *the application note* for CRC algorithm and programming example.

The 5-bit CRC value is calculated using the first 16 data bits plus the three “0s” in the MSBs of the check byte. The result is then appended to this 19-bit data to create the 24-bit SPI data frame. The MAX22194 verifies the received CRC bits, and if no error is detected, the MAX22194 updates the configuration per the SDI data. If a CRC error is detected, the MAX22194 does not change the configuration, but asserts the CRCERR bit in the FAULT1 register. If the mask bit CRCERR_M in the F1MASK register is not set, the $\overline{\text{FAULT}}$ pin is asserted low.

The check byte that the MAX22194 appends to the SDO data has the format, as shown in *Figure 16* and *Figure 17*. The CR[4:0] bits on SDO are calculated based on the 16-bit SDO data plus three “0s”, with two MSB bits considered as 0 during the calculation. This allows the controller to check for the errors on the SDO data received from the MAX22194.

In daisy-chain mode with CRC enabled, the CR[4:0] bits are calculated on all the data sent before the CRC bits, including the first 16 data bits plus the three “0s”. The two MSB bits and data bits 9 to 16 in a read command in the SDI data stream can be 0 or 1 as they have no impact on the MAX22194 configuration, but these bits are used to calculate the CRC bits (CR[4:0]).

## Table 6. SPI Frame Length

| MODE | DAISY | CRCEN | SPI FRAME LENGTH |
|---|---|---|---|
| Addressable SPI Mode, CRC Disabled | 0 | 0 | 16-bit |
| Addressable SPI Mode, CRC Enabled | 0 | 1 | 24-bit |
| Daisy-Chain SPI Mode, CRC Disabled | 1 | 0 | 16-bit per device in the chain |
| Daisy-Chain SPI Mode, CRC Enabled | 1 | 1 | 24-bit per device in the chain |

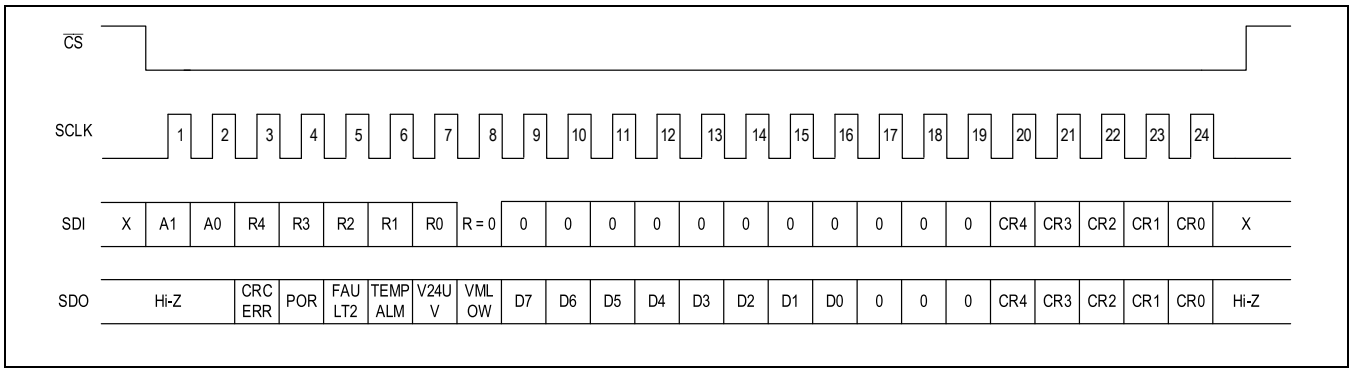



*Figure 16. Addressable SPI Read Command with CRC Enabled*

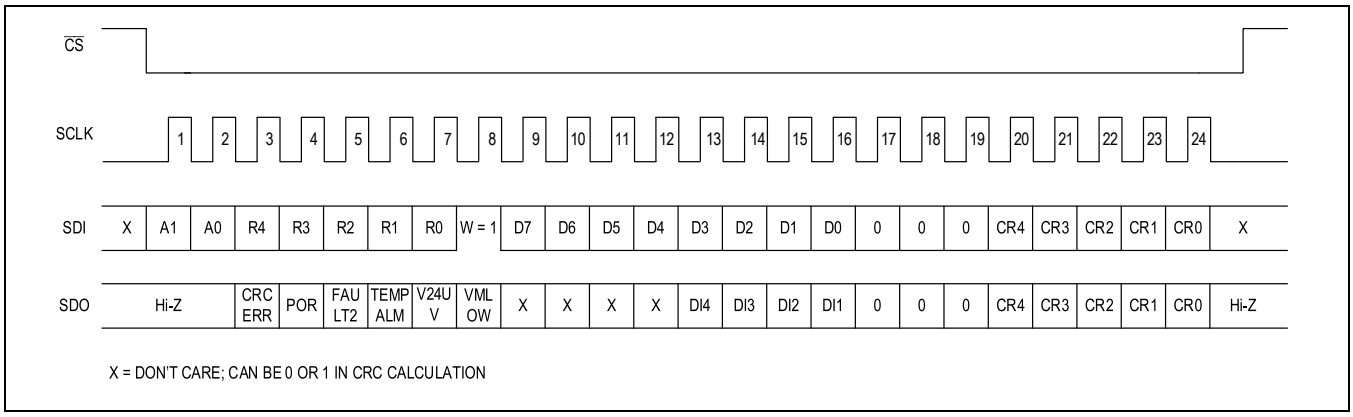



*Figure 17. Addressable SPI Write Command with CRC Enabled*

### Number of Clock Cycles on the SPI

The MAX22194 checks the number of SCLK pulses in each SPI cycle (between $\overline{CS}$ going low and going high). When CRC is enabled (CRCEN held high), the SPI8CLK bit is set if the number of SCLK pulses is not equal to 24. When CRC is disabled (CRCEN held low), the SPI8CLK bit is set if the number of SCLK pulses is not equal to 16. The SPI command is ignored when wrong number of SCLK pulses is received. In the daisy-chain mode, the SPI8CLK is set when the number of SCLK pulses is not a multiple of 16 (CRC disabled) or 24 (CRC enabled).

## Register Map

| ADDRESS | NAME | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|
| **MAX22194** | | | | | | | | | |
| 0x00 | DISTATE[7:0] | Reserved | Reserved | Reserved | Reserved | DI4 | DI3 | DI2 | DI1 |
| 0x01 | FAULT1[7:0] | CRCERR | POR | FAULT2 | OTSHDN1 | TEMPALM | V24UV | VMLOW | Reserved |
| 0x02 | F1MASK[7:0] | CRCERR_M | Reserved | FAULT2_M | OTSHDN1_M | TEMPALM_M | V24UV_M | VMLOW_M | Reserved |
| 0x03 | CNFG1[7:0] | HITHR1 | SOURCE1 | CURR1[1:0] | | FLTEN1 | DELAY1[2:0] | | |
| 0x04 | CNFG2[7:0] | HITHR2 | SOURCE2 | CURR2[1:0] | | FLTEN2 | DELAY2[2:0] | | |
| 0x05 | CNFG3[7:0] | HITHR3 | SOURCE3 | CURR3[1:0] | | FLTEN3 | DELAY3[2:0] | | |
| 0x06 | CNFG4[7:0] | HITHR4 | SOURCE4 | CURR4[1:0] | | FLTEN4 | DELAY4[2:0] | | |
| 0x0B | GLOBLCFG[7:0] | GPO | LEDINT | Reserved | FSPICLR | CLRFILTR | Reserved[1:0] | | REFDISHTCFG |
| 0x0C | LED[7:0] | Reserved | Reserved | GPO6 | GPO5 | LED4 | LED3 | LED2 | LED1 |
| 0x0D | FAULT2[7:0] | Reserved[2:0] | | | VAUV | SPI8CLK | OTSHDN2 | RFDIO | RFDIS |
| 0x0E | F2MASK[7:0] | ID[2:0] | | | VAUV_M | SPI8CLK_M | OTSHDN2_M | RFDIO_M | RFDIS_M |

### Register Details

#### DISTATE (0x0)

Digital Input State. DI_ is the state of the corresponding IN_ pin after filtering.

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | Reserved | Reserved | Reserved | Reserved | DI4 | DI3 | DI2 | DI1 |
| **Reset** | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| **Access Type** | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| Reserved | 7 | Reserved | Reserved |
| Reserved | 6 | Reserved | Reserved |
| Reserved | 5 | Reserved | Reserved |
| Reserved | 4 | Reserved | Reserved |
| DI4 | 3 | IN4 state in normal mode. In counter mode, data is not valid. | 0x0: IN4 = OFF state (low in sink modes, or high in source modes)<br>0x1: IN4 = ON state (high in sink modes, or low in source modes) |
| DI3 | 2 | IN3 state in normal mode. In counter mode, data is not valid. | 0x0: IN3 = OFF state (low in sink modes, or high in source modes)<br>0x1: IN3 = ON state (high in sink modes, or low in source modes) |
| DI2 | 1 | IN2 state in normal mode. In counter mode, data is not valid. | 0x0: IN2 = OFF state (low in sink modes, or high in source modes)<br>0x1: IN2 = ON state (high in sink modes, or low in source modes) |
| DI1 | 0 | IN1 state in normal mode. In counter mode, data is not valid. | 0x0: IN1 = OFF state (low in sink modes, or high in source modes)<br>0x1: IN1 = ON state (high in sink modes, or low in source modes) |

## FAULT1 (0x1)

FAULT1 Register Sources

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | CRCERR | POR | FAULT2 | OTSHDN1 | TEMPALM | V24UV | VMLOW | Reserved |
| **Reset** | 0b0 | 0b1 | 0b1 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| **Access Type** | Read Clears All | Read Clears All | Read, Ext | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| CRCERR | 7 | CRC error detected in SPI frame. CRC error detection is enabled when CRCEN is held high. | 0x0: No SPI CRC error was detected.<br>0x1: An SPI CRC error was detected. |
| POR | 6 | Power On Reset (POR) | 0x0: Normal operating condition<br>0x1: A power-on-reset (POR) event was detected. All registers are reset to power-on-reset/default values. |
| FAULT2 | 5 | FAULT2 Register Bits. This is the logical OR of the unmasked bits in the FAULT2 register. The bit is automatically cleared when the unmasked bits in the FAULT2 register are cleared. To mask the FAULT2 register bits, refer to the F2MASK register. | 0x0: No unmasked bit in the FAULT2 register is set.<br>0x1: At least one of the unmasked bits in the FAULT2 register is set. |
| OTSHDN1 | 4 | Thermal Shutdown | 0x0: Normal operating condition<br>0x1: Thermal Shutdown threshold (150°C, typ) has been exceeded. All input channels, input sink or source currents and LED matrix are turned off to reduce power |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| | | | dissipation. GPO drivers, SPI and internal regulator remain active. |
| TEMPALM | 3 | Temperature Alarm | 0x0: Normal operating condition<br>0x1: Temperature Alarm threshold (115°C, typ) has been exceeded. The device is in normal operating condition. |
| V24UV | 2 | $V_{24}$ Undervoltage Monitor | 0x0: The $V_{24}$ supply voltage is above the $V_{24}$ undervoltage threshold.<br>0x1: The $V_{24}$ supply voltage is below the $V_{24}$ undervoltage threshold. |
| VMLOW | 1 | $V_M$ Voltage Comparator Output Status | 0x0: The input voltage of the $V_M$ comparator is higher than 0.81V (rising, typ).<br>0x1: The input voltage of the $V_M$ comparator is lower than 0.78V (falling, typ). |
| Reserved | 0 | Reserved | Reserved |

## F1MASK (0x2)

Mask bits controlling assertion of the $\overline{FAULT}$ pin on the FAULT1 register events.

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | CRCERR_M | Reserved | FAULT2_M | OTSHDN1_M | TEMPALM_M | V24UV_M | VMLOW_M | Reserved |
| **Reset** | 0b0 | 0b0 | 0b1 | 0b0 | 0b0 | 0b1 | 0b1 | 0b0 |
| **Access Type** | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| CRCERR_M | 7 | CRC Error Mask | 0x0: CRCERR unmasked. The $\overline{FAULT}$ pin is asserted when a CRC error is detected.<br>0x1: CRCERR masked. The $\overline{FAULT}$ pin is not asserted when a CRC error is detected. |
| Reserved | 6 | Reserved | Reserved |
| FAULT2_M | 5 | FAULT2 Mask | 0x0: FAULT2 unmasked. The $\overline{FAULT}$ pin is asserted when an unmasked bit in the FAULT2 register is set.<br>0x1: FAULT2 masked. The $\overline{FAULT}$ pin is not asserted when an unmasked bit in the FAULT2 register is set. |
| OTSHDN1_M | 4 | Thermal Shutdown Mask | 0x0: OTSHDN1 unmasked. The $\overline{FAULT}$ pin is asserted when thermal shutdown threshold temperature (150°C, typ) is exceeded.<br>0x1: OTSHDN1 masked. The $\overline{FAULT}$ pin is not asserted when thermal shutdown threshold temperature (150°C, typ) is exceeded. |
| TEMPALM_M | 3 | Temperature Alarm Mask | 0x0: TEMPALM unmasked. The $\overline{FAULT}$ pin is asserted when temperature alarm threshold (115°C, typ) is exceeded.<br>0x1: TEMPALM masked. The $\overline{FAULT}$ pin is not asserted when temperature alarm threshold (115°C, typ) is exceeded. |
| V24UV_M | 2 | $V_{24}$ Undervoltage Mask | 0x0: V24UV unmasked. The $\overline{FAULT}$ pin is asserted when $V_{24}$ is below its undervoltage threshold.<br>0x1: V24UV masked. The $\overline{FAULT}$ pin is not asserted when $V_{24}$ is below its undervoltage threshold. |
| VMLOW_M | 1 | $V_M$ Low Voltage Mask | 0x0: VMLOW unmasked. The $\overline{FAULT}$ pin is asserted when $V_M$ is below the $V_M$ comparator threshold. |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| | | | 0x1: VMLOW masked. The $\overline{FAULT}$ pin is not asserted when $V_M$ is below the $V_M$ comparator threshold. |
| Reserved | 0 | Reserved | Reserved |

## CNFG1 (0x3)

IN1 Channel Configuration

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | HITHR1 | SOURCE1 | CURR1[1:0] | | FLTEN1 | DELAY1[2:0] | | |
| **Reset** | 0b0 | 0x0 | 0b00 | | 0b1 | 0b100 | | |
| **Access Type** | Write, Read | Write, Read | Write, Read | | Write, Read | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| HITHR1 | 7 | Channel 1 Voltage Threshold Selection for DI Modes | 0x0: In DI modes (CURR1[1:0] = 0x00, 0x01, 0x02), IN1 voltage threshold is low.<br>0x1: In DI modes (CURR1[1:0] = 0x00, 0x01, 0x02), IN1 voltage threshold is high. |
| SOURCE1 | 6 | Channel 1 Digital Input Sink or Source Mode Selection | 0x0: Sink Mode<br>0x1: Source Mode |
| CURR1 | 5:4 | The CURR1[1:0] bits select the channel 1 sink or source current scaling factor relative to the current set by the REFDI resistor. Refer to Table 1 for CNFG_ register configuration in different input modes. | 0x0: Sink or source current is turned off. Input comparator threshold is set to HTL mode.<br>0x1: 1x Current<br>0x2: 3x Current<br>0x3: TTL operation with sink or source current off |
| FLTEN1 | 3 | Channel 1 Glitch Filter Enable | 0x0: Input glitch filter is disabled.<br>0x1: Input glitch filter is enabled. |
| DELAY1 | 2:0 | Channel 1 Input Glitch Filter Delay | 0x0: 50µs<br>0x1: 100µs<br>0x2: 400µs<br>0x3: 800µs<br>0x4: 1.6ms<br>0x5: 3.2ms<br>0x6: 12.8ms<br>0x7: 20ms |

## CNFG2 (0x4)

IN2 Channel Configuration

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | HITHR2 | SOURCE2 | CURR2[1:0] | | FLTEN2 | DELAY2[2:0] | | |
| **Reset** | 0b0 | 0x0 | 0b00 | | 0b1 | 0b100 | | |
| **Access Type** | Write, Read | Write, Read | Write, Read | | Write, Read | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| HITHR2 | 7 | Channel 2 Voltage Threshold Selection for DI Modes | 0x0: In DI modes (CURR2[1:0] = 0x00, 0x01, 0x02), IN2 voltage threshold is low.<br>0x1: In DI modes (CURR2[1:0] = 0x00, 0x01, 0x02), IN2 voltage threshold is high. |
| SOURCE2 | 6 | Channel 2 Digital Input Sink or Source Mode Selection | 0x0: Sink Mode<br>0x1: Source Mode |
| CURR2 | 5:4 | The CURR2[1:0] bits select the channel 2 sink or source current scaling factor relative to the current set by the REFDI resistor. Refer to Table 1 for CNFG_ register configuration in different input modes. | 0x0: Sink or source current is turned off. Input comparator threshold is set to HTL mode.<br>0x1: 1x Current<br>0x2: 3x Current<br>0x3: TTL operation with sink or source current off |
| FLTEN2 | 3 | Channel 2 Glitch Filter Enable | 0x0: Input glitch filter is disabled.<br>0x1: Input glitch filter is enabled. |
| DELAY2 | 2:0 | Channel 2 Input Glitch Filter Delay | 0x0: 50µs<br>0x1: 100µs<br>0x2: 400µs<br>0x3: 800µs<br>0x4: 1.6ms<br>0x5: 3.2ms<br>0x6: 12.8ms<br>0x7: 20ms |

## CNFG3 (0x5)

IN3 Channel Configuration

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | HITHR3 | SOURCE3 | CURR3[1:0] | | FLTEN3 | DELAY3[2:0] | | |
| **Reset** | 0b0 | 0x0 | 0b00 | | 0b1 | 0b100 | | |
| **Access Type** | Write, Read | Write, Read | Write, Read | | Write, Read | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| HITHR3 | 7 | Channel 3 Voltage Threshold Selection for DI Modes | 0x0: In DI modes (CURR3[1:0] = 0x00, 0x01, 0x02), IN3 voltage threshold is low.<br>0x1: In DI modes (CURR3[1:0] = 0x00, 0x01, 0x02), IN3 voltage threshold is high. |
| SOURCE3 | 6 | Channel 3 Digital Input Sink or Source Mode Selection | 0x0: Sink Mode<br>0x1: Source Mode |
| CURR3 | 5:4 | The CURR3[1:0] bits select the channel 3 sink or source current scaling factor relative to the current set by the REFDI resistor. Refer to Table 1 for CNFG_ register configuration in different input modes. | 0x0: Sink or source current is turned off. Input comparator threshold is set to HTL mode.<br>0x1: 1x Current<br>0x2: 3x Current<br>0x3: TTL operation with sink or source current off |
| FLTEN3 | 3 | Channel 3 Glitch Filter Enable | 0x0: Input glitch filter is disabled.<br>0x1: Input glitch filter is enabled. |
| DELAY3 | 2:0 | Channel 3 Input Glitch Filter Delay | 0x0: 50µs<br>0x1: 100µs<br>0x2: 400µs<br>0x3: 800µs |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| | | | 0x4: 1.6ms<br>0x5: 3.2ms<br>0x6: 12.8ms<br>0x7: 20ms |

## CNFG4 (0x6)

IN4 Channel Configuration

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | HITHR4 | SOURCE4 | CURR4[1:0] | | FLTEN4 | DELAY4[2:0] | | |
| **Reset** | 0b0 | 0x0 | 0b00 | | 0b1 | 0b100 | | |
| **Access Type** | Write, Read | Write, Read | Write, Read | | Write, Read | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| HITHR4 | 7 | Channel 4 Voltage Threshold Selection for DI Modes | 0x0: In DI modes (CURR4[1:0] = 0x00, 0x01, 0x02), IN4 voltage threshold is low.<br>0x1: In DI modes (CURR4[1:0] = 0x00, 0x01, 0x02), IN4 voltage threshold is high. |
| SOURCE4 | 6 | Channel 4 Digital Input Sink or Source Mode Selection | 0x0: Sink Mode<br>0x1: Source Mode |
| CURR4 | 5:4 | The CURR4[1:0] bits select the channel 4 sink or source current scaling factor relative to the current set by the REFDI resistor. Refer to Table 1 for CNFG_ register configuration in different input modes. | 0x0: Sink or source current is turned off. Input comparator threshold is set to HTL mode.<br>0x1: 1x Current<br>0x2: 3x Current<br>0x3: TTL operation with sink or source current off |
| FLTEN4 | 3 | Channel 4 Glitch Filter Enable | 0x0: Input glitch filter is disabled.<br>0x1: Input glitch filter is enabled. |
| DELAY4 | 2:0 | Channel 4 Input Glitch Filter Delay | 0x0: 50µs<br>0x1: 100µs<br>0x2: 400µs<br>0x3: 800µs<br>0x4: 1.6ms<br>0x5: 3.2ms<br>0x6: 12.8ms<br>0x7: 20ms |

## GLOBLCFG (0xB)

Global Configuration

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | GPO | LEDINT | Reserved | FSPICLR | CLRFILTR | Reserved[1:0] | | REFDISHTCFG |
| **Reset** | 0b0 | 0b0 | 0b0 | 0b1 | 0b0 | 0x0 | | 0b0 |
| **Access Type** | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| GPO | 7 | Configure LO1 to LO6 Outputs to be LED Matrix or GPO Drivers | 0x0: LO1 to LO5 are open-drain outputs driving the LED matrix. The LEDs are turned on or off using the LED1 to LED4 bits in the LED register if the LEDINT bit is 0, or controlled autonomously by IN1 to IN4 input status if the LEDINT bit is 1.<br>0x1: LO1 to LO6 are push-pull logic outputs that are driven high or low using the GPO6, GPO5, and LED4 to LED1 bits in the LED register. The LEDINT bit is "don't care" in this mode. |
| LEDINT | 6 | LED Matrix User Control or Autonomous Control Selection | 0x0: When the GPO bit is 0, the LO1 to LO5 pins are controlled by the LED1 to LED4 bits in the LED register. This bit is "don't care" when the GPO bit is 1.<br>0x1: When the GPO bit is 0, the LO1 to LO5 pins are controlled autonomously based on the status of the IN_ pins. LED1 to LED4 reflect the IN1 to IN4 input status respectively. This bit is "don't care" when the GPO bit is 1. |
| Reserved | 5 | Reserved | Reserved |
| FSPICLR | 4 | Configures how the bits in the FAULT1 register are cleared | 0x0: Fault bits in the FAULT1 register, except OTSHDN1 bit, are cleared automatically during a successful (no error) SPI read or write command. Bit FAULT2 is cleared when all unmasked fault bits in the FAULT2 register are cleared by reading it.<br>0x1: Fault bits in FAULT1 register are only cleared when the FAULT1 register is read. |
| CLRFILTR | 3 | Fix all input glitch filters to mid-scale value | 0x0: All input filters operate normally.<br>0x1: All input glitch filters are fixed at mid-scale value for the chosen delay. The filters resume normal operation when CLRFILTR is set to 0. |
| Reserved | 2:1 | Reserved | Reserved |
| REFDISHTCFG | 0 | REFDI Pin Short Detection Enable | 0x0: Disables the detection of a short-circuit condition on the REFDI pin<br>0x1: Enable the detection of a short-circuit condition on the REFDI pin |

## LED (0xC)

LED or GPO On or Off Control Register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | Reserved | Reserved | GPO6 | GPO5 | LED4 | LED3 | LED2 | LED1 |
| **Reset** | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| **Access Type** | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| Reserved | 7 | Reserved | Reserved |
| Reserved | 6 | Reserved | Reserved |
| GPO6 | 5 | LO6 Control | 0x0: The LO6 pin is driven low when the GPO bit is 1. LO6 is “don’t care” when the GPO pin is 0.<br>0x1: The LO6 pin is driven high when the GPO bit is 1. LO6 is “don’t care” when the GPO pin is 0. |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| GPO5 | 4 | LO5 Control | 0x0: The LO5 pin is driven low when the GPO bit is 1. The LO5 pin is connected in the LED matrix when the GPO bit is 0.<br>0x1: The LO5 pin is driven high when the GPO bit is 1. The LO5 pin is connected in the LED matrix when the GPO bit is 0. |
| LED4 | 3 | LED4 or LO4 Control | 0x0: LED4 is turned off when the GPO and LEDINT bits are both 0, or the LO4 pin is driven low when the GPO bit is 1.<br>0x1: LED4 is turned on when the GPO and LEDINT bits are both 0, or the LO4 pin is driven high when the GPO bit is 1. |
| LED3 | 2 | LED3 or LO3 Control | 0x0: LED3 is turned off when the GPO and LEDINT bits are both 0, or the LO3 pin is driven low when the GPO bit is 1.<br>0x1: LED3 is turned on when the GPO and LEDINT bits are both 0, or the LO3 pin is driven high when the GPO bit is 1. |
| LED2 | 1 | LED2 or LO2 Control | 0x0: LED2 is turned off when the GPO and LEDINT bits are both 0, or the LO2 pin is driven low when the GPO bit is 1.<br>0x1: LED2 is turned on when the GPO and LEDINT bits are both 0, or the LO2 pin is driven high when the GPO bit is 1. |
| LED1 | 0 | LED1 or LO1 Control | 0x0: LED1 is turned off when the GPO and LEDINT bits are both 0, or the LO1 pin is driven low when the GPO bit is 1.<br>0x1: LED1 is turned on when the GPO and LEDINT bits are both 0, or the LO1 pin is driven high when the GPO bit is 1. |

## FAULT2 (0xD)

FAULT2 Register Sources

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | Reserved[2:0] | | | VAUV | SPI8CLK | OTSHDN2 | RFDIO | RFDIS |
| **Reset** | 0x0 | | | 0x1 | 0b0 | 0b0 | 0b0 | 0b0 |
| **Access Type** | Read Only | | | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| Reserved | 7:5 | Reserved | Reserved |
| VAUV | 4 | $V_A$ Undervoltage Monitor | 0x0: The $V_A$ supply voltage is above the $V_A$ undervoltage threshold.<br>0x1: The $V_A$ supply voltage is below the $V_A$ undervoltage threshold. |
| SPI8CLK | 3 | Number of SCLK Cycles Error | 0x0: No SPI SCLK cycle error. In the addressable SPI mode, the MAX22194 has received a number of clock cycles equal to 24 if CRC is enabled, or 16 if CRC is disabled. In the daisy-chain mode, the device has received a number of clock cycles equal to a multiple of 24 if CRC is enabled, or a multiple of 16 if CRC is disabled.<br>0x1: SPI SCLK cycle error. In the addressable SPI mode, |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| | | | the MAX22194 has received a number of clock cycles not equal to 24 if CRC is enabled, or 16 if CRC is disabled. In the daisy-chain mode, the device has received a number of clock cycles not equal to a multiple of 24 if CRC is enabled, or a multiple of 16 if CRC is disabled. The SPI command is ignored when wrong number of SCLK pulses is received. |
| OTSHDN2 | 2 | System Thermal Shutdown | 0x0: System Thermal Shutdown threshold (165°C, typ) has not been exceeded.<br>0x1: System Thermal Shutdown threshold (165°C, typ) has been exceeded. All input channels, input sink or source currents, LED matrix, GPO drivers, SPI and internal regulator are turned off to reduce power dissipation. |
| RFDIO | 1 | Open-Circuit Error Detected on the REFDI Pin | 0x0: Normal operating condition<br>0x1: An open-circuit condition is detected on the REFDI pin. This bit is 1 when thermal shutdown happens, because REFDI function turns off in thermal shutdown. No action on the input channels when this condition occurs. |
| RFDIS | 0 | Short-circuit fault is detected on the REFDI pin. The short-circuit detection on the REFDI pin is enabled by setting the REFDISHTCFG bit to 1. If REFDISHTCFG is 0, the RFDIS fault keeps the previous latched value when the short-circuit detection is on. | 0x0: Normal operating condition<br>0x1: A short-circuit condition is detected on the REFDI pin. All the input channels are disabled as long as the short-circuit condition on REFDI is present. |

## F2MASK (0xE)

Mask bits controlling assertion of the FAULT2 bit in the FAULT1 register. The FAULT2 bit is the logic OR of all the bits in the FAULT2 register which are not masked.

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | ID[2:0] | | | VAUV_M | SPI8CLK_M | OTSHDN2_M | RFDIO_M | RFDIS_M |
| **Reset** | 0x1 | | | 0x0 | 0b0 | 0b1 | 0b0 | 0b0 |
| **Access Type** | Read Only | | | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| ID | 7:5 | Chip ID | |
| VAUV_M | 4 | $V_A$ Undervoltage Mask | 0x0: VAUV unmasked. The FAULT2 bit in the FAULT1 register follows the VAUV bit setting.<br>0x1: VAUV masked. The FAULT2 bit in the FAULT1 register does not change if the VAUV bit changes. |
| SPI8CLK_M | 3 | Mask for Number of SCLK Cycles Error | 0x0: SPI8CLK unmasked. The FAULT2 bit in the FAULT1 register follows the SPI8CLK bit setting.<br>0x1: SPI8CLK masked. The FAULT2 bit in the FAULT1 register does not change if the SPI8CLK bit changes. |
| OTSHDN2_M | 2 | System Thermal Shutdown Mask | 0x0: OTSHDN2 unmasked. The FAULT2 bit in the FAULT1 register follows the OTSHDN2 bit setting.<br>0x1: OTSHDN2 masked. The FAULT2 bit in the FAULT1 register does not change if the OTSHDN2 bit changes. |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RFDIO_M | 1 | Mask for Open-Circuit Error on the REFDI Pin | 0x0: RFDIO unmasked. The FAULT2 bit in the FAULT1 register follows the RFDIO bit setting.<br>0x1: RFDIO masked. The FAULT2 bit in the FAULT1 register does not change if the RFDIO bit changes. |
| RFDIS_M | 0 | Mask for Short-Circuit Error on the REFDI Pin | 0x0: RFDIS unmasked. The FAULT2 bit in the FAULT1 register follows the RFDIS bit setting.<br>0x1: RFDIS masked. The FAULT2 bit in the FAULT1 register does not change if the RFDIS bit changes. |

## Applications Information

### Power Supply Sequencing

The MAX22194 does not require special power supply sequencing. The logic interface supply ($V_L$) is set independently from the field supply ($V_{24}$) or LDO output ($V_A$) levels.

### Power Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass $V_{24}$ and $V_A$ with 1µF ceramic capacitors to GND and bypass $V_L$ with 0.1µF ceramic capacitor to GND, respectively. Place the bypass capacitors as close as possible to the power supply input pins.

### PCB Layout Recommendations

The PCB designer should follow some critical recommendations to get the best performance from the design.

- Keep the input/output traces as short as possible. To keep signal paths low-inductance, avoid using vias.
- Have a solid ground plane underneath the entire EP area with multiple thermal vias for best thermal performance.
- Maximize the metal coverage for all layers, especially the top and bottom layers to optimize the heat dissipation.
- Use 2oz copper for the top and bottom layers, if possible, so that more heat can be drawn to the PCB.
- Maximize the number of vias under the package for thermal purposes. If possible, fill the via with copper, which further enhances the vertical heat transfer through the PCB.

### Powering $V_A$ Supply Externally

The $V_A$ pin can alternatively be powered by an external 3V to 5.5V supply. In this configuration, disable the on-chip regulator by connecting REGEN pin to GND. This configuration reduces the power dissipation in the chip by 1.3mA x ($V_{24}$ - 5V), typical. When powering the MAX22194 from an external 3.3V or 5V supply on $V_A$, $V_{24}$ must be powered by external 24V supply for source configurations. If the MAX22194 is only operated in sink or TTL configurations, $V_{24}$ can be powered by the external $V_A$ supply, and a 24V supply is not needed.

When $V_{24}$ is powered by the $V_A$ supply, the device always indicates a 24V undervoltage fault due to the V24UV bit in the FAULT1 register, and the $\overline{FAULT}$ pin is always active (low) if the bit is unmasked in the F1MASK register. To overcome this, set bit V24UV_M in the F1MASK register to 1.

### Isolating the SPI

A companion digital isolator, the MAX14483, is optimized to support the MAX22194. The MAX14483 is a six-channel, 3.75k$V_{RMS}$, low-power digital isolator ideal for interfacing to low-voltage products such as microcontrollers or FPGAs. *Figure 18* demonstrates a MAX22194 and a MAX22196 in daisy-chain operation, showing SPI signals, control signals, and power monitoring signal isolated between the field and logic side of the design. A single MAX14483 can be used for multiple MAX22194 and MAX22196 devices. *Figure 19* demonstrates a MAX22194 and a MAX22196 operated in addressable SPI mode, meaning they share a common chip select ($\overline{CS}$) signal from the SPI controller (MCU or FPGA).

The addressable SPI mode can accommodate up to four devices sharing a common $\overline{CS}$ signal. When more than four devices are required in a module, daisy-chain configuration can be used. In daisy-chain mode, the number of SPI clock cycles per read or write command is N x 16 with CRC disabled, or N x 24 with CRC enabled, where N is the number of devices in the daisy chain, creating a longer SPI read/write delay.

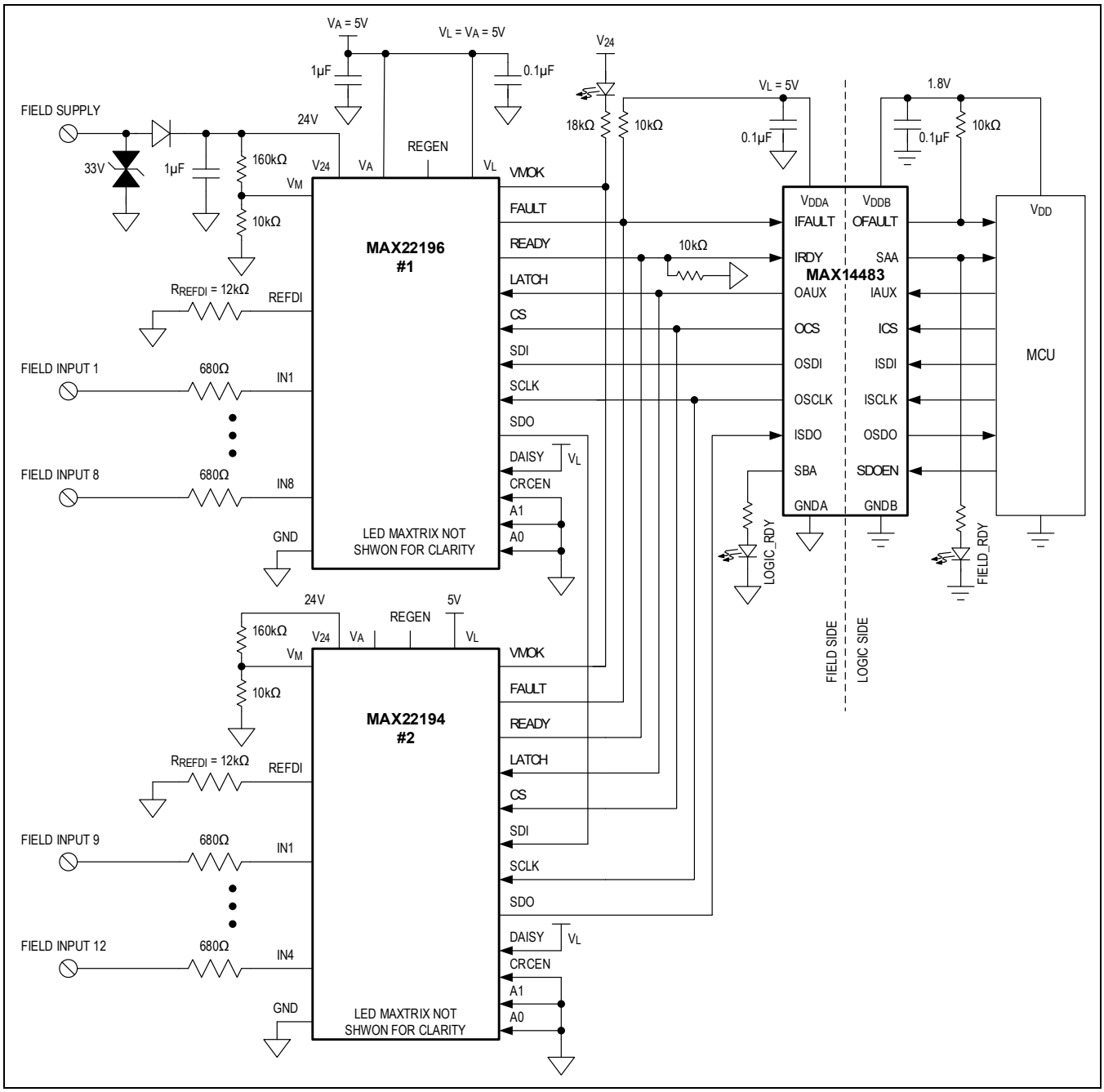



*Figure 18. 12-Channel Digital Input with Isolated SPI Daisy-Chain Mode*

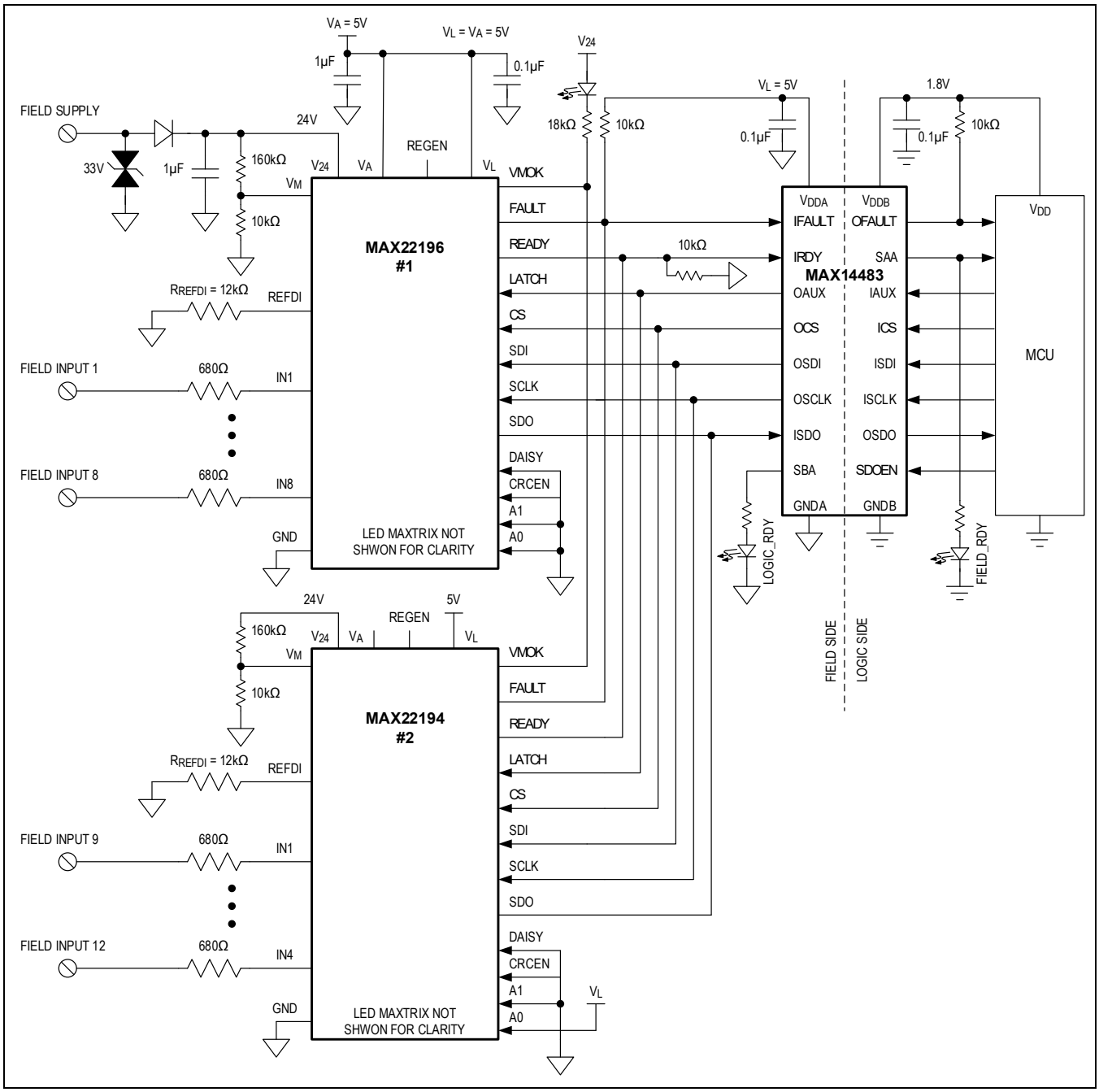



*Figure 19. 12-Channel Digital Input with Isolated Addressable SPI Mode*

## LED Matrix Power Dissipation

Heating due to high power dissipation is one of the main challenges in digital input modules. Assuming 2mA average current to light an LED and the LEDs on one row of the matrix are on simultaneously, the power dissipation of the LED matrix, including the LEDs, series resistors and internal switches, can be estimated as 5V x 3 x 2mA = 30mW. When $V_A$ is powered by the internal LDO (REGEN unconnected), the power dissipation due to the LDO loss with a maximum 30V field supply is (30V – 5V) x 3 x 2mA = 150mW. In such applications, it is recommended to power the $V_A$ supply externally (REGEN connected to GND) using an onboard step-down DC-DC converter. Assuming the DC-DC converter output is 3.3V with 90% efficiency, the power dissipation of the LED matrix can be reduced to 3.3V x 3 x 2mA = 19.8mW. The DC-

DC converter loss is only 2.2mW. *Figure 20* illustrates the 12-channel digital input module with $V_A$ powered by the onboard DC-DC converter.

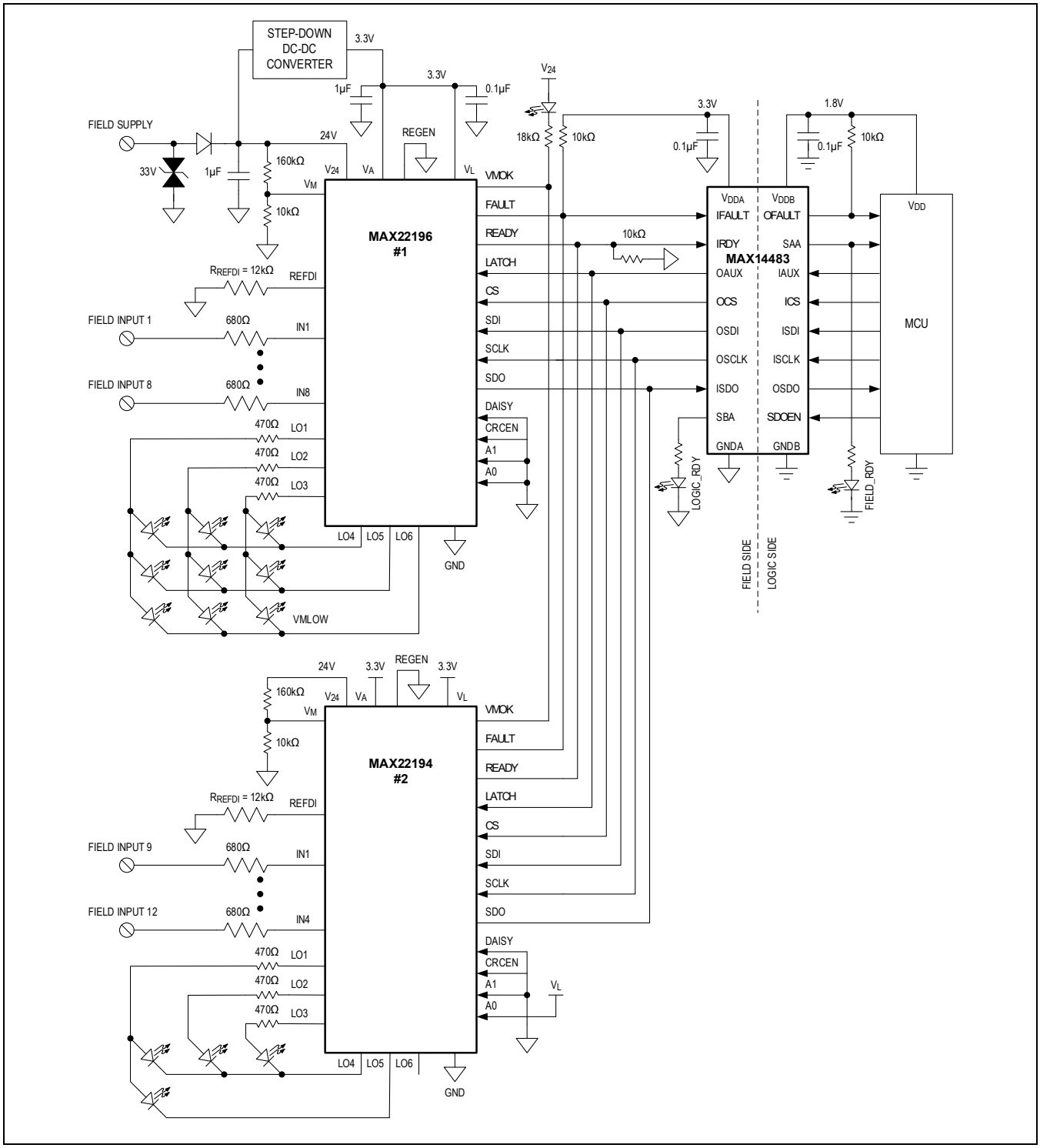



*Figure 20. 12-Channel Digital Input Module with $V_A$ and $V_L$ Powered by External DC-DC Converter*

## IEC 61131-2 EMC Requirements

The MAX22194 is required to operate reliably in harsh industrial environments. The device can meet the transient immunity requirements as specified in IEC 61131-2, including Electrostatic Discharge (ESD) per IEC 61000-4-2, Electrical Fast Transient/Burst (EFT) per IEC 61000-4-4, and Surge Immunity per IEC 61000-4-5. Analog Devices, Inc.'s proprietary process technology provides robust input channels and field supply with internal ESD structures and high 'Absolute Maximum Ratings' (see the *Absolute Maximum Ratings* section), but external components are also required to absorb excessive energy from ESD and surge transients. The circuit with external components shown in *Figure 21* allows the device to meet and exceed the transient immunity requirements as specified in IEC 61131-2 and related IEC 61000-4-x standards. The system shown in *Figure 21*, using the components shown in *Table 7*, is designed to be robust against ESD, EFT, and surge specifications, as listed in *Table 8*. In all these tests, the part or DUT is soldered onto a properly designed application board with necessary external components.

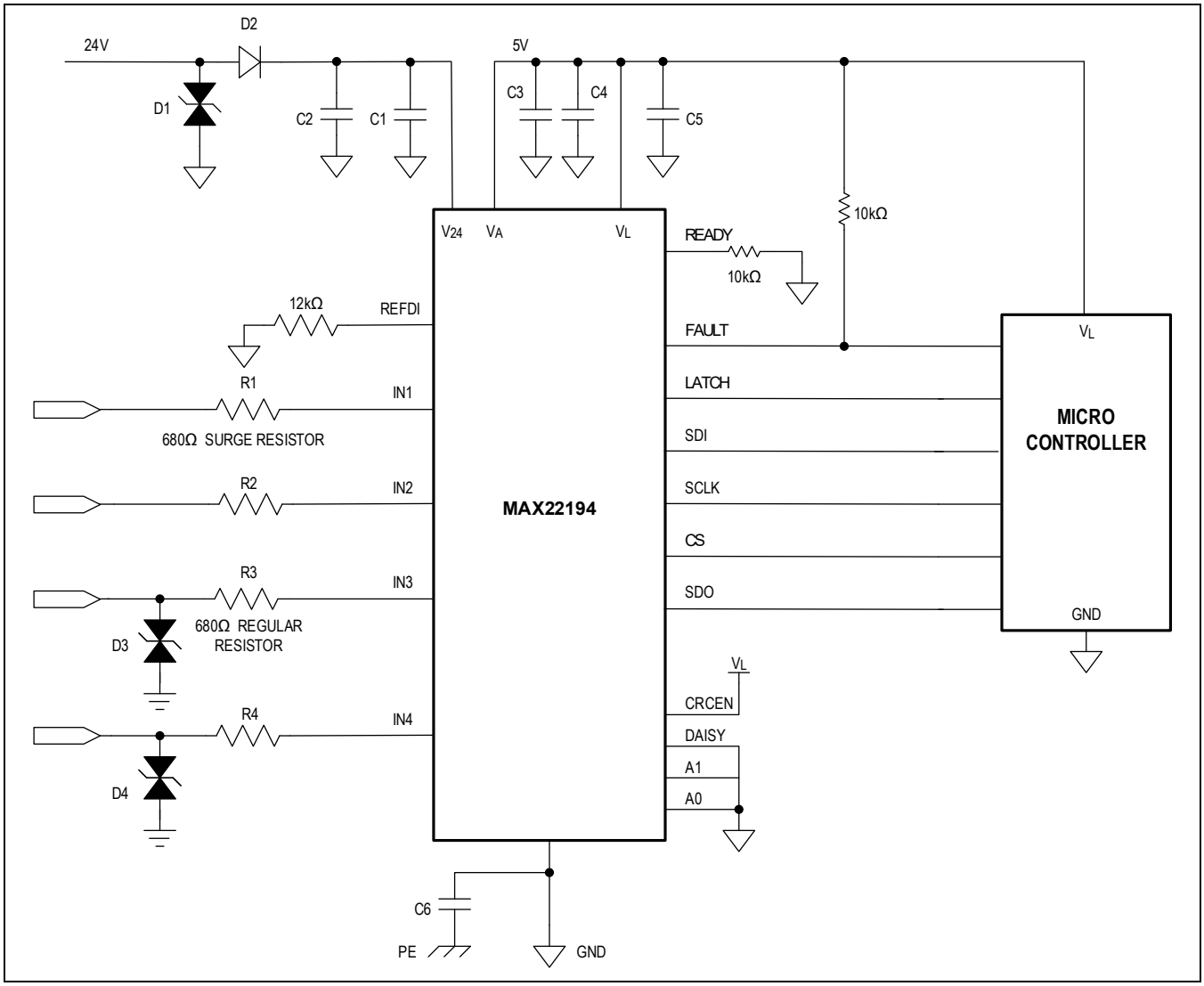



*Figure 21. Typical EMC Protection Circuitry for the MAX22194*

## Table 7. Recommended Components for EMC Protection

| COMPONENT | DESCRIPTION | REQUIRED / RECOMMENDED / OPTIONAL |
|---|---|---|
| C1 | 0.1µF, 100V low ESR ceramic capacitor | Recommended |
| C2 | 1µF, 100V low ESR ceramic capacitor | Required |
| C3 | 0.1µF, 16V low ESR ceramic capacitor | Recommended |
| C4 | 1µF, 16V low ESR ceramic capacitor | Required |
| C5 | 0.1µF, 16V low ESR ceramic capacitor | Required |
| C6 | 3300pF, 2220 safety rated Y capacitor | Recommended |
| R1, R2 | 680Ω, 2512, 1.5W pulse withstanding resistor (CMB0207, RPC2512, CRCW2512-IF or similar) | Required |
| R3, R4 | 680Ω, 0603, 0.1W resistor | Required |
| D1 | Bidirectional TVS diode, SMAJ33CA (42Ω) or SM30T39CAY (2Ω) | Required |
| D2 | Diode for reverse current protection | Required |
| D3, D4 | Bidirectional TVS diode, SMAJ33CA (42Ω) | Required |
| All other resistors | 0603 0.1W resistors | Required |
| All LEDs (not shown in *Figure 21*) | LED for visual input status indication | Recommended |

## Table 8. Transient Immunity Test Results

| TEST | | RESULT |
|---|---|---|
| IEC 61000-4-2 Electrostatic Discharge (ESD) | Contact ESD | ±8kV |
| | Air-Gap ESD | ±15kV |
| IEC 61000-4-4 Electrical Fast Transient (EFT) | Input Line | ±4kV |
| IEC 61000-4-5 Surge Immunity (1.2/50µs, 42Ω) | Line-to-Ground | ±1kV |
| | Line-to-Line | ±1kV |
| | Power Supply | ±500V |

### ESD Protection of Field Inputs

The input resistor limits the energy into the MAX22194 IN_ pins and protects the internal ESD structure from excessive transient energy. An input series resistor is required and should be rated to withstand such ESD levels. The MAX22194 input channels can withstand up to ±8kV ESD contact discharge and ±15kV ESD air-gap discharge with an input series resistor of 680Ω or larger. The input resistor value shifts the field voltage switching threshold scaled by the input current; thus, it determines the input characteristics of the application. The package of the resistor should be large enough to prevent the arcing across the two resistor pads. Arcing depends on the ESD level applied to the field input and the application's pollution degree.

### EFT Protection of Field Inputs

The input channels can withstand up to ±4kV, 5kHz, or 100kHz fast transients (*Figure 22*) with performance criterion A, normal operation within specification limits. A capacitive coupling clamp is used to couple the fast transients (burst) from the EFT generator to the field inputs of the MAX22194 without any galvanic connection to the MAX22194 input pins.

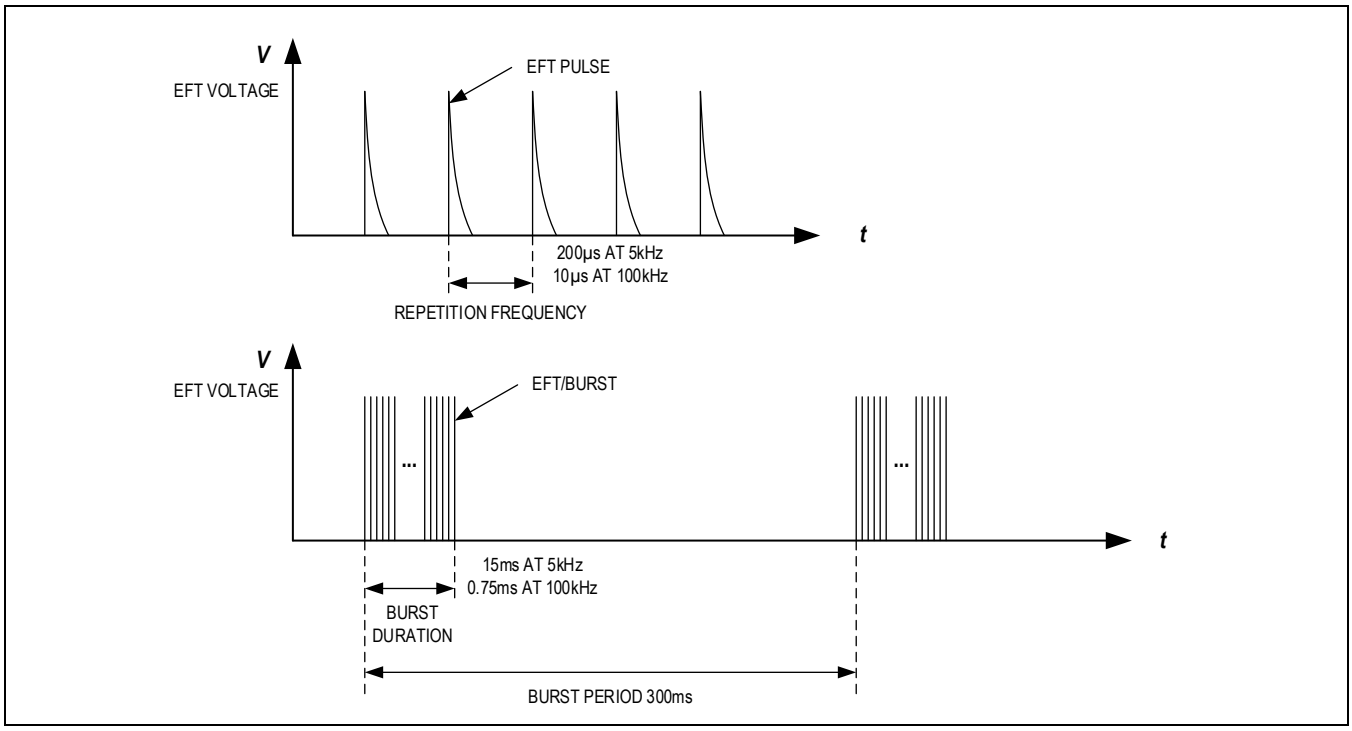



*Figure 22. Electrical Fast Transient/Burst Waveform*

### Surge Protection of Field Inputs

To protect the IN_ pins against IEC 61000-4-5 surges (*Figure 23* and *Figure 24*), two options exist. The first option is to use a series pulse withstanding resistor, as illustrated on IN1 and IN2 in *Figure 21*. A pulse resistor greater or equal to 680Ω should be used to withstand ±1kV/42Ω, 1.2/50µs surge pulses. The pulse resistor should support dissipation of the surge energy. Examples of suitable resistors are CMB0207 MELF, RPC2512, or CRCW2512-IF thick film as well as others. The required resistor value is defined by the Type 1, 2, 3, or other input characteristics. Capacitors for filtering should not be connected to the IN_ pins. Higher levels of surge tolerance can be achieved using higher series resistor values on IN_ inputs: doubling the resistor value doubles the surge tolerance. However, higher resistor values increase the field threshold voltages, scaled by $I_{IN}$ x $R_{IN}$. Ensure that the threshold voltages meet the IEC 61131-2 limits.

The second option, which can result in a smaller overall footprint, is to use a bidirectional TVS to GND at the field input with a low-power series resistor, as shown on IN3 and IN4 in *Figure 21*. The TVS must be able to absorb the surge energy and has the function of limiting the peak voltage so that the resistor only sees a low differential voltage during the surge transient. Suitable TVS include SMAJ33CA, SPT02-236, or PDFN3-32, which has a smaller footprint, offering protection against ±1kV/42Ω surges.

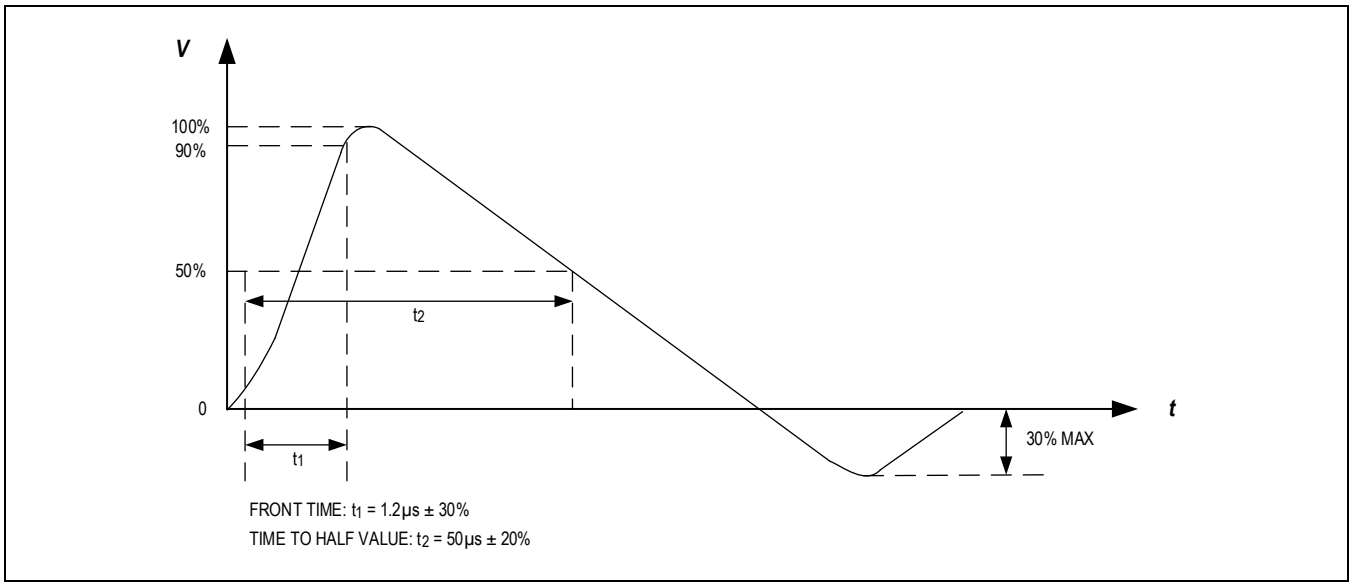



*Figure 23. IEC 61000-4-5 1.2/50µs Surge Voltage Waveform*

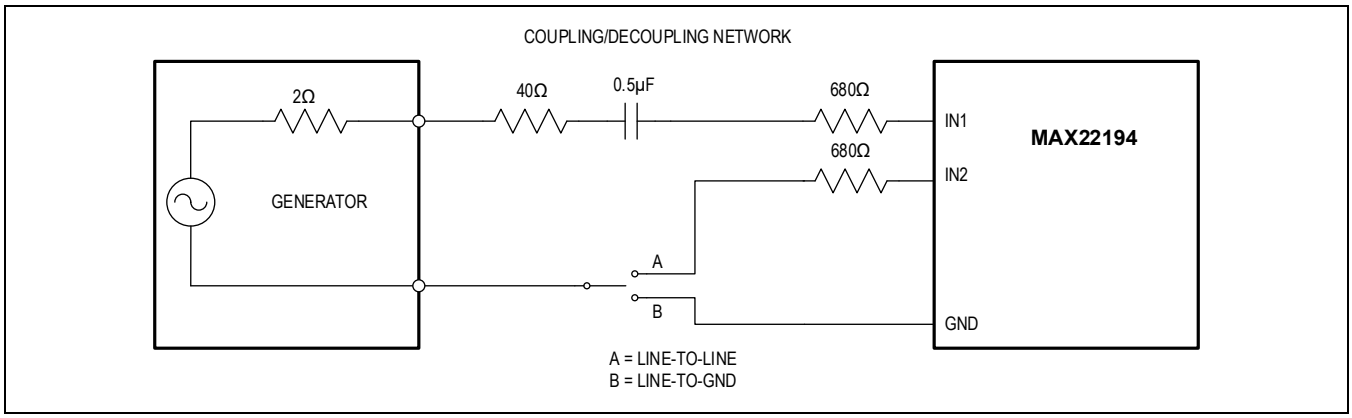



*Figure 24. IEC 61000-4-5 Surge Testing Method*

### Surge Protection of the 24V Field Supply

In order to protect the $V_{24}$ pin against ±500V/42Ω, 1.2µs/50µs surges (*Figure 23*), an SMAJ33CA TVS can be applied to the $V_{24}$ pin, along with a series diode for reverse current protection. To protect against ±500V/2Ω, 1.2µs/50µs surges, an SM30T39CAY TVS can be applied to the $V_{24}$ pins.

## Typical Application Circuits

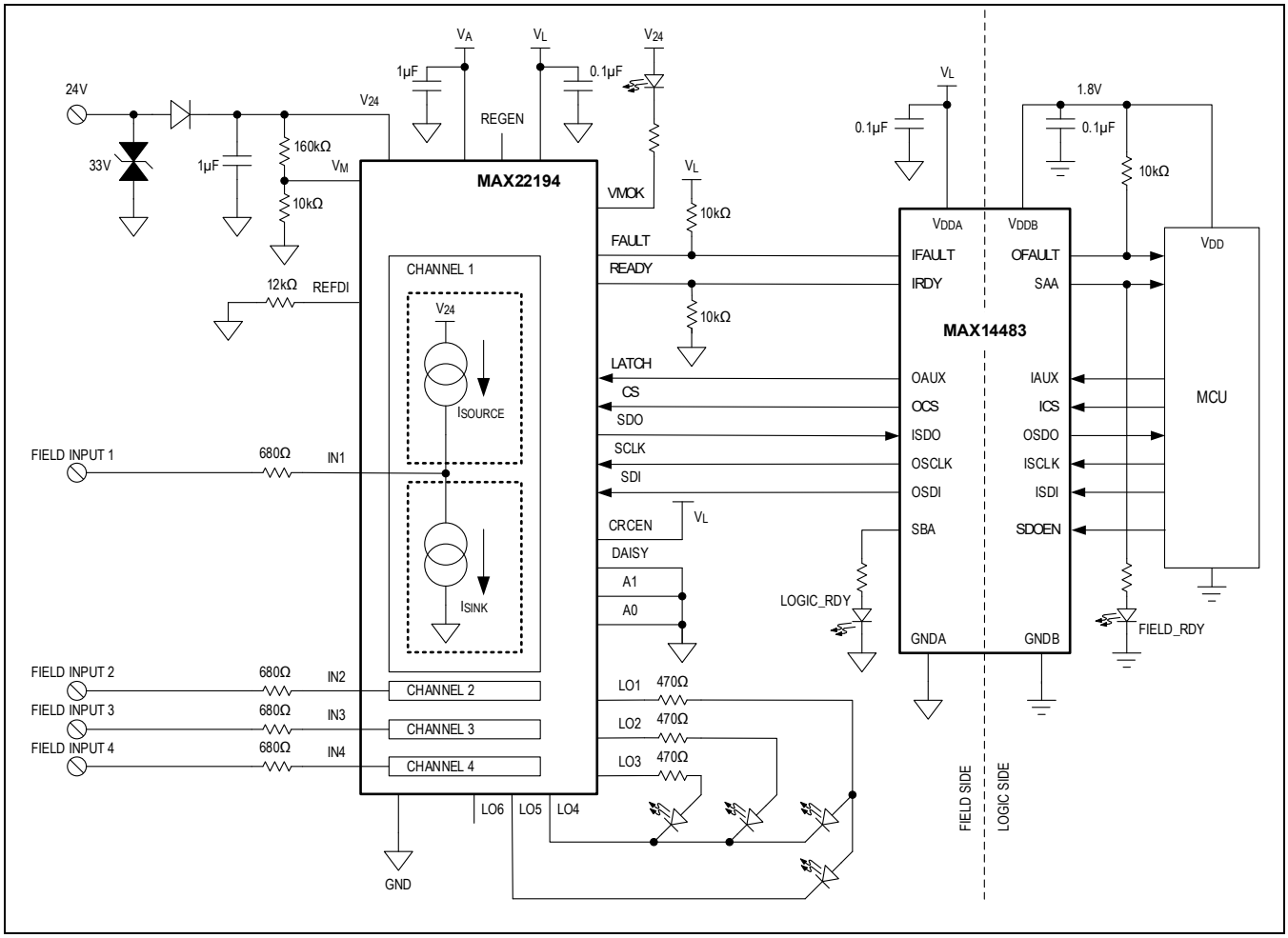



*Figure 25. Quad-Channel Isolated Sink or Source Digital Input Module*

## Ordering Information

| PART NUMBER | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX22194ATJ+ | -40°C to 125°C | 32-TQFN |
| MAX22194ATJ+T | -40°C to 125°C | 32-TQFN |

*+Denotes lead(Pb)-free/RoHS-compliant package.*

*T = Tape and Reel.*

## Chip Information

PROCESS: BiCMOS

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 03/24 | Release for market intro | — |