*Click **here** to ask an associate for production status of specific part numbers.*

MAX22212

36V, 7.6A High Current Single H-Bridge with Integrated Current Sense

General Description

The MAX22212 integrates a high current 36V, $7.6A_{MAX}$ H-Bridge to drive one Brushed DC motor or one half of a stepper motor. The H-Bridge FETs feature very low impedance, resulting in high driving efficiency and low heat generation. The typical total R_{ON} (high-side + low-side) is 0.125Ω. The H-Bridge can be PWM controlled by using three logic inputs (DIN1, DIN2, and EN).

The MAX22212 features an accurate current drive regulation (CDR), which can be used to limit the start up current of a brushed DC motor or to control the phase current for stepper operation. The bridge output current is sensed by a non-dissipative integrated current sensing (ICS) and it is then compared with a user configurable setpoint (I_{TRIP}). When the bridge current exceeds the setpoint, the device enforces the decay for a fixed OFF-time (t_{OFF}). Four different decay methods are supported (Slow Decay, Fast Decay, and two Mixed Decay modes). The non-dissipative ICS eliminates the bulky external power resistors normally required for this function resulting in a dramatic space and power saving compared with mainstream applications based on the external sense resistor.

A current proportional to the internally-sensed motor current is output to the external pins (ISENA, ISENB). By connecting an external resistor from these pins to GND, a voltage proportional to the motor current is generated. The voltage across this resistor can be used as inputs to ADCs of an external motor controller if motion control algorithm requires the current/torque information.

In addition, one open-drain output (CDR pin) is asserted every time the internal current regulation takes control of the driver so that the activity of the internal current loop can be monitored.

The maximum user configurable full-scale current (I_{FS_MAX}) can be set up to 7.6A limited by the overcurrent protection (OCP). An external resistor connected from REF to GND sets the full-scale current (I_{FS}) threshold. An integrated sinusoidal 4-bit DAC allows the user to dynamically modify the current regulation set-point (I_{TRIP}) from zero to IFS. Because of thermal considerations, the recommended maximum RMS current on a standard 4-layers PCB is $4A_{RMS}$.

In applications in which the requirement of maximum full-scale current is less than 3.8A and high current control accuracy is desired, the half full scale (HFS) logic input pin can be set high to halve the current rating and double the low-side FET R_{ON}. This results in better current control loop accuracy in the bottom end of the current range.

The MAX22212 features overcurrent protection (OCP), thermal shutdown (TSD), and undervoltage lockout (UVLO) protection. An open-drain active low $\overline{FAULT}$ pin is activated every time a fault condition is detected. During thermal shutdown and undervoltage lockout events, the driver is disabled until normal operations are restored.

The MAX22212 is available into a small TQFN32 5mm x 5mm package or in a TSSOP28 4.4mm x 9.7mm package.

Applications

- Stepper-Motor Driver
- Brushed DC Motor Driver
- Solenoid Driver
- Latched Valves

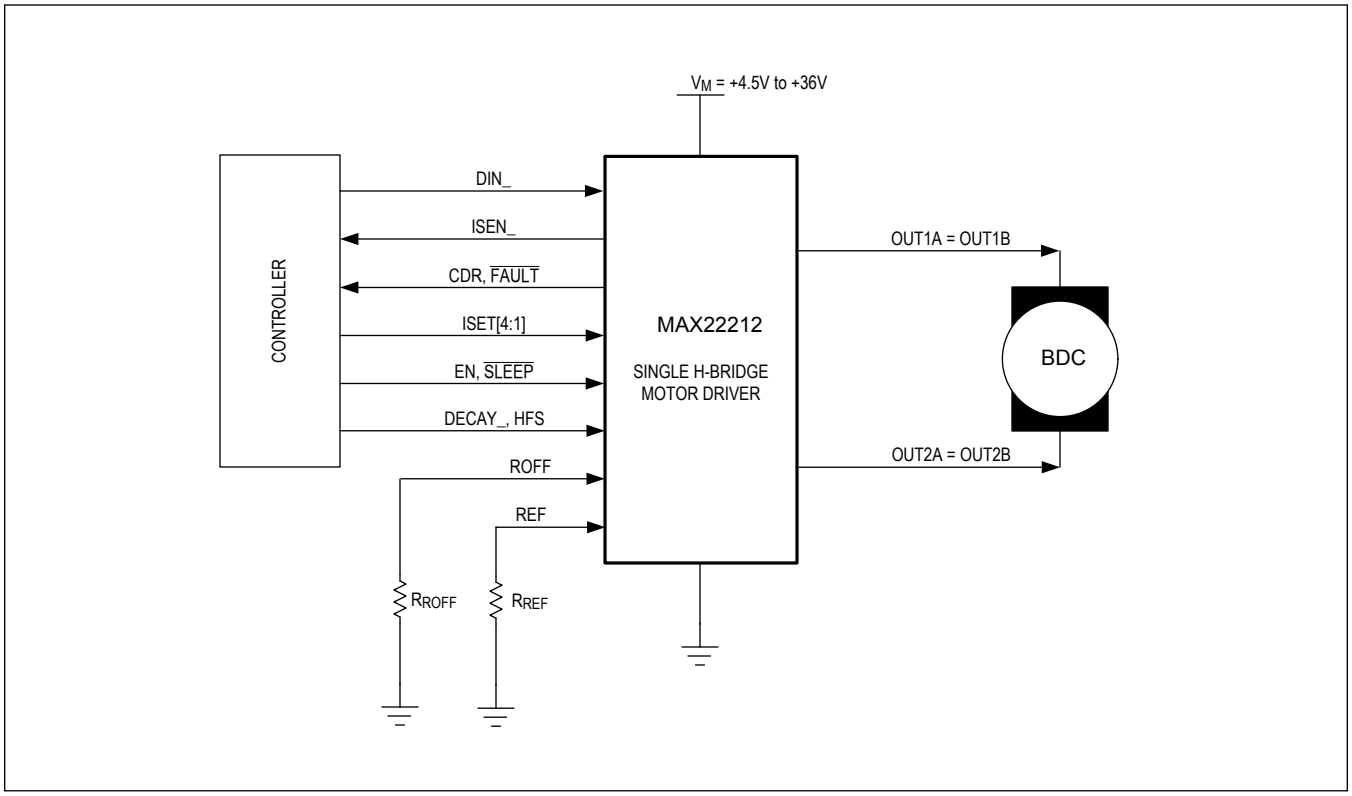
Benefits and Features

- One H-Bridge with +36V Voltage Rating
  - Total $R_{DS(ON)}$ (High-Side + Low-Side): 125mΩ Typical (T_A = 25°C)
- Current Ratings per H-Bridge (Typical at T_A = 25°C):
  - I_{FS_MAX} = 7.6A (Max Full-Scale Current Setting for Internal Current Drive Regulation)
  - I_{RMS} = $4A_{RMS}$ Recommended Maximum RMS Current
- Integrated Current Control
  - Full-Scale DAC Current Programmable with External Resistor
  - Internal Current Sensing (ICS) Eliminates External Bulky Resistors and Improves Efficiency
  - Current Drive Regulation Monitor Output Pin (CDR Pin).
  - Integrated DAC Sets the Output Current from 16 Levels
  - Four Decay Modes Supported (Slow, Fast, and Two Mixed Modes)
  - Fixed OFF Time Configurable with External Resistor
- Current Sense Output (Current Monitor)
- Fault Indicator Pin ($\overline{FAULT}$)
- Low Power Mode (Sleep Mode)
- Protections
  - Overcurrent Protection for each Channel (OCP)
  - Undervoltage Lockout (UVLO)
  - Thermal Shutdown T_J = 165°C (TSD)
- TQFN32 5mm x 5mm Package or in a TSSOP28 4.4mm x 9.7mm Package

***Ordering Information** appears at end of data sheet.*

19-101538; Rev 1; 1/24

Simplified Block Diagram



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Absolute Maximum Ratings

V_M to GND ..... -0.3V to +42V
V_{DD} to GND..... -0.3V to min (+2.2V, V_M + 0.3V)
PGND to GND ..... -0.3V to +0.3V
OUT_..... -0.3V to (V_M + 0.3)V
V_{CP} to GND..... (V_M - 0.3V) to min (+42V, V_M + 6V)
C_{P2} to GND ..... -0.3V to min (+42V, V_M + 0.3V)
C_{P1} to GND ..... (V_M - 0.3V) to min (+42V, V_M + 6V)
FAULT to GND ..... -0.3V to +6V
CDR to GND..... -0.3V to +6V
ISET_ to GND ..... -0.3V to +6V
REF to GND ..... -0.3V to min (+2.2V, V_{DD} + 0.3V)
ROFF to GND ..... -0.3V to min (+2.2V, V_{DD} + 0.3V)
ISEN_ to GND..... -0.3V to min (+2.2V, V_{DD} + 0.3V)
DIN_ to GND..... -0.3V to +6V
EN to GND ..... -0.3V to +6V
HFS to GND..... -0.3V to +6V
DECAY_ to GND..... -0.3V to +6V
SLEEP to GND ..... -0.3V to min (+42V, V_M + 0.3V)
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +160°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32-Pin TQFN—5mm x 5mm

Package Code	T3255-8C
Outline Number	**21-0140**
Land Pattern Number	**90-0013**
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	47°C/W
Junction to Case (θ_{JC})	1.7°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	1.7°C/W

28-Pin TSSOP—4.4mm x 9.7mm

Package Code	U28E+5C
Outline Number	**21-0108**
Land Pattern Number	**90-0147**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	24.65°C/W
Junction to Case (θ_{JC})	1.52°C/W

For the latest package outline information and land patterns (footprints), go to ***https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html***.

Electrical Characteristics

(V_M = +4.5V to +36V, R_{ROFF} = from 15kΩ to 120kΩ , R_{REF} = from 12kΩ to 72kΩ , typical values are T_A = +25°C and V_M = +24V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Note 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply-Voltage Range	V_M		4.5		36	V
Sleep-Mode Current Consumption	I_{VM}	$\overline{SLEEP}$ = logic low		4	11	µA
Quiescent Current Consumption	I_{VM}	$\overline{SLEEP}$ = logic high		2	4	mA
1.8V Regulator Output Voltage	V_{VDD}	V_M = +4.5V, I_{LOAD} = internal consumption	1.74	1.8	1.86	V
V_{DD} Current Limit	$I_{V18(LIM)}$		20			mA
V_{DD} UVLO Rising	$UVLOV18_R$	V_{DD} rising	1.59	1.65	1.69	V
V_{DD} UVLO Falling	$UVLOV18_F$	V_{DD} falling	1.535	1.58	1.635	V
Charge-Pump Voltage	V_{CP}			V_M + 2.7		V
LOGIC LEVEL INPUTS/OUTPUTS						
Input Voltage Level—High	V_{IH}		1.2			V
Input Voltage Level—Low	V_{IL}				0.65	V
Input Hysteresis	V_{HYS}			110		mV
Pull-Down Current	I_{PD}	To GND	16	34	50	µA
Open-Drain Output Logic-Low Voltage	V_{OL}	I_{LOAD} = 5mA			0.2	V
Open-Drain Output Logic-High Leakage Current	I_{OH}	V_{PIN} = 3.3V	-1		+1	µA
$\overline{SLEEP}$ Voltage Level High	$V_{IH(\overline{SLEEP})}$		0.9			V
$\overline{SLEEP}$ Voltage Level Low	$V_{IL(\overline{SLEEP})}$				0.6	V
$\overline{SLEEP}$ Pull-Down Input Resistance	$R_{PD(\overline{SLEEP})}$		0.8	1.5		MΩ
OUTPUT SPECIFICATIONS						
Output ON-Resistance Low-Side	$R_{ON(LS)}$	HFS = logic low, OUT1A = OUT1B, OUT2A = OUT2B		0.0625	0.11	Ω
		HFS = logic high, OUT1A = OUT1B, OUT2A = OUT2B		0.11	0.21	
Output On-Resistance High-Side	$R_{ON(HS)}$	OUT1A = OUT1B, OUT2A = OUT2B		0.0625	0.11	Ω
Output Leakage	I_{LEAK}	Driver OFF	-10		10	µA
Dead Time	t_{DEAD}			100		ns
Output Slew Rate	SR			200		V/µs

Electrical Characteristics (continued)

(V_M = +4.5V to +36V, R_{ROFF} = from 15kΩ to 120kΩ , R_{REF} = from 12kΩ to 72kΩ , typical values are T_A = +25°C and V_M = +24V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Note 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PROTECTION CIRCUITS						
Overcurrent Protection Threshold	OCP		7.6			A
Overcurrent Protection Blanking Time	t_{OCP}		1	2.2	3.2	µs
Autoretry OCP Time	t_{RETRY}			3		ms
UVLO Threshold on V_M	V_{UVLO}	V_M rising	3.85	4	4.15	V
UVLO Threshold on V_M Hysteresis	$UVLO_{HYS}$			0.12		V
Thermal Protection Threshold Temperature	TSD			+165		°C
Thermal Protection Temperature Hysteresis	TSD_{HYS}			20		°C
CURRENT REGULATION						
REF Output Voltage	V_{REF}		0.882	0.9	0.918	V
I_{TRIP} Current Regulation Constant	K_{IFS}	HFS = logic low		72		KV
		HFS = logic high		36.8		kV
Current Trip Regulation Accuracy	DITRIP1	HFS = logic low, I_{OUT} = 2.2A to 6A	-5		5	%
		HFS = logic high, I_{OUT} = 1.1A to 3A	-5		5	
	DITRIP2	HFS = logic low, I_{OUT} = 1A to 2.2A	-10		10	
		HFS = logic high, I_{OUT} = 0.5A to 1.1A	-10		10	
Fixed OFF – Time Internal	t_{OFF}	ROFF shorted to V_{DD}	16	20	24	µs
Fixed OFF – Time Constant	K_{TOFF}	R_{ROFF} from 15kΩ to 120kΩ		0.667		µs/kΩ
PWM Blanking Time	t_{BLK}		1.4	2.8	4	µs
CURRENT-SENSE MONITOR						
ISEN_ Voltage Range	ISEN	Voltage range at ISEN_ pins	0		1.1	V
Current-Monitor Scaling Factor	K_{ISEN}	HFS = logic low. See the I_{SEN} output-current equation in the Current Sense Output (ISEN) - Current monitor section.		7500		A/A
		HFS = logic high. See the I_{SEN} output-current equation in the Current Sense Output (ISEN) - Current monitor section.		3840		
Current Monitor Accuracy	$DKISEN_1$	HFS = logic low, I_{OUT} = 1.4A to 6A	-5		+5	%
		HFS = logic high, I_{OUT} = 0.7A to 3A	-5		+5	
	$DKISEN_2$	HFS = logic low, I_{OUT} = 0.8A to 1.4A	-10		+10	
		HFS = logic high, I_{OUT} = 0.4A to 0.7A	-10		+10	
Current-Sense Output -3dB Small-Signal Bandwidth	BW			400		KHz

Electrical Characteristics (continued)

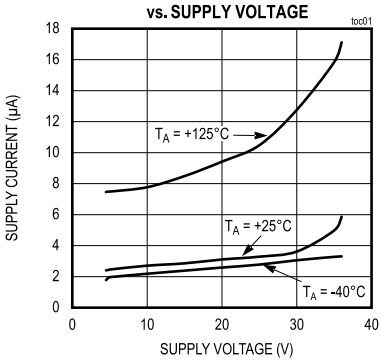
(V_M = +4.5V to +36V, R_{ROFF} = from 15kΩ to 120kΩ , R_{REF} = from 12kΩ to 72kΩ , typical values are T_A = +25°C and V_M = +24V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Note 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FUNCTIONAL TIMING						
Sleep Time	t_{SLEEP}	$\overline{SLEEP}$ = logic 1 to logic 0 for OUT_ to become three-state			150	µs
Wake-Up Time from Sleep	t_{WAKE}	$\overline{SLEEP}$ = logic 0 to logic 1 to resume normal operation			3	ms
Enable Time	t_{EN}	Time from EN_ pin rising edge to driver on			0.4	µs
Disable Time	t_{DIS}	Time from EN_ pin falling edge to driver off			0.6	µs

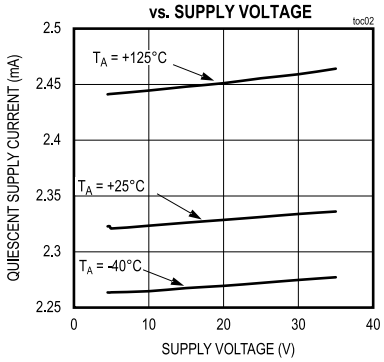
Typical Operating Characteristics

(V_M = +4.5V to +36V; T_A = 25°C unless otherwise noted.)

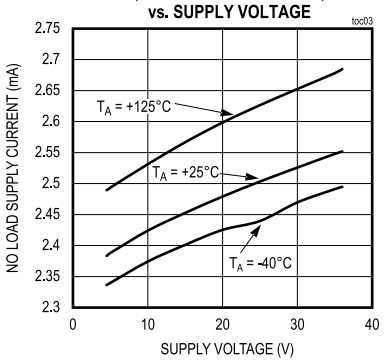
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



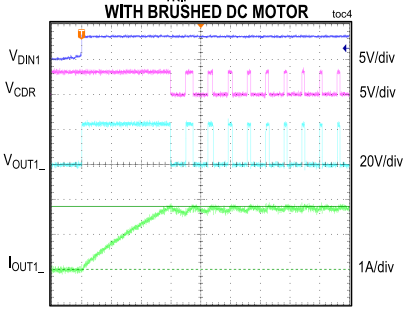
QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



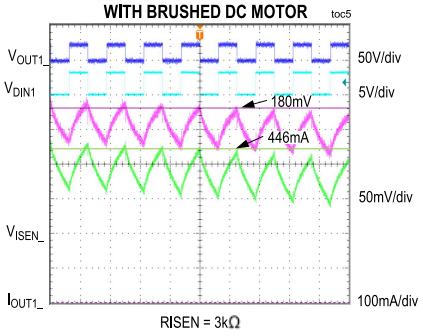
NO LOAD SWITCHING SUPPLY CURRENT (20kHz, 50% DUTY CYCLE) vs. SUPPLY VOLTAGE



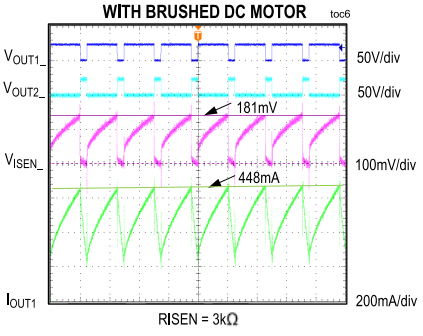
INRUSH CURRENT LIMIT 1.8A I_{TRIP} THRESHOLD WITH BRUSHED DC MOTOR



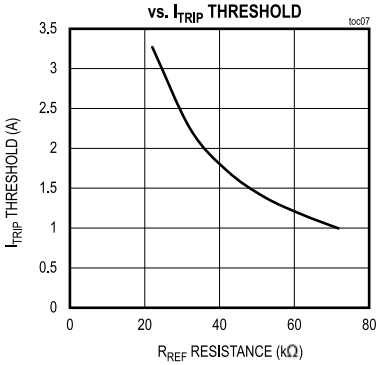
LOAD CURRENT AND ISEN VOLTAGE AT 20kHz SLOW DECAY PWM INPUT WITH BRUSHED DC MOTOR



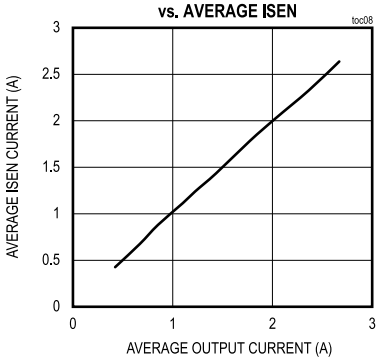
LOAD CURRENT AND ISEN VOLTAGE AT 20kHz FAST DECAY PWM INPUT WITH BRUSHED DC MOTOR



R_{REF} RESISTANCE vs. I_{TRIP} THRESHOLD

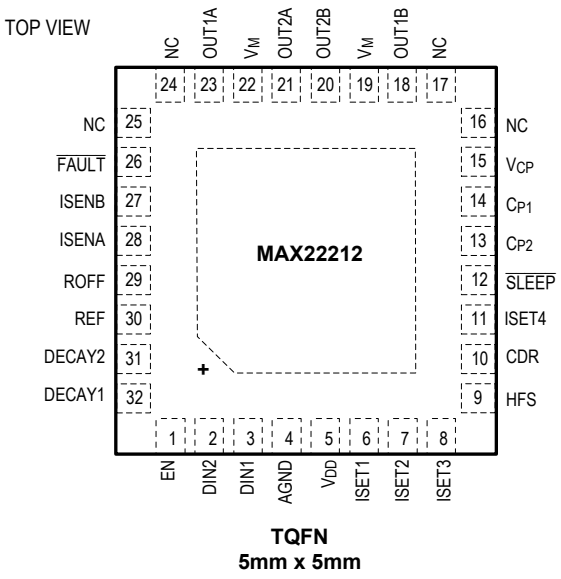


AVERAGE OUTPUT CURRENT vs. AVERAGE ISEN



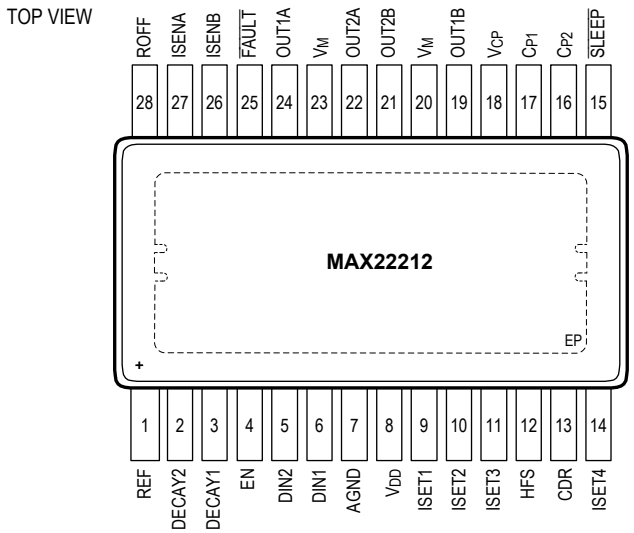
Pin Configurations

TQFN Pin Configuration



TQFN
5mm x 5mm

TSSOP Pin Configuration



TSSOP 28
4.4mm x 9.7mm

Pin Description

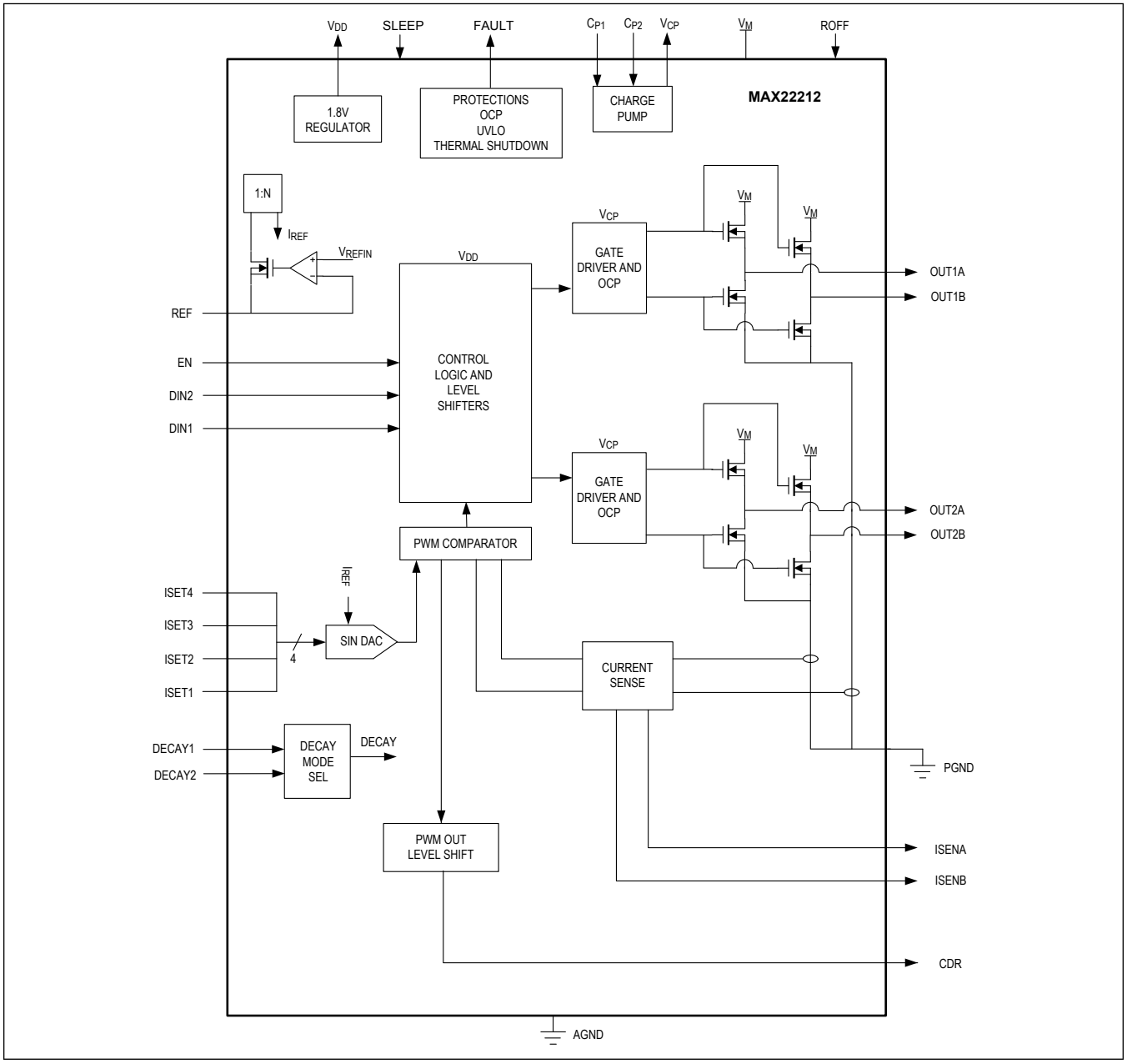
PIN		NAME	FUNCTION	TYPE
TQFN	TSSOP			
30	1	REF	Programmable Current Analog Input. Connect a resistor from REF to GND to set the full scale current.	Analog Input
29	28	ROFF	OFF Time (t_{OFF}) Programmable Resistor Pin. Connect ROFF to V_{DD} to use the internal fixed t_{OFF} time. Connect a resistor from ROFF to GND to set the fixed OFF time to a desired value.	Analog Input
26	25	$\overline{FAULT}$	Active-Low, Open-Drain, Output Fault Indicator. $\overline{FAULT}$ goes low to indicate that one or more of the protection mechanisms has been activated. Connect a pull-up resistor from $\overline{FAULT}$ to the microcontroller supply voltage.	Open Drain Output
10	13	CDR	Open-Drain Output. Current Drive Regulator monitor output	Open Drain Output
4	7	AGND	Analog Ground. Connect to ground plane.	GND
19, 22	20, 23	V_M	Supply Voltage Input. Connect a V_M-rated 1µF (minimum) surface-mounted device capacitor from V_M to GND close to the device, and a 10µF (minimum) electrolytic bypass capacitor from V_M to GND. Higher values can be considered depending on application requirements.	Supply

Pin Description (continued)

PIN		NAME	FUNCTION	TYPE
TQFN	TSSOP			
5	8	V_{DD}	1.8V Linear Regulator Output. Bypass V_{DD} with a 2.2µF capacitor connected close to the device.	Output
18, 23	19, 24	OUT1_	Driver Output Pin. OUT1A and OUT1B are not internally connected and must be externally connected.	Output
20, 21	21, 22	OUT2_	Driver Output Pin. OUT2A and OUT2B are not internally connected and must be externally connected.	Output
27, 28	26, 27	ISEN_	Current-Sense Output Monitor. ISENA and ISENB are not internally connected and must be connected externally.	Output
2, 3	5, 6	DIN_	CMOS PWM Input	Logic Input
1	4	EN	Logic Input Pin. Enable Pin.	Logic Input
15	18	V_{CP}	Charge-Pump Output. Connect a 1µF capacitor between V_{CP} and V_M as close as possible to the device.	Output
14	17	C_{P1}	Charge-Pump Flying Capacitor Pin 1. Connect a 22nF capacitor between CP1 and CP2, as close as possible to the device.	Output
13	16	C_{P2}	Charge-Pump Flying Capacitor Pin 2. Connect a 22nF capacitor between CP1 and CP2, as close as possible to the device.	Output
12	15	$\overline{SLEEP}$	Active-Low Sleep Pin	Logic Input
31, 32	2, 3	DECAY_	Logic Input. Set the Decay Mode.	Logic Input
9	12	HFS	Set Output Current Full Scale. HFS = 0 coefficient is 100%. HFS = 1 coefficient is 50%.	Logic Input
6, 7, 8, 11	9, 10, 11, 14	ISET_	Programmable Current Logic Input.	Logic Input
16, 17, 24, 25	—	NC	No Connection. Not internally connected.	
EP	EP	PGND	Power GND. Connect to ground plane. The thermal exposed pad (EP) is also the electrical power GND pin and must be properly connected to GND.	GND

Functional Diagrams

Diagram



Detailed Description

The MAX22212 integrates an high current 36V, 7.6A_{MAX} H-Bridge. It can be used to drive one Brushed DC motor or one half of a stepper motor. The H-Bridge FETs feature very low impedance, resulting in high driving efficiency and low heat generation. The typical total R_{ON} (high-side + low-side) is 0.125Ω. The H-Bridge can be individually PWM controlled by using three logic inputs (DIN1, DIN2, and EN).

The MAX22212 features an accurate current drive regulation (CDR), which can be used to limit the start-up current of a Brushed DC motor or to control the phase current for stepper operation. The bridge output current is sensed by a non-dissipative Integrated Current Sensing (ICS) and it is then compared with a user configurable setpoint (I_{TRIP}). When the bridge current exceeds the setpoint, the device enforces the decay for a fixed OFF-time (t_{OFF}). Four different decay methods are supported (Slow Decay, Fast Decay, two Mixed Decay modes). The non-dissipative Integrated Current Sensing eliminates the bulky external power resistors, which are normally required for this function, resulting in dramatic space and power savings compared with mainstream applications using an external sense resistor.

A current proportional to the internally-sensed motor current is output to external pins (ISENA, ISENB). By connecting an external resistor from these pins to GND, a voltage proportional to the motor current is generated. The voltage across this resistor can be used as inputs to ADCs of an external motor controller if the motion control algorithm requires the current/torque information.

In addition, one open-drain output (CDR pin) is asserted every time the internal current regulation takes control of the driver so that the activity of the internal current loop can be monitored.

The maximum user configurable full-scale current (I_{FS_MAX}) can be set up to 7.6A limited by the overcurrent protection. An external resistor connected from REF to GND sets the full-scale current (I_{FS}) threshold. An integrated sinusoidal 4-bit DAC allows the user to dynamically modify the current regulation set-point (I_{TRIP}) from zero to IFS. Because of thermal considerations, the recommended maximum RMS current on a standard 4-layer PCB is 4A_{RMS}.

In applications in which the requirement of maximum full-scale current is less than 3.8A and high current control accuracy is desired, the half-full-scale (HFS) logic input pin can be set high to halve the current rating and double the low-side FET R_{ON}. This results in better current control loop accuracy in the bottom end of the current range.

The MAX22212 features over current protection (OCP), thermal shutdown (TSD), and undervoltage lockout (UVLO) protection. An open-drain active low $\overline{FAULT}$ pin is activated every time a fault condition is detected. During thermal shutdown and undervoltage lockout events, the driver is disabled until normal operations are restored.

The MAX22212 is available into a small TQFN32 5mm x 5mm package or in a TSSOP28 4.4mm x 9.7mm package.

Sleep Mode ($\overline{SLEEP}$ Pin)

The $\overline{SLEEP}$ pin can be driven low to place the device into the lowest power-consumption mode possible, with all outputs three-stated, the internal circuits biased off, and the charge pump disabled. A pull-down resistor should be connected between $\overline{SLEEP}$ and GND to ensure the part is disabled whenever this pin is not actively driven. Driving the $\overline{SLEEP}$ pin high wakes up the device and returns it to normal mode. t_{WAKE} is 3ms (max).

PWM Control

When the bridge current is below the programmed threshold (i.e., $I_{BRIDGE} < I_{TRIP}$), the H-Bridge is controlled by three logic inputs (DIN1, DIN2, and EN).

Table 1 shows the control Truth Table.

Table 1. MAX22212 Truth Table

EN	DIN1	DIN2	OUT1	OUT2	DESCRIPTION
0	X	X	High-Z	High-Z	H-Bridge disabled. High impedance (HiZ)
1	0	0	L	L	Brake Low; Slow decay
1	1	0	H	L	Reverse (current from OUT1 to OUT2)
1	0	1	L	H	Forward (current from OUT2 to OUT1)
1	1	1	H	H	Brake High; Slow decay

PWM techniques can be used to vary the output duty cycle and hence to implement motor control.

Current-Sense Output (ISEN) - Current Monitor

Currents proportional to the internally-sensed motor currents are output to pins ISENA and ISENB. The current is sensed only when the low side FET is ON and sinks current. ISENA must be externally tied to ISENB to sum up the currents and monitor the full-bridge current. When used in this configuration, the ISEN = ISENA + ISENB current reflects the motor current during the Forward, Reverse, and Brake Low (Slow Decay) statuses while it is zeroed during Fast Decay or Coast Status.

The following equation shows the relationship between the current sourced at ISEN = ISENA + ISENB and the motor current.

$$I_{ISEN}(A) = \frac{I_{OUT}(A)}{K_{ISEN}}$$

Equation - ISEN Output Current

in which K_{ISEN} represents the current mirror factor between the output current and its replica at pin ISEN. K_{ISEN} is typically 7500 KA/A (when HFS = 0). For instance, if the instantaneous output current is 2A, the current sourced at ISEN is 266µA.

Figure 1 shows an idealized behavior of the ISEN = ISENA + ISENB current when Slow or Fast Decay are used. Blanking Times, delays, and rise/fall edges are ignored.

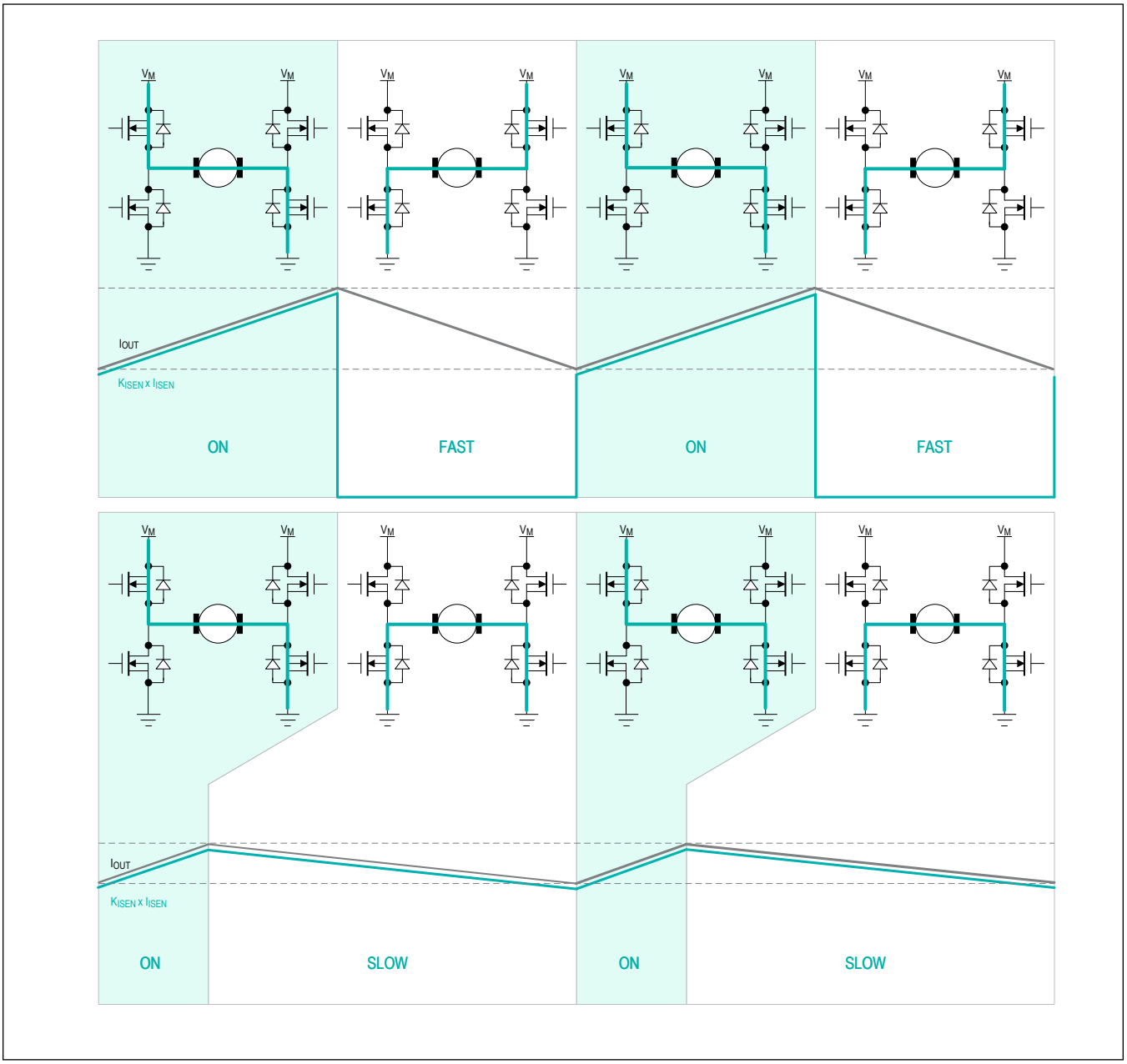


Figure 1. ISEN Current

By connecting an external signal resistor, R_{ISEN} , between ISENA = ISENB and GND, a voltage proportional to the motor current is generated. The voltage across the R_{ISEN} can be input into the ADC of an external controller in applications in which the motor control algorithm requires the current/torque information. The system designer can choose an R_{ISEN} value so that the peak voltage meets the ADC input full-scale requirement. The following equation shows the formula to calculate R_{ISEN} once the ADC full-scale voltage (V_{FS}) and the maximum operating current (I_{MAX}) are known.

$$R_{ISEN}(\Omega) = K_{ISEN} \times \frac{V_{FS}(V)}{I_{MAX}(A)}$$

Equation - R_{ISEN} Setting

The R_{ISEN} value also sets the output impedance of the Current-Sense Output circuit (ISEN_ output impedance). Normally, the input impedance of the ADC is much higher than R_{ISEN} enabling a direct connection to the ISEN pin without attenuation. If a low input impedance ADC was used, a preamplifier (buffer) would be required.

The Current-Sense Output circuit bandwidth and step response performances (see Specifications) ensure the current monitor tracks the driver current in PWM motor drive application.

Current Drive Regulation

The MAX22212 features embedded current drive regulation (CDR). The embedded CDR provides an accurate control of the current flowing into the motor windings. The bridge current is sensed by a non-dissipative Integrated Current Sensing (ICS) circuit and it is then compared with the threshold current (I_{TRIP}). As soon as the bridge current exceeds the threshold, the device enforces the decay for a fixed OFF-time (t_{OFF}). The device supports different decay modes as described in the following paragraphs. Once t_{OFF} has elapses, the driver is re-enabled for the next PWM cycle. During current regulation, the PWM duty cycle and frequency depend on the supply voltage, on the motor inductance, and on motor speed and load conditions. The t_{OFF} duration can be configured with an external resistor connected to the ROFF pin.

Setting the Full-Scale Current – IFS

Connect a resistor from REF to GND to set the full-scale chopping current I_{FS}.

The following equation shows the typical I_{FS} current as a function of the R_{REF} shunt resistor connected to pin REF. The proportionality constant K_{IFS} is typically 72KV if HFS = 0 and 36.8KV if HFS = 1. The external resistor recommended range is from 9.5KΩ to 100KΩ.

$$I_{FS} = \frac{K_{IFS(KV)}}{R_{REF(K\Omega)}}$$

When HFS logic input pin is driven logic low, the power FETs $R_{DS(ON)}$ is set to a minimum of 0.125Ω (high-side + low-side). When HFS logic input pin is set logic high, the power FETs have higher $R_{DS(ON)}$ of 0.18Ω (high-side + low-side). This operating mode is recommended for applications in which the maximum current does not exceed 3.8A and high accuracy at the bottom end of the current range is desirable. Table 2 summarizes the HFS settings.

Table 2. HFS Truth Table

HFS	MAXIMUM FS SETTING	TYPICAL $R_{DS(ON)}$ (HIGH-SIDE + LOW-SIDE)	NOTES
0	7.6A	0.125Ω	Optimized efficiency and extended operating range up to 7.6A_{FS}
1	3.8A	0.18Ω	Reduced operating range up to 3.8A_{FS}. Improved current accuracy control at the bottom end of the current range

Bridge Current Control

Four input pins, ISET[4:1], are used to program the output current. Table 3 shows the bridge current levels for each input combination.

Table 3. H-Bridge ISET Pins Truth Table

ISET4	ISET3	ISET2	ISET1	CURRENT (% OF IFS)
0	0	0	0	100
0	0	0	1	99.2
0	0	1	0	97.7
0	0	1	1	95.3

Table 3. H-Bridge ISET Pins Truth Table (continued)

0	1	0	0	91.4
0	1	0	1	86.7
0	1	1	0	81.3
0	1	1	1	74.2
1	0	0	0	67.2
1	0	0	1	58.6
1	0	1	0	50
1	0	1	1	40.6
1	1	0	0	31.3
1	1	0	1	21.1
1	1	1	0	10.2
1	1	1	1	0

Setting the Fixed OFF Time (t_{OFF})

The current regulation circuit is based on a constant t_{OFF} PWM control. If during the ON phase, the bridge current exceeds the target I_{TRIP} threshold, the OFF phase begins and the current decays. The OFF phase has a fixed time duration t_{OFF}.

The t_{OFF} can be configured to a desired value by connecting an external resistor to pin ROFF. When the ROFF pin is shorted to V_{DD}, the t_{OFF} time is internally set at a fixed value (20µs typical). By connecting an external resistor to the pin ROFF, the user can configure t_{OFF} as shown in the following equation in which R_{ROFF} is an external resistor (in kΩ) connected from the ROFF pin to GND and K_{TOFF} is an internal constant equal to 0.667µs/kΩ.

$$t_{OFF}(\mu s) = R_{ROFF} \times K_{TOFF}$$

The t_{OFF} can be programmed from a range of 10µs to 80µs.

CDR Open-Drain Output

This pin is an active-low open-drain output, which is asserted during the fixed decay time interval (t_{OFF}) enforced by the current drive regulation loop. This way, an external controller can monitor if the integrated current loop has taken control of the driver overwriting the status of the PWM logic inputs (DIN1, DIN2). The CDR signal can be used by the external controller for several reasons and provides information about the actual load during current regulation.

In the use case in which the PWM logic inputs are permanently held in Forward or Reverse mode and motor control is entirely entrusted to the internal Current Drive Regulation loop, the CDR pin outputs a PWM logic signal which is a replica of the PWM voltage applied to the load. By processing this signal and comparing its duty cycle with the expected one, a stall detection algorithm can be implemented. The CDR output can also be used as a trigger signal for an external ADC when sampling the ISEN current.

A pullup resistor must be connected from the CDR pins to the controller voltage supply.

The timing diagram in Figure 2 shows the behavior of this function when the motor spins in forward direction with DIN2 held firmly high (Case A) or when DIN2 is toggling (Cases B and C), respectively. The CDR output is asserted only when the decay mode is forced by the internal Current Regulation loop. Note that any PWM transition by the current drive regulation loop resets the fixed off time of the CDR circuit. In Case B, the actual Decay Interval is longer than t_{OFF}, whereas in Case C, the actual Decay Off interval is shorter.

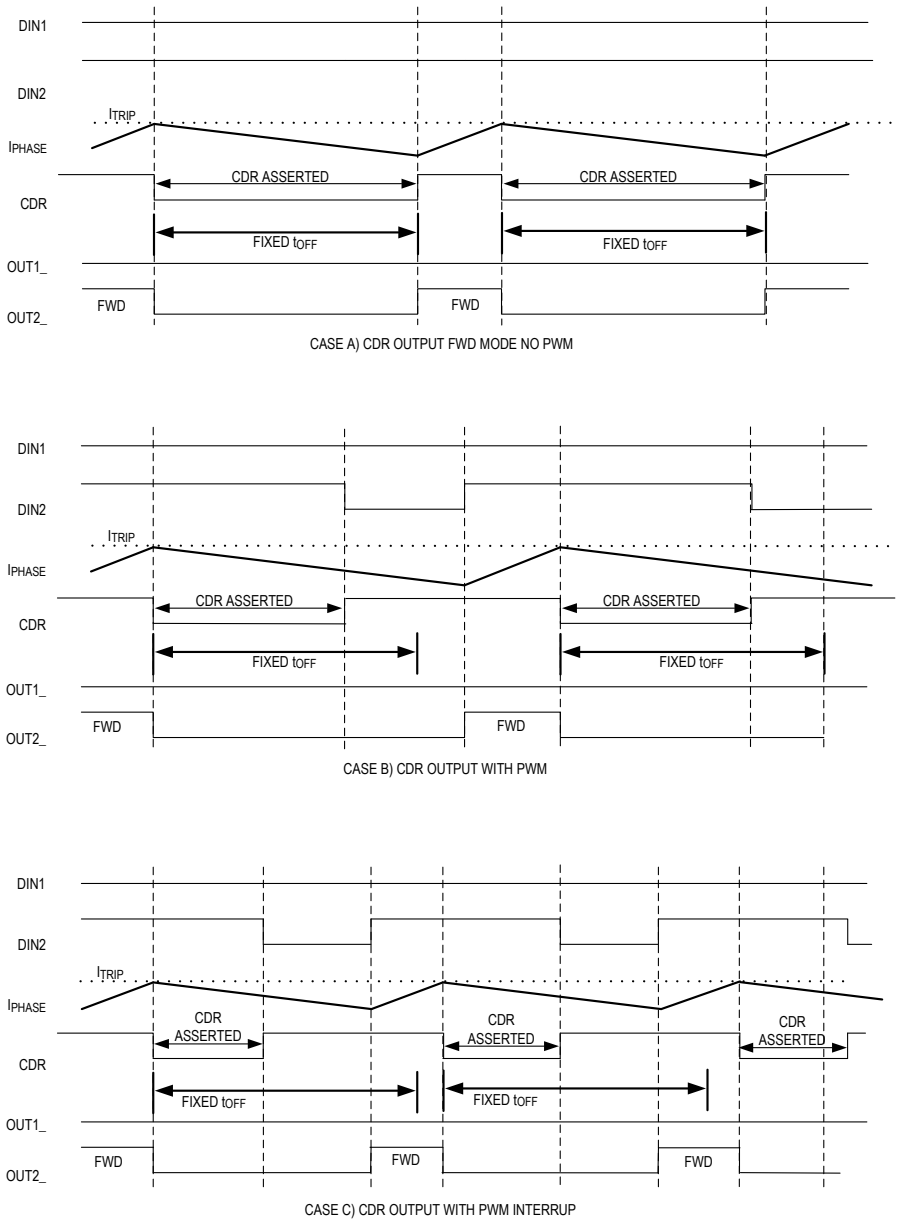


Figure 2. CDR Monitor Timing Diagram

Setting the Decay Mode

Two logic input pins allow to set the Decay Mode during t_{OFF}. The MAX22212 supports slow, fast, and two different mixed decay modes.

Table 4 shows the Truth Table for the Decay Mode selection.

Table 4. Decay Mode Truth Table

DECAY2	DECAY1	DECAY MODE
0	0	Slow

Table 4. Decay Mode Truth Table (continued)

0	1	Mixed 30% Fast/70% Slow
1	0	Mixed 60% Fast/40% Slow
1	1	Fast

Fault Protection

Overcurrent Protection – (OCP)

An overcurrent protection (OCP) protects the device against short circuits to the rails (supply voltage and ground) and across the outputs (OUTA and OUTB). The OCP threshold is set at 7.6A minimum. If the output current is larger than the OCP threshold for longer than the Over Current Protection blanking time (t_{OCP}), an OCP event is detected.

When an OCP event is detected, the H-Bridge is immediately disabled, and a fault indication is output on pin $\overline{FAULT}$. The H-Bridge is kept in a high impedance mode for 3ms (see t_{RETRY} specification). The H-Bridge is then re-enabled according to the current state. If the short circuit is still present, this cycle repeats. Otherwise, normal operation resumes. Avoid prolonged operation under the short-circuit failure mode as a prolonged OCP event affects the device reliability.

Undervoltage-Lockout Protection

When the V_M supply voltage is below the UVLO threshold, all OUT_ outputs are three-stated and the $\overline{FAULT}$ pin is driven low. The OUT_ outputs automatically return to their current state (defined by EN_ and DIN_) when the V_M supply voltage exceeds the OVLO threshold (max) and $\overline{FAULT}$ is driven high.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX22212ATJ+T	-40°C to +125°C	32 TQFN - 5mm x 5mm
MAX22212AUI+T	-40°C to +125°C	28 TSSOP - 4.4mm x 9.7mm

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/23	Release for Market Intro	—
1	1/24	Updated *Absolute Maximum Ratings*, *Package Information*, *Electrical Characteristics*, *Pin Description*, *Detailed Description*, and *Ordering Information* sections	6 –9, 12, 13, 15, 21, 22