

EVALUATION KIT
AVAILABLE



WCDMA Quasi-Direct Modulator with VGA and PA Driver

MAX2395

General Description

The MAX2395 fully monolithic quasi-direct modulator IC is designed for use in WCDMA/UMTS transmitters. The quasi-direct modulation architecture reduces system cost, component count, and board space compared to transmitters using an IF SAW filter with IF VCO and IF synthesizer blocks.

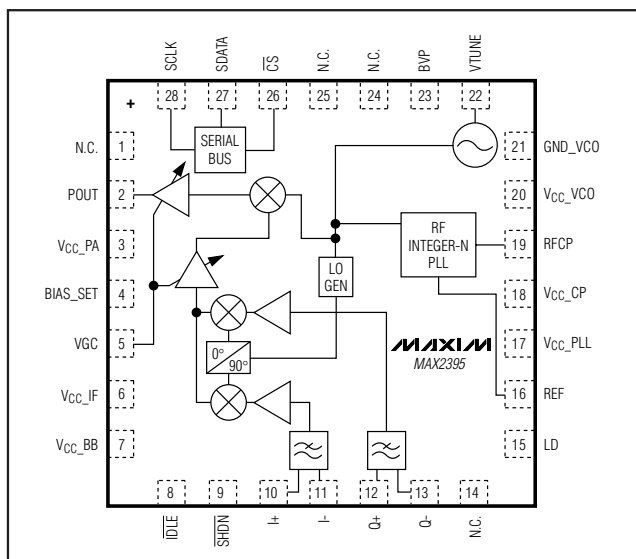
The MAX2395 includes I/Q baseband filters, an IF I/Q modulator with VGA, a fully monolithic VCO with PLL, an upconverter mixer, an RF VGA, and a power amplifier (PA) driver. The use of the quasi-direct modulator scheme ensures 5% (typ) EVM and a 30dB (min) carrier suppression. The RF VGA and IF VGA provide a nominal 90dB of output power control. No external local oscillators are required, enabling efficient implementation of variable duplex offset systems.

The PLL is programmed by loading data on the SPI™/MICROWIRE™-compatible 3-wire serial bus. The IC operates from a single +2.7V to +3.3V supply. The devices are available in space-saving 28-pin QFN and thin QFN exposed-pad packages (5mm x 5mm).

Applications

WCDMA Phones
UMTS/EDGE Phones
W-TDD Phones

Pin Configuration/ Functional Diagram



Features

- ◆ 5% EVM for P_{OUT} = +6dBm
- ◆ 1920MHz to 1980MHz Operation
- ◆ +2.7V to +3.3V Single-Supply Operation
- ◆ +6dBm Output Power at 72mA
- ◆ 81dB Minimum Automatic Gain-Control (AGC) Range
- ◆ Automatic I_{CC} Throttle Back for Optimal Power Consumption
- ◆ No IF SAW Filter Necessary
- ◆ On-Chip RF PLL, with Fully Monolithic VCO
- ◆ Ultra-Low External Component Count

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|-------------|----------------|-------------|
| MAX2395EGI | -40°C to +85°C | 28 QFN-EP* |
| MAX2395ETI | -40°C to +85°C | 28 TQFN-EP* |
| MAX2395ETI+ | -40°C to +85°C | 28 TQFN-EP* |

*EP = Exposed pad.

+Denotes a lead(Pb)-free/RoHS-compliant package.

SPI is a trademark of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.



Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642 or visit Maxim's website at www.maxim-ic.com.

WCDMA Quasi-Direct Modulator with VGA and PA Driver

MAX2395

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND-0.3V to +3.6V
 All Other Pins to GND.....-0.3V to V_{CC_} + 0.3V
 I₋, Q₋, REF to GND.....1V_{P-P}
 Digital Input Current±10mA

Continuous Power Dissipation (T_A = +70°C)
 28-Pin QFN (derate 20.8mW/°C above +70°C)1667mW
 28-Pin TQFN (derate 21.3mW/°C above +70°C)1702mW
 Operating Temperature Range-40°C to +85°C
 Junction Temperature.....+150°C
 Storage Temperature Range-65°C to +160°C
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +3.3V, R_{BIAS} = 12kΩ, T_A = -40°C to +85°C. Typical values are at V_{CC} = +2.85V and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--|-----------------------|------|-----------------------|-------|
| Supply Voltage Range | | 2.7 | 2.85 | 3.3 | V |
| Operating Supply Current | V _{VGC} = 0.35V | | 46 | 60 | mA |
| | P _{OUT} = 0dBm | | 67 | 82 | |
| | P _{OUT} = +6dBm | | 72 | 90 | |
| Idle Current | $\overline{\text{IDLE}} = V_{\text{IL}}$ | IDLE_PRG = 0 | 16 | 21 | |
| | | IDLE_PRG = 1 | 19 | 27 | |
| Shutdown Current | $\overline{\text{SHDN}} = 0$ | | 0.5 | 10 | μA |
| VGC Input Current | | -10 | | +10 | μA |
| VGC Input Current During Shutdown | $\overline{\text{SHDN}} = V_{\text{IL}}$ | | | 1 | μA |
| Gain-Control Voltage Range | | 0.35 | | 2.20 | V |
| Lock Indicator High—Leakage Current | PLL locked, V _{LD} = V _{CC} | | | 4 | μA |
| Lock Indicator Low—Sink Voltage | PLL unlocked, sinking 100μA | | | 0.4 | V |
| $\overline{\text{SHDN}}$ Input Logic-High, V _{DH} | | 1.5 | | V _{CC} | V |
| $\overline{\text{SHDN}}$ Input Logic-Low | | 0 | | 0.5 | V |
| $\overline{\text{SHDN}}$ Input Resistance | Resistance to ground | 50 | | | kΩ |
| Digital Input Logic-High, V _{IH} | All digital input pins including $\overline{\text{IDLE}}$, SDATA, SCLK, and $\overline{\text{CS}}$ (Note 3) | 0.7 x V _{DH} | | V _{CC} | V |
| Digital Input Logic-Low, V _{IL} | All digital input pins including $\overline{\text{IDLE}}$, SDATA, SCLK, and $\overline{\text{CS}}$ (Note 3) | 0 | | 0.3 x V _{DH} | V |
| Digital Control Pin Input Current | $\overline{\text{IDLE}}$, SDATA, SCLK, and $\overline{\text{CS}}$ | -10 | | +10 | μA |
| I/Q Input Leakage Current | | -10 | | +10 | μA |
| I/Q DC Common-Mode Voltage | | 1.35 | 1.45 | 1.65 | V |

WCDMA Quasi-Direct Modulator with VGA and PA Driver

MAX2395

AC ELECTRICAL CHARACTERISTICS

MAX2395 EV kit, $V_{CC} = +2.7V$ to $+3.3V$, $R_{BIAS} = 12k\Omega$, V_{VGC} adjusted to obtain maximum rated output power, and $T_A = -40^\circ C$ to $+85^\circ C$. I/Q inputs driven differentially with low-impedance source based on 3GPP UpLink reference measurement channel (12.2kbps), envelope level 1V_{p-p}. Typical values are at $V_{CC} = +2.85V$ and $T_A = +25^\circ C$, unless otherwise noted. See Tables 1 and 3 for register settings.) (Note 2)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--|---|--|------|--------|---------|-----|
| CASCADED RF SPECIFICATIONS | | | | | | |
| RF Frequency Range (Notes 4, 6) | | 1920 | 1950 | 1980 | MHz | |
| Maximum Output Power (Note 6) | VGC set for maximum output power while meeting ACPR1, ACPR2, out-of-band emissions, and output noise density specifications | 6 | | | dBm | |
| Out-of-Band Emissions (Note 6) | At $f = 1575MHz$ | | -31 | -24 | dBc | |
| | At $RF + 2 \times IF$ (image) | | -13 | -8.5 | | |
| Adjacent Channel Power Ratio, ACPR1 (Notes 5, 6) | $\Delta f = \pm 5MHz/3.84MHz$ BW | $P_{OUT} > 0dBm$ and $T_A > 0^\circ C$ | | -48 | -45 | dBc |
| | | $P_{OUT} \leq 0dBm$ and $T_A \leq 0^\circ C$ | | -45 | -43 | |
| Alternate Channel Power Ratio, ACPR2 (Notes 5, 6) | $\Delta f = \pm 10MHz/3.84MHz$ BW | | -60 | -57 | dBc | |
| Output Noise Power Density (Note 6) | $P_{OUT} = +6dBm$ at 1920MHz, noise measured at 1880MHz | | -140 | -137 | dBc/Hz | |
| | $P_{OUT} = +6dBm$ at 1980MHz, noise measured at 2110MHz | | -146 | -143 | | |
| Minimum Output Power | $V_{VGC} = 0.35V$ | | -85 | -78 | dBm | |
| Carrier Suppression | | 30 | | | dB | |
| Sideband Suppression | | 32 | | | dB | |
| EVM (Note 6) | Including BB filter, $P_{OUT} = +6dBm$ | | 5 | 7.5 | %RMS | |
| | Including BB filter, $P_{OUT} = -44dBm$ | | 8.6 | 14.6 | | |
| I/Q MODULATION BASEBAND INPUTS | | | | | | |
| Passband Amplitude Ripple | DC to 2MHz (Notes 6, 7) | -0.3 | | +0.4 | dB | |
| Baseband Selectivity | Relative to passband | At 8.08MHz | 8 | 35 | dB | |
| | | At 13.44MHz | 25 | 50 | | |
| INTEGER-N RF PLL | | | | | | |
| Main PLL Integer Division Ratios | 16-bit register (64/65 dual-modulus prescaler) | 4032 | 9750 | 65,535 | | |
| Reference Frequency Range | | 8 | 19.2 | 40 | MHz | |
| Input Frequency for Reference Frequency Doubler | OPCTRL register bit 7 = 1 | 13 | | 16 | MHz | |
| Reference-Divider Ratio | 9-bit register | | 80 | 511 | | |
| Charge-Pump Nominal Currents (Sink or Source) | Locked, $RCP1/RCP0 = 0\ 1$, $V_{CC}/2$ | 1200 | 1500 | 1800 | μA | |
| | Locked, $RCP1/RCP0 = 1\ 1$, $V_{CC}/2$ | 2000 | 2500 | 3000 | | |
| Charge-Pump Leakage Current | | | | 20 | nA | |

WCDMA Quasi-Direct Modulator with VGA and PA Driver

MAX2395

AC ELECTRICAL CHARACTERISTICS (continued)

MAX2395 EV kit, $V_{CC} = +2.7V$ to $+3.3V$, $R_{BIAS} = 12k\Omega$, V_{VGC} adjusted to obtain maximum rated output power, and $T_A = -40^\circ C$ to $+85^\circ C$. I/Q inputs driven differentially with low-impedance source based on 3GPP UpLink reference measurement channel (12.2kbps), envelope level 1V_{p-p}. Typical values are at $V_{CC} = +2.85V$ and $T_A = +25^\circ C$, unless otherwise noted. See Tables 1 and 3 for register settings.) (Note 2)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--|-----|-------|------|--------------------|
| ON-CHIP VCO | | | | | |
| Phase Noise | At 3MHz offset, measured at the center of the RF band (Note 6) | | -130 | -128 | dBc/Hz |
| Supply Pushing | Supply stepped from +2.7V to +3.3V, with on-chip voltage regulator | | ±0.15 | | MHz/V |
| RF VCO Pulling | When switching from IDLE mode to active Tx mode | | ±0.1 | | MHz _{p-p} |
| 3-WIRE SERIAL BUS INTERFACE | | | | | |
| Data to Clock Setup, t_{CS} | Figure 1 (Note 6) | 20 | | | ns |
| Data to Clock Hold Time, t_{CH} | Figure 1 (Note 6) | 10 | | | ns |
| Clock Pulse-Width High, t_{CWH} | Figure 1 (Note 6) | 20 | | | ns |
| Clock Pulse-Width Low, t_{CWL} | Figure 1 (Note 6) | 20 | | | ns |
| Clock to Load Enable/Setup Time, t_{ES} | Figure 1 (Note 6) | 20 | | | ns |
| Clock Frequency | (Note 6) | | | 20 | MHz |

Note 1: The following parameters are characterized using the register settings below.

Table 1. Characterization Register Settings

| REGISTER | SETTINGS | ADDRESS | FUNCTION |
|----------|-----------------------------|-------------------|------------------------------|
| RFR | 4050 hex (80 dec for +R) | 0000 _b | Reference-divider register |
| OPCTRL | 3B7D hex | 0100 _b | Operational control settings |

Note 2: Guaranteed at $T_A = +25^\circ C$ and $T_A = +85^\circ C$ by production test, and guaranteed by design and characterization at $T_A = -40^\circ C$.

Note 3: V_{DH} is the high voltage applied to the shutdown pin.

Note 4: Output power, linearity, noise power, and LO leakage specifications are met over this frequency range.

Note 5: Specifications valid for all output power levels, unless limited by thermal noise at lower output power levels.

Note 6: Guaranteed by design and characterization.

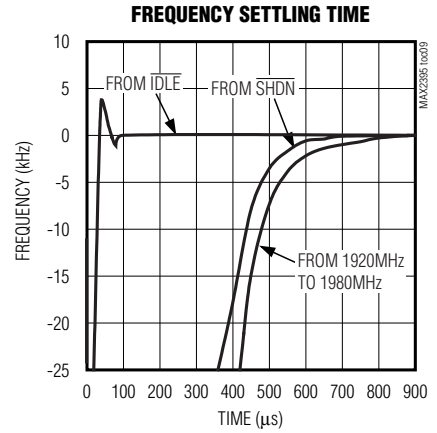
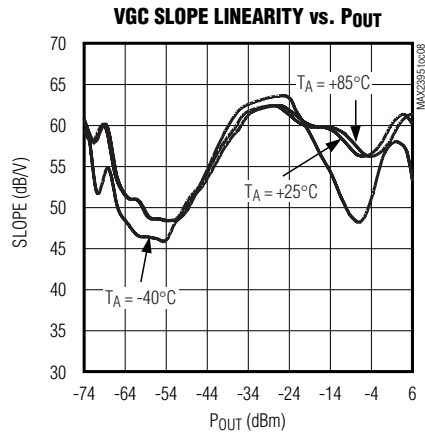
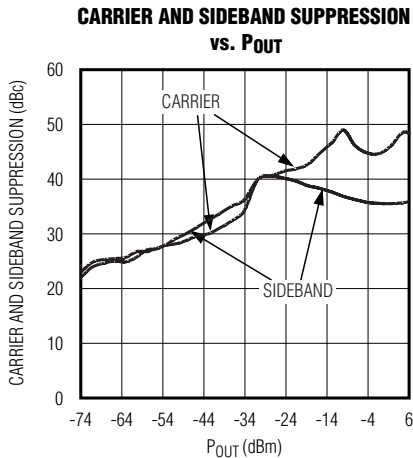
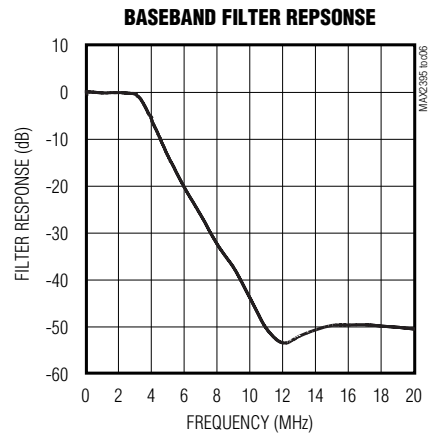
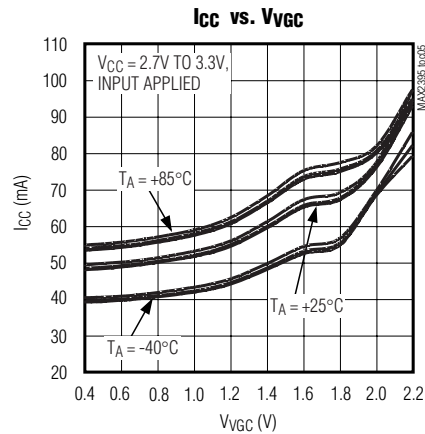
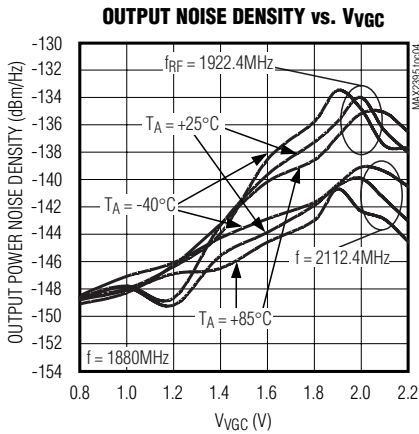
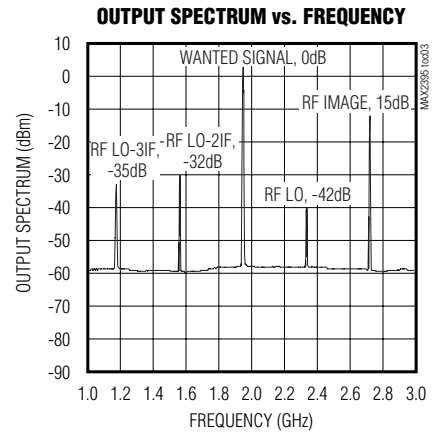
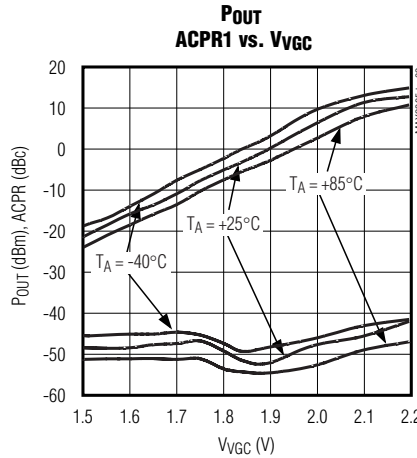
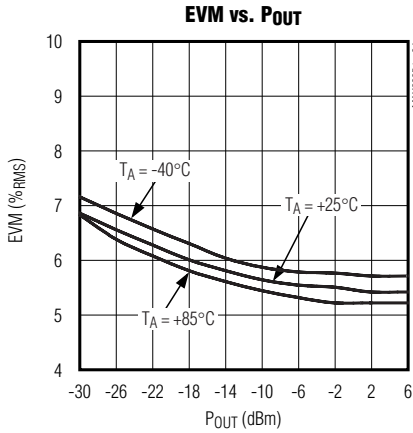
Note 7: Tested at 1MHz and 2MHz in the passband.

WCDMA Quasi-Direct Modulator with VGA and PA Driver

Typical Operating Characteristics

($V_{CC} = +2.85V$, $f_{RF} = 1950MHz$, $MPL = 1$, and $T_A = +25^\circ C$, unless otherwise noted.)

MAX2395



WCDMA Quasi-Direct Modulator with VGA and PA Driver

MAX2395

Pin Description

| PIN | NAME | FUNCTION |
|------------|--------------------------|---|
| 1 | N.C. | Connect to RF GND on PCB |
| 2 | POUT | Transmitter Output. This is an open-collector output and requires a pullup inductor to the supply voltage. This pullup inductor can be part of the output matching network and can be connected directly to the battery. |
| 3 | VCC_PA | Supply for the PA Driver. This pin must be bypassed with a capacitor to system ground as close to the pin as possible. Do not share the ground vias for the bypass capacitor with any other branch (see the <i>Typical Operating Circuit</i>). |
| 4 | BIAS_SET | Bias-Setting Pin. The DC voltage at this pin is a bandgap voltage. For nominal bias, connect a 12k Ω resistor to ground. The value of this resistor can be adjusted to alter current consumption, linearity, and noise performance of the RF output. |
| 5 | VGC | Gain-Control Pin. Analog input pin controls both the IF VGA and RF VGA gain. When not driven, the voltage on this pin is typically +1.5V. An RC filter on this pin must be used to filter out DAC noise or the PDM clock. |
| 6 | VCC_IF | Supply for IF Section. Bypass to system ground with a capacitor as close to the pin as possible. Do not share the ground vias for the bypass capacitor with any other branch (see the <i>Typical Operating Circuit</i>). |
| 7 | VCC_BB | Supply for Baseband Section. Bypass to system ground with a capacitor as close to the pin as possible. Do not share the ground vias for the bypass capacitor with any other branch (see the <i>Typical Operating Circuit</i>). |
| 8 | $\overline{\text{IDLE}}$ | Idle CMOS Digital Input. Drive LOW to place the device in WCDMA compressed mode (VCO and PLL are ON; all others are OFF). A small RC lowpass filter can be used to minimize the effect of external digital noise. |
| 9 | $\overline{\text{SHDN}}$ | Shutdown CMOS Digital Input. Drive LOW to place the device in shutdown (everything OFF except serial interface and registers, which retain their values). A small RC lowpass filter can be used to minimize the effect of external digital noise. A logic-low on the $\overline{\text{SHDN}}$ pin overrides the serial bus $\overline{\text{SHDN}}$ bit status. |
| 10, 11 | I+, I- | Differential I-Channel Baseband Inputs to the Baseband Filter |
| 12, 13 | Q+, Q- | Differential Q-Channel Baseband Inputs to the Baseband Filter |
| 14, 24, 25 | N.C. | Leave Open |
| 15 | LD | Lock CMOS Output. This pin is an open-drain output. Output HIGH indicates the RF PLL is locked. |
| 16 | REF | Reference Frequency Input. This pin is internally biased to approximately +1.0V and must be AC-coupled to the reference source. This is a high-impedance port and can be externally terminated to the desired impedance. |
| 17 | VCC_PLL | Supply for PLL. Bypass with a capacitor to GND (see the <i>Typical Operating Circuit</i>). |
| 18 | VCC_CP | Supply for Synthesizer Charge Pump. Bypass with a capacitor to GND (see the <i>Typical Operating Circuit</i>). |
| 19 | RFCP | RF Charge-Pump Output. Connect the RF PLL's loop filter between RFCP and system ground. Keep the line from this pin to the tank tune input as short as possible to prevent spurious pickup. Connect the loop filter as close to the tune input as possible. |

WCDMA Quasi-Direct Modulator with VGA and PA Driver

Pin Description (continued)

| PIN | NAME | FUNCTION |
|-----|-----------------|--|
| 20 | VCC_VCO | Supply for VCO. Bypass to system ground with a capacitor as close to the pin as possible. Do not share ground vias for the bypass capacitor with any other branch (see the <i>Typical Operating Circuit</i>). |
| 21 | GND_VCO | RF VCO Varactor Ground. Connect to the ground at the PLL loop-filter capacitors. Do not connect to the exposed pad. |
| 22 | VTUNE | Oscillator-Frequency Tuning Voltage Input |
| 23 | BYP | Bypass with a Capacitor to GND. The capacitor is used by the on-chip VCO voltage regulator (see the <i>Typical Operating Circuit</i>). |
| 26 | \overline{CS} | 3-Wire Serial Bus Enable Input (Figure 1) |
| 27 | SDATA | 3-Wire Serial Bus Data Input (Figure 1) |
| 28 | SCLK | 3-Wire Serial Bus Clock Input (Figure 1) |
| — | EP | Exposed Pad. Connect to the ground plane for proper heat dissipation. |

Detailed Description

The MAX2395 quasi-direct modulator accepts differential I/Q baseband inputs with external common-mode bias. A gain-control voltage pin (VGC) controls the gain of the IF and RF VGAs simultaneously to achieve the best current consumption and linearity performance.

GmC Filters

The internal GmC filters are used to eliminate noise and baseband DAC aliasing signals above 8MHz. The GmC filter can be bypassed (GMC_EN bit, OPCTRL register bit 3), lowering the total current at the expense of no filtering. To speed up the settling time when transitioning from IDLE to transmit mode, the filter can be forced to stay active in IDLE mode using the IDLE_PRG bit (OPCTRL register bit 1). Contact factory if bypass mode is used.

I/Q Modulator

Differential in-phase (I) and quadrature-phase (Q) input pins are designed to be DC-coupled and biased with the baseband output from a digital-to-analog converter (DAC). The I₋ and Q₋ inputs need a DC bias, which can range from 1.35V to 1.65V. The current draw is negligible and the differential input capacitance is 4pF. The VCO frequency is divided by 6 to produce the RF I/Q LO signals.

IF/RF VGA

The part offers approximately 90dB of gain-control range. An external voltage must be applied using a DAC allowing for dynamic gain control. To minimize the noise contribution from the DAC to the RF signal, place an RC filter at this pin (refer to the MAX2395 Evaluation Kit data sheet). The PA driver is included in the RF VGA.

Internal VCO and Tank

The integrated monolithic VCO and tank is tuned through the VTUNE pin. The RF/IF LO signals are generated from this oscillator.

PLL

The internal PLL uses a charge-pump output to drive a loop filter. The loop filter is typically a passive 2nd-order lead lag filter with a bandwidth of 10kHz. The loop filter must be optimized for a selected charge-pump current, where $K_{VCO} = 90\text{MHz/V}$. The internal architecture requires the RF VCO to run at 1.2x the desired frequency, mandating a 240kHz comparison frequency for an output step size of 200kHz. The LD output indicates whether the PLL is locked. An output high indicates a lock condition.

There is an optional frequency doubler at the input of the PLL reference divider. When using a 13MHz reference frequency, either a 40kHz comparison can be used or the internal frequency doubler is enabled to allow a comparison frequency of 80kHz. The optional frequency double can be activated by setting OPCTRL register bit 7 = 1.

PA Driver/RF Upconverter

The IF signal is upconverted with an image reject RF mixer, and differentially fed into the PA driver. The PA driver converts differential input signals to a single-ended output. The driver requires a pullup inductor, which is part of the output matching network.

WCDMA Quasi-Direct Modulator with VGA and PA Driver

Register Definition

The MAX2395 includes three programmable, 20-bit registers consisting of two divide registers and an operational control register. These registers are programmed from the SPI/ MICROWIRE-compatible serial port. The 4 least significant bits (LSBs) are reserved for the register's address. The register bits have been assigned to allow sharing of the 3-wire bus with the MAX2390/MAX2391/MAX2392/MAX2401 receiver ICs. The 16 most significant bits (MSBs) are used for register data. Data is shifted in MSB first, followed by the 4-bit address. When \overline{CS} is low, the clock input is active and data is shifted with the rising edge of the clock. When \overline{CS} transitions to high, the shift register is latched into the register selected by the contents of the address bits. Power-up defaults for the three registers are shown in Table 2. Initialize the registers according to the characterization table (Table 1).

The RFM register sets the main frequency divide ratio for the RF PLL. The RFR register sets the reference frequency divide ratio. The RF VCO frequency is determined by the following:

$$\text{RF VCO frequency} = f_{\text{REFin}} \times (\text{RFM}/\text{RFR})$$

where f_{REFin} is the external input reference frequency for the MAX2395.

The operational control register (OPCTRL) controls the state of the IC. See Table 3 for the function of each bit.

The RFR divide register includes test bits B9–B15. These bits are used to troubleshoot the VCO and synthesizer section (see Table 4). These bits are not needed for normal use and should be left as the values at power-up.

The device offers several different operation modes for conserving power. Table 5 explains how to implement each mode.

Shutdown and Idle Mode™

The part offers a shutdown mode and idle mode for optimal power management. In shutdown mode, all functions are turned off except the serial interface. When the part is shut down using the OPCTRL register, the IC draws a residual current of 60 μ A (typ). In idle mode, the VCO, PLL, and serial interface remain on to minimize startup time. The GmC filter can be software programmed to power on or off during idle mode (see Table 5).

Idle Mode is a trademark of Maxim Integrated Products, Inc.

Applications Information

External Matching to PA

The Tx outputs are internally matched to 50 Ω . The open-collector output requires a pullup inductor to V_{CC} . The selection of matching in the MAX2395 Evaluation Kit allows optimization of ACPR.

Electromagnetic Compliance Considerations

Two major concepts should be employed to produce a low-spur and EMC-compliant transmitter: Minimize circular current-loop area to reduce H-field radiation, and minimize losses. To minimize circular current-loop area, bypass as close to the device as possible and use the distributed capacitance of a ground plane. To minimize losses, make RF traces short.

Program only the necessary bits in any register to minimize clock cycles. RC filtering can also be used to slow the clock edges on the 3-wire interface, reducing high-frequency spectral content. RC filtering also provides for transient protection against IEC 802 testing by shunting high frequencies to ground, while the series resistance attenuates the transients for error-free operation. The same applies to the logic-input pins (SHDN, IDLE).

High-frequency bypass capacitors are required close to the pins with a dedicated via to ground. The package provides minimal inductance ground by using an exposed pad under the part. Provide at least five low-inductance vias under the pad to ground to minimize ground inductance. Use a solid ground plane wherever possible. Any cutout in the ground plane may act as a slot radiator and reduce its shield effectiveness.

Layout Issues

The MAX2395 Evaluation Kit can be used as a reference for board layout. Gerber files are available upon request at www.maxim-ic.com.

To minimize coupling between different sections of the IC, the ideal power-supply layout is a star configuration, which has a large decoupling capacitor at a central V_{CC} node. The V_{CC} traces branch out from this node, each going to a separate V_{CC} node in the circuit. At the end of each trace is a bypass capacitor with impedance to ground less than 1 Ω at the frequency of interest. This arrangement provides local decoupling at each V_{CC} pin. Use at least one via per bypass capacitor.

WCDMA Quasi-Direct Modulator with VGA and PA Driver

MAX2395

Table 2. Register Power-Up Default States (f_{REF} = 19.2MHz, f_{RF} = 1950MHz)

| REGISTER | DEFAULT | ADDRESS | FUNCTION |
|----------|-----------------------------|-------------------|------------------------------|
| RFM | 9750 dec | 0010 _b | Main-divider ratio register |
| RFR | 4050 hex (80 dec for +R) | 0000 _b | Reference-divider register |
| OPCTRL | 197D hex | 0100 _b | Operational control settings |

Table 3. Operation Control Register (OPCTRL) Bit Assignments

| BIT NAME | POWER-UP STATE | BIT LOCATION (0 = LSB) | FUNCTION |
|--------------------------|----------------|---------------------------|---|
| $\overline{\text{SHDN}}$ | 1 | 0 | Setting this bit to zero shuts down everything except the serial interface and registers, which retain their values. It is overridden by a logic-low on the $\overline{\text{SHDN}}$ pin. |
| IDLE_PRG | 0 | 1 | If bit is set to 1, this leaves the GmC filters and the servo loop ON when the $\overline{\text{IDLE}}$ pin goes LOW. If bit is set to zero, the GmC filters shut off when the $\overline{\text{IDLE}}$ pin goes LOW. |
| — | 1 | 2 | Leave in power-up state. |
| GmC_EN | 1 | 3 | Setting this bit to zero bypasses GmC filters. |
| PLL_EN | 1 | 4 | Setting this bit to zero shuts off the RF PLL. |
| VCO_EN | 1 | 5 | Setting this bit to zero shuts off the RF VCO. |
| PA_RF_IF_EN | 1 | 6 | Setting this bit to zero shuts off the PA driver, RF upconverter, and IF modulator sections. |
| X2_EN | 0 | 7 | Setting this bit to 1 enables the X2 multiplier for use in the REF divider section when TCXO frequency is 13MHz. |
| MPL | 1 | 8 | Maximum power level setting: 1 = +6dBm; 0 = +3dBm |
| PRD_Bias | 0 | 9 | Predriver bias: 0 = -25%; 1 = nominal |
| OUT_Bias | 0 | 10 | Output bias: 0 = nominal; 1 = +30% |
| RCP1, RCP0 | 1 1 | 12, 11 | A 2-bit word sets the RF charge-pump current as follows: 0 0 = 1000 μ A 0 1 = 1500 μ A 1 0 = 2000 μ A 1 1 = 2500 μ A |
| AML1, AML0 | 0 0 | 14, 13 | A 2-bit word sets the Ameliorator current as follows: 0 0 = Off 0 1 = Low (nominal) 1 0 = Mid 1 1 = High These bits are used in DC offset trimming mode, where DC_TRM = 1. |
| DC_TRM | 0 | 15 | Setting this bit to 1 enables the DC offset trimming mode. |

WCDMA Quasi-Direct Modulator with VGA and PA Driver

Table 4. Reference-Divider (RFR) Register

| BIT NAME | POWER-UP STATE | BIT LOCATION (0 = LSB) | FUNCTION |
|------------------------|----------------|------------------------|---|
| RFR8 to RFR0 | 001010000 | 8 to 0 | Reference-divider register bits |
| LD1, LD0 | 0 0 | 10, 9 | 0 0 = Normal operation (lock-detect output at LD pin) 0 1 = RFM-DIV output 1 0 = RFR-DIV output 1 1 = Low logic output |
| RCPT2, RCPT1, RCPT0 | 0 0 0 | 13, 12, 11 | RF CP test bits: 0 0 0 = Normal mode 0 0 1 = Source sink ON 0 1 1 = Sink ON 1 0 1 = Source ON 1 1 0 = Source, sink OFF |
| RESERVED | 1 | 14 | Program to 1 for normal operation |
| RESERVED | 0 | 15 | Program to 0 for normal operation |

Table 5. Power-Down Modes

| SHDN PIN (9) | SHDN BIT (0) | IDLE PIN (8) | IDLE_PRG BIT (1) | POWER-DOWN MODES | COMMENTS | SERIAL BUS | I/Q MOD, RF UC, PA DRIVER | RF VCO | RF PLL | GmC |
|--------------|--------------|--------------|------------------|------------------|---|------------|---------------------------|--------|--------|-----|
| 0 | X | X | X | SHDN mode | All OFF except serial bus and registers (which retain values). A zero on the SHDN pin overrides the SHDN bit. | OFF | OFF | OFF | OFF | OFF |
| 1 | 0 | X | X | | | ON | | | | |
| 1 | 1 | 0 | 0 | IDLE mode | All OFF except RF PLL, RF VCO, serial bus, and registers (which retain values). RF PLL and RF VCO are on or off depending on the control-bit values before toggling the IDLE pin to zero. | ON | OFF | X | X | OFF |
| 1 | 1 | 0 | 1 | | | ON | OFF | X | X | X |
| 1 | 1 | 1 | X | Power-up mode | The 5 different TX blocks can be toggled ON/OFF using the serial bus. | ON | X | X | X | X |

WCDMA Quasi-Direct Modulator with VGA and PA Driver

MAX2395

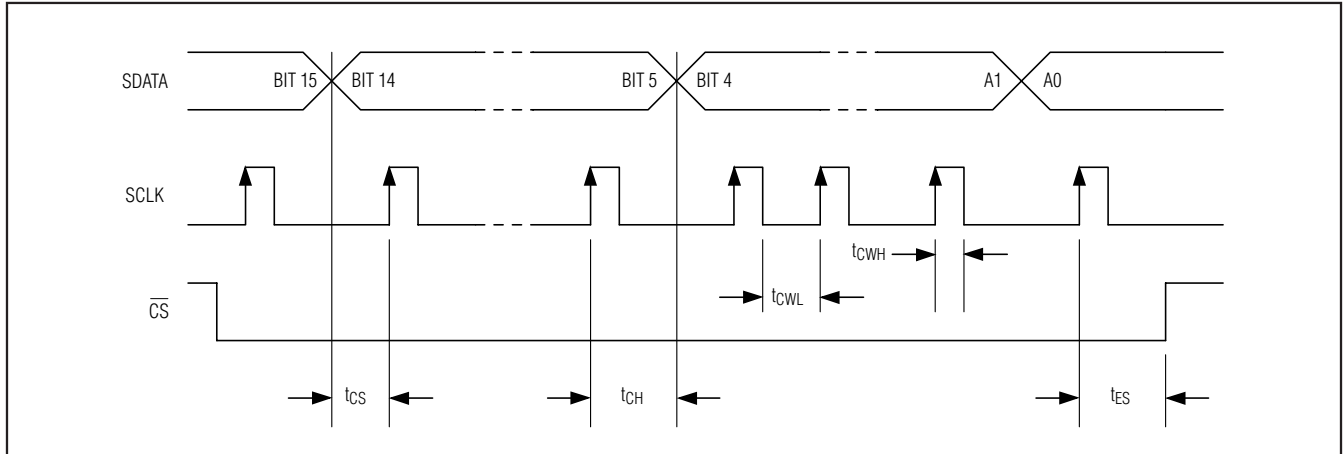


Figure 1. 3-Wire SPI/MICROWIRE Serial-Interface Timing Diagram

| 20-BIT REGISTER | | | | | | | | | | | | | | | | ADDRESS | | | |
|--------------------------------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|
| DATA 16 BITS | | | | | | | | | | | | | | | | ADDRESS 4 BITS | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | A3 | A2 | A1 | A0 |
| RFM DIVIDE RATIO REGISTER (16 BITS) | | | | | | | | | | | | | | | | ADDRESS | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 0 | 0 | 1 | 0 |
| RFR DIVIDE RATIO REGISTER (9 BITS) | | | | | | | | | | | | | | | | ADDRESS | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 0 | 0 | 0 | 0 |
| OPERATION CONTROL REGISTER (16 BITS) | | | | | | | | | | | | | | | | ADDRESS | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 0 | 1 | 0 | 0 |

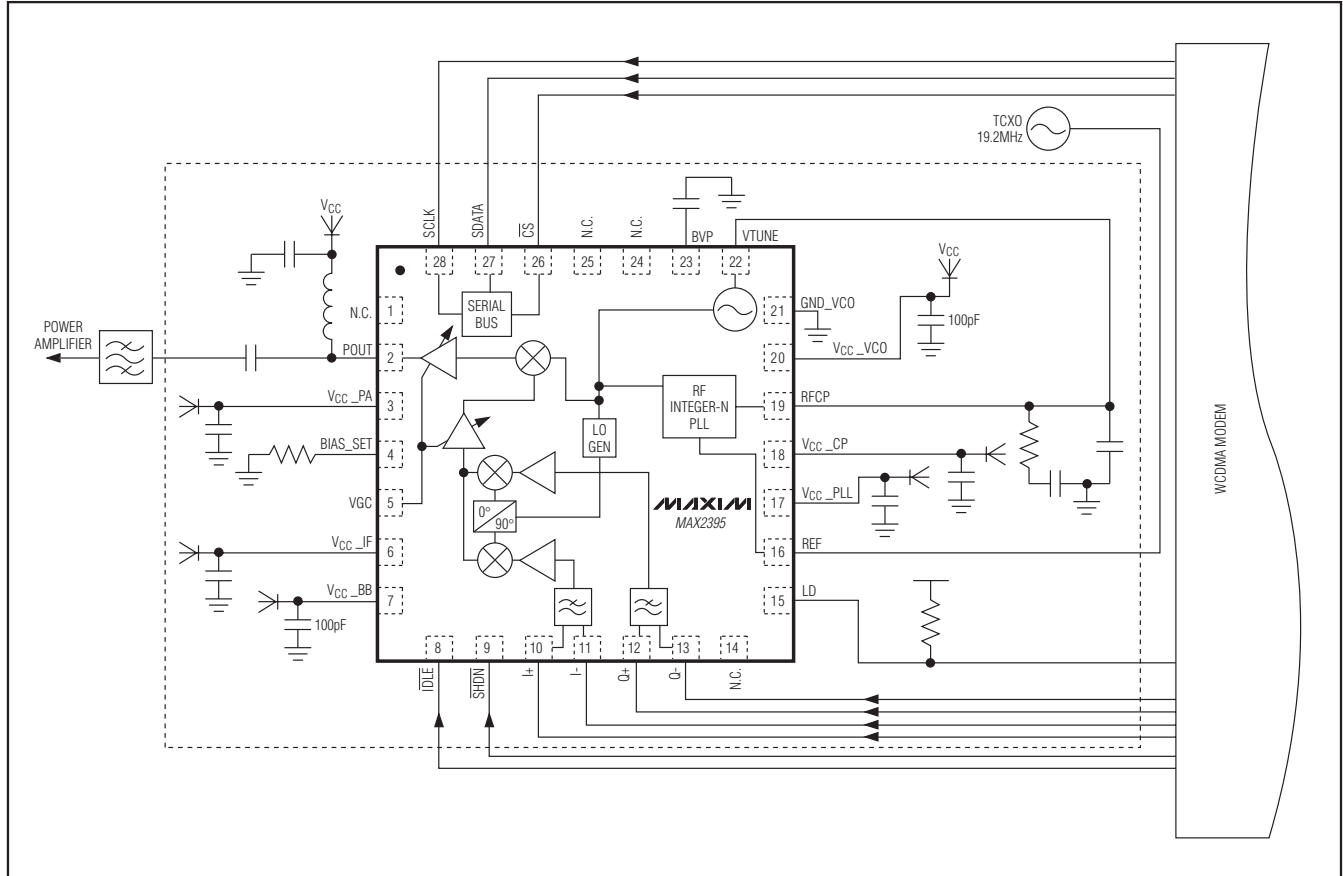
Figure 2. Register Assignments

It is recommended that the exposed pad be soldered to a ground plane on the PCB, either directly or through an array of plated via holes. Soldering the pad to ground is critical for proper heat dissipation. Use a solid ground plane wherever possible. Any cutout in the ground plane may act as a slot radiator and reduce its shield effectiveness.

WCDMA Quasi-Direct Modulator with VGA and PA Driver

MAX2395

Typical Operating Circuit



Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|--------------|--------------|-------------------------|
| 28 QFN-EP | G2855-2 | 21-0091 |
| 28 TQFN-EP | T2855-3 | 21-0140 |

WCDMA Quasi-Direct Modulator with VGA and PA Driver

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|--|---------------|
| 2 | 5/05 | — | — |
| 3 | 1/09 | Removed obsolete parts MAX2394/MAX2403/MAX2407 from data sheet | 1–13 |

MAX2395

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 _____ 13