Automotive, 65V, 2A/3A Mini Buck Converters

MAX25262/MAX25263

General Description

The MAX25262/MAX25263 are small, synchronous buck converters with integrated high-side and low-side switches. The device is designed to deliver up to 2A/3A with 3.5V to 65V input voltages while using only 3.5µA quiescent current at no load. The IC comes with a small 20ns minimum on-time capability, which enables the large step-down conversions in a single stage without skipping cycles. A max duty cycle of 98% and low high-side FET ON-resistance enable a low dropout operation for low input voltage applications.

The voltage quality can be monitored by observing the PGOOD signal. The device offers two fixed 5V and 3.3V output voltages. In addition, the device can be configured for 1V to 20V output voltages using an external resistor-divider. The frequency is internally fixed at 2.1MHz, which allows for small external components, reduced output ripple, and guarantees no AM interference. A 400kHz option is also offered to provide the minimum switching losses and maximum efficiency. For high efficiency at light load, the IC enters skip mode at light loads when FSYNC is pulled low. A pin-selectable forced pulse-width modulation (PWM) mode is also available for EMI-critical applications. The IC comes in a symmetrical flip-chip package that offers superior EMI performance. Further, the pin-selectable spread spectrum helps to enhance EMI performance.

Applications

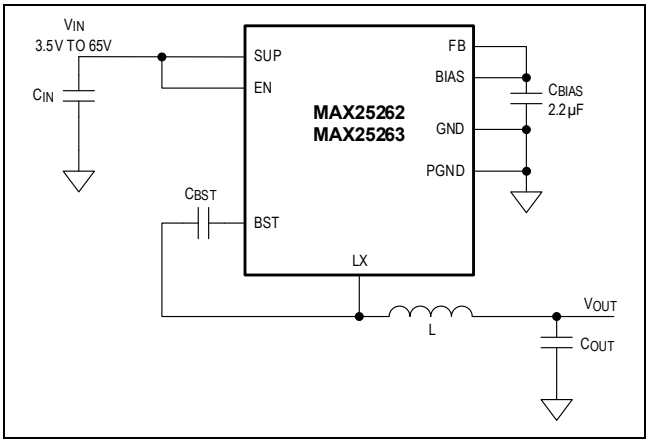
- Double Battery Automotive Systems
- Automotive Instrument Cluster
- Distributed DC Power Systems
- Navigation and Radio Head Units

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Meets Stringent Original Equipment Manufacturer (OEM) Module Power Consumption and Performance Specifications
  - 2A/3A Output-Current Capability
  - 3.5µA Supply Current in Standby Mode
- Enables Double Battery Operation
  - Wide Input Supply Range from 3.5V to 65V
  - Programmable 1V to 20V Output Voltage
  - Fixed 5V/3.3V/12V Options Available
- EMI-Reduction Features Reduce Interference with Sensitive Radio Bands without Sacrificing Wide Input Voltage Range
  - 20ns (typ) Minimum On-Time Guarantees Skip-Free Operation for 3.3V Output at 2.1MHz and 24V_{IN}
  - Spread-Spectrum Option
  - Phase-Locked Loop (PLL) Frequency Synchronization
- Protection Features Improve System Reliability
  - PGOOD Output and High-Voltage EN Input Simplify Power Sequencing
  - Undervoltage Lockout
  - Overtemperature and Short-Circuit Protection
  - AEC-Q100 Qualified

Simplified Block Diagram



19-101221; Rev 4; 2/24

Absolute Maximum Ratings

EN, SUP to PGND ..... -0.3V to +70V
LX to PGND (*Note 1*) ..... -0.3V to SUP+0.3V
SYNC, BIAS to GND ..... -0.3V to +6V
SPS, FB, EXTVCC to AGND ..... -0.3V to BIAS+0.3V
PGOOD to GND ..... -0.3V to +6V
GND to PGND ..... -0.3V to +0.3V
OUT to PGND ..... -0.3V to +22V
BST to LX ..... -0.3V to +6V

Continuous Power Dissipation (T_A = +70°C, derate 35.71mW/°C above +70°C) 2857.14mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C
Lead Temperature (soldering,10s) ..... +300°C

Note 1: Self-protected against transient voltages exceeding these limits for ≤ 50ns under normal operation and loads up to the maximum rated output current.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range			-40 to +125	°C

Package Information

Package Code	F173B3FY+1
Outline Number	*21-100429*
Land Pattern Number	*90-100162*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	28°C/W
Junction to Case (θ_{JC})	8°C/W

Electrical Characteristics

(V_{SUP} = V_{EN} = 24V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C (*Note 2* and *Note 3*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}	Normal operation	3.5		65	V
Supply Current	I_{IN}	V_{EN} = 0V		1.5	5	µA
		V_{EN} = V_{SUP}, switching, EXTVCC = 3.3V		3.5		
Buck Fixed Output Voltage	V_{OUT}	V_{FB} = V_{BIAS}, 3.2V < V_{OUT} < 13V, PWM mode	-2		2	%
		V_{FB} = V_{BIAS}, 3.2V < V_{OUT} < 13V, Skip mode	-3		3	
Regulated Feedback Voltage	V_{FB}		0.985	1	1.015	V
Feedback Leakage Current	I_{FB}	T_A = +25°C		0.01	1	µA

(V_{SUP} = V_{EN} = 24V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C (*Note 2* and *Note 3*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Feedback Line Regulation Error		V_{SUP} = 3.5V to 65V, V_{FB} = 1V			0.01		%/V
Maximum Duty Cycle				96	98		%
Minimum On-Time	t_{ON_MIN}				20		ns
Switching Frequency Accuracy	f_{SW_400kHz}			360	400	440	kHz
	$f_{SW\_2.1MHz}$			1.9	2.1	2.32	MHz
Current Limit	$ILIM_{2A}$	2A version		2.6	3.6	5	A
	$ILIM_{3A}$	3A version		3.4	4.75	6.2	
Soft-Start Time	t_{SS}	(*Note 5*)	2.1MHz setting	2.75	4	4.75	ms
		(*Note 5*)	400kHz setting	4	5	6	ms
LX Leakage Current	ILX_{LKG}	V_{LX} = V_{PGND} or V_{IN}, T_A = +25°C			0.001	1	µA
High-Side Switch On-Resistance	RON_{HS}	I_{LX} = 1A, V_{BIAS} = 5V			108	250	mΩ
Low-Side Switch On-Resistance	RON_{LS}	I_{LX} = 1A, V_{BIAS} = 5V			56	120	mΩ
PGOOD							
PGOOD UV Threshold	V_{PGOOD_H}	% of V_{OUT}, rising		93	95	97	%
	V_{PGOOD_F}	% of V_{OUT}, falling		91.5	93	95.5	
PGOOD OV Threshold		% of V_{OUT}, rising		106	108	110	%
		% of V_{OUT}, falling		103.5	105.5	107.5	
PGOOD Output Low Voltage		I_{SINK} = 1mA			0.03	0.2	V
PGOOD Leakage Current		V_{PGOOD} = 5V, T_A = +25°C			0.01	1	µA
PGOOD Debounce Time		Fault detection, falling			63		µs
		Fault detection, rising			47		
PGOOD Assertion Time		PGOOD low to high			47		µs
SYNC INPUT							
SYNC Frequency Range		f_{SW} = 2.1MHz		1.8		2.6	MHz
		f_{SW} = 400kHz		250		550	kHz
SYNC Switching Thresholds		High threshold		1.4			V
		Low threshold				0.4	
SYNC Pull-Down		Resistance to GND			1		MΩ
SPS INPUT							
SPS Switching Thresholds		High threshold		1.5			V
		Low threshold				0.4	
INTERNAL LDO BIAS AND EXTVCC							
Internal BIAS Voltage		V_{SUP} > 6V			5		V
BIAS UVLO Threshold		$V_{BIASRising}$			3.1	3.3	V
		$V_{BIASFalling}$		2.4	2.65		
EXTVCC Operating Range				3.25		5.5	V

(V_{SUP} = V_{EN} = 24V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C (*Note 2* and *Note 3*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTVCC Threshold	$V_{THEXTVCC}$	EXTVCC rising, hysteresis = 110mV		3.09	3.25	V
THERMAL OVERLOAD						
Thermal Shutdown Temperature		(*Note 4*)		170		°C
Thermal Shutdown Hysteresis		(*Note 4*)		15		°C
EN LOGIC INPUT						
High Threshold		ENHigh	1.8			V
Low Threshold		ENLow			0.8	V
EN Input Bias Current		EN_Logic inputs only, T_A = +25°C		0.01	1	µA
SPREAD SPECTRUM						
Spread Spectrum		Percentage of f_{SW}		±6		%

Note 2: Limits are 100% tested at +25°C. Limits over operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at +25°C.

Note 3: This device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

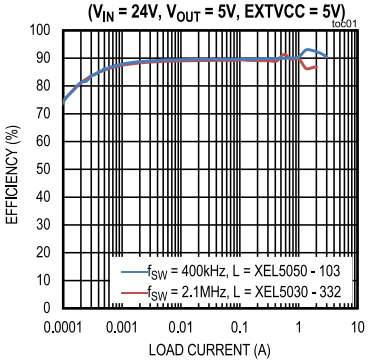
Note 4: Guaranteed by design, not production tested.

Note 5: Soft-start time is measured as the time taken from EN going high to PGOOD going high.

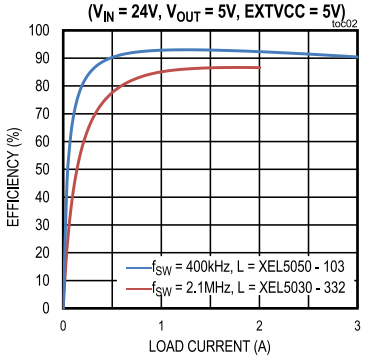
Typical Operating Characteristics

(V_{SUP} = 24V, T_A = +25°C, unless otherwise stated.)

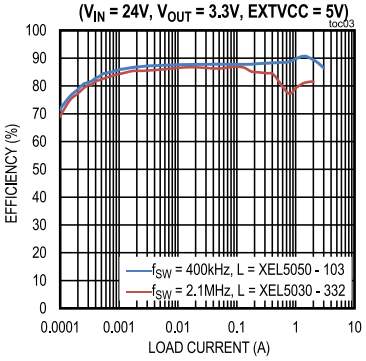
EFFICIENCY vs. LOAD CURRENT
SKIP MODE
(V_{IN} = 24V, V_{OUT} = 5V, EXTVCC = 5V)



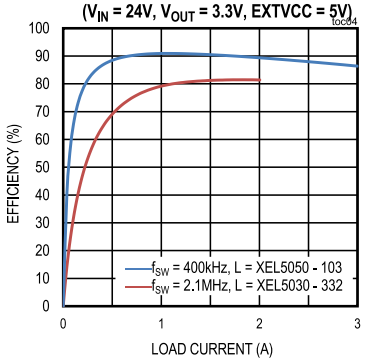
EFFICIENCY vs. LOAD CURRENT
FPWM MODE
(V_{IN} = 24V, V_{OUT} = 5V, EXTVCC = 5V)



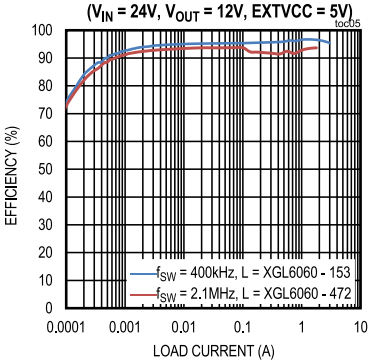
EFFICIENCY vs. LOAD CURRENT
SKIP MODE
(V_{IN} = 24V, V_{OUT} = 3.3V, EXTVCC = 5V)



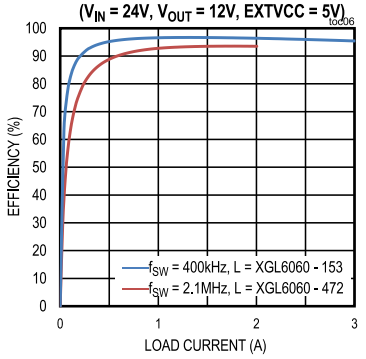
EFFICIENCY vs. LOAD CURRENT
FPWM MODE
(V_{IN} = 24V, V_{OUT} = 3.3V, EXTVCC = 5V)



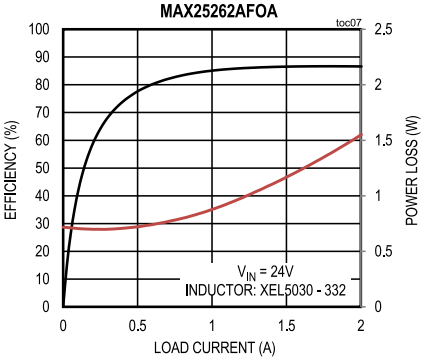
EFFICIENCY vs. LOAD CURRENT
SKIP MODE
(V_{IN} = 24V, V_{OUT} = 12V, EXTVCC = 5V)



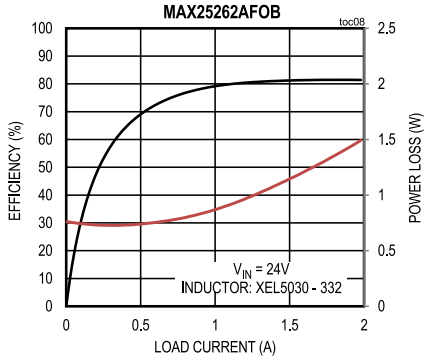
EFFICIENCY vs. LOAD CURRENT
FPWM MODE
(V_{IN} = 24V, V_{OUT} = 12V, EXTVCC = 5V)



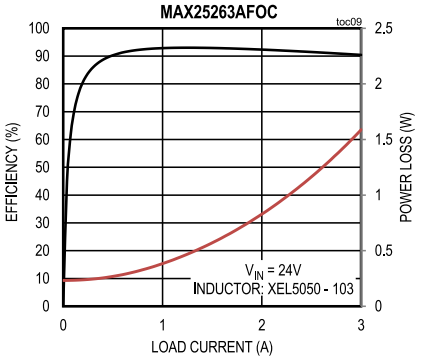
EFFICIENCY AND POWER LOSS
vs. LOAD CURRENT
MAX25262AFOA



EFFICIENCY AND POWER LOSS
vs. LOAD CURRENT
MAX25262AFOB

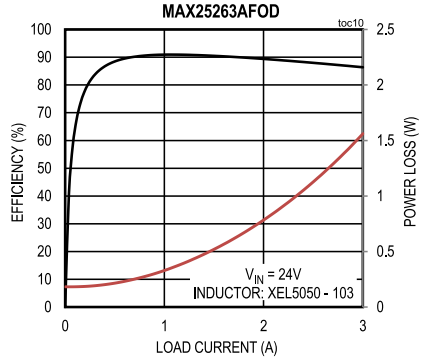


EFFICIENCY AND POWER LOSS
vs. LOAD CURRENT
MAX25263AFOC

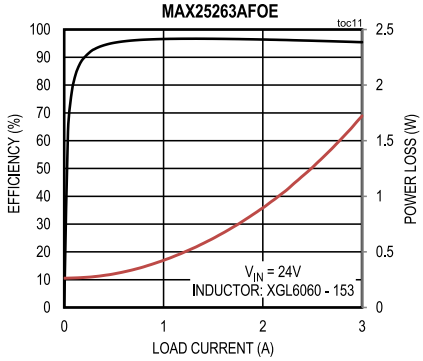


(V_{SUP} = 24V, T_A = +25°C, unless otherwise stated.)

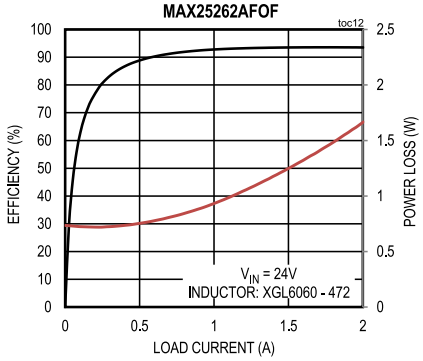
EFFICIENCY AND POWER LOSS vs. LOAD CURRENT MAX25263AFOD



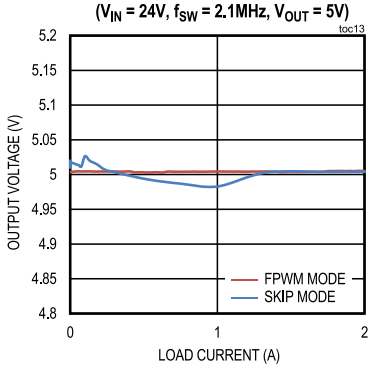
EFFICIENCY AND POWER LOSS vs. LOAD CURRENT MAX25263AFOE



EFFICIENCY AND POWER LOSS vs. LOAD CURRENT MAX25262AFOF



LOAD REGULATION (V_{IN} = 24V, f_{SW} = 2.1MHz, V_{OUT} = 5V)



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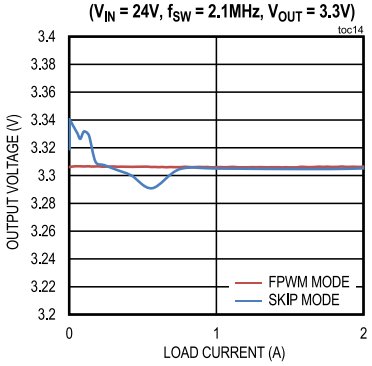
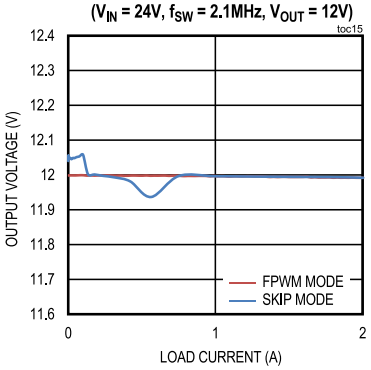
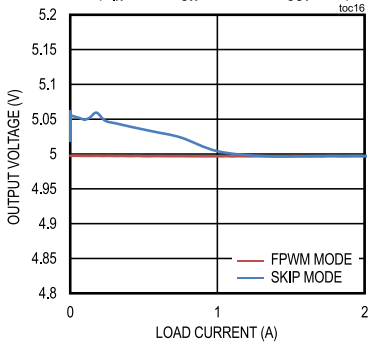


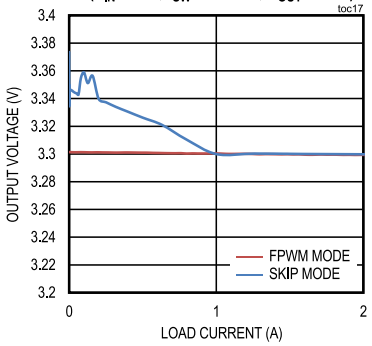
LOAD REGULATION (V_{IN} = 24V, f_{SW} = 2.1MHz, V_{OUT} = 12V)



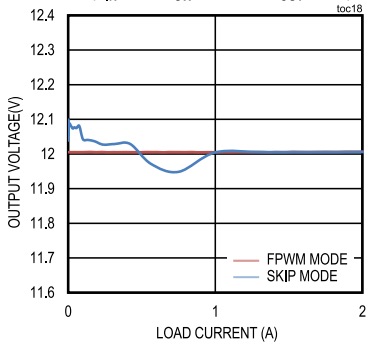
LOAD REGULATION (V_{IN} = 24V, f_{SW} = 400kHz, V_{OUT} = 5V)



LOAD REGULATION (V_{IN} = 24V, f_{SW} = 400kHz, V_{OUT} = 3.3V)

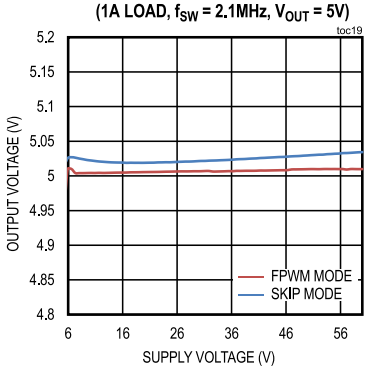


LOAD REGULATION (V_{IN} = 24V, f_{SW} = 400kHz, V_{OUT} = 12V)

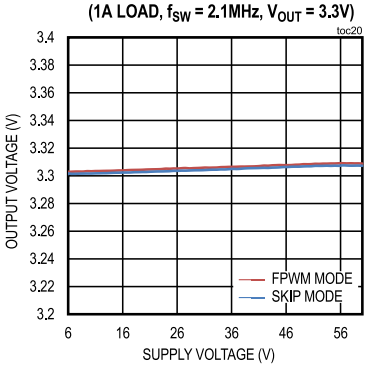


(V_{SUP} = 24V, T_A = +25°C, unless otherwise stated.)

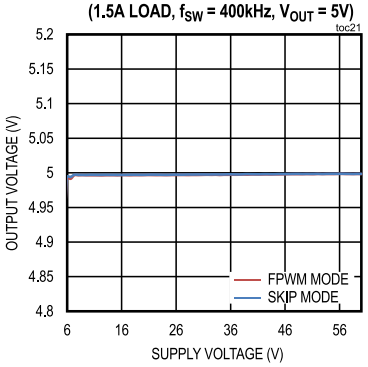
LINE REGULATION
(1A LOAD, f_{SW} = 2.1MHz, V_{OUT} = 5V)



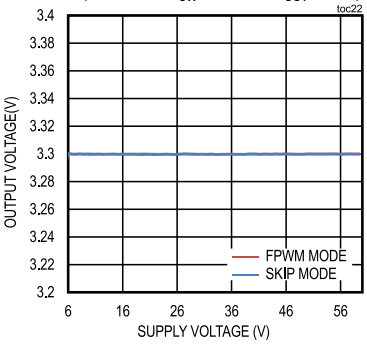
LINE REGULATION
(1A LOAD, f_{SW} = 2.1MHz, V_{OUT} = 3.3V)



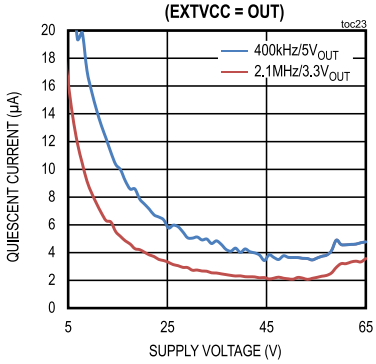
LINE REGULATION
(1.5A LOAD, f_{SW} = 400kHz, V_{OUT} = 5V)



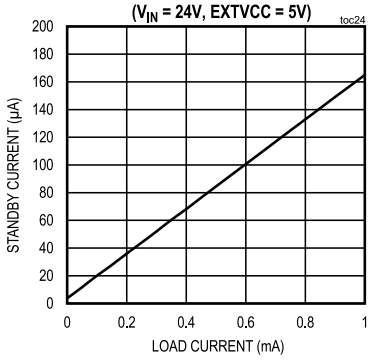
LINE REGULATION
(1.5A LOAD, f_{SW} = 400kHz, V_{OUT} = 3.3V)



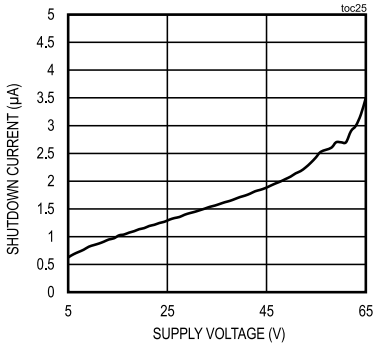
QUIESCENT CURRENT vs. SUPPLY VOLTAGE
(EXTVCC = OUT)



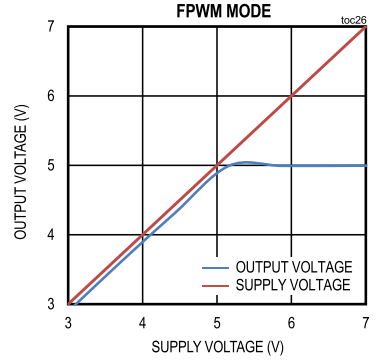
STANDBY CURRENT vs. LOAD CURRENT
MAX25262AFOB
(V_{IN} = 24V, EXTVCC = 5V)



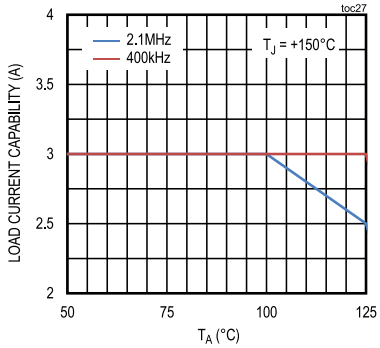
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE
MAX25263AFOC



OUTPUT VOLTAGE vs. SUPPLY VOLTAGE
MAX25263AFOC
FPWM MODE

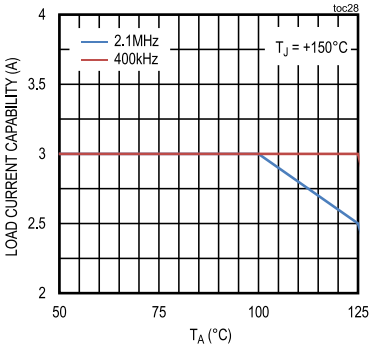


THERMAL DERATING CURVE
V_{SUP} = 24V, V_{OUT} = 3.3V

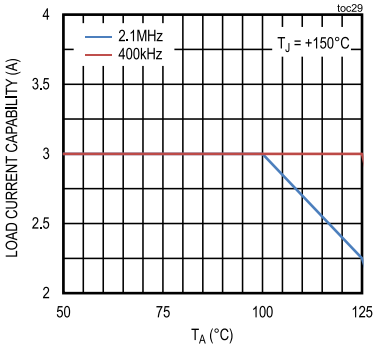


(V_{SUP} = 24V, T_A = +25°C, unless otherwise stated.)

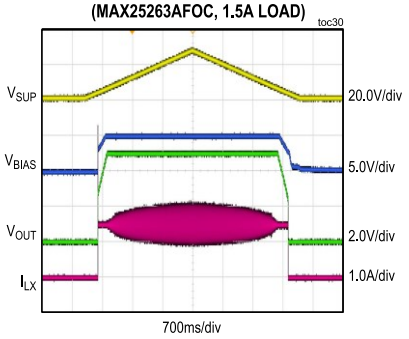
THERMAL DERATING CURVE
V_{SUP} = 24V, V_{OUT} = 5V



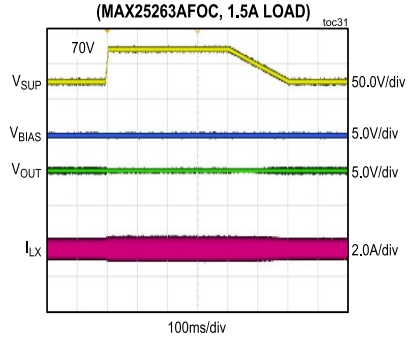
THERMAL DERATING CURVE
V_{SUP} = 24V, V_{OUT} = 12V



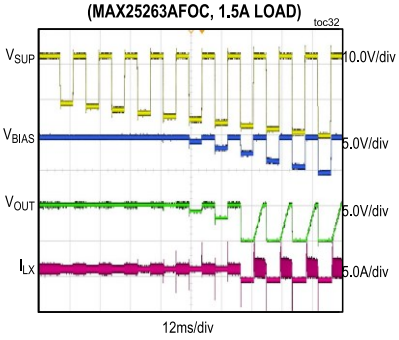
SLOW INPUT VOLTAGE RISING
(MAX25263AFOC, 1.5A LOAD)



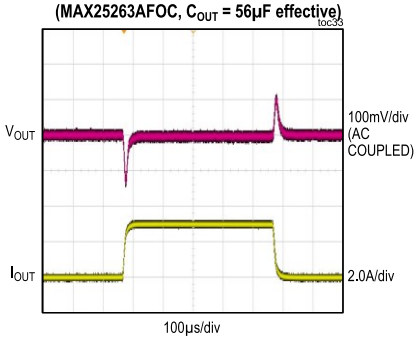
LOAD DUMP
(MAX25263AFOC, 1.5A LOAD)



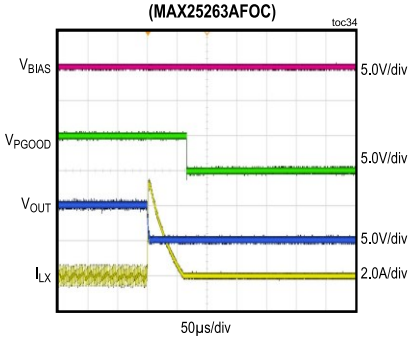
DIPS AND DROPS
(MAX25263AFOC, 1.5A LOAD)



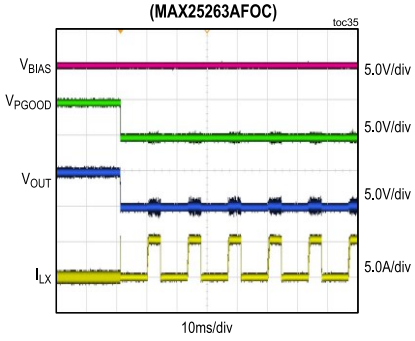
LOAD TRANSIENT
(MAX25263AFOC, C_{OUT} = 56µF effective)



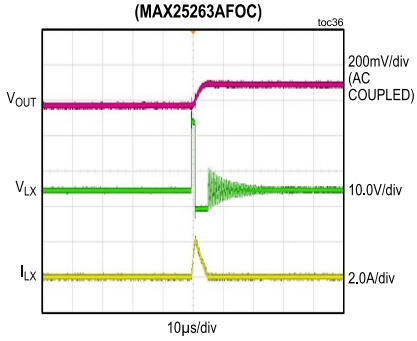
SHORT CIRCUIT RESPONSE
(MAX25263AFOC)



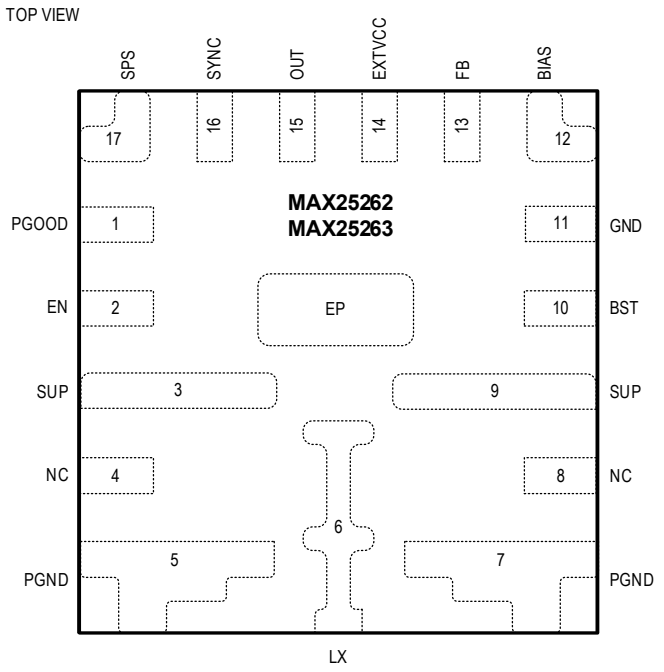
HIPCUP MODE
(MAX25263AFOC)



SKIP MODE NO LOAD OPERATION
(MAX25263AFOC)



Pin Configurations



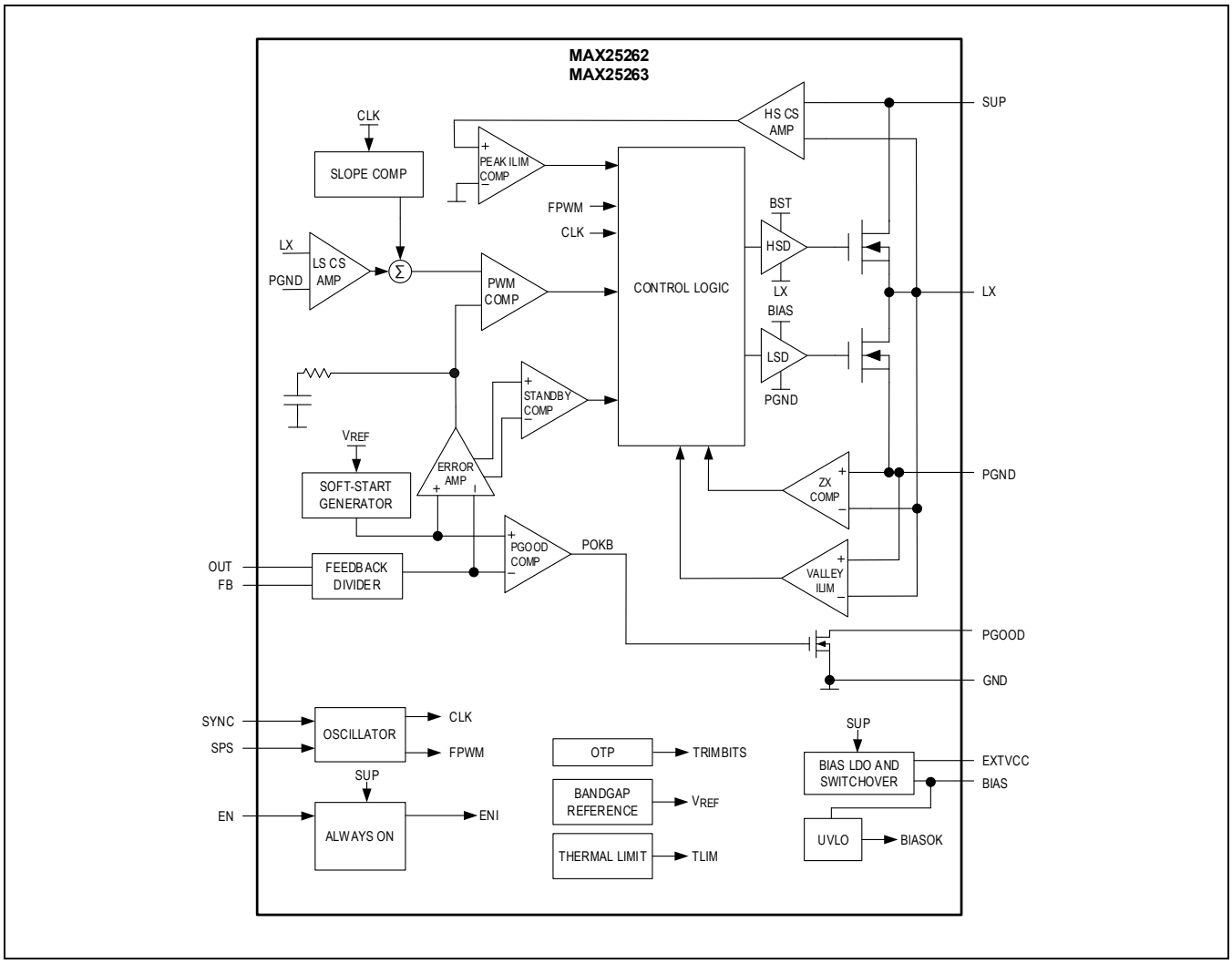
17 FC2QFN
3.5mm x 3.75mm

Pin Descriptions

PIN	NAME	FUNCTION
1	PGOOD	Open-Drain Output. Pull up PGOOD with an external resistor connected to a positive voltage lower than 5.5V. PGOOD is high impedance when OUT is in regulation.
2	EN	Supply (SUP) Voltage Tolerant, Active-High Digital Enable Input for the Converter.
3,9	SUP	Supply Input. Internal high-side supply powers the internal switch and LDO. Each SUP pin needs 2.2µF bypass capacitors and 0.1µF ceramic capacitors connected to them. The 0.1µF capacitor needs to be as close to the SUP pin as possible, followed by the 2.2µF capacitor.
4,8	NC	No Connect. Do not route through these pins.
5,7	PGND	Power Ground. Connect all PGND pins together.
6	LX	Inductor Connection. Connect LX to the switched side of the inductor.
10	BST	Bootstrap Capacitor Connection. Connect a ceramic capacitor of 0.1µF between BST and LX.
11	GND	Analog Ground
12	BIAS	Linear Regulator (LDO) Output. BIAS powers the internal circuitry. Bypass with a minimum of 2.2µF ceramic capacitor to ground.
13	FB	Feedback Input. For external feedback, connect a resistor-divider from OUT to FB to GND to set the output voltage. Connect FB to BIAS to select a fixed output voltage (P/N dependent).
14	EXTVCC	External V_{CC} Power and Switchover Comparator Input. Connect a voltage between 3.25V and 5.5V to EXTVCC to power the IC and bypass the internal bias LDO. Connect EXTVCC to ground if not used.
15	OUT	Output Sense Input. When using the internal preset feedback divider, FB is connected to BIAS, and the converter uses OUT to sense the output voltage.

16	SYNC	External Clock-Synchronization Input. Connect FSYNC to GND to enable Skip mode. Connect FSYNC to BIAS or an external clock to enable Forced-PWM mode. The SYNC input cannot exceed the BIAS voltage when driven externally.
17	SPS	Spread-Spectrum Enable Input. Connect to BIAS to enable spread spectrum. Connect to GND to disable spread spectrum.
—	EP	Exposed Pad. Connect to the input supply voltage along with pins 3 and 9.

Functional Diagram



Detailed Description

The MAX25262/MAX25263 are 2A and 3A current-mode step-down converters, respectively, with integrated high-side and low-side MOSFETs. The devices operate with 3.5V to 65V input voltages while using only 3.5µA (typ) quiescent current at no load. The switching frequency is fixed internally at 400kHz or 2.1MHz and can be synchronized to an external clock. The spread-spectrum option is pin selectable. The devices' output voltage is available as fixed 5V or 3.3V, or adjustable between 1V and 20V. The wide input voltage range, along with the ability to operate at a 98% duty cycle during undervoltage transients, makes these devices ideal for automotive applications. In light-load applications, a logic input (SYNC) allows the devices to operate either in skip mode for reduced current consumption, or in fixed-frequency FPWM mode to eliminate frequency variation and helps to minimize the EMI.

The IC comes in a small, 3.5mm x 3.75mm FCQFN package with pinout optimized to enhance EMI performance. The protection features include cycle-by-cycle current limit and thermal shutdown with automatic recovery.

Internal 5V BIAS LDO

An internal 5V BIAS LDO supplies the IC internal circuitry. The SUP pins supply the internal BIAS LDO. Bypass the BIAS pin with a minimum 2.2µF ceramic capacitor. To minimize the internal power dissipation, bypass the BIAS pin to an external 5V rail using the EXTVCC pin.

EXTVCC Switchover

The internal LDO can be bypassed by connecting an external 3.25V to 5.5V supply or the buck converter output to EXTVCC. With a valid supply connected to the EXTVCC pin, BIAS is internally switched to EXTVCC, and the internal LDO turns off. This configuration has two main advantages:

1. Reduces IC internal power dissipation.
2. Improves light-load efficiency as the internal supply current is scaled down proportionally to the duty cycle when the buck output is connected to EXTVCC.

If EXTVCC drops below 3V (typ), the internal regulator is enabled, and the BIAS switches back to internal LDO at 5V.

Connecting 5V to the EXTVCC pin is recommended for optimal efficiency since any voltage lower than 5V on EXTVCC causes the R_{DSON} of the FETs to increase, which increases the internal power dissipation.

Note: An output or external voltage higher than 5V should not be connected to EXTVCC since it can exceed the pin's Absolute Maximum rating and can permanently damage the IC.

Switching Frequency/External Synchronization

The MAX25262/MAX25263 feature an internal oscillator with 400kHz and 2.1MHz fixed frequency options. The 2.1MHz frequency operation optimizes the application for the smallest component size, at the cost of lower efficiency. The 400kHz frequency operation offers the best overall efficiency at the expense of component size and board space.

Apply an external clock to SYNC to enable the frequency synchronization. The MAX25262/MAX25263 use a phase-locked loop (PLL) to synchronize the internal oscillator to an external clock signal. The external SYNC signal should have a duty cycle of between 25% and 75%.

Spread-Spectrum Option

The ICs feature enhanced EMI performance with a spread-spectrum option. The spread-spectrum option is pin selectable using the SPS pin. To enable spread spectrum, pull the SPS pin high. When spread spectrum is enabled, the operating frequency is varied ±6% centered at the switching frequency (typ). The modulation signal is a triangular wave with a frequency of 4.5kHz at 2.1MHz and 0.8kHz at 400kHz (typ).

Internal spread spectrum is disabled if the devices are synchronized to an external clock. However, the devices do not filter the input clock on the SYNC pin and pass any modulation (including spread spectrum) present on the signal driving external clock.

SYNC Mode Selection

Drive FSYNC low to enable Skip mode. In Skip mode, the inductor current is not allowed to turn negative. Once inductor current reaches zero, the low-side MOSFET is turned off. The high-side FET is not turned on again until the FB voltage drops below the reference voltage. The high-side FET on-time is fixed but adaptable, determined by the V_{SUP}, V_{OUT}, and f_{SW}.

Driving the FSYNC high or external clock synchronization prevents the IC from entering the Skip mode by disabling the zero-crossing detection of the inductor current. This allows the inductor current to reverse at light load and during transients. Forced-PWM mode is useful in improving load-transient response and eliminating unknown frequency harmonics that can interfere with AM radio bands.

Overcurrent Protection

The MAX25262/MAX25263 have a cycle-by-cycle current limit and include a hiccup mode to prevent any damage from overcurrent or short-circuit on the power channel. When the inductor current continuously exceeds the current limit, the output voltage starts decreasing. If the IC detects the output voltage below 70% of the programmed regulation value, it turns off that channel. After waiting for about 10ms of hiccup time, the IC restarts that channel and soft-start initiates. If the overcurrent or short-circuit condition is removed, then the IC output voltage goes back to regulation or continues the hiccup cycle.

Soft-Start

When the IC is enabled, the soft-start circuitry gradually ramps up the reference voltage during soft-start time to reduce the input surge current during startup. Before soft-start begins, the BIAS voltage must exceed its UVLO threshold (3.1V, typ).

For the parts using an external divider or fixed internal output parts that have an output voltage higher or equal to 5V, the 2.1MHz parts have a 2.75ms ramp time, and the 400kHz parts have a 3.6ms ramp time.

For fixed output parts that have an output voltage lower than 5V, the soft-start ramp time can be calculated as follows:

$$t_{SS-RAMP}(ms) = \frac{V_{OUT}}{5} \times 2.75 \; for \; 2.1MHz$$

$$t_{SS-RAMP}(ms) = \frac{V_{OUT}}{5} \times 3.6 \; for \; 400kHz$$

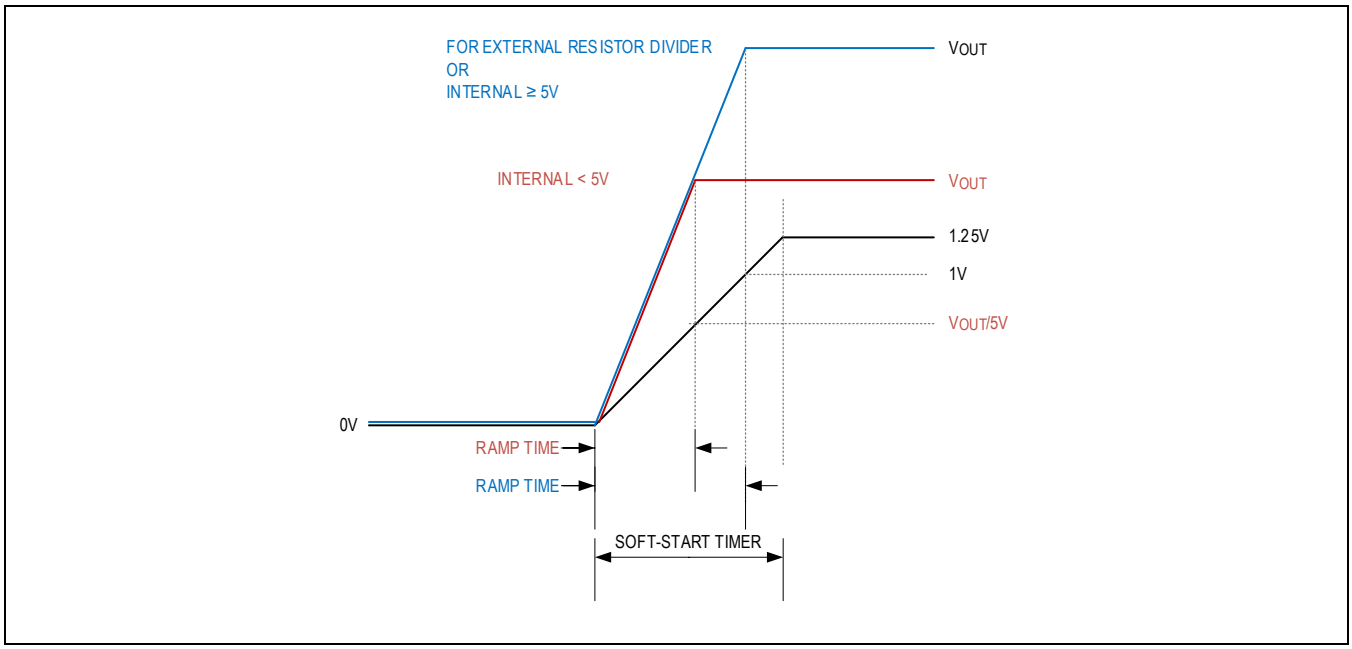


Figure 1. Soft-Start Ramp Times and Timer

Internal Gate Driver Supply

The integrated high-side and low-side FETs are driven by the BIAS. The IC will use the internal LDO at 5V for the FET gate drive. However, if the EXTVCC pin is connected to an appropriate voltage from an external source (or OUT), the internal LDO is turned off, and the gate drive voltage is equal to the voltage on EXTVCC.

An external +5V supply on EXTVCC is recommended since it reduces the power dissipation in the internal LDO. When driven at 5V, the FETs offer lesser R_{DSON} and this further reduces the power dissipation. Both of these factors contribute to an improved efficiency.

Thermal Overload Protection

The thermal overload protection limits total power dissipation in the ICs. When the junction temperature exceeds +170°C, an internal thermal sensor shuts down the ICs, allowing them to cool. The thermal sensor turns on the IC only after the junction temperature falls by 15°C (typ).

Undervoltage Lockout (UVLO)

The internal 5V BIAS LDO undervoltage-lockout (UVLO) circuitry inhibits switching if the BIAS voltage drops below its 2.65V (typ) UVLO falling threshold. Once the BIAS voltage rises above its UVLO rising threshold (3.1V, typ) and EN is pulled high, the IC starts switching and its output voltage begins soft-start.

Frequency Foldback

The frequency foldback is implemented in the buck converters only when operating at 2.1MHz. When the input voltage of a buck converter drops close to the output voltage, the converter runs at a maximum duty cycle of 98% (typ). To prevent the output voltage drifting out of regulation, frequency foldback is used to automatically reduce the switching frequency from 2.1MHz to 262.5kHz and maintain a high duty cycle of 98% (typ). The frequency foldback occurs when the input voltage drops below the threshold as calculated by $V_{SUP} = 1.4 \times V_{OUT}$. For the 3.3V part, this threshold is calculated by $V_{SUP} = 1.56 \times V_{OUT}$.

Power-Good Indicator (PGOOD)

PGOOD is an open-drain, power-good indicator that indicates the status of the output voltage regulation.

PGOOD is actively pulled low when the IC is disabled and during soft-start after enable, PGOOD is high impedance when the output voltage rises above 95% (typ) of the nominal regulation voltage. PGOOD is pulled low after the debounce time when the output voltage drops below 93% (typ) of the nominal regulation voltage or when output voltage rises above 108% (typ) of the nominal regulation voltage. PGOOD goes high after the assertion time expires once the output voltage falls to below 105.5% (typ) of the nominal regulation voltage. Connect a 20kΩ (typ) pull-up resistor from the PGOOD to the relevant logic rail in order to level-shift the signal.

Applications Information

Setting Output Voltage

As shown in *Figure 2*, connect FB to BIAS to enable a fixed buck output voltage set by a preset internal resistive divider connected between OUT and GND. To externally adjust the output voltage between 1V and 20V, connect a resistive voltage-divider from the converter output (OUT) to FB and then to AGND. Set R_{FB2} to any value between 10kΩ and 100kΩ and use the following equation to calculate the top-side (R_{FB1}):

$$R_{FB1} = R_{RB2} \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where, $V_{FB} = 1V\,(typ)$

For more information, see the *Electrical Characteristics* table.

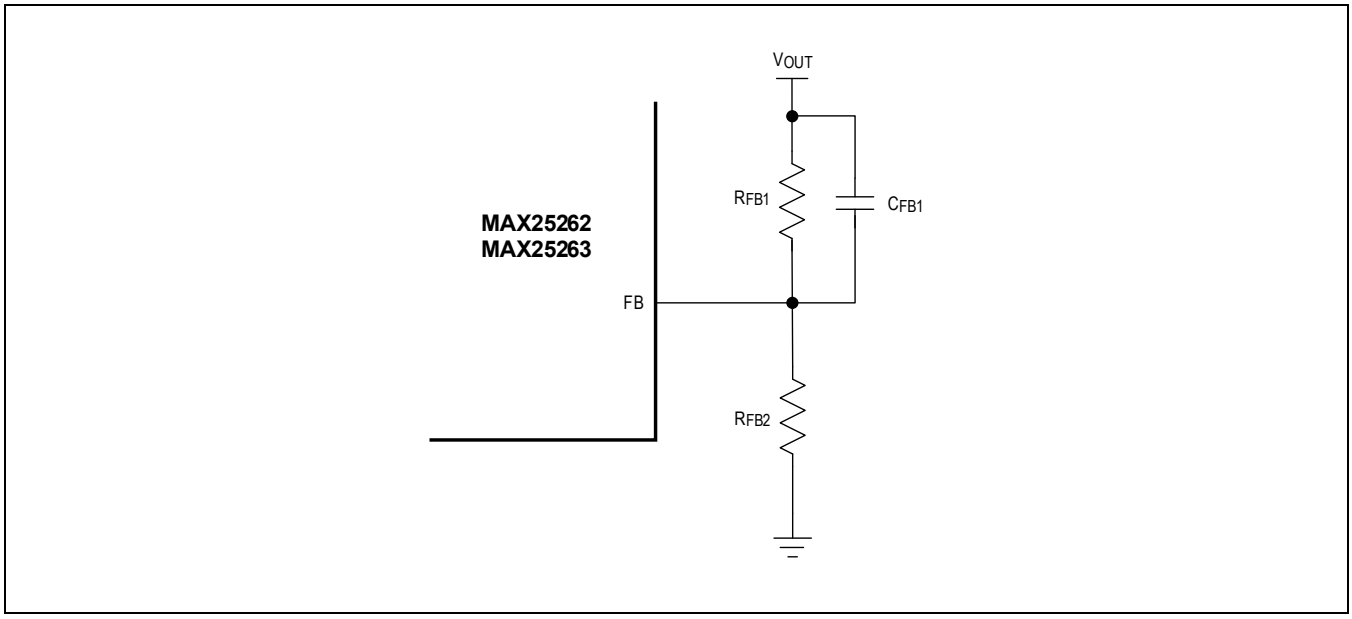


Figure 2. Setting Output Voltage

Note: For an output voltage higher that 12V, contact the factory.

Input Capacitor

A total capacitance of 4.7µF is recommended to ensure proper buck operation. Use of low-ESR ceramic capacitors is required. The IC package features two symmetrical SUP pins. Connect high frequency ceramic capacitors (e.g., 0.1µF 0603) from the SUP pins to ground. These capacitors need to be close to the IC pin and placed symmetrically to mitigate the EMI better. For more information, see the *PCB Layout Guidelines* section.

The input capacitor RMS current requirement (I_{RMS}) can be calculated as follows:

$$I_{RMS} = I_{LOAD(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{SUP} - V_{OUT})}}{V_{SUP}}$$

The I_{RMS} has a maximum value when the input voltage equals twice the output voltage:

$V_{SUP} = 2 \times V_{OUT}$

Therefore,

$I_{RMS} = \frac{I_{LOAD(MAX)}}{2}$

Choose an input capacitor with a temperature rise of less than 10°C at the calculated input I_{RMS} for longevity and reliability.

The input-voltage ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR} that peaks at the end of an on-cycle. Calculate the input capacitance and equivalent series resistance (ESR) required for a specific ripple by using the following equations:

$$ESR[\Omega] = \frac{\Delta V_{ESR}}{\left(I_{LOAD(MAX)} + \frac{\Delta I_{P-P}}{2}\right)}$$

$$C_{IN}[\mu F] = \frac{I_{LOAD(MAX)} \times \frac{V_{OUT}}{V_{IN}}}{\Delta V_Q \times f_{SW}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and,

$I_{LOAD(MAX)}$ = Maximum output current in A

ΔI_{P-P} = Peak-to-peak inductor current in A

f_{SW} = Switching frequency in MHz

L = Inductor value in µH

Inductor Selection

The MAX25262/MAX25263 are offered in two switching frequency options: 2.1MHz and 400kHz. The inductor selection is based on the compromise between the size, efficiency, control-loop bandwidth, and stability of the converter.

The key parameters for inductor selection are inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). The nominal required inductance is calculated as:

$$L_{nom} = \frac{(V_{IN} - V_{OUT}) \times D}{f_{SW} \times I_{OUT} \times LIR}$$

where LIR is the ratio of the inductor peak-to-peak ripple current to DC average current, and 0.35 is a typical value to use.

The inductance value also depends on the compensation design, which in this case is done internally. Hence, a value of inductance for each application is recommended to optimize the size of the solution, efficiency, and compensation design. For the recommended inductors, see *Table 1* for optimum transient response and the highest efficiency. The inductor's saturation current rating must meet or exceed the LX current limit.

A large inductor reduces the ripple; however, it increases the size and cost of the solution and slows the response.

Note: If a smaller ripple is needed, contact the factory for an optimized design.

Table 1. Recommended External Component Selection

FIXED OUTPUT				
FREQUENCY (kHz)	2100		400	
V_{OUT} (V)	3.3/5	12	3.3/5	12
MIN C_{OUT} (µF)	24	12.6	56	29.4
TYP C_{OUT} (µF)	32	16.8	64	33.6
L (µH)	3.3	4.7	10	15

EXTERNAL RESISTOR-DIVIDER					
ADJUSTED V_{OUT} (V)	**FREQUENCY (kHz)**	**L (µH)**	**MIN C_{OUT} (µF)**	**TYP C_{OUT} (µF)**	**C_{FF} (pF)**
1 to 2	2100	1	80	100	15
	400	6.8	240	260	100
2 to 4	2100	3.3	60	80	15
	400	10	160	180	82
4 to 8	2100	3.3	20	40	10
	400	15	60	80	20
8 to 12	2100	4.7	10	20	6.2
	400	15	20	30	15

Output Capacitor

The ESR of the capacitor and its derating at the nominal output voltage are the deterministic factors in selecting the output capacitor. The ESR and voltage derating are relative to the physical size of the capacitor. The capacitance is relative to the physical size of the capacitor as well as its chemical composition.

The total capacitance needed at the output is determined by the value needed to prevent V_{SAG} and V_{SOAR}. Generally if the capacitor size is calculated to meet the overshoot requirement, undershoot requirement is also addressed by the same value.

The total voltage sag (V_{SAG}) can be calculated as follows:

$$V_{SAG} = \frac{L \times \left(\Delta I_{LOAD(MAX)}\right)^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})} + \frac{\Delta I_{LOAD(MAX)} \times (t - \Delta t)}{C_{OUT}}$$

The amount of overshoot (V_{SOAR}) during a full-load to no-load transient due to stored inductor energy can be calculated as follows:

$$V_{SOAR} = \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 \times L}{2 \times C_{OUT} \times V_{OUT}}$$

For the recommended output capacitance, see *Table 1*.

ESR Considerations

The output capacitor should have low ESR to meet the output ripple and load-transient requirements. When a large capacitor with low ESR is used, the ESR of the filter capacitor dominates the output voltage ripple:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

PCB Layout Guidelines

Careful PCB layout is critical to achieving low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. For a good PCB layout, see *Figure 3* and the following guidelines:

- Use the correct footprint for the IC and place as many copper planes as possible under the IC footprint to ensure efficient heat transfer.
- Place the ceramic input bypass capacitors, C_{BP} and C_{IN}, as close as possible to the SUP and PGND pins on both sides of the IC. Use low impedance connections (no vias or other discontinuities) between the capacitors and IC pins. C_{BP} should be located closest to the IC and should have very good high-frequency performance (small package size + high capacitance). Use flexible terminations or other technologies instead of series capacitors for these functions if failure modes are a concern. This provides the best EMI rejection and minimizes the internal noise of the device, which can degrade performance.
- Place the inductor (L), output capacitors (C_{OUT}), boost capacitor (C_{BST}), and BIAS capacitor (C_B) in such a way as to minimize the area enclosed by the current loops. Place the inductor (L) as close as possible to the IC LX pin and minimize the area of the LX node. Place the output capacitors (C_{OUT}) near the inductor such that the ground side of C_{OUT} is near the C_{IN} ground connection to minimize the current in the loop area. Place the BIAS capacitor (C_B) next to the BIAS pin.
- Use a contiguous copper GND plane on the layer next to the IC to shield the entire circuit. GND should also be poured around the entire circuit on the top side. Ensure that all heat-dissipating components have adequate connections to the copper for cooling. Use multiple vias to interconnect GND planes/areas for low impedance and maximum heat dissipation. Place vias on the GND pin and at the GND terminals of the IC and input/output/bypass capacitors.
  Note: Do not separate or isolate PGND and GND connections with separate planes or areas.
- Place the feedback resistor-divider (if used) near the IC and route the feedback and OUT connections away from the inductor, LX node, and other noisy signals.

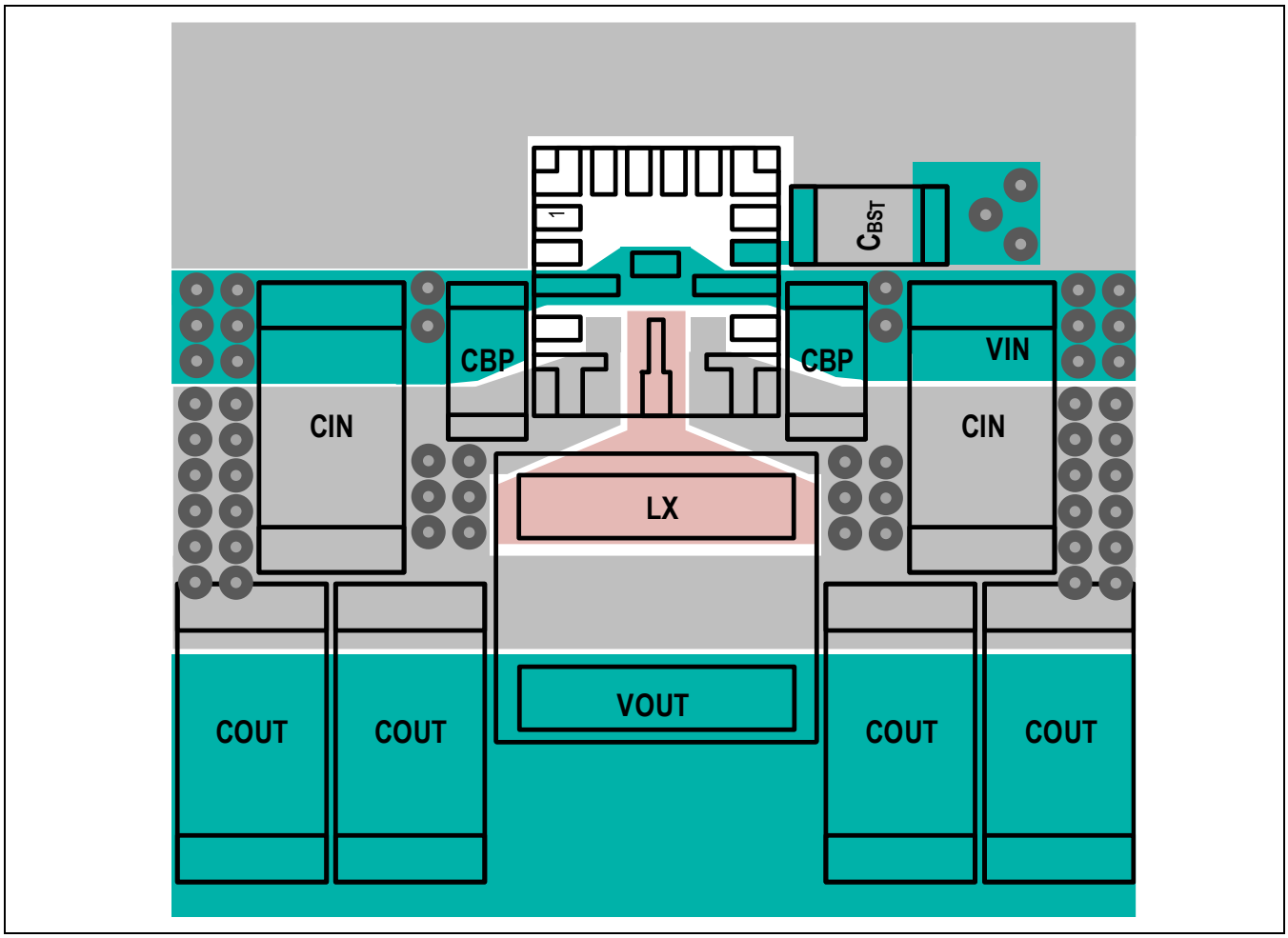
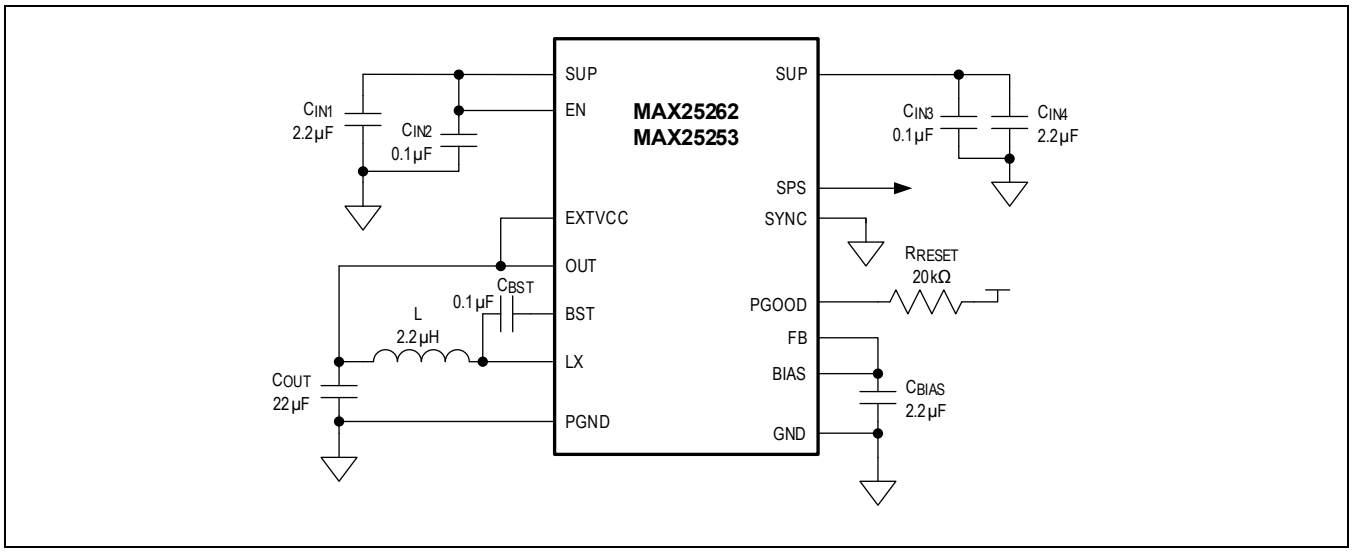


Figure 3. Simplified Layout Example

Typical Application Circuits



Ordering Information

PART NUMBER	DESCRIPTION	I_{OUT} (A)	FREQUENCY (kHz)
MAX25262AFOA/VY+	Fixed 5V output or 1V to 12V external resistor-divider	2	2100
MAX25262AFOB/VY+	Fixed 3.3V output or 1V to 12V external resistor-divider	2	2100
MAX25262AFOF/VY+	Fixed 12V output or 1V to 12V external resistor-divider	2	2100
MAX25263AFOA/VY+	Fixed 5V output or 1V to 12V external resistor-divider	3**	2100
MAX25263AFOB/VY+	Fixed 3.3V output or 1V to 12V external resistor-divider	3**	2100
MAX25263AFOC/VY+	Fixed 5V output or 1V to 12V external resistor-divider	3	400
MAX25263AFOE/VY+	Fixed 12V output or 1V to 12V external resistor-divider	3	400
MAX25263AFOF/VY+	Fixed 12V output or 1V to 12V external resistor-divider	3**	2100

Contact factory for variants with different options, including an output voltage higher than 12V.

/VY+ Denotes AEC-Q100 automotive-qualified parts in a side-wettable package.

+ Indicates a lead(Pb)-free/RoHS-compliant package.

***MAX25263AFOA/VY+, MAX25263AFOB/VY+, and MAX25263AFOF/VY+ support 3A peak currents for transients up to 200ms. Maximum continuous current is 2A.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/22	Release for market intro	—
1	4/23	Updated Electrical Characteristics table, Typical Operating Characteristics, Pin Descriptions, Detailed Description, Applications Information, and Ordering Information	4, 7, 8, 9, 10, 12–19, 21
2	8/23	Updated Ordering Information	21
3	12/23	Updated Ordering Information	21
4	2/24	Updated Ordering Information	21