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MAX31342

Low-Current, Real-Time Clock with I²C Interface

General Description

The MAX31342 low-current, real-time clock (RTC) is a time-keeping device that provides an extremely low time-keeping current, permitting longer life from a power supply. The MAX31342 supports 6pF high-ESR crystals, which broaden the pool of usable crystals for the devices. This device is accessed through an I²C serial interface. An integrated power-on reset function ensures deterministic default register status upon power-up.

Other features include two time-of-day alarms, interrupt outputs, a programmable square-wave output, and a serial bus timeout mechanism. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in 24-hour mode. The MAX31342 also includes an input for synchronization. When a reference clock (e.g., 32kHz, 50Hz/60Hz Power Line, GPS 1PPS) is present at the CLKIN pin and the enable external clock input bit (ECLK) is set to 1, the MAX31342 RTC is frequency-locked to the external clock and the clock accuracy is determined by the external source.

The device is available in lead(Pb)-free/RoHS-compliant, 8-pin wafer-level package (WLP) 1mm x 2mm package with 0.5mm pitch. The device supports the -40°C to +85°C extended temperature range.

Applications

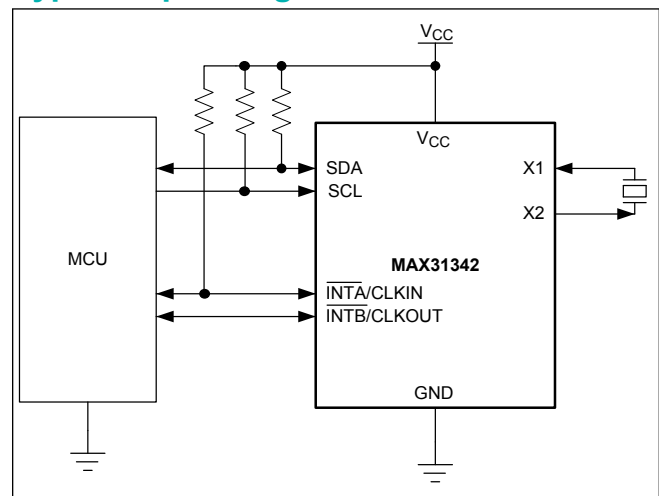
- Medical
- Wearables
- Point-of-Sale (POS)
- Telematics
- Portable Instruments
- Portable Audio
- Power Meters

Benefits and Features

- Increases Battery Life
 - 150nA Timekeeping Current
 - Wide Range of External Crystals with $C_L = 6\text{pF}$ and ESR up to 100k Ω for Minimal Current Draw
- Provides Flexible Configurability
 - Programmable Square Wave Output for Clock Monitoring
- Saves Board Space
 - Integrated Load Capacitors for Crystal Oscillator
 - 1mm x 2mm, 8-Bump WLP with 0.5mm Pitch
- Value Add Features for Ease of Use
 - +1.6V to +3.6V Operating Voltage Range
 - Countdown Timer with Repeat Function
- Integrated Protection
 - Power-On Reset for Default Configuration
 - Lockup-Free Operation with Bus Timeout

[Ordering Information](#) appears at end of data sheet.

Typical Operating Circuit



Absolute Maximum Ratings

| | | | |
|---|-----------------|-----------------------------|--|
| Voltage Range on Any Pin Relative to Ground | -0.3V to +6V | Soldering Temperature | See the IPC/JEDEC J-STD-020A Specification |
| Operating Temperature Range | -40°C to +85°C | | |
| Junction Temperature | +150°C | | |
| Storage Temperature Range | -55°C to +150°C | | |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

8 WLP

| | |
|---|--|
| Package Code | W80D1-1 |
| Outline Number | 21-100291 |
| Land Pattern Number | Refer to Application Note 1891 |
| Thermal Resistance, Four-Layer Board: | |
| Junction-to-Ambient (θ_{JA}) | 49°C/W |
| Junction-to-Case Thermal Resistance (θ_{JC}) | N/A |

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{CC} = +1.6V to +3.6V, typical values at V_{CC} = +3.0V, unless otherwise noted. Limits are 100% tested at T_A = +25°C, unless otherwise noted. Limits over the operating temperature range, and relevant supply voltage range, are guaranteed by design and characterization (Note 1).)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|----------------------|--|-----------------------|------|------------------------|-------|
| DC CHARACTERISTICS | | | | | | |
| Operating Voltage Range | V _{CC} | Full operation (Note 2) | 1.6 | | 3.6 | V |
| Minimum Timekeeping Voltage | V _{CC} TMIN | T _A = +25°C (Note 2) (Note 3) | | 1 | | V |
| Timekeeping Current: CLKIN = GND or CLKIN = V _{CC} (Note 3) | I _{CC} T | V _{CC} = +1.6V | | 130 | 300 | nA |
| | | V _{CC} = +3.0V | | 150 | 330 | |
| Maximum Supply Voltage Rise Slew Rate | T _{VCCR} | | | 3 | | V/μs |
| Data Retention Current (Oscillator Stopped and I ² C Inactive) | I _{BATDR} | T _A = +25°C | | 6 | | nA |
| ESD Protection (All Pins) | | Human Body Model (HBM) | | ±2.5 | | kV |
| LOGIC INPUTS and OUTPUTS | | | | | | |
| Logic 1 Input | V _{IH} | (Note 2) | 0.7 x V _{CC} | | V _{CC} + 0.3 | V |
| Logic 0 Input | V _{IL} | (Note 2) | -0.3 | | +0.3 x V _{CC} | V |
| Input Leakage (SCL, CLKIN/INTA) | I _{IL} | Input clock enabled | -0.1 | | +0.1 | μA |
| Output Leakage (CLKIN/INTA, CLKOUT/INTB) | I _O | Input clock disabled | -1.0 | | +1.0 | μA |
| Output Logic 1 V _{OH} = +1.0V (CLKOUT/INTB) | I _{OH} | V _{CC} ≥ 1.6V | -1.0 | | | mA |
| Output Logic 0, V _{OL} = +0.4V (SDA, CLKIN/INTA, CLKOUT/INTB) | I _{OL} | V _{CC} ≥ 1.6V | 2.0 | | | mA |
| I²C INTERFACE | | | | | | |
| SCL Clock Frequency | f _{SCL} | (Note 4) (Note 10) | 10 | | 400 | kHz |
| Bus Free Time Between a STOP and START Condition | t _{BUF} | | 1.3 | | | μs |
| Hold Time (Repeated) START Condition | t _{HD:STA} | (Note 5) | 0.6 | | | μs |
| Low Period of SCL Clock | t _{LOW} | | 1.3 | | | μs |
| High Period of SCL Clock | t _{HIGH} | | 0.6 | | | μs |
| Data Hold Time | t _{HD:DAT} | (Note 6) (Note 7) | 0 | | 0.9 | μs |

Electrical Characteristics (continued)

($V_{CC} = +1.6V$ to $+3.6V$, typical values at $V_{CC} = +3.0V$, unless otherwise noted. Limits are 100% tested at $T_A = +25^{\circ}C$, unless otherwise noted. Limits over the operating temperature range, and relevant supply voltage range, are guaranteed by design and characterization (Note 1).)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------|--------------------------|-----|-------------------|-----|---------|
| Data Setup Time | $t_{SU:DAT}$ | $V_{CC} = 3V$. (Note 8) | 100 | | | ns |
| Setup Time for a Repeated, START Condition | $t_{SU:STA}$ | | 0.6 | | | μs |
| Minimum Rise Time of Both SDA and SCL Signals | t_R | (Note 9) | | 20 + 0.1 C_B | | ns |
| Maximum Rise Time of Both SDA and SCL Signals | t_R | | | 300 | | ns |
| Minimum Fall Time for Both SDA and SCL Signals | t_F | (Note 9) | | 20 + 0.1 C_B | | ns |
| Maximum Fall Time for Both SDA and SCL Signals | t_F | | | 300 | | ns |
| Setup Time for STOP Condition | $t_{SU:STO}$ | | 0.6 | | | μs |
| Maximum Capacitive Load for Each Bus Line | C_B | (Note 9) | | 400 | | pF |
| I/O Capacitance | $C_{I/O}$ | | | 10 | | pF |
| SCL Spike Suppression | t_{SP} | | | 30 | | ns |
| Oscillator Stop Flag (OSF) Delay | t_{OSF} | (Note 11) | | 35 | 100 | ms |
| Timeout Interval | $t_{TIMEOUT}$ | (Note 12) | 25 | | 35 | ms |

Note 1: Limits at $-40^{\circ}C$ and $85^{\circ}C$ are guaranteed by design; not production tested.

Note 2: Voltage referenced to ground.

Note 3: Specified with I²C bus inactive. Oscillator operational.

Note 4: The minimum SCL clock frequency is limited by the bus timeout feature, which resets the serial bus interface if SCL is held low for $t_{TIMEOUT}$.

Note 5: After this period, the first clock pulse is generated.

Note 6: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 7: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 8: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000 + 250 = 1250ns$ before the SCL line is released.

Note 9: C_B is the total capacitance of one bus line, including all connected devices, in pF.

Note 10: Guaranteed by design; not 100% production tested.

Note 11: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over the voltage range of $2.4V \leq V_{CC} \leq V_{CCMAX}$.

Note 12: The MAX31342 can detect the SCL clock low signal longer than the $t_{TIMEOUT}$. When this occurs, the device I²C interface is in reset state. Once the device detects a START condition where SCL is held low shorter than $t_{TIMEOUT}$, it exits out of reset and SDA output is released. The oscillator must be running for this function to work.

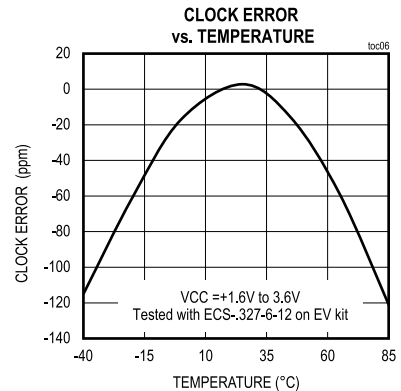
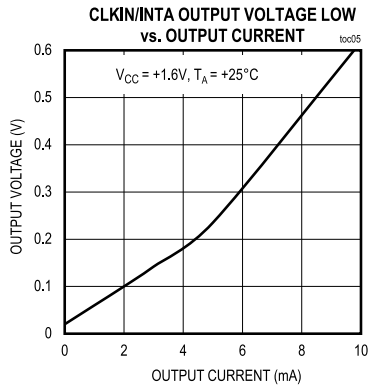
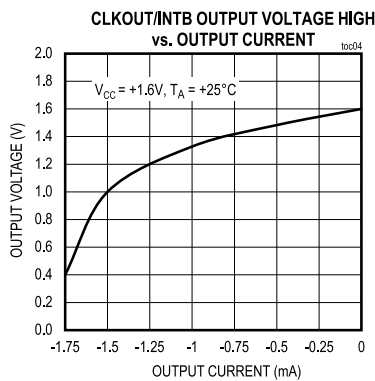
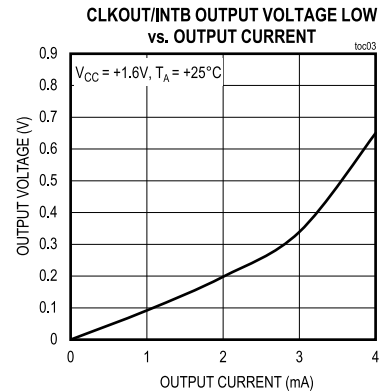
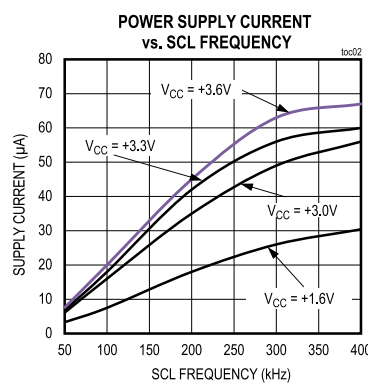
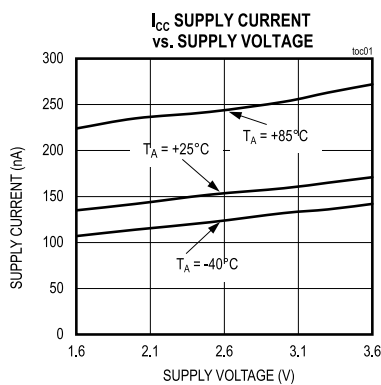
Electrical Characteristics—Crystal Parameters

(V_{CC} = +1.6V to +3.6V, typical values at V_{CC} = +3.0V, AIN threshold voltage at V_{TH1} = 1.4V, unless otherwise noted. Limits are 100% tested at T_A = +25°C. Note 1.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|----------------|--|-----|--------|-----|-------|
| Nominal Frequency | f _O | Recommended value for external crystal | | 32.768 | | kHz |
| Maximum Series Resistance | ESR | Recommended value for external crystal | | 100 | | kΩ |
| Load Capacitance | C _L | | | 6 | | pF |

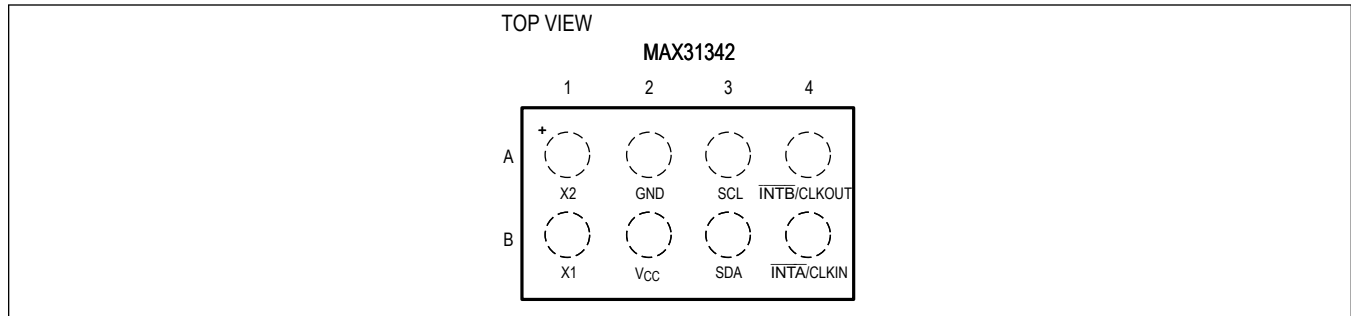
Typical Operating Characteristics

(V_{CC} = 3.0V; T_A = +25°C, unless noted otherwise.)



Pin Configuration

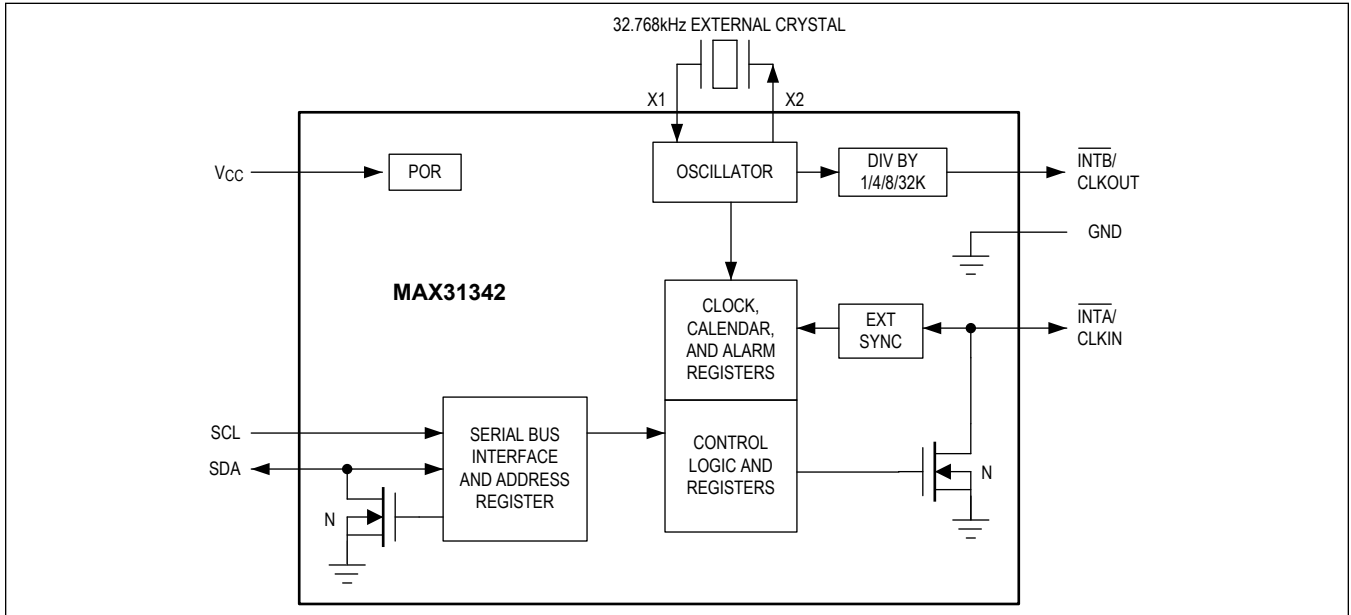
8 WLP



Pin Description

| PIN | NAME | FUNCTION |
|-----|-----------------|--|
| A1 | X2 | Second Crystal Input for an External 32.768kHz Crystal with 6pF Load Capacitance. |
| A2 | GND | Ground |
| A3 | SCL | Serial-Clock Input. SCL is used to synchronize data movement on the serial interface. The SCL pin is open-drain and requires an external pullup resistor. |
| A4 | INTB/CLKOUT | Square-Wave Clock or Active-Low Interrupt Output. This pin is used to output a programmable square wave or an alarm interrupt signal. This is a CMOS push-pull output and does not require an external pullup resistor. If not used, this pin can be left unconnected. See Table 1 for details. |
| B1 | X1 | First Crystal Input for an External 32.768kHz Crystal with 6pF Load Capacitance. |
| B2 | V _{CC} | Supply Voltage |
| B3 | SDA | Serial-Data Input/Output. SDA is the input/output pin for the I ² C serial interface. The SDA pin is open-drain and requires an external pullup resistor. |
| B4 | INTA/CLKIN | Clock Input/Active-Low Interrupt Output. This I/O pin is used to output an alarm interrupt or accept an external clock input to drive the RTC counter. In the output mode, this is an open-drain and requires an external pullup resistor. If not used, connect this pin to ground. See Table 1 for details. |

Functional Diagram



Detailed Description

Introduction

The MAX31342 low-current RTC are timekeeping devices that consume an extremely low timekeeping current, permitting longer battery life. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for each month with fewer than 31 days, including corrections for leap year through 2199. The clock operates in 24-hour mode.

The MAX31342 is accessed through an I²C serial interface. An integrated power-on reset function ensures deterministic default register status upon power-up. However, a soft reset command should be issued after a brownout or a short blackout to properly reset the MAX31342. Other features include two time-of-day alarms, two interrupts, a programmable square-wave output, and a bus timeout mechanism that resets the I²C bus if it remains inactive for a minimum of t_{TIMEOUT} .

The MAX31342 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. The device supports a high-ESR crystal, which broadens the pool of usable crystals for the device. The MAX31342 uses a 6pF crystal, which decreases oscillator current draw. The MAX31342 also accepts an external clock reference for synchronization. The external clock can be a 32.768kHz, 50Hz, 60Hz, or 1Hz source. When the enable oscillator bit (OSCONZ) is a 0, the MAX31342 uses the oscillator for timekeeping. If the enable external clock input bit (ECLK) is set to 1, the time base derived from the oscillator is compared to the 1Hz signal that is derived from the CLKIN signal. The conditioned signal drives the RTC time and date counters. When the external clock is lost or when the frequency differs more than $\pm 0.8\%$ from the crystal frequency, the LOS flag is asserted.

The time and calendar information is obtained by reading the appropriate register bytes after the Rd_RTC bit is set. The Register Map shows the RTC registers. The time and calendar data are set or initialized by writing the appropriate register bytes followed by a SET_RTC bit of Config_reg2 register transition from 0 to 1. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format. The device runs in 24-hour mode. The century bit (bit 7 of the Month register) is toggled when the Years register overflows from 99 to 00. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation. When reading or writing the time and date registers, secondary buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the secondary buffers are synchronized to the internal registers on any I²C START and when the register pointer rolls over to zero. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read.

The MAX31342 is available in lead (Pb)-free/RoHS-compliant, 8-bump WLP with 0.5mm pitch, and supports the -40°C to $+85^{\circ}\text{C}$ extended temperature range.

I²C Interface

Address and data are transferred serially through an I²C serial interface. The I²C interface is guaranteed to operate when V_{CC} is between 1.6V and 3.6V. The I²C interface is accessible whenever V_{CC} is at a valid level. To prevent invalid device operation, the I²C interface should not be accessed when V_{CC} is below 1.6V. The slave address is defined as the 7 most significant bits (MSBs) sent by the master after a START condition. The address is 0xD2 (left justified with LSB set to 0). The eighth bit is used to define a write or read operation.

If a microcontroller connected to the MAX31342 resets during I²C communications, it is possible that the microcontroller and the MAX31342 could become unsynchronized. When the microcontroller resets, the MAX31342 I²C interface can be placed into a known state by holding SCL low for t_{TIMEOUT} . Doing so limits the minimum frequency at which the I²C interface can be operated. If data is being written to the device when the interface timeout is exceeded, prior to the acknowledge, the incomplete byte of data is not written.

Burst read/write allows the controller to read/write multiple consecutive bytes from a device. It is initiated in the same manner as the byte read/write operation, but instead of terminating the read/write cycle after the first data byte is transferred, the controller can read/write to the whole register array. In burst write operation, after the receipt of each

byte, the device responds with an acknowledge, and the address is internally incremented by one. When the address pointer reaches the end of the register address list, it goes back to the first register address. In burst read mode, the controller responds with an acknowledge, indicating it waits for additional data. The device continues to output data for each acknowledge received. The controller terminates the read operation by not responding with an acknowledge and issuing a STOP condition.

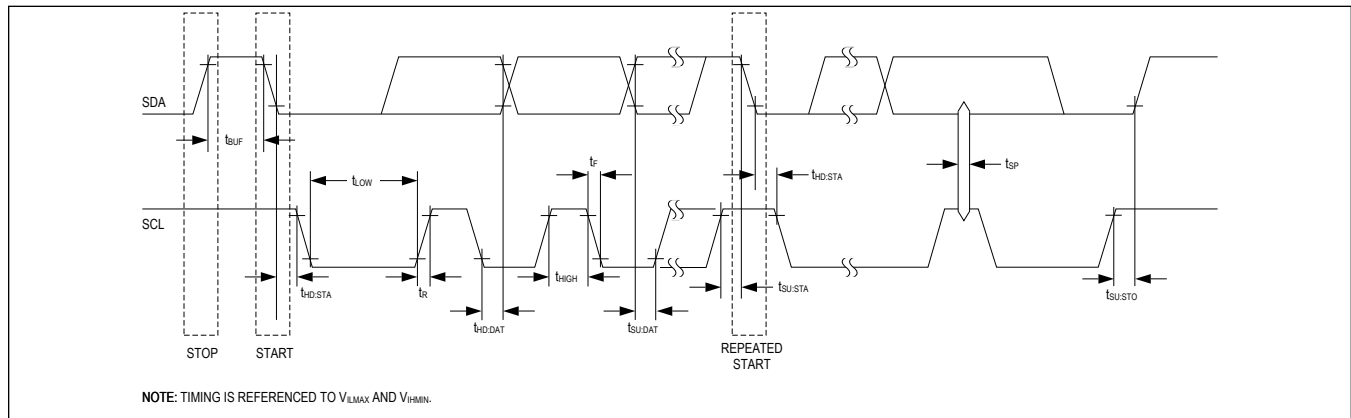


Figure 1. Data Transfer on I²C Serial Bus

RTC Startup Process

Use the following procedure to enable RTC and set time.

1. Exit software reset and enable oscillator (SWRSTN = 1 and OSCONZ = 0) in register Config_reg1 (0x00).
2. Write RTC time to registers 0x06-0x0C.
3. Write SET_RTC = 1 in register Config_reg2 (0x01).
4. Wait 10ms.
5. Write SET_RTC = 0 in register Config_reg2 (0x01).

Oscillator Circuit

The MAX31342 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. The MAX31342 includes integrated capacitive loading for a 6pF C_L crystal. See the [Electrical Characteristics](#) table for the external crystal parameters. The startup time of the oscillator circuit is usually less than 1 second when using a crystal with the specified characteristics. An additional 4s are needed for the chip to reach stable, low-current operation.

Clock Accuracy

When running from the internal oscillator, the accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. [Figure 2](#) and [Figure 3](#) show a typical PCB layout for isolation of the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations with Maxim Real-Time Clocks* on Maxim's website for detailed information.

Layout Example



Figure 2. Top Layer



Figure 3. Bottom Layer

Minimizing the Clock Synchronization Delay

When external clock input is disabled (ECLK = 0), the countdown chain is driven by internal high-speed clock. The output of the countdown chain is the 1Hz clock that drives the RTC logic. By default, Clk_sync_reg (58h) = 0x02 and the countdown chain is reset whenever the Set_RTC transitions from 0 to 1. That means after Set_RTC becomes 1, RTC registers (06h – 0Ch) will transfer to internal RTC counter and the next RTC update will happen 1 second later with less than 10ms synchronization delay. If external clock (50Hz/60Hz/32KHz) is used, set Clk_sync_reg = 0x01 to minimize the synchronization delay to less than 100ms. If external 1Hz clock is used, set Clk_sync_reg = 0x00. The maximum synchronization delay will be 1s.

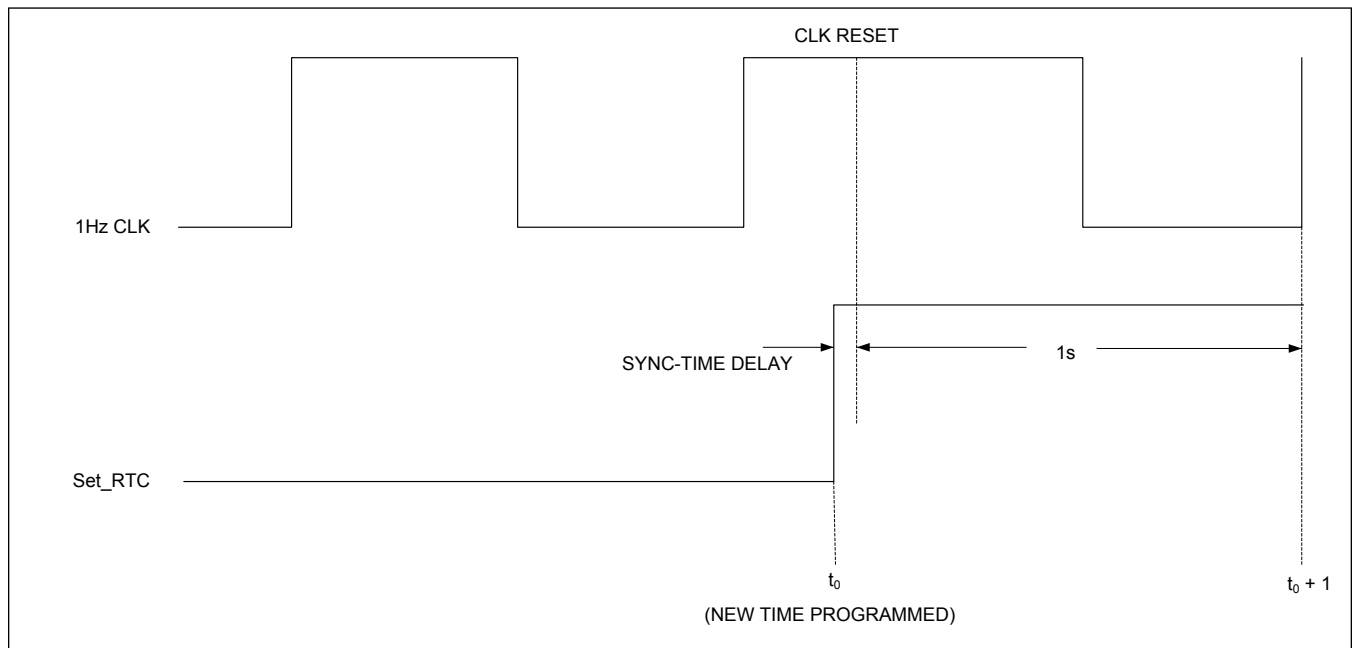


Figure 4. Clock Synchronization Delay

Interrupts Status and Output

When an interrupt is asserted, the interrupt output pin changes from high to low, and all its corresponding registers will update after 2ms. That includes the Int_status_reg(05h). The Interrupt status bit and output can be cleared by reading the Int_status_reg. Pin INTB/CLKOUT corresponds to Alarm2, while pin INTA/CLKIN corresponds to Alarm1, and D1 and AIN interrupts. Interrupt mode can be set based on [Table 1](#).

Table 1. Interrupt Modes

| INTCN | ECLK | INTA/CLKIN | INTB/CLKOUT |
|-------|------|-----------------------------|-----------------------------|
| 0 | 0 | INTA: Alarm1, Alarm2, Timer | CLKOUT |
| 0 | 1 | CLKIN | CLKOUT |
| 1 | 0 | INTA: Alarm1, Timer | INTB: Alarm2 |
| 1 | 1 | CLKIN | INTB: Alarm1, Alarm2, Timer |

Data Retention Mode

The MAX31342 features a Data Retention mode wherein the device shuts down its internal functional blocks (including the oscillator) except the I²C interface. The device consumes 6nA (typ) in this mode. It retains all the register contents, including the last valid date and time values. The device can resume counting from here when this mode is exited and the oscillator is enabled again.

Procedure to Enter Data Retention Mode:

1. Write DATA_RETEN = 1 in Config_reg2 (01h)
2. Write OSCONZ = 1 in Config_reg1 (00h)

Procedure to Exit Data Retention Mode:

1. Write DATA_RETEN = 0 in Config_reg2 (01h)
2. Write OSCONZ = 0 in Config_reg1 (00h)

Countdown Timer

The MAX31342 features a countdown timer with a pause function. The timer can be configured by writing into registers 03h (Timer_config) and 17h (Timer_init). The Timer_init register should be loaded with the initial value from which the timer would start counting down. The Timer_config register allows these configuration options:

- Select the frequency of the timer using the TFS[1:0] field.
- Start/stop the timer using the TE (Timer Enable) bit.
- Enable/disable the timer repeat function using the TRPT bit. This function reloads and restarts the timer with the same init value once it counts down to zero. In repeat mode, the first timer interrupt indicates the timer has started counting.
- Pause/resume the countdown at any time when the timer is enabled using the TPAUSE bit (explained below).

The timer can be programmed to assert the $\overline{\text{INTA}}$ or $\overline{\text{INTB}}$ output (see [Table 2](#)) whenever it counts down to zero. This can be enabled/disabled using the TIE bit in register 04h (Int_en_reg).

The TPAUSE bit is only valid when TE = 1. This bit must be reset to 0 whenever TE is reset to 0.

The table below highlights the steps to be used for various use cases involving TE and TPAUSE.

Table 2. Countdown Timer Sequence

| SEQUENCE | TE | TPAUSE | ACTION |
|--------------------------|----|--------|--|
| Step 1 | 0 | 0 | Countdown timer is reset, and ready for next countdown operation. Timer_init can be programmed in this state. |
| Step 2 | 1 | 0 | Countdown timer starts counting down from the value programmed in Timer_init |
| Step 3a (Optional) | 1 | 1 | Countdown timer is paused, and is ready to start counting down when TPAUSE is programmed back to '0'. Contents of the countdown timer are preserved in this state. |
| Step 3b If 3a is true | 1 | 0 | Countdown timer is brought out of pause state, and starts counting down from the paused value. |
| — | 0 | 1 | Not allowed |

Typical use cases:

- Countdown timer without pause: Step 1, Step 2, Step 1, and so on.
- Countdown timer with pause: Step 1, Step 2, Step 3a, Step 3b, Step 1, and so on.

Register Map

Register Map

| ADDRESS | NAME | MSB | | | | | | | LSB |
|---------|-------------------------------------|------------------------------|-----------------------------|------------------------------|--------------------------|---------------------------------|--------------------------|---------------------------------|-------------------------|
| REGBLK | | | | | | | | | |
| 0x00 | Config_reg1[7:0] | ECLK | INTCN | CLKSEL[1:0] | | OSCON_Z | RS[1:0] | | SWRST_N |
| 0x01 | Config_reg2[7:0] | - | DATA_RETEN | - | - | I2C_TIME_OUT_EN | Rd_RTC | Set_RTC | - |
| 0x03 | Timer_config[7:0] | - | - | TPAUSE | TE | - | TRPT | TFS[1:0] | |
| 0x04 | Int_en_reg[7:0] | - | DOSF | - | - | - | TIE | A2IE | A1IE |
| 0x05 | Int_status_reg[7:0] | LOS | OSF | - | - | - | TIF | A2F | A1F |
| 0x06 | Seconds[7:0] | - | sec_10[2:0] | | | seconds[3:0] | | | |
| 0x07 | Minutes[7:0] | - | min_10[2:0] | | | minutes[3:0] | | | |
| 0x08 | Hours[7:0] | - | Reserved | hr_10[1:0] | | hour[3:0] | | | |
| 0x09 | Day[7:0] | - | - | - | - | - | day[2:0] | | |
| 0x0A | Date[7:0] | - | - | date_10[1:0] | | date[3:0] | | | |
| 0x0B | Month[7:0] | century | - | - | month_10 | month[3:0] | | | |
| 0x0C | Year[7:0] | year_10[3:0] | | | | year[3:0] | | | |
| 0x0D | Alm1_sec[7:0] | A1M1 | sec_10[2:0] | | | seconds[3:0] | | | |
| 0x0E | Alm1_min[7:0] | A1M2 | min_10[2:0] | | | minutes[3:0] | | | |
| 0x0F | Alm1_hrs[7:0] | A1M3 | Reserved | hr_10[1:0] | | hour[3:0] | | | |
| 0x10 | Alm1day_date[7:0] | A1M4 | DY_DT | date_10[1:0] | | day_date[3:0] | | | |
| 0x11 | Alm1_mon[7:0] | A1M5 | A1M6 | - | month_10 | month[3:0] | | | |
| 0x12 | Alm1_year[7:0] | year_10[3:0] | | | | year[3:0] | | | |
| 0x13 | Alm2_min[7:0] | A2M2 | min_10[2:0] | | | minutes[3:0] | | | |
| 0x14 | Alm2_hrs[7:0] | A2M3 | Reserved | hr_10[1:0] | | hour[3:0] | | | |
| 0x15 | Alm2day_date[7:0] | A2M4 | DY_DT | date_10[1:0] | | day_date[3:0] | | | |
| 0x16 | Timer_Count[7:0] | Count[7:0] | | | | | | | |
| 0x17 | Timer_Init[7:0] | Count[7:0] | | | | | | | |
| 0x58 | Clock_sync_reg[7:0] | - | - | - | - | - | - | SYNC_DELAY[1:0] | |

Register Details

[Config_reg1 \(0x00\)](#)

Configuration Register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|-----------------------|-----------------------------|---|------------------------|-------------------------|---|------------------------|
| Field | ECLK | INTCN | CLKSEL[1:0] | | OSCONZ | RS[1:0] | | SWRSTN |
| Reset | 0x0 | 0x0 | 0x0 | | 0x1 | 0x3 | | 0x0 |
| Access Type | Write, Read | Write, Read | Write, Read | | Write, Read | Write, Read | | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| ECLK | 7 | Enable external clock input | 0x0: Disable the external clock 0x1: Enable the external clock |
| INTCN | 6 | Interrupt control bit. Selects $\overline{\text{INTB}}$ /CLKOUT pin output function | 0x0: Output is square wave 0x1: Output is interrupt |
| CLKSEL | 5:4 | Selects the CLKIN frequency | 0x0: 1Hz 0x1: 50Hz 0x2: 60Hz 0x3: 32.768KHz |
| OSCONZ | 3 | Oscillator is on when set to 0. Oscillator is off when set to 1. | 0x0: Enable the oscillator 0x1: Disable the oscillator |
| RS | 2:1 | Square wave output frequency selection on CLKOUT pin | 0x0: 1Hz 0x1: 4.098kHz 0x2: 8.192kHz 0x3: 32.768kHz |
| SWRSTN | 0 | Software reset | 0x0: Resets the digital block 0x1: Device is not on reset mode |

[Config_reg2 \(0x1\)](#)

Configuration Register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|----------------------------|---|---|--------------------------------|------------------------|-------------------------|---|
| Field | – | DATA_RETEN | – | – | I2C_TIMEOUT_EN | Rd_RTC | Set_RTC | – |
| Reset | – | 0x0 | – | – | 0x1 | 0x1 | 0x0 | – |
| Access Type | – | Write, Read | – | – | Write, Read | Write, Read | Write, Read | – |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------|------|---|--|
| DATA_RETEN | 6 | Sets the device into data retention mode. | 0x0: Normal operation mode 0x1: Data retention mode |
| I2C_TIMEOUT_EN | 3 | I ² C timeout enable | 0x0: Disables the I ² C timeout 0x1: Enables the I ² C timeout |
| Rd_RTC | 2 | Read RTC | 0x0: Reads previous programmed RTC value in registers 06h–0Ch 0x1: Reads Current RTC value in registers 06h–0Ch |
| Set_RTC | 1 | Set RTC | 0 to 1 transition loads RTC registers (06h–0Ch) contents to countdown chain. See <i>Detailed</i> |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|--------------------|
| | | | <i>Description</i> |

Timer_config (0x3)

Countdown timer configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|------------------------|--------------------|---|----------------------|--------------------------|---|
| Field | – | – | TPAUSE | TE | – | TRPT | TFS[1:0] | |
| Reset | – | – | 0x0 | 0x0 | – | 0x1 | 0x3 | |
| Access Type | – | – | Write, Read | Write, Read | – | Write, Read | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|--|
| TPAUSE | 5 | Timer Pause. This field is valid only when TE = 1. Reset TPAUSE when TE is reset to 0. See <i>Countdown Timer</i> section. | 0x0: Resume timer countdown from paused state 0x1: Pause timer |
| TE | 4 | Timer enable | 0x0: Timer is reset. New timer countdown value (Timer_Init) can be programmed in this state. Note: TPAUSE must be reset to 0 prior to setting TE to 1. 0x1: Timer enabled countdown starts |
| TRPT | 2 | Timer repeat mode | 0x0: Countdown timer will halt once it reaches zero 0x1: Countdown timer reloads the value from the Timer_init register upon reaching zero and continues counting. |
| TFS | 1:0 | Timer frequency selection | 0x0: 1024Hz 0x1: 256Hz 0x2: 64Hz 0x3: 16Hz |

Int_en_reg (0x4)

Interrupt Enable register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|----------------------|---|---|---|---------------------|----------------------|----------------------|
| Field | – | DOSF | – | – | – | TIE | A2IE | A1IE |
| Reset | – | 0x0 | – | – | – | 0x0 | 0x0 | 0x0 |
| Access Type | – | Write, Read | – | – | – | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--------------------------|---|
| DOSF | 6 | Disable Oscillator flag | 0x0: OSF indicates oscillator status 0x1: Disables the oscillator flag (OSF = 0) |
| TIE | 2 | Timer interrupt enable | 0x0: Disabled 0x1: Enabled |
| A2IE | 1 | Alarm 2 interrupt enable | 0x0: Disabled 0x1: Enabled |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------------------|-------------------------------|
| A1IE | 0 | Alarm1 interrupt enable | 0x0: Disabled 0x1: Enabled |

Int_status_reg (0x5)

Interrupt Status register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---------------------|---|---|---|---------------------|---------------------|---------------------|
| Field | LOS | OSF | – | – | – | TIF | A2F | A1F |
| Reset | 0x0 | 0x1 | – | – | – | 0x0 | 0x0 | 0x0 |
| Access Type | Read Clears All | Read Clears All | – | – | – | Read Clears All | Read Clears All | Read Clears All |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|--|
| LOS | 7 | Loss of signal. Valid only for external clock modes (ECLK = 1) | 0x0: Oscillator clock frequency is within 0.8% of external clock frequency 0x1: Oscillator clock frequency differs more than 0.8% from the external clock frequency |
| OSF | 6 | Oscillator stop flag | 0x0: Oscillator is running or when DOSF = 1 0x1: Oscillator has stopped |
| TIF | 2 | Timer interrupt flag | 0x0: Count down timer is not zero 0x1: Countdown timer reached zero |
| A2F | 1 | Alarm2 flag | 0x0: Alarm2 not triggered 0x1: Alarm2 triggered |
| A1F | 0 | Alarm1 flag | 0x0: Alarm1 not triggered 0x1: Alarm1 triggered |

Seconds (0x6)

Seconds configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|-----------------------------|---|---|------------------------------|---|---|---|
| Field | – | sec_10[2:0] | | | seconds[3:0] | | | |
| Reset | – | 0x0 | | | 0x0 | | | |
| Access Type | – | Write, Read | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|--------------------------------|
| sec_10 | 6:4 | RTC seconds in multiples of 10 |
| seconds | 3:0 | RTC seconds value. |

Minutes (0x7)

Minutes configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|-----------------------------|---|---|------------------------------|---|---|---|
| Field | – | min_10[2:0] | | | minutes[3:0] | | | |
| Reset | – | 0x0 | | | 0x0 | | | |
| Access Type | – | Write, Read | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|--------------------------------|
| min_10 | 6:4 | RTC minutes in multiples of 10 |
| minutes | 3:0 | RTC minutes value |

Hours (0x8)

Hours configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|-------------|-------------|---|-------------|---|---|---|
| Field | – | Reserved | hr_10[1:0] | | hour[3:0] | | | |
| Reset | – | 0x0 | 0x0 | | 0x0 | | | |
| Access Type | – | Write, Read | Write, Read | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|------------------------------|
| Reserved | 6 | User must enter 0. |
| hr_10 | 5:4 | RTC hours in multiples of 10 |
| hour | 3:0 | RTC hours value |

Day (0x9)

Day configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|-------------|---|---|
| Field | – | – | – | – | – | day[2:0] | | |
| Reset | – | – | – | – | – | 0x1 | | |
| Access Type | – | – | – | – | – | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|---------------------|
| day | 2:0 | RTC day of the week |

Date (0xA)

Date configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|--------------|---|-------------|---|---|---|
| Field | – | – | date_10[1:0] | | date[3:0] | | | |
| Reset | – | – | 0x0 | | 0x1 | | | |
| Access Type | – | – | Write, Read | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|-----------------------------|
| date_10 | 5:4 | RTC date in multiples of 10 |
| date | 3:0 | RTC date |

Month (0xB)

Month configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------------|---|---|--------------------------|----------------------------|---|---|---|
| Field | century | – | – | month_10 | month[3:0] | | | |
| Reset | 0x0 | – | – | 0x0 | 0x1 | | | |
| Access Type | Write, Read | – | – | Write, Read | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|------------------------------|---|
| century | 7 | Century bit | 0x0: Year is in current century 0x1: Year is in next century |
| month_10 | 4 | RTC month in multiples of 10 | |
| month | 3:0 | RTC months | |

[Year \(0xC\)](#)

Year configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------------------|---|---|---|---------------------------|---|---|---|
| Field | year_10[3:0] | | | | year[3:0] | | | |
| Reset | 0x0 | | | | 0x0 | | | |
| Access Type | Write, Read | | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|--------------------------|
| year_10 | 7:4 | RTC year multiples of 10 |
| year | 3:0 | RTC years |

[Alm1_sec \(0xD\)](#)

| DY_DT | A1M6 | A1M5 | A1M4 | A1M3 | A1M2 | A1M1 | ALARM RATE |
|-------|------|------|------|------|------|------|-----------------------------------|
| x | 1 | 1 | 1 | 1 | 1 | 1 | Once per sec |
| x | 1 | 1 | 1 | 1 | 1 | 0 | Sec match |
| x | 1 | 1 | 1 | 1 | 0 | 0 | Min and sec match |
| x | 1 | 1 | 1 | 0 | 0 | 0 | Hour, min, and sec match |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | Date and Time match |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | Month, Date, and Time match |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | Year, Month, Date, and Time match |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | Day and Time match |

Alarm 1 can be set by writing to registers 0Dh - 12h. See Register Map. The alarm can be programmed by the A1IE bit in Int_en_reg (04h) register to activate the INTA/CLKIN output on an alarm match condition. Bit 7 of each of the time-of-day/date alarm registers, and Bit 7 and 6 of month alarm register are mask bits. When all the mask bits of each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-of-day/date alarm registers. The alarm can also be programmed to repeat every second, minute, hour, day, date, month, or year. The table above shows the possible settings. Configurations not listed in the table result in illogical operation. The DY_DT bit (bit 6 of the alarm day/date registers) controls whether the alarm value stored in bits 0–5 that register reflects the day of the week or the date of the month. If DY_DT is written to logic 0, the alarm is the result of a match with date of the month. If DY_DT is written to logic 1, the alarm is the result of a match with day of the week.

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|-----------------------------|---|---|------------------------------|---|---|---|
| Field | A1M1 | sec_10[2:0] | | | seconds[3:0] | | | |
| Reset | 0x0 | 0x0 | | | 0x0 | | | |
| Access Type | Write, Read | Write, Read | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|-----------------------------------|
| A1M1 | 7 | Alarm1 mask bit for seconds |
| sec_10 | 6:4 | Alarm1 seconds in multiples of 10 |
| seconds | 3:0 | Alarm1 seconds |

Alm1_min (0xE)

Alarm1 Minutes configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|-----------------------------|---|---|------------------------------|---|---|---|
| Field | A1M2 | min_10[2:0] | | | minutes[3:0] | | | |
| Reset | 0x0 | 0x0 | | | 0x0 | | | |
| Access Type | Write, Read | Write, Read | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|-----------------------------------|
| A1M2 | 7 | Alarm1 mask bit for minutes |
| min_10 | 6:4 | Alarm1 minutes in multiples of 10 |
| minutes | 3:0 | Alarm1 minutes |

Alm1_hrs (0xF)

Alarm1 Hours configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|--------------------------|----------------------------|---|---------------------------|---|---|---|
| Field | A1M3 | Reserved | hr_10[1:0] | | hour[3:0] | | | |
| Reset | 0x0 | 0x0 | 0x0 | | 0x0 | | | |
| Access Type | Write, Read | Write, Read | Write, Read | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|---------------------------------|
| A1M3 | 7 | Alarm1 mask bit for hours |
| Reserved | 6 | User must enter 0. |
| hr_10 | 5:4 | Alarm1 hours in multiples of 10 |
| hour | 3:0 | Alarm1 hours |

Alm1day_date (0x10)

Alarm1 Day/Date configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|-----------------------|------------------------------|---|-------------------------------|---|---|---|
| Field | A1M4 | DY_DT | date_10[1:0] | | day_date[3:0] | | | |
| Reset | 0x0 | 0x0 | 0x0 | | 0x0 | | | |
| Access Type | Write, Read | Write, Read | Write, Read | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--------------------------------|---|
| A1M4 | 7 | Alarm1 mask bit for day/date | |
| DY_DT | 6 | | 0x0: Alarm when date match 0x1: Alarm when day match |
| date_10 | 5:4 | Alarm1 date in multiples of 10 | |
| day_date | 3:0 | Alarm1 day/date | |

Alm1_mon (0x11)

Alarm1 Month configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|----------------------|---|--------------------------|----------------------------|---|---|---|
| Field | A1M5 | A1M6 | – | month_10 | month[3:0] | | | |
| Reset | 0x1 | 0x1 | – | 0x0 | 0x0 | | | |
| Access Type | Write, Read | Write, Read | – | Write, Read | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|----------------------------------|
| A1M5 | 7 | Alarm1 mask bit for month |
| A1M6 | 6 | Alarm1 mask bit for year |
| month_10 | 4 | Alarm1 months in multiples of 10 |
| month | 3:0 | Alarm1 months |

Alm1_year (0x12)

Alarm1 Year configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------------------|---|---|---|---------------------------|---|---|---|
| Field | year_10[3:0] | | | | year[3:0] | | | |
| Reset | 0x0 | | | | 0x0 | | | |
| Access Type | Write, Read | | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|---------------------------------|
| year_10 | 7:4 | Alarm1 years in multiples of 10 |
| year | 3:0 | Alarm1 years |

Alm2_min (0x13)

| DY_DT | A2M4 | A2M3 | A2M1 | ALARM RATE |
|-------|------|------|------|------------------------------|
| x | 1 | 1 | 1 | Once per minute |
| x | 1 | 1 | 0 | Minute match |
| x | 1 | 0 | 0 | Hour and minute match |
| 0 | 0 | 0 | 0 | Date, hour, and minute match |
| 1 | 0 | 0 | 0 | Day, hour, and minute match |

Alarm 2 can be set by writing to registers 13h–15h. See Register Map. The alarm can be programmed by the A2IE bit in Int_en_reg (04h) register to activate the INTB/CLKIN output on an alarm match condition. Bit 7 of each of the time-of-day/ date alarm registers are mask bits. When all the mask bits of each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-of-day/date

alarm registers. The alarm can also be programmed to repeat every minute, hour, day, or date. The table below shows the possible settings. Configurations not listed in the table result in illogical operation. The DY_DT bit (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0-5 that register reflects the day of the week or the date of the month. If DY_DT is written to logic 0, the alarm is the result of a match with date of the month. If DY_DT is written to logic 1, the alarm is the result of a match with day of the week.

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|---|---|--------------|---|---|---|
| Field | A2M2 | min_10[2:0] | | | minutes[3:0] | | | |
| Reset | 0x0 | 0x0 | | | 0x0 | | | |
| Access Type | Write, Read | Write, Read | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|-----------------------------------|
| A2M2 | 7 | Alarm2 mask bit for minutes |
| min_10 | 6:4 | Alarm2 minutes in multiples of 10 |
| minutes | 3:0 | Alarm2 minutes |

Alm2_hrs (0x14)

Alarm2 Hours configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|---|-------------|---|---|---|
| Field | A2M3 | Reserved | hr_10[1:0] | | hour[3:0] | | | |
| Reset | 0x0 | 0x0 | 0x0 | | 0x0 | | | |
| Access Type | Write, Read | Write, Read | Write, Read | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|---------------------------------|
| A2M3 | 7 | Alarm2 mask bit for hours |
| Reserved | 6 | User must enter 0. |
| hr_10 | 5:4 | Alarm2 hours in multiples of 10 |
| hour | 3:0 | Alarm2 hours |

Alm2day_date (0x15)

Alarm2 Day/Date Configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|--------------|---|---------------|---|---|---|
| Field | A2M4 | DY_DT | date_10[1:0] | | day_date[3:0] | | | |
| Reset | 0x0 | 0x0 | 0x0 | | 0x0 | | | |
| Access Type | Write, Read | Write, Read | Write, Read | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|---|
| A2M4 | 7 | Alarm2 mask bit for day/date | |
| DY_DT | 6 | This bit selects alarm when day match or date match. | 0x0: Alarm when date match 0x1: Alarm when day match |
| date_10 | 5:4 | Alarm2 date in multiples of 10 | |
| day_date | 3:0 | Alarm2 day/date | |

Timer Count (0x16)

Countdown timer value register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------------|---|---|---|---|---|---|---|
| Field | Count[7:0] | | | | | | | |
| Reset | 0x00 | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|-------------------------------------|
| Count | 7:0 | Countdown timer current count value |

Timer Init (0x17)

Countdown timer Initialization register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------------|---|---|---|---|---|---|---|
| Field | Count[7:0] | | | | | | | |
| Reset | 0x00 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|--|
| Count | 7:0 | Countdown timer initial value. The timer is loaded with the contents of this register when it reaches to zero in repeat mode |

Clock sync_req (0x58)

Clock Synchronization Configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|---------------------------------|---|
| Field | – | – | – | – | – | – | SYNC_DELAY[1:0] | |
| Reset | – | – | – | – | – | – | 0x10 | |
| Access Type | – | – | – | – | – | – | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------|------|--|--|
| SYNC_DELAY | 1:0 | Synchronization delay is the time it takes for the internal countdown chain to reset after the rising edge of Set_RTC. See Minimizing the Clock Synchronization Delay section for further details. To minimize the delay, select the appropriate setting based on the clock configuration. | 0x0: Synchronization delay setting for external 1Hz clock (ECLK = 1, CLKSEL = 0) mode. Delay is less than 1 second. 0x1: Synchronization delay setting for external 50Hz/60Hz/32KHz clock (ECLK = 1, CLKSEL = 1/2/3) mode. Delay is less than 100ms. 0x2: Synchronization delay setting for internal oscillator mode (OSCONZ = 0, ECLK = 0). Delay is less than 10ms. 0x3: Reserved |

Ordering Information

| PART NUMBER | TEMP RANGE | PIN-PACKAGE |
|---------------|----------------|-------------|
| MAX31342EWA+T | -40°C to +85°C | 8 WLP |

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|--|-------------------------------|
| 0 | 12/18 | Initial release | — |
| 1 | 1/19 | Updated <i>Ordering Information</i> | 28 |
| 2 | 4/19 | Updated <i>General Description, Benefits and Features, Typical Operating Characteristics, Detailed Description, and Register Map</i> | 1, 8–10, 12, 13, 16–20, 22–26 |

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