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MAX32662

Arm Cortex-M4 Processor with FPU-Based Microcontroller (MCU) with 256KB Flash and 80KB SRAM

General Description

In the DARWIN family, the MAX32662 is an ultra-low-power, cost-effective, highly integrated 32-bit microcontroller designed for small battery-powered devices. It combines a flexible peripheral and feature mix with the powerful Arm® Cortex®-M4 processor with floating point unit (FPU) in a small form factor.

The MAX32662 enables complex edge-based designs without compromising battery life, and it also offers legacy designs an easy and cost optimal upgrade path from 8- or 16-bit microcontrollers.

Integrating 256KB of flash memory and 80KB of SRAM, the MAX32662 easily accommodates sensor code and complex algorithms.

Peripherals include SPI, UART, I^2C, I^2S, CAN 2.0B, and a 12-bit ADC.

A ROM-based secure bootloader uses 256-bit elliptic curve digital signature algorithm (ECDSA-256) encryption to ensure trusted and authenticated updates of customer software.

The device is available in a 5mm x 5mm, 32-pin TQFN-EP.

Applications

- Sports Watches
- Fitness Monitors
- Wearable Medical Patches
- Portable Medical Devices
- Industrial Sensors
- IoT

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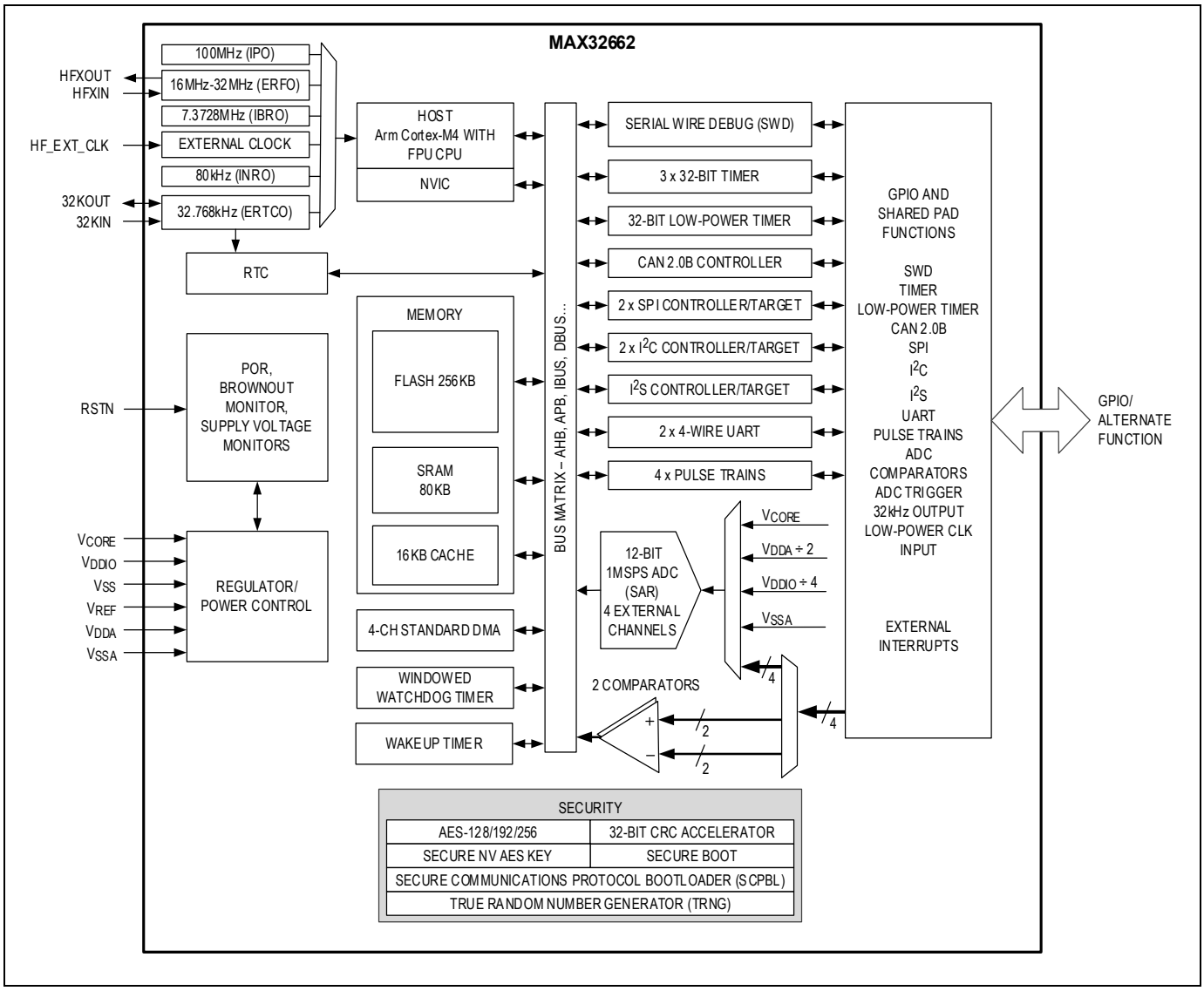
CoreMark is a registered trademark of EMBCC.

Benefits and Features

- High-Efficiency Microcontroller for Low-Power, High-Reliability Devices
  - 256KB Flash
  - 80KB SRAM, Optionally Preserved in Lowest Power BACKUP Mode
  - 16KB Unified Cache
  - Memory Protection Unit (MPU)
  - Dual- or Single-Supply Operation: 1.7V to 3.6V
  - Wide Operating Temperature: -40°C to +105°C
- Flexible Clock Sources
  - Internal High-Speed 100MHz
  - Internal Low-Power 7.3728MHz
  - Ultra-Low-Power 80kHz
  - 16MHz–32MHz (External Crystal Required)
  - 32.768kHz (External Crystal Required)
  - External Clock Inputs for CPU and Low-Power Timer
- Power Management Maximizes Uptime for Battery Applications
  - 50µA/MHz at 0.9V up to 12MHz (CoreMark®) in ACTIVE Mode
  - 44µA/MHz at 1.1V up to 100MHz (While(1)) in ACTIVE Mode
  - 2.15µA Full Memory Retention Current in BACKUP Mode at V_{DDIO} = 1.8V
  - 2.4µA Full Memory Retention Current in BACKUP Mode at V_{DDIO} = 3.3V
  - 350nA Ultra-Low-Power RTC
  - Wakeup from Low-Power Timer
- Optimal Peripheral Mix Provides Platform Scalability
  - Up to 21 General-Purpose I/O Pins
  - 4-Channel, 12-Bit, 1Msps ADC
  - Two SPI Controller/Target
  - One I^2S Controller/Target
  - Two 4-Wire UART
  - Two I^2C Controller/Target
  - One CAN 2.0B Controller
  - 4-Channel Standard DMA Controller
  - Three 32-Bit Timers
  - One 32-Bit Low-Power Timer
  - One Watchdog Timer
  - CMOS-Level 32.768kHz Calibration Output
  - AES-128/192/256 Hardware Accelerator

***Ordering Information* appears at end of data sheet.**

19-101629; Rev 0; 1/23


MAX32662
100MHz (IPO)
16MHz-32MHz (ERFO)
7.3728MHz (IBRO)
EXTERNAL CLOCK
80kHz (INRO)
32.768kHz (ERTCO)
HFXOUT
HFXIN
HF_EXT_CLK
32KOUT
32KIN
RTC
HOST
Arm Cortex-M4 WITH FPU CPU
NVIC
MEMORY
FLASH 256KB
SRAM 80KB
16KB CACHE
4-CH STANDARD DMA
WINDOWED WATCHDOG TIMER
WAKEUP TIMER
BUS MATRIX – AHB, APB, IBUS, DBUS...
SERIAL WIRE DEBUG (SWD)
3 x 32-BIT TIMER
32-BIT LOW-POWER TIMER
CAN 2.0B CONTROLLER
2 x SPI CONTROLLER/TARGET
2 x I2C CONTROLLER/TARGET
I2S CONTROLLER/TARGET
2 x 4-WIRE UART
4 x PULSE TRAINS
12-BIT 1MSPS ADC (SAR) 4 EXTERNAL CHANNELS
VCORE
VDDA ÷ 2
VDDIO ÷ 4
VSSA
2 COMPARATORS
GPIO AND SHARED PAD FUNCTIONS
SWD
TIMER
LOW-POWER TIMER
CAN 2.0B
SPI
I2C
I2S
UART
PULSE TRAINS
ADC
COMPARATORS
ADC TRIGGER
32kHz OUTPUT
LOW-POWER CLK INPUT
EXTERNAL INTERRUPTS
GPIO/ ALTERNATE FUNCTION
POR, BROWNOUT MONITOR, SUPPLY VOLTAGE MONITORS
RSTN
REGULATOR/ POWER CONTROL
VCORE
VDDIO
VSS
VREF
VDDA
VSSA
SECURITY
AES-128/192/256
32-BIT CRC ACCELERATOR
SECURE NV AES KEY
SECURE BOOT
SECURE COMMUNICATIONS PROTOCOL BOOTLOADER (SCPBL)
TRUE RANDOM NUMBER GENERATOR (TRNG)

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Absolute Maximum Ratings

V_{CORE}, HFXIN, HFXOUT ..... -0.2V to +1.21V

V_{DDIO}, V_{DDA} ..... -0.3V to +3.63V

32KIN, 32KOUT, RSTN, GPIO (*Note 1*) -0.3V to V_{DDIO} + 0.3V

Total Current into All GPIO Combined (sink) 100mA

V_{SS}, V_{SSA} 100mA

Output Current (sink) by Any GPIO Pin 25mA

Output Current (source) by Any GPIO Pin ..... -25mA

32 TQFN-EP Continuous Power Dissipation (Single Layer Board) (T_A = +70°C, derate 21.28 mW/°C above +70°C.) 1170.2mW

32 TQFN-EP Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 27.8mW/°C above +70°C.) 1527.8mW

20 WLP Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 18.02 mW/°C above +70°C.) 1441.7mW

Operating Temperature Range ..... -40°C to +105°C

Storage Temperature Range ..... -65°C to +125°C

Soldering Temperature (reflow) ..... +260°C

Note 1: No device pin can exceed 3.63V. All voltages with respect to V_{SS}, unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32 TQFN-EP

Package Code	T3255+6C
Outline Number	*21-0140*
Land Pattern Number	*90-0630*
Thermal Resistance, Single-Layer Board	
Junction to Ambient (θ_{JA})	47°C/W
Junction to Case (θ_{JC})	—
Thermal Resistance, Four-Layer Board	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

20 WLP

Package Code	W201P2+1
Outline Number	*21-100648*
Land Pattern Number	*Refer to Application Note 1891*
Thermal Resistance, Single-Layer Board	
Junction to Ambient (θ_{JA})	—
Junction to Case (θ_{JC})	—
Thermal Resistance, Four-Layer Board	
Junction to Ambient (θ_{JA})	55.49°C/W
Junction to Case (θ_{JC})	—

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER / BOTH SINGLE-SUPPLY OPERATION AND DUAL-SUPPLY OPERATION							
Supply Voltage	V_{DDIO}	V_{DDIO} must be connected to V_{DDA}		1.71	1.8	3.63	V
Supply Voltage, Core	V_{CORE}	Dual-supply operation	PWRSEQ_LPCTRL.ovr = 0b00	0.855	0.9	0.945	V
			PWRSEQ_LPCTRL.ovr = 0b01	0.95	1.0	1.05	
			Default PWRSEQ_LPCTRL.ovr = 0b10	1.045	1.1	1.155	
		No power supply connection for single-supply operation			—		
Supply Voltage, Analog	V_{DDA}	V_{DDA} must be connected to V_{DDIO}		1.71	1.8	3.63	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DDIO}		1.58		1.71	V
		Monitors V_{CORE} during dual-supply operation		0.74		0.845	
Power-On Reset Voltage	V_{POR}	Monitors V_{DDIO}			1.4		V
		Monitors V_{CORE} during dual-supply operation			0.6		
POWER / SINGLE-SUPPLY OPERATION (V_{DDIO} ONLY); f_{SYS_OSC} = IPO							
V_{DDIO} Current, ACTIVE Mode	I_{DDIO_DACTS}	Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in ACTIVE mode executing CoreMark; inputs tied to V_{SS} or V_{DDIO}; outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		54		µA/MHz
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		52		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		50		
		Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in ACTIVE mode executing CoreMark; inputs tied to V_{SS} or	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		53		
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V,		51		

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		V_{DDIO}; outputs source/sink 0mA	$f_{SYS\_CLK(MAX)}$ = 50MHz				
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		49		
		Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in ACTIVE mode executing While(1); inputs tied to V_{SS} or V_{DDIO}; outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		44		
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		42		
	I_{DD_DACTS}	Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in ACTIVE mode executing While(1); inputs tied to V_{SS} or V_{DDIO}; outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		40		
		Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in ACTIVE mode executing While(1); inputs tied to V_{SS} or V_{DDIO}; outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		43		
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		41		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		39		
	I_{DD_FACTS}	Fixed, IPO enabled, total current into V_{DDIO}	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V. See		685		µA

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		and V_{DDA} pins, V_{DDIO} = 3.3V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	*Table 8* for temperature variance.				
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V. See *Table 8* for temperature variance.		585		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V. See *Table 8* for temperature variance.		510		
		Fixed, IPO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 1.8V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V. See *Table 8* for temperature variance.		665		
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V. See *Table 8* for temperature variance.		565		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V. See *Table 8* for temperature variance.		490		
V_{DD} Current, SLEEP Mode	I_{DD_DSLPS}	Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in SLEEP mode, standard DMA with 2 channels active, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		27		µA/MHz
V_{DDIO} Current, SLEEP Mode	I_{DDIO_DSLPS}	Dynamic, IPO enabled, total	PWRSEQ_LPCTRL.ovr = 0b01, internal regulator		26		µA/MHz

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in SLEEP mode, standard DMA with 2 channels active, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz				
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		26		
		Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in SLEEP mode, standard DMA with 2 channels active, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		27		
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		26		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		26		
		Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in SLEEP mode, DMA disabled, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		12		
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		11		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		11		
		Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in SLEEP mode, DMA disabled, inputs	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		12		

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA					
		Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		11		
		Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in SLEEP mode, DMA disabled, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		11		
	I_{DDIO_FSLPS}	Fixed, IPO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 3.3V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V. See *Table 9* for temperature variance.		685		µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V. See *Table 9* for temperature variance.		585		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V. See *Table 9* for temperature variance.		510		
		Fixed, IPO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 1.8V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V. See *Table 9* for temperature variance.		665		
			PWRSEQ_LPCTRL.ovr = 0b01,		565		

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			internal regulator set to 1.0V. See *Table 9* for temperature variance.				
		Fixed, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V. See *Table 9* for temperature variance.		490		
SLEEP Mode Resume Time	t_{SLP_ONS}	f_{SYS_OSC} = IPO, time from power mode exit to execution of application code			1.5		µs
DEEPSLEEP Mode Resume Time	t_{DSL_ONS}	f_{SYS_OSC} = IPO, time from power mode exit to execution of application code	fastwk_en = 1		75		µs
			fastwk_en = 0		210		
BACKUP Mode Resume Time	t_{BKU_ONS}	f_{SYS_OSC} = IPO, time from power mode exit to execution of application code	fastwk_en = 1		910		ms
			fastwk_en = 0		1020		
STORAGE Mode Resume Time	t_{STO_ONS}	f_{SYS_OSC} = IPO, time from power mode exit to execution of application code	fastwk_en = 1		920		ms
			fastwk_en = 0		1030		
POWER / SINGLE-SUPPLY OPERATION (V_{DDIO} ONLY); f_{SYS_OSC} = IBRO							
V_{DDIO} Current, ACTIVE Mode	I_{DDIO_DACTS}	Dynamic, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in ACTIVE mode, executing CoreMark, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		55		µA/MHz
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		52		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		49		

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		Dynamic, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in ACTIVE mode, executing CoreMark, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		54		
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		51		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		48		
		Dynamic, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in ACTIVE mode, executing While(1), inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		44		
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		41		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		39		
		Dynamic, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in ACTIVE mode, executing While(1), inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		43		
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		41		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V,		38		

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			$f_{SYS\_CLK(MAX)}$ = 7.3728MHz				
	I_{DDIO_FACTS}	Fixed, IBRO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 3.3V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V. See *Table 10* for temperature variance.		280		µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V. See *Table 10* for temperature variance.		255		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V. See *Table 10* for temperature variance.		235		
		Fixed, IBRO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 1.8V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V. See *Table 10* for temperature variance.		255		
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V. See *Table 10* for temperature variance.		230		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V. See *Table 10* for temperature variance.		210		
V_{DDIO} Current, SLEEP Mode	I_{DDIO_DSLPS}	Dynamic, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in SLEEP mode, standard DMA with 2	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		26		µA/MHz
			PWRSEQ_LPCTRL.ovr = 0b01,		25		

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		channels active, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz				
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		24		
		Dynamic, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in SLEEP mode, standard DMA with 2 channels active, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		26		
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		25		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		23		
		Dynamic, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in SLEEP mode, DMA disabled, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		11		
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		10		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		9		
		Dynamic, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in SLEEP	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		11		

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		mode, DMA disabled, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		10		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		9		
	I_{DDIO_FSLPS}	Fixed, IBRO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 3.3V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V. See *Table 11* for temperature variance.		280		µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V. See *Table 11* for temperature variance.		255		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V. See *Table 11* for temperature variance.		235		
		Fixed, IBRO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 1.8V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V. See *Table 11* for temperature variance.		255		
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V. See *Table 11* for temperature variance.		230		
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V. See *Table 11* for		210		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			temperature variance.				
SLEEP Mode Resume Time	t_{SLP_ONS}	f_{SYS_OSC} = IBRO, time from power mode exit to execution of application code			20.5		µs
DEEPSLEEP Mode Resume Time	t_{DSL_ONS}	f_{SYS_OSC} = IBRO, time from power mode exit to execution of application code	fastwk_en = 1		205		µs
			fastwk_en = 0		350		
BACKUP Mode Resume Time	t_{BKU_ONS}	f_{SYS_OSC} = IBRO, time from power mode exit to execution of application code	fastwk_en = 1		11.55		ms
			fastwk_en = 0		11.67		
STORAGE Mode Resume Time	t_{STO_ONS}	f_{SYS_OSC} = IBRO, time from power mode exit to execution of application code	fastwk_en = 1		11.72		ms
			fastwk_en = 0		11.74		
POWER / SINGLE-SUPPLY OPERATION (V_{DDIO} ONLY)							
V_{DDIO} Fixed Current, DEEPSLEEP Mode	I_{DDIO_FDSLS}	Standby state with full data retention and 80KB SRAM retained	V_{DDIO} = 3.3V, PWRSEQ_LPCTRL.bg_dis = 0. See *Table 12* for temperature variance.		3.6		µA
			V_{DDIO} = 1.8V, PWRSEQ_LPCTRL.bg_dis = 0. See *Table 12* for temperature variance.		3.3		
V_{DDIO} Fixed Current, BACKUP Mode	I_{DDIO_FBKUS}	V_{DDIO} = 3.3V, RTC disabled	0KB SRAM retained, retention regulator disabled. See *Table 13* for temperature variance.		0.45		µA
			20KB SRAM retained. See *Table 13* for temperature variance.		1.25		
			40KB SRAM retained. See *Table 13* for temperature variance.		1.6		
			60KB SRAM retained. See *Table 13* for temperature variance.		2		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			80KB SRAM retained. See *Table 13* for temperature variance.		2.4		
		V_{DDIO} = 1.8V, RTC disabled	0KB SRAM retained, retention regulator disabled. See *Table 13* for temperature variance.		0.25		
			20KB SRAM retained. See *Table 13* for temperature variance.		1		
			40KB SRAM retained. See *Table 13* for temperature variance.		1.4		
			60KB SRAM retained. See *Table 13* for temperature variance.		1.8		
			80KB SRAM retained. See *Table 13* for temperature variance.		2.15		
V_{DDIO} Fixed Current, STORAGE Mode	I_{DDIO_FSTOS}	V_{DDIO} = 3.3V. See *Table 14* for temperature variance.			0.23		µA
		V_{DDIO} = 1.8V. See *Table 14* for temperature variance.			0.06		
POWER / DUAL-SUPPLY OPERATION (V_{DDIO} AND V_{CORE}); f_{SYS_OSC} = IPO							
V_{CORE} Current, ACTIVE mode	I_{CORE_DACTD}	Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing CoreMark, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		53		µA/MHz
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		52		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		46		
		Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode,	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		43		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		executing While(1), inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		41		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		37		
	I_{CORE_FACTD}	Fixed, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V. See *Table 15* for temperature variance.		250		µA
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V. See *Table 15* for temperature variance.		145		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V. See *Table 15* for temperature variance.		70		
V_{DDIO} Current, ACTIVE mode	I_{DDIO_DACTD}	Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in ACTIVE mode, executing CoreMark, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		2		µA/MHz
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		2		
		Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in ACTIVE mode, executing CoreMark, inputs tied to V_{SS} or	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V,		2		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		V_{DDIO}, outputs source/sink 0mA	$f_{SYS\_CLK(MAX)}$ = 50MHz				
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		2		
		Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in ACTIVE mode, executing While(1), inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		2		
		Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in ACTIVE mode, executing While(1), inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		2		
	I_{DDIO_FACTD}	Fixed, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V. See *Table 16* for temperature variance.		385		µA
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V. See *Table 16* for temperature variance.		385		
			PWRSEQ_LPCTRL.ovr = 0b00,		385		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			V_{CORE} = 0.9V. See *Table 16* for temperature variance.				
		Fixed, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V. See *Table 16* for temperature variance.		370		
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V. See *Table 16* for temperature variance.		370		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V. See *Table 16* for temperature variance.		370		
V_{CORE} Current, SLEEP Mode	I_{CORE_DSLPD}	Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, standard DMA with 2 channels active, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		28		µA/MHz
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		26		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		24		
		Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, DMA disabled, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		12		
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		11		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V,		10		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			$f_{SYS\_CLK(MAX)}$ = 12MHz				
	I_{CORE_FSLPD}	Fixed, IPO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V. See *Table 17* for temperature variance.		250		µA
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V. See *Table 17* for temperature variance.		145		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V. See *Table 17* for temperature variance.		70		
V_{DDIO} Current, SLEEP Mode	I_{DDIO_DSLPD}	Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in SLEEP mode, standard DMA with 2 channels active, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		2		µA/MHz
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		2		
		Dynamic, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in SLEEP mode, standard DMA with 2 channels active, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		2		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
	I_{DDIO_FSLPD}	Fixed, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V. See *Table 18* for temperature variance.		385		µA
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V. See *Table 18* for temperature variance.		385		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V. See *Table 18* for temperature variance.		385		
		Fixed, IPO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V. See *Table 18* for temperature variance.		370		
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V. See *Table 18* for temperature variance.		370		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V. See *Table 18* for temperature variance.		370		
SLEEP Mode Resume Time	t_{SLP_OND}	f_{SYS_OSC} = IPO, time from power mode exit to execution of application code			1.5		µs
DEEPSLEEP Mode Resume Time	t_{DSL_OND}	f_{SYS_OSC} = IPO, time from power mode exit to execution of application code	fastwk_en = 1		75		µs
			fastwk_en = 0		210		
BACKUP Mode Resume Time	t_{BKU_OND}	f_{SYS_OSC} = IPO, time from power mode exit to execution of application code	fastwk_en = 1		910		ms
			fastwk_en = 0		1020		
STORAGE Mode Resume Time	t_{STO_OND}	f_{SYS_OSC} = IPO, time from power mode exit to	fastwk_en = 1		920		ms
			fastwk_en = 0		1030		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		execution of application code					
POWER / DUAL-SUPPLY OPERATION (V_{DDIO} AND V_{CORE}); f_{SYS_OSC} = IBRO							
V_{CORE} Current, ACTIVE mode	I_{CORE_DACTD}	Dynamic, IBRO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing CoreMark, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		54		µA/MHz
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		50		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		41		
		Dynamic, IBRO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing While(1), inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		44		
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		40		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		34		
	I_{CORE_FACTD}	Fixed, IBRO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V. See *Table 19* for temperature variance.		105		µA
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V. See *Table 19* for temperature variance.		80		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V. See *Table 19* for temperature variance.		55		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DDIO} Current, ACTIVE Mode	I_{DDIO_DACTD}	Dynamic, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in ACTIVE mode, executing CoreMark, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		2		µA/MHz
			PWRSEQ_LPCTRL.ovr = 0b01, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b00, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		2		
		Dynamic, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in ACTIVE mode, executing CoreMark, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b01, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b00, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		2		
		Dynamic, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in ACTIVE mode, executing While(1), inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b01, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b00, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		2		
		Dynamic, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in ACTIVE mode, executing While(1), inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b01, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		2		
			PWRSEQ_LPCTRL.ovr = 0b00, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		2		
	I_{DDIO_FACTD}	Fixed, IBRO enabled, total current into V_{DDIO}	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V. See		115		µA

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		pin, V_{DDIO} = 3.3V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	*Table 20* for temperature variance.				
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V. See *Table 20* for temperature variance.		115		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V. See *Table 20* for temperature variance.		115		
		Fixed, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V. See *Table 20* for temperature variance.		90		
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V. See *Table 20* for temperature variance.		90		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V. See *Table 20* for temperature variance.		90		
V_{CORE} Current, SLEEP Mode	I_{CORE_DSLPD}	Dynamic, IBRO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, standard DMA with 2 channels active, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		27		µA/MHz
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		25		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		21		
		Dynamic, IBRO enabled, total current into V_{CORE}	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V,		12		

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		pin, CPU in SLEEP mode, DMA disabled, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	$f_{SYS\_CLK(MAX)}$ = 7.3728MHz				
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		11		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		10		
	I_{CORE_FSLPD}	Fixed, IBRO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V. See *Table 21* for temperature variance.		250		µA
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V. See *Table 21* for temperature variance.		145		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V. See *Table 21* for temperature variance.		70		
V_{DDIO} Current, SLEEP Mode	I_{DDIO_DSLPD}	Dynamic, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in SLEEP mode, standard DMA with 2 channels active, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		37.0		µA/MHz
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		38		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		37		
		Dynamic, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in SLEEP	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		39		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		mode, standard DMA with 2 channels active, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		39		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		38		
	I_{DDIO_FSLPD}	Fixed, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 3.3V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V. See *Table 22* for temperature variance.		115		µA
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V. See *Table 22* for temperature variance.		115		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V. See *Table 22* for temperature variance.		115		
		Fixed, IBRO enabled, total current into V_{DDIO} pin, V_{DDIO} = 1.8V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V. See *Table 22* for temperature variance.		90		
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V. See *Table 22* for temperature variance.		90		
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V. See *Table 22* for temperature variance.		90		
SLEEP Mode Resume Time	t_{SLP_OND}	f_{SYS_OSC} = IBRO, time from power mode exit to execution of application code			20.5		µs
DEEPSLEEP Mode Resume Time	t_{DSL_OND}	f_{SYS_OSC} = IBRO, time from power mode exit to	fastwk_en = 1		205		µs
			fastwk_en = 0		350		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		execution of application code					
BACKUP Mode Resume Time	t_{BKU_OND}	f_{SYS_OSC} = IBRO, time from power mode exit to execution of application code	fastwk_en = 1		11.55		ms
			fastwk_en = 0		11.67		
STORAGE Mode Resume Time	t_{STO_OND}	f_{SYS_OSC} = IBRO, time from power mode exit to execution of application code	fastwk_en = 1		11.72		ms
			fastwk_en = 0		11.74		
POWER / DUAL-SUPPLY OPERATION (V_{DDIO} AND V_{CORE})							
V_{CORE} Fixed Current, DEEPSLEEP Mode	I_{CORE_FDSLPD}	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	PWRSEQ_LPCTRL.bg_dis = 0. See *Table 23* for temperature variance.		6.8		µA
		V_{DDIO} = 3.3V, V_{CORE} = 0.855V	PWRSEQ_LPCTRL.bg_dis = 0. See *Table 23* for temperature variance.		2.7		
		V_{DDIO} = 1.8V, V_{CORE} = 1.1V.	PWRSEQ_LPCTRL.bg_dis = 0. See *Table 23* for temperature variance.		6.8		
		V_{DDIO} = 1.8V, V_{CORE} = 0.855V	PWRSEQ_LPCTRL.bg_dis = 0. See *Table 23* for temperature variance.		2.7		
V_{DDIO} Fixed Current, DEEPSLEEP Mode	I_{DDIO_FDSLPD}	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	PWRSEQ_LPCTRL.bg_dis = 0. See *Table 24* for temperature variance.		0.19		µA
		V_{DDIO} = 3.3V, V_{CORE} = 0.855V	PWRSEQ_LPCTRL.bg_dis = 0. See *Table 24* for temperature variance.		0.19		
		V_{DDIO} = 1.8V, V_{CORE} = 1.1V	PWRSEQ_LPCTRL.bg_dis = 0. See *Table 24* for temperature variance.		0.05		
		V_{DDIO} = 1.8V, V_{CORE} = 0.855V	PWRSEQ_LPCTRL.bg_dis = 0. See *Table 24* for		0.05		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			temperature variance.				
V_{CORE} Fixed Current, BACKUP Mode	I_{CORE_FBKUD}	0KB SRAM retained, RTC disabled, retention regulator disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V. See *Table 25* for temperature variance.		0.33		µA
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V. See *Table 25* for temperature variance.		0.18		
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V. See *Table 25* for temperature variance.		0.33		
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V. See *Table 25* for temperature variance.		0.18		
		20KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V. See *Table 25* for temperature variance.		1.28		
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V. See *Table 25* for temperature variance.		0.54		
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V. See *Table 25* for temperature variance.		1.28		
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V. See *Table 25* for temperature variance.		0.54		
		40KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V. See *Table 25* for temperature variance.		2.23		
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V. See *Table 25* for		0.9		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			temperature variance.				
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V. See *Table 25* for temperature variance.		2.23		
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V. See *Table 25* for temperature variance.		0.9		
		60KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V. See *Table 25* for temperature variance.		3.2		
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V. See *Table 25* for temperature variance.		1.2		
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V. See *Table 25* for temperature variance.		3.2		
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V. See *Table 25* for temperature variance.		1.2		
		80KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V. See *Table 25* for temperature variance.		4.1		
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V. See *Table 25* for temperature variance.		1.6		
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V. See *Table 25* for temperature variance.		4.1		
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V. See *Table 25* for		1.6		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			temperature variance.				
V_{DDIO} Fixed Current, BACKUP Mode	I_{DDIO_FBKUD}	0KB SRAM retained, RTC disabled, retention regulator disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V. See *Table 25* for temperature variance.		0.19		µA
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V. See *Table 26* for temperature variance.		0.19		
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V. See *Table 26* for temperature variance.		0.05		
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V. See *Table 26* for temperature variance.		0.05		
		20KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V. See *Table 26* for temperature variance.		0.19		
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V. See *Table 26* for temperature variance.		0.19		
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V. See *Table 26* for temperature variance.		0.05		
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V. See *Table 26* for temperature variance.		0.05		
		40KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V. See *Table 26* for temperature variance.		0.19		
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V. See *Table 26* for		0.19		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			temperature variance.				
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V. See *Table 26* for temperature variance.		0.05		
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V. See *Table 26* for temperature variance.		0.05		
		60KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V. See *Table 26* for temperature variance.		0.19		
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V. See *Table 26* for temperature variance.		0.19		
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V. See *Table 26* for temperature variance.		0.05		
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V. See *Table 26* for temperature variance.		0.05		
		80KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V. See *Table 26* for temperature variance.		0.19		
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V. See *Table 26* for temperature variance.		0.19		
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V. See *Table 26* for temperature variance.		0.05		
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V. See *Table 26* for		0.05		

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			temperature variance.				
V_{CORE} Fixed Current, STORAGE Mode	I_{CORE_FSTOD}	V_{DDIO} = 3.3V, V_{CORE} = 1.1V. See *Table 27* for temperature variance.			0.33		µA
		V_{DDIO} = 3.3V, V_{CORE} = 0.855V. See *Table 27* for temperature variance.			0.18		
		V_{DDIO} = 1.8V, V_{CORE} = 1.1V. See *Table 27* for temperature variance.			0.33		
		V_{DDIO} = 1.8V, V_{CORE} = 0.855V. See *Table 27* for temperature variance.			0.18		
V_{DDIO} Fixed Current, STORAGE Mode	I_{DDIO_FSTOD}	V_{DDIO} = 3.3V, V_{CORE} = 1.1V. See *Table 28* for temperature variance.			0.22		µA
		V_{DDIO} = 3.3V, V_{CORE} = 0.855V. See *Table 28* for temperature variance.			0.22		
		V_{DDIO} = 1.8V, V_{CORE} = 1.1V. See *Table 28* for temperature variance.			0.06		
		V_{DDIO} = 1.8V, V_{CORE} = 0.855V. See *Table 28* for temperature variance.			0.06		
CLOCKS							
System Clock Frequency	f_{SYS_CLK}			0		f_{IPO}	MHz
Internal Primary Oscillator (IPO)	f_{IPO}	Default PWRSEQ_LPCTRL.ovr = 0b10			100		MHz
Internal Baud Rate Oscillator (IBRO)	f_{IBRO}				7.3728		MHz
Internal Nanoring Oscillator (INRO)	f_{INRO}	Measured at V_{DDIO} = 1.8V			80		kHz
External RTC Oscillator (ERTCO)	f_{ERTCO}	32kHz watch crystal, C_L = 6pF, ESR < 90kΩ, C_0 ≤ 2pF			32.768		kHz
External RF Oscillator Frequency (ERFO)	f_{ERFO}	32MHz crystal, CL = 12pF, ESR ≤ 50Ω, C_0≤ 7pF, temperature stability ±20ppm, initial tolerance ±20ppm			32		MHz
RTC Operating Current	I_{RTC}	All power modes, RTC enabled			0.35		µA
RTC Power-up Time	t_{RTC_ON}				250		ms
External System Clock Input Frequency	f_{EXT_CLK}	HF_EXT_CLK selected, V_{DDIO} ≥ 3.0V	Minimum voltage vs. frequency requirements for PWRSEQ_LPCTRL.ovr settings must be followed.			50	MHz
		HF_EXT_CLK selected, V_{DDIO} < 3.0V	Minimum voltage vs. frequency requirements for PWRSEQ_LPCTRL.ovr settings must be followed.			25	
External Low-Power Timer Clock Input Frequency	$f_{EXT\_LPTMR\_CLK}$	LP_EXT_CLK selected, V_{DDIO} ≥ 3.0V				10	MHz
		LP_EXT_CLK selected, V_{DDIO} < 3.0V				5	
GENERAL-PURPOSE I/O							

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage for All GPIO, RSTN	V_{IL_GPIO}	Pin configured as GPIO			0.3 × V_{DDIO}	V
Input High Voltage for All GPIO, RSTN	V_{IH_GPIO}	Pin configured as GPIO	0.7 × V_{DDIO}			V
Output Low Voltage for All GPIO Except P0.6, P0.9, P0.12, and P0.13	V_{OL_GPIO}	V_{DDIO} = 1.71V, I_{OL} = 1mA, DS[1:0] = 00 (*Note 2*)		0.2	0.4	V
		V_{DDIO} = 1.71V, I_{OL} = 2mA, DS[1:0] = 10 (*Note 2*)		0.2	0.4	
		V_{DDIO} = 1.71V, I_{OL} = 4mA, DS[1:0] = 01 (*Note 2*)		0.2	0.4	
		V_{DDIO} = 1.71V, I_{OL} = 6mA, DS[1:0] = 11 (*Note 2*)		0.2	0.4	
Output Low Voltage for GPIO P0.6, P0.9, P0.12, and P0.13	V_{OL_I2C}	V_{DDIO} = 1.71V, I_{OL} = 2mA, DS = 0 (*Note 2*)		0.2	0.4	V
		V_{DDIO} = 1.71V, I_{OL} = 10mA, DS = 1 (*Note 2*)		0.2	0.4	
Output High Voltage for All GPIO Except P0.6, P0.9, P0.12, and P0.13	V_{OH_VGPIO}	V_{DDIO} = 1.71V, I_{OH} = 1mA, DS[1:0] = 00 (*Note 2*)	V_{DDIO} - 0.4			V
		V_{DDIO} = 1.71V, I_{OH} = 2mA, DS[1:0] = 10 (*Note 2*)	V_{DDIO} - 0.4			
		V_{DDIO} = 1.71V, I_{OH} = 4mA, DS[1:0] = 01 (*Note 2*)	V_{DDIO} - 0.4			
		V_{DDIO} = 1.71V, I_{OH} = 6mA, DS[1:0] = 11 (*Note 2*)	V_{DDIO} - 0.4			
Output High Voltage for GPIO P0.6, P0.9, P0.12, and P0.13	V_{OH_I2C}	V_{DDIO} = 1.71V, I_{OH} = 2mA, DS = 0 (*Note 2*)	V_{DDIO} - 0.4			V
		V_{DDIO} = 1.71V, I_{OH} = 10mA, DS = 1 (*Note 2*)	V_{DDIO} - 0.4			
Combined I_{OL}, All GPIO	I_{OL_TOTAL}				100	mA
Combined I_{OH}, All GPIO	I_{OH_TOTAL}		-100			mA
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input/Output Pin Capacitance for All Pins	C_{IO}			4		pF
Input Leakage Current Low	I_{IL}	V_{IN} = 0V, internal pull-up disabled	-200		+200	nA
Input Leakage Current High	I_{IH}	V_{IN} = 3.63V, internal pull-up disabled	-800		+800	nA
RSTN Assertion Time	t_{RSTN}	Device in ACTIVE mode, RSTN device pin assertion duration to entry into device reset state		6 x t_{SYS_CLK}		µs
Input Pull-up Resistor RSTN	R_{PU_VDDIO}	Internal pull-up to V_{DDIO} = V_{RST}, RSTN at V_{IH}		18.7		kΩ
		Internal pull-up to V_{DDIO} = 3.63V, RSTN at V_{IH}		10.0		
Input Pull-up Resistor for All GPIO	R_{PU}	Device pin configured as GPIO, internal pull-up to V_{DDIO} = V_{RST}. device pin at V_{IH}		18.7		kΩ

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		Device pin configured as GPIO, internal pull-up to V_{DDIO}= 3.63V, device pin at V_{IH}			10.0		
Input Pull-down Resistor for All GPIO	R_{PD}	Device pin configured as GPIO, internal pull-down to V_{SS}, V_{DDIO}= V_{RST}, device pin at V_{IL}			17.6		kΩ
		Device pin configured as GPIO, internal pull-down to V_{SS}, V_{DDIO}= V_{RST}, device pin at V_{IL}			8.8		
12-BIT SAR ADC							
V_{DDA} Standby Current	I_{VDDA}	ADC_CTRL0.resetb = 0, ADC_CTRL0.bias_en = 0, ADC_CTRL0.adc_en = 0 MCR_ADCCFG1.amp_en = 0 MCR_ADCCFG1.ain_inp_en = 0b1111, input buffer disabled	V_{DDA} = 1.8V		340		µA
			V_{DDA} = 3.3V		361		
V_{DDA} ADC Active Current	I_{ADC}	ADC Active, reference buffer disabled, ADC clock = 25MHz. Additional current above I_{VDDA}.	MCR_ADCCFG0.ext_ref = 0, MCR_ADCCFG0.int_ref = 0, V_{DDA} = 1.8V		202		µA
			MCR_ADCCFG0.ext_ref = 0, MCR_ADCCFG0.int_ref = 1, V_{DDA} = 3.3V		353		
		ADC Active, reference buffer disabled, ADC clock = 16MHz. Additional current above I_{VDDA}.	MCR_ADCCFG0.ext_ref = 0, MCR_ADCCFG0.int_ref = 0, V_{DDA} = 1.8V		167		
			MCR_ADCCFG0.ext_ref = 0, MCR_ADCCFG0.int_ref = 1, V_{DDA} = 3.3V		280		
Bandgap Temperature Coefficient	V_{TEMPCO}	Box method			±25		ppm
12-BIT SAR ADC/INPUT BUFFER ENABLED (MCR_ADCCFG1.thru_pad_sw_enx = 1; MCR_ADCCFG1.thru_en = 1; MCR_ADCCFG1.amp_en = 1)							
Resolution					12		bits
Effective Number of Bits	ENOB	ADC_CLKCTRL.clkdiv = 0b000. AINx input pk-pk = V_{REF} - 10mV			10		bits
External Reference Voltage	V_{REF}	$V_{REF} \le V_{DDA}$,		2.048		V_{DDA}	V

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		MCR_ADCCFG0.ext_ref = 1, MCR_ADCCFG1.ain_inp_en = 0b0001					
Internal Reference Voltage	V_{INT_REF}	MCR_ADCCFG0.ext_ref = 0, MCR_ADCCFG0.int_ref = 0			1.25		V
		MCR_ADCCFG0.ext_ref = 0, MCR_ADCCFG0.int_ref = 1			2.048		
ADC Clock Rate Maximum	f_{ACLK}				25		MHz
Input Voltage Range	V_{AIN}	AIN[3:0], ADC_DATA.chan = [3:0]	MCR_ADCCFG1.divsel = 0b00	V_{SSA} + 0.05		MIN(V_{REF}, V_{DDIOH})	V
			MCR_ADCCFG1.divsel = 0b01	V_{SSA} + 0.05		MIN(V_{REF}, V_{DDIOH})	
			MCR_ADCCFG1.divsel = 0b10	V_{SSA} + 0.05		MIN(2 x V_{REF}, V_{DDIOH})	
			MCR_ADCCFG1.divsel = 0b11	V_{SSA} + 0.05		MIN(3 x V_{REF}, V_{DDIOH})	
ADC Buffer Current	$I_{ADCBUFFER}$				54		µA
Input Impedance	R_{AIN}				100		kΩ
Analog Input Capacitance	C_{AIN}	Fixed capacitance to V_{SSA}			2		pF
Integral Nonlinearity	INL				±1.5		LSb
Differential Nonlinearity	DNL				±0.75		LSb
Offset Error	V_{OS}	Chopping enabled			±0.25		LSb
ADC Input Buffer Offset	V_{OS}				±1.5		LSb
ADC Sample Rate	f_{ADC}					25	kHz
ADC Setup Time	t_{ADC_SU}	Any power-up of ADC clock or ADC bias to CpuAdcStart				500	µs
ADC Input Leakage	I_{ADC_LEAK}				±1.2		nA
12-BIT SAR ADC/INPUT BUFFER DISABLED (MCR_ADCCFG1.thru_pad_sw_enx = 0; MCR_ADCCFG1.thru_en = 0; MCR_ADCCFG1.amp_en = 0)							
Resolution					12		bits
Effective Number of Bits	ENOB	ADC_CLKCTRL.clkdiv = 0b000. AINx input pk-pk = V_{REF} - 10mV			10		bits
External Reference Voltage	V_{REF}	$V_{REF} \le V_{DDA}$, MCR_ADCCFG0.ext_ref = 1		2.048		V_{DDA}	V
Internal Reference Voltage	V_{INT_REF}	MCR_ADCCFG0.ext_ref = 0, MCR_ADCCFG0.int_ref = 0			1.25		V
		MCR_ADCCFG0.ext_ref = 0, MCR_ADCCFG0.int_ref = 1			2.048		
ADC Clock Rate Maximum	f_{ACLK}				25		MHz
Input Voltage Range	V_{AIN}	AIN[3:0], ADC_DATA.chan = [3:0]	MCR_ADCCFG1.divsel = 0b00	V_{SSA} + 0.05		V_{REF}	V

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Impedance	R_{AIN}			1.2		MΩ
Analog Input Capacitance	C_{AIN}	Fixed capacitance to V_{SSA}		2		pF
		Dynamically switched capacitance		1.2		
Integral Nonlinearity	INL			±1.5		LSb
Differential Nonlinearity	DNL			±0.75		LSb
Offset Error	V_{OS}	Chopping enabled		±0.25		LSb
ADC Sample Rate	f_{ADC}				1	Msps
ADC Setup Time	t_{ADC_SU}	Any power-up of ADC clock or ADC bias to CpuAdcStart			500	µs
ADC Input Leakage	I_{ADC_LEAK}	ADC inactive or channel not selected		±1.2		nA
COMPARATORS						
Input Offset Voltage	V_{OFFSET}			±1		mV
Input Hysteresis	V_{HYST}	AINCOMPHYST[1:0] = 00		±23		mV
		AINCOMPHYST[1:0] = 01		±50		
		AINCOMPHYST[1:0] = 10		±2		
		AINCOMPHYST[1:0] = 11		±7		
Input Voltage Range	V_{IN_CMP}	Common-mode range	0		V_{DDIO}	V
FLASH MEMORY						
Flash Erase Time	t_{M_ERASE}	Mass erase		20		ms
	t_{P_ERASE}	Page erase		20		
Flash Programming Time per Word	t_{PROG}			42		µs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +125°C	10			years

Note 2: When using a GPIO bias voltage of 2.97V, the drive current capability of the GPIO is 2x that of its drive strength when using a GPIO bias voltage of 1.71V.

Electrical Characteristics – I²C

(Timing specifications are guaranteed by design and not production tested. T_A = -40°C to +105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STANDARD-MODE						
Output Fall Time	t_{OF}	Standard-mode, from $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
SCL Clock Frequency	f_{SCL}		0		100	kHz
Low Period SCL Clock	t_{LOW}		4.7			µs
High Time SCL Clock	t_{HIGH}		4.0			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		4.7			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		4.0			µs

(Timing specifications are guaranteed by design and not production tested. T_A = -40°C to +105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Setup Time	$t_{SU;DAT}$			300		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			800		ns
Fall Time for SDA and SCL	t_F			200		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		4.0			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		4.7			µs
Data Valid Time	$t_{VD;DAT}$		3.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		3.45			µs
FAST-MODE						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Low Period SCL Clock	t_{LOW}		1.3			µs
High Time SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			µs
Data Setup Time	$t_{SU;DAT}$			125		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			30		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.6			ms
Bus Free Time Between a Stop and Start Condition	t_{BUS}		1.3			µs
Data Valid Time	$t_{VD;DAT}$		0.9			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9			µs
FAST-MODE PLUS						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		80		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Low Period SCL Clock	t_{LOW}		0.5			µs

(Timing specifications are guaranteed by design and not production tested. T_A = -40°C to +105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Time SCL Clock	t_{HIGH}		0.26			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.26			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.26			µs
Data Setup Time	$t_{SU;DAT}$			50		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			50		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.26			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		0.5			µs
Data Valid Time	$t_{VD;DAT}$		0.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.45			µs

Electrical Characteristics – I²S

(Timing specifications are guaranteed by design and not production tested. T_A = -40°C to +105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TARGET MODE						
Bit Clock Frequency	f_{BCLKS}				25	MHz
Bit Clock Period	t_{BCLKS}		$1/f_{BCLKS}$			ns
BCLK High Time	$t_{WBCLKHS}$			0.5		$1/f_{BCLKS}$
BCLK Low Time	$t_{WBCLKLS}$			0.5		$1/f_{BCLKS}$
LRCLK Setup Time	t_{LRCLK_BCLKS}			25		ns
Delay Time, BCLK to SD (Output) Valid	t_{BCLK_SDOS}			12		ns
Setup Time for SD (Input)	t_{SU_SDIS}			6		ns
Hold Time SD (Input)	t_{HD_SDIS}			3		ns
CONTROLLER MODE						
Bit Clock Frequency	f_{BCLKM}	Source only from ERFO			32	MHz
Bit Clock Period	t_{BCLKM}		$1/f_{BCLKM}$			ns
BCLK High Time	$t_{WBCLKHM}$			0.5		$1/f_{BCLKM}$
BCLK Low Time	$t_{WBCLKLM}$			0.5		$1/f_{BCLKM}$
Delay Time BCLK to LRCLK Valid	t_{LRCLK_BCLKM}			20		ns
Delay Time, BCLK to SD (Output) Valid	t_{BCLK_SDOM}			20		ns
Setup Time for SD (Input)	t_{SU_SDIM}			10		ns

(Timing specifications are guaranteed by design and not production tested. T_A = -40°C to +105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hold Time SD (Input)	t_{HD_SDIM}			10		ns

Electrical Characteristics – SPI

(Timing specifications are guaranteed by design and not production tested.T_A = -40°C to +105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROLLER MODE						
SPI Controller Operating Frequency	f_{MCK}	f_{SYS_CLK} = 100MHz, $f_{MCK(MAX)}$ = $f_{SYS\_CLK}/2$			50	MHz
SPI Controller SCK Period	t_{MCK}			$1/f_{MCK}$		ns
SCK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}		$t_{MCK}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Low Idle	t_{MLH}			$t_{MCK}/2$		ns
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCK}/2$		ns
TARGET MODE						
SPI Target Operating Frequency	f_{SCK}				50	MHz
SPI Target SCK Period	t_{SCK}			$1/f_{SCK}$		ns
SCK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
SSx Active to First Shift Edge	t_{SSE}			10		ns
MOSI Input to SCK Sample Edge Rise/Fall Setup	t_{SIS}			5		ns
MOSI Input from SCK Sample Edge Transition Hold	t_{SIH}			1		ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}			5		ns
SCK Inactive to SSx Inactive	t_{SSD}			10		ns
SSx Inactive Time	t_{SSH}			$1/f_{SCK}$		µs
MISO Hold Time After SSx Deassertion	t_{SLH}			$1/f_{SCK}$		ns

Timing Diagrams

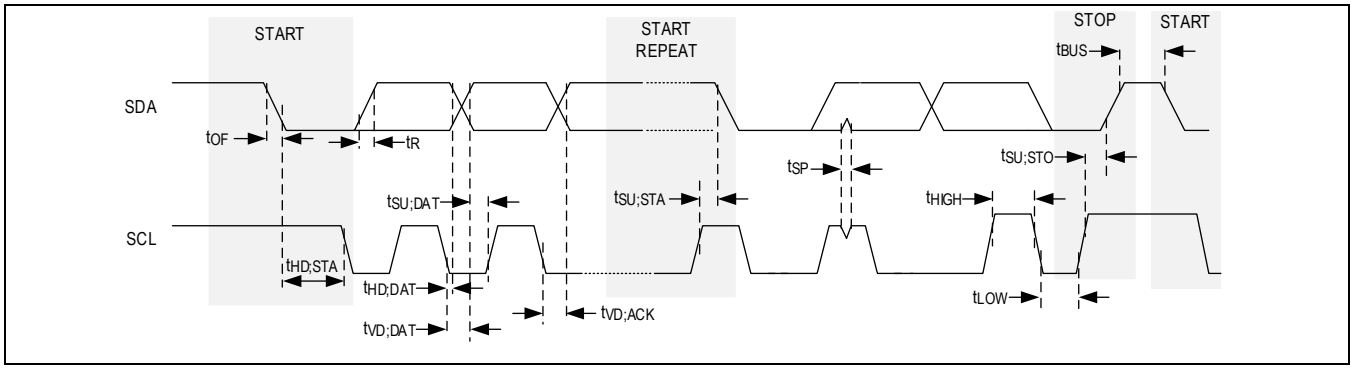


Figure 1. I²C Timing Diagram

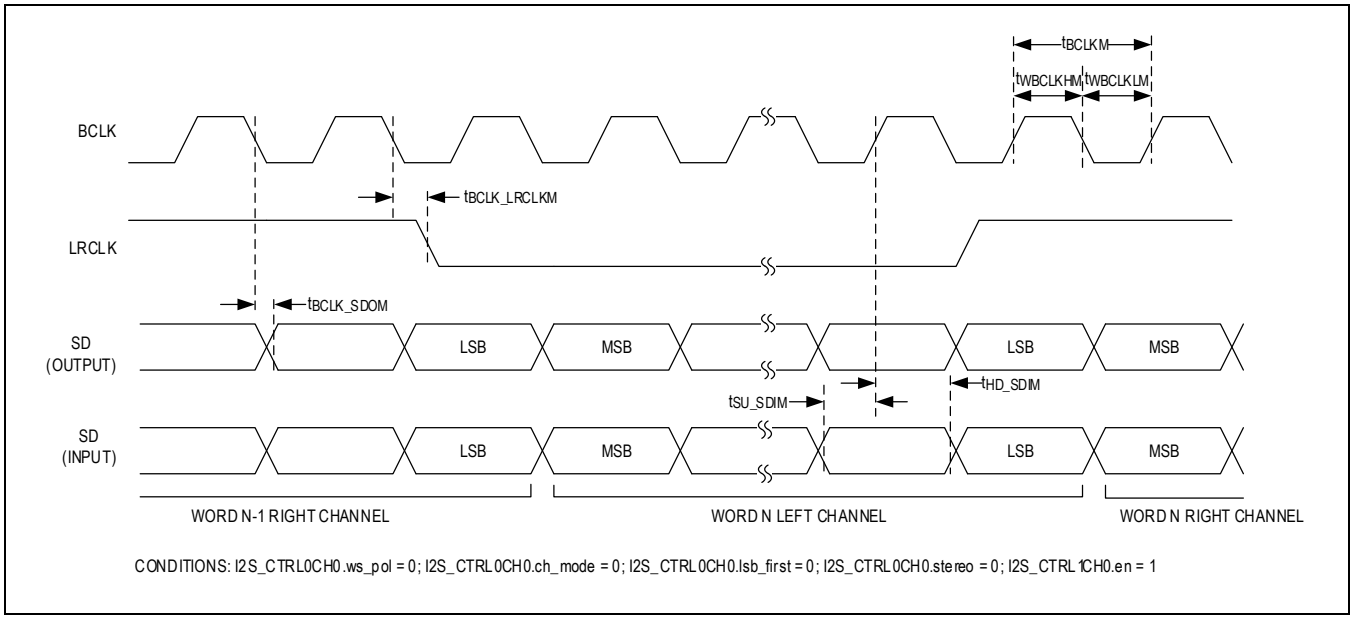


Figure 2. I²S Controller Timing Diagram

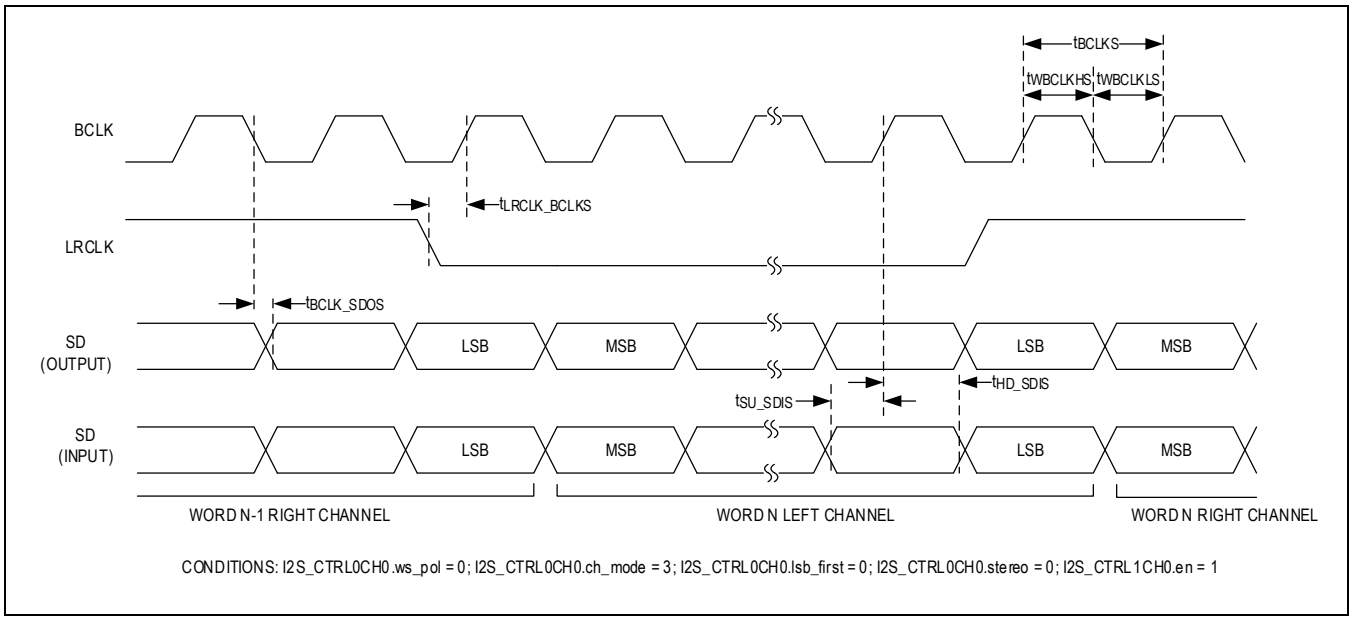


Figure 3. I²S Target Timing Diagram

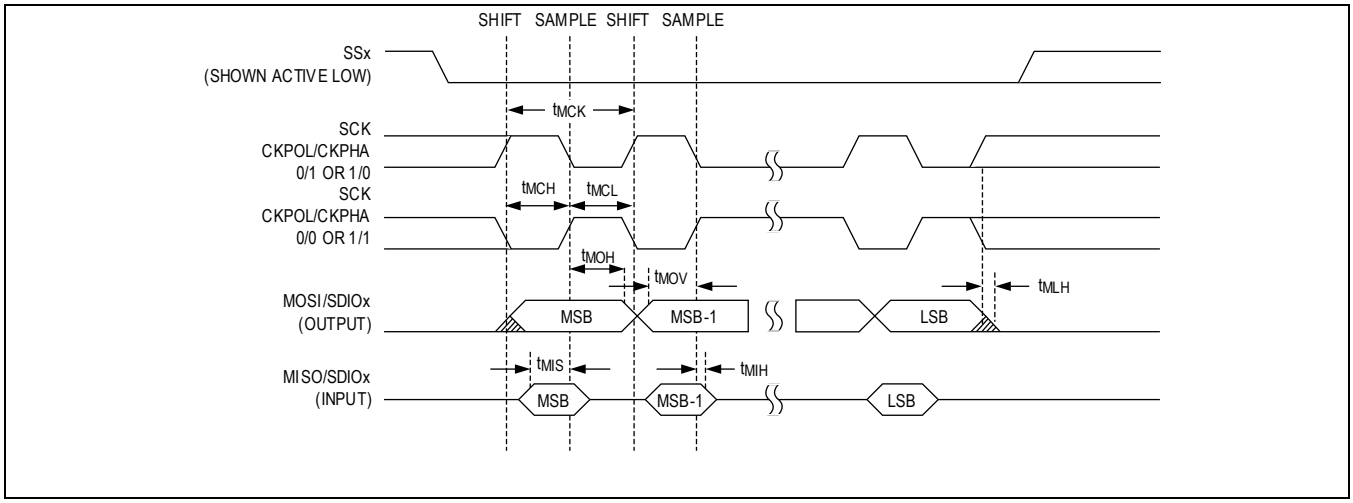


Figure 4. SPI Controller Mode Timing Diagram

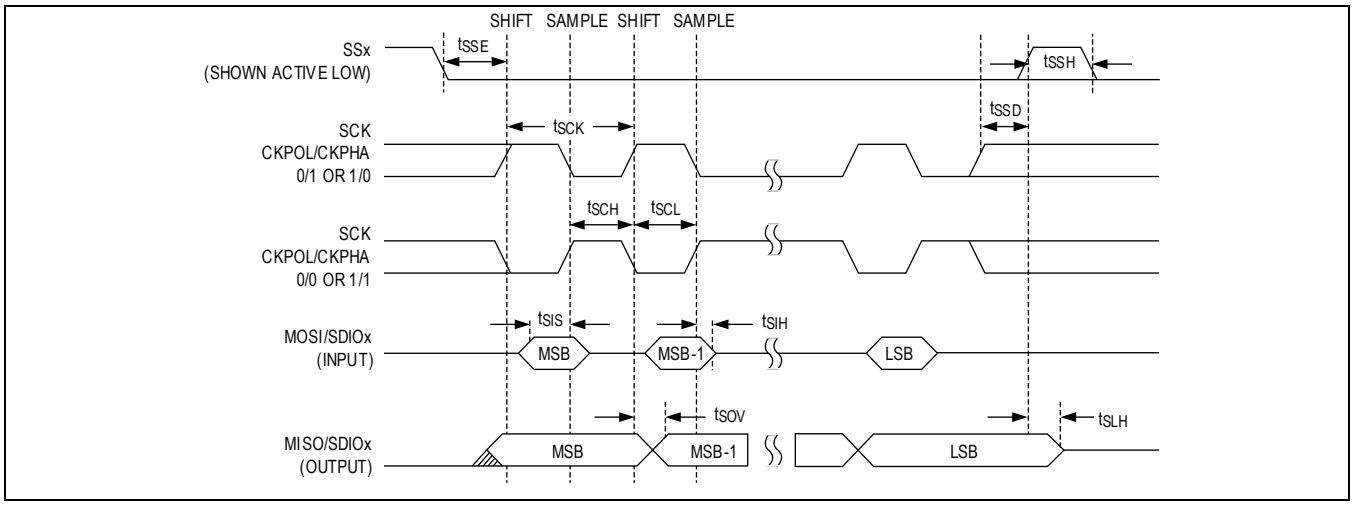
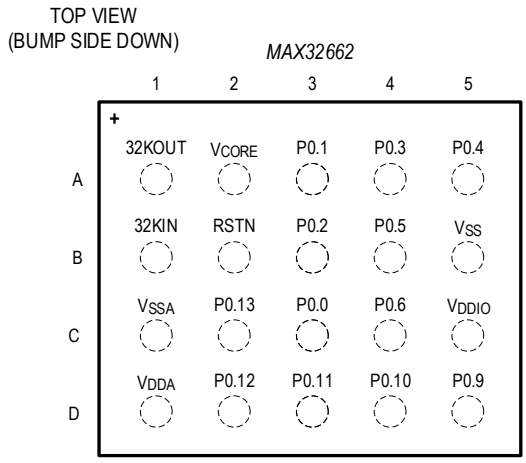


Figure 5. SPI Target Mode Timing Diagram

Pin Configuration – 20 WLP



20 WLP
(2.30mm x 1.92mm)

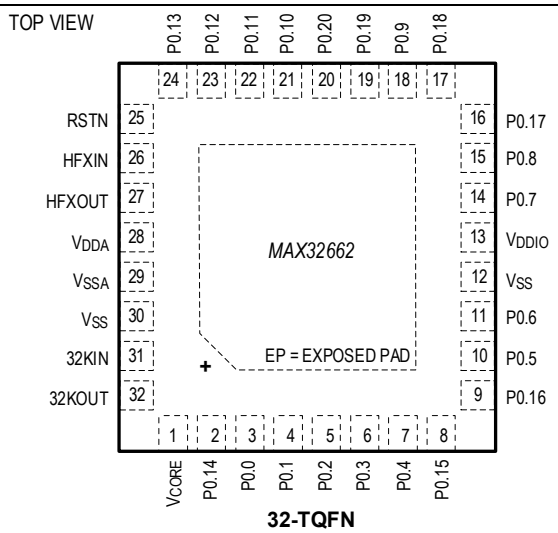
Pin Descriptions – 20 WLP

PIN	NAME	FUNCTION MODES						FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function3	Alternate Function4	Alternate Function5	
POWER								
A2	V_{CORE}	—	—	—	—	—	—	Digital Supply Voltage. Bypass with 1µF to V_{SS}.
C5	V_{DDIO}	—	—	—	—	—	—	GPIO Supply Voltage. Bypass with 1µF to V_{SS}. This pin must be connected to the V_{DDA} device pin at the PCB level.
D1	V_{DDA}	—	—	—	—	—	—	Analog Supply Voltage. Bypass this pin to V_{SSA} with 1µF. This pin must be connected to the V_{DDIO} device pin at the PCB level.
C1	V_{SSA}	—	—	—	—	—	—	Analog Ground
B5	V_{SS}	—	—	—	—	—	—	Digital Ground
RESET AND CONTROL								
B2	RSTN	—	—	—	—	—	—	Active-Low, External System Reset Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a system reset and begins execution. This pin has an internal pull-up, R_{PU_VDDIO}, to the V_{DDIO} supply.
CLOCK								

PIN	NAME	FUNCTION MODES						FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function3	Alternate Function4	Alternate Function5	
A1	32KOUT	—	—	—	—	—	—	32kHz Crystal Oscillator Output. Refer to the *MAX32662 User Guide* for determination of the required external stability capacitors.
B1	32KIN	—	—	—	—	—	—	32kHz Crystal Oscillator Input. Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Refer to the *MAX32662 User Guide* for determination of the required external stability capacitors. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
GPIO AND ALTERNATE FUNCTION								
C3	P0.0	P0.0	SWDIO	PT0B	TMR0C_OA	TMR1D_OA	ADC_TRIG_E	Serial-Wire Debug I/O; Pulse Train 0 Port Map B; TMR0 Output 32 Bits or Lower 16 Bits Port Map C; TMR1 Output 32 Bits or Lower 16 Bits Port Map D; ADC Trigger Input Port Map E
A3	P0.1	P0.1	SWDCLK	PT1B	TMR0C_IA	TMR1D_IA	—	Serial-Wire Debug Clock; Pulse Train 1 Port Map B; TMR0 Input 32 Bits or Lower 16 Bits Port Map C; TMR1 Input 32 Bits or Lower 16 Bits Port Map D
B3	P0.2	P0.2	SPI0A_CITO	UART1B_TX	TMR0C_IA	PT0D	I2S0E_SDO	SPI0 Controller In Target Out Port Map A; UART1 Transmit Port Map B; TMR0 Input 32 Bits or Lower 16 Bits Port Map C; Pulse Train 0 Port Map D; I2S0 Serial Data Output Port Map E
A4	P0.3	P0.3	SPI0A_COPI	UART1B_RX	TMR0C_OA	PT1D	I2S0E_SDI	SPI0 Controller Out Target In Port Map A; UART1 Receive Port Map B; TMR0 Output 32 Bits or Lower 16 Bits Port Map C; Pulse Train 1 Port Map D; I2S0 Serial Data Input Port Map E
A5	P0.4	P0.4	SPI0A_SCK	UART1B_CTS	TMR1C_IA	PT2D	I2S0E_BCLK	SPI0 Serial Clock Port Map A; UART1 CTS Port Map B; TMR1 Input 32 Bits or Lower 16 Bits Port Map C; Pulse Train 2 Port Map D; I2S0 Bit Clock Port Map E
B4	P0.5	P0.5	SPI0A_TS0	UART1B_RTS	TMR1C_OA	PT3D	I2S0E_LRCLK	SPI0 Target Select 0 Port Map A; UART1 RTS Port Map B; TMR1 Output 32 Bits or Lower 16 Bits Port Map C; Pulse Train 3 Port Map D; I2S0 Left/Right Clock Port Map E
C4	P0.6	P0.6 (SCPBL default	I2C1A_SCL	CAN0B_RX	TMR2C_IA	HF_EXT_CLK	PT2E	I2C1 SCL Port Map A; CAN Receive Port Map B; TMR2 Input 32 Bits or Lower 16 Bits Port Map C; External Clock Input; Pulse Train 2 Port Map

PIN	NAME	FUNCTION MODES						FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function3	Alternate Function4	Alternate Function5	
		stimulus pin)						E. See *Bootloader Activation* for more information.
D5	P0.9	P0.9	I2C1A_SDA	CAN0B_TX	TMR2C_OA	ADC_TRIG_D	PT3E	I2C1 SDA Port Map A; CAN Transmit Port Map B; TMR2 Output 32 Bits or Lower 16 Bits Port Map C; ADC Trigger Input Port Map D; Pulse Train 3 Port Map E
D4	P0.10	P0.10	UART0A_TX	SPI1B_TS0	—	AIN3/AIN_C0_P/AIN_C1_P	—	UART0 Transmit Port Map A; SPI1 Target Select 0 Port Map B; ADC Input 3/Comparator 0/1 Positive Input
D3	P0.11	P0.11	UART0A_RX	SPI1B_SCK	32KCAL	AIN2/AIN_C0_P/AIN_C1_P	LP_EXT_CLK	UART0 Receive Port Map A; SPI1 Serial Clock Port Map B; 32.768kHz Calibration Output; ADC Input 2/Comparator 0/1 Positive Input; LPTMR0 External Clock Input
D2	P0.12	P0.12	I2C0A_SCL	SPI1B_COTI	LPTMR0C_IA	AIN1/AIN_C0_N/AIN_C1_N	LPTMR0E_OAN	I2C0 SCL Port Map A; SPI1 Controller Out Target In Port Map B; LPTMR0 Input 32 Bits or Lower 16 Bits Port Map C; ADC Input 1/Comparator 0/1 Negative Input; LPTMR0 Inverted Output 32 Bits or Lower 16 Bits Port Map E
C2	P0.13	P0.13	I2C0A_SDA	SPI1B_CITO	LPTMR0C_OA	AIN0/VREF/AIN_C0_N/AIN_C1_N	—	I2C0 SDA Port Map A; SPI1 Controller In Target Out Port Map B; LPTMR0 Output 32 Bits or Lower 16 Bits Port Map C; ADC Input 0/Comparator 0/1 Negative Input; ADC Reference. When used as V_{REF} for the ADC, requires 1µF bypass to V_{SSA} and AIN0 is not available.

Pin Configuration – 32 TQFN



32-TQFN
5mm x 5mm x 0.5mm pitch

Pin Descriptions – 32 TQFN

PIN	NAME	FUNCTION MODES						FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	Alternate Function 5	
POWER								
1	V_{CORE}	—	—	—	—	—	—	Digital Supply Voltage. Bypass with 1µF to V_{SS}.
13	V_{DDIO}	—	—	—	—	—	—	GPIO Supply Voltage. Bypass with 1µF to V_{SS}. This pin must be connected to the V_{DDA} device pin at the PCB level.
28	V_{DDA}	—	—	—	—	—	—	Analog Supply Voltage. This pin must be connected to the V_{DDIO} device pin at the PCB level. Bypass this pin to V_{SSA} with 1µF.
29	V_{SSA}	—	—	—	—	—	—	Analog Ground
12, 30	V_{SS}	—	—	—	—	—	—	Digital Ground
EP	V_{SS}	—	—	—	—	—	—	Digital Ground. Exposed pad. This pad must be connected to V_{SS}. Refer to the *MAX32662 User Guide* for additional information.
RESET AND CONTROL								
25	RSTN	—	—	—	—	—	—	Active-Low, External System Reset Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state,

PIN	NAME	FUNCTION MODES						FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	Alternate Function 5	
								the device performs a system reset and begins execution. This pin has an internal pull-up, R_{PU_VDDIO}, to the V_{DDIO} supply.
CLOCK								
32	32KOUT	—	—	—	—	—	—	32kHz Crystal Oscillator Output. Refer to the *MAX32662 User Guide* for determination of the required external stability capacitors.
31	32KIN	—	—	—	—	—	—	32kHz Crystal Oscillator Input. Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Refer to the *MAX32662 User Guide* for determination of the required external stability capacitors. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
26	HFXIN	—	—	—	—	—	—	High-Frequency Crystal Oscillator Input. Connect a crystal between HFXIN and HFXOUT. Refer to the *MAX32662 User Guide* for determination of the required external stability capacitors. Optionally, this pin can be configured as the input for an external square-wave source.
27	HFXOUT	—	—	—	—	—	—	High-Frequency Crystal Oscillator Output. Connect a crystal between HFXIN and HFXOUT. Refer to the *MAX32662 User Guide* for determination of the required external stability capacitors.
GPIO AND ALTERNATE FUNCTION								
3	P0.0	P0.0	SWDIO	PT0B	TMR0C_OA	TMR1D_OA	ADC_TRIG_E	Serial Wire Debug I/O; Pulse Train 0 Port Map B; TMR0 Output 32 Bits or Lower 16 Bits Port Map C; TMR1 Output 32 Bits or Lower 16 Bits Port Map D; ADC Trigger Input Port Map E
4	P0.1	P0.1	SWDCLK	PT1B	TMR0C_IA	TMR1D_IA	—	Serial Wire Debug Clock; Pulse Train 1 Port Map B; TMR0 Input 32 Bits or Lower 16 Bits Port Map C; TMR1 Input 32 Bits or Lower 16 Bits Port Map D

PIN	NAME	FUNCTION MODES						FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	Alternate Function 5	
5	P0.2	P0.2	SPI0A_CITO	UART1B_TX	TMR0C_IA	PT0D	I2S0E_SDO	SPI0 Controller In Target Out Port Map A; UART1 Transmit Port Map B; TMR0 Input 32 Bits or Lower 16 Bits Port Map C; Pulse Train 0 Port Map D; I2S0 Serial Data Output Port Map E
6	P0.3	P0.3	SPI0A_COTI	UART1B_RX	TMR0C_OA	PT1D	I2S0E_SDI	SPI0 Controller Out Target In Port Map A; UART1 Receive Port Map B; TMR0 Output 32 Bits or Lower 16 Bits Port Map C; Pulse Train 1 Port Map D; I2S0 Serial Data Input Port Map E
7	P0.4	P0.4	SPI0A_SCK	UART1B_CTS	TMR1C_IA	PT2D	I2S0E_BCLK	SPI0 Serial Clock Port Map A; UART1 CTS Port Map B; TMR1 Input 32 Bits or Lower 16 Bits Port Map C; Pulse Train 2 Port Map D; I2S0 Bit Clock Port Map E
10	P0.5	P0.5	SPI0A_TS0	UART1B_RTS	TMR1C_OA	PT3D	I2S0E_LRCLK	SPI0 Target Select 0 Port Map A; UART1 RTS Port Map B; TMR1 Output 32 Bits or Lower 16 Bits Port Map C; Pulse Train 3 Port Map D; I2S0 Left/Right Clock Port Map E
11	P0.6	P0.6 (SCPBL default stimulus pin)	I2C1A_SCL	CAN0B_RX	TMR2C_IA	HF_EXT_CLK	PT2E	I2C1 SCL Port Map A; CAN Receive Port Map B; TMR2 Input 32 Bits or Lower 16 Bits Port Map C; External Clock Input; Pulse Train 2 Port Map E. See *Bootloader Activation* for more information.
14	P0.7	P0.7	SPI1A_CITO	UART0B_CTS	TMR2C_IA	UART0D_RX	—	SPI1 Controller In Target Out Port Map A; UART0 CTS Port Map B; TMR2 Input 32 Bits or Lower 16 Bits Port Map C; UART0 Receive Port Map D
15	P0.8	P0.8	SPI1A_COTI	UART0B_RTS	TMR2C_OA	UART0D_TX	—	SPI1 Controller Out Target In Port Map A; UART0 RTS Port Map B; TMR2 Output 32 Bits or Lower 16 Bits Port Map C; UART0 Transmit Port Map D
18	P0.9	P0.9	I2C1A_SDA	CAN0B_TX	TMR2C_OA	ADC_TRIG_D	PT3E	I2C1 SDA Port Map A; CAN Transmit Port Map B; TMR2 Output 32 Bits or Lower 16 Bits Port Map C; ADC Trigger Input Port Map D; Pulse Train 3 Port Map E
21	P0.10	P0.10	UART0A_TX	SPI1B_TS0	—	AIN3/AIN_C0_P/AIN_C1_P	—	UART0 Transmit Port Map A; SPI1 Target Select 0 Port Map B; ADC Input 3/Comparator 0/1 Positive Input

PIN	NAME	FUNCTION MODES						FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	Alternate Function 5	
22	P0.11	P0.11	UART0A_RX	SPI1B_SCK	32KCAL	AIN2/AIN_C0_P/AIN_C1_P	LP_EXT_CLK	UART0 Receive Port Map A; SPI1 Serial Clock Port Map B; 32.768kHz Calibration Output; ADC Input 2/Comparator 0/1 Positive Input; LPTMR0 External Clock Input
23	P0.12	P0.12	I2C0A_SCL	SPI1B_COTI	LPTMR0C_IA	AIN1/AIN_C0_N/AIN_C1_N	LPTMR0E_OAN	I2C0 SCL Port Map A; SPI1 Controller Out Target In Port Map B; LPTMR0 Input 32 Bits or Lower 16 Bits Port Map C; ADC Input 1/Comparator 0/1 Negative Input; LPTMR0 Inverted Output 32 Bits or Lower 16 Bits Port Map E
24	P0.13	P0.13	I2C0A_SDA	SPI1B_CITO	LPTMR0C_OA	AIN0/VREF/AIN_C0_N/AIN_C1_N	—	I2C0 SDA Port Map A; SPI1 Controller In Target Out Port Map B; LPTMR0 Output 32 Bits or Lower 16 Bits Port Map C; ADC Input 0/Comparator 0/1 Negative Input; When used as V_{REF} for the ADC, requires 1µF bypass to V_{SSA} and AIN0 is not available.
2	P0.14	P0.14	PT0A	—	—	—	—	Pulse Train 0 Port Map A
8	P0.15	P0.15	PT1A	CAN0B_RX	TMR2C_IA	TMR0D_IA	—	Pulse Train 1 Port Map A; CAN Receive Port Map B; TMR2 Input 32 Bits or Lower 16 Bits Port Map C; TMR0 Input 32 Bits or Lower 16 Bits Port Map D
9	P0.16	P0.16	PT2A	CAN0B_TX	TMR2C_OA	TMR0D_OA	—	Pulse Train 2 Port Map A; CAN Transmit Port Map B; TMR2 Output 32 Bits or Lower 16 Bits Port Map C; TMR0 Output 32 Bits or Lower 16 Bits Port Map D
16	P0.17	P0.17	SPI1A_SCK	—	ADC_TRIG_C	UART0D_CTS	—	SPI1 Serial Clock Port Map A; ADC Trigger Input Port Map C; UART0 CTS Port Map D
17	P0.18	P0.18	SPI1A_TS0	—	—	UART0D_RTS	—	SPI1 Target Select 0 Port Map A; UART0 RTS Port Map D
19	P0.19	P0.19	UART0A_RTS	—	TMR1C_IA	—	—	UART0 RTS Port Map A; TMR1 Input 32 Bits or Lower 16 Bits Port Map C
20	P0.20	P0.20	UART0A_CTS	—	TMR1C_OA	—	—	UART0 CTS Port Map A; TMR1 Output 32 Bits or Lower 16 Bits Port Map C

Detailed Description

The device features five powerful and flexible power modes, and can operate from a single-supply battery or a dual-supply provided by a PMIC. The I2C ports support Standard-mode, Fast-mode, Fast-mode Plus, and High-speed modes, operating up to 3400kbps. The SPI ports can run up to 50MHz in both controller and peripheral mode. The 12-bit SAR ADC provides an integrated reference generator and a single-ended input multiplexer. The integrated CAN 2.0B interface is compliant with Bosch CAN 2.0B specification (2.0B Active) according to ISO 11898-1. Three general-purpose 32-bit timers, one low-power 32-bit timer, one windowed watchdog timer, and a real-time clock (RTC) are also provided. An I2S interface provides digital audio streaming to a codec. An Elliptic Curve Digital Signature Algorithm (ECDSA)-based cryptographic secure bootloader is available in ROM.

Arm Cortex-M4 Processor with FPU Engine

The Arm Cortex-M4 with FPU processor combines high-efficiency signal processing functionality with low power, low cost, and ease of use.

The Arm Cortex-M4 with FPU DSP supports single instruction, multiple data (SIMD) path DSP extensions, providing:

- Four parallel 8-bit add/sub
- Floating point single precision
- Two parallel 16-bit add/sub
- Two parallel MACs
- 32- or 64-bit accumulate
- Signed, unsigned, data with or without saturation

Memory

Internal Flash Memory

The 256KB internal flash memory provides nonvolatile storage of program and data memory.

Internal SRAM

The internal 80KB SRAM provides low-power retention of application information in all power modes except STORAGE. The SRAM can be divided into granular banks that create a flexible SRAM retention architecture. This data retention feature is optional and is configurable. This granularity allows the application to minimize its power consumption by only retaining the essential data.

Clocking Scheme

The internal primary oscillator (IPO) operates at a nominal frequency of 100MHz. Optionally, the software can select one of five other oscillators depending upon power needs:

- 80kHz oscillator (INRO)
- 32.768kHz oscillator (external crystal required) (ERTCO)
- 7.3728MHz oscillator (IBRO)
- 16MHz–32MHz oscillator (external crystal required) (ERFO)
- External square-wave clocks up to 50MHz

This IPO is the primary clock source for digital logic and peripherals. An external 32.768kHz timebase is required when using the RTC. A separate external square-wave clock can be used as a source for LPTMR0 in the always-ON domain.

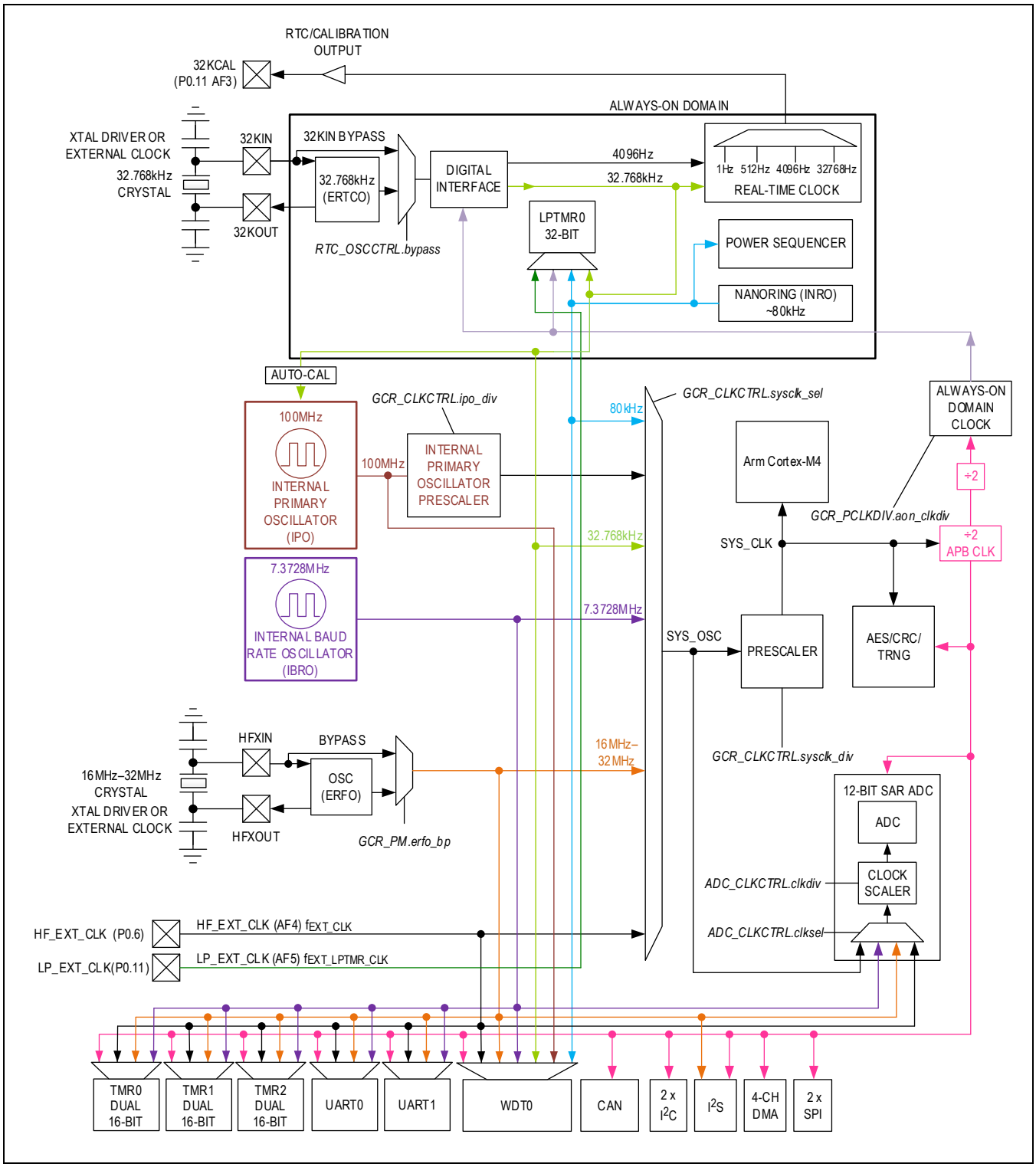


Figure 6. Clocking Scheme Diagram

General-Purpose I/O and Special Function Pins

Most general-purpose I/O (GPIO) pins share both a firmware-controlled I/O function and one or more special function signals associated with peripheral modules. Software can individually enable pins for GPIO or peripheral special function use. Configuring a pin as a special function supersedes its use as a software-controlled I/O. Multiplexing between peripheral and GPIO functions is usually static but can also be done dynamically by software. The electrical characteristics of a GPIO pin are identical whether the pin is configured as an I/O or special function, except where explicitly noted in the *Electrical Characteristics* tables.

In GPIO mode, each pin of a port has an interrupt function that can be independently enabled by software and configured as a level- or edge-sensitive interrupt. All GPIOs share the same interrupt vector. Some packages do not have all of the GPIOs available.

When configured as GPIOs, the following features are provided. These features can be independently enabled or disabled on a per-pin basis.

- Configurable as input, output, bidirectional, or high-impedance
- Optional internal pull-up resistor or internal pull-down resistor when configured as input
- Exit from low-power modes on rising or falling edge
- Selectable standard- or high-drive modes

The MAX32662 provides up to 21 GPIOs for the 32-pin TQFN.

Standard DMA Controller

The standard direct memory access (DMA) controller provides a means to offload the CPU for memory/peripheral data transfer leading to a more power-efficient system. It allows automatic one-way data transfer between two entities. These entities can be either memories or peripherals. The transfers are done without using CPU resources. The DMA peripheral supports the following features:

- 4 channel
- Peripheral to SRAM transfer
- SRAM to peripheral transfer
- SRAM to SRAM transfer
- Event support
- All DMA transactions consist of an AHB burst read into the DMA FIFO followed immediately by an AHB burst write from the FIFO.

Power Management

Power Management Unit

The power management unit (PMU) provides the optimal mix of high-performance and low-power consumption. It exercises intelligent, precise control of power distribution to the CPU and peripheral circuitry.

The PMU provides the following features:

- User-configurable system clock
- Automatic enabling and disabling of crystal oscillators based on power mode
- Multiple clock domains
- Unused peripherals can be selectively powered down
- Fast wake up of powered-down peripherals when activity detected

Operating Modes

ACTIVE

In this mode, the CPU executes software, and all digital and analog peripherals are available on demand. Dynamic clocking disables local clocks in peripherals that are not in use. This mode corresponds to the Arm Cortex-M4 processor with FPU ACTIVE mode.

SLEEP

This mode allows for lower power consumption operations than ACTIVE mode. The CPU is asleep, peripherals are on, and the standard DMA block is available. The GPIO or any active peripheral can be configured to interrupt and cause a transition to ACTIVE mode. This mode corresponds to the Arm Cortex-M4 processor's SLEEP mode.

DEEPSLEEP

In this mode, CPU and critical peripheral configuration settings and all volatile memory is preserved.

The device status is as follows:

- The CPU is powered down. System state and all SRAM is retained.
- The GPIO pins retain their state.
- The transition from DEEPSLEEP to ACTIVE mode is faster than the transition from BACKUP mode because system initialization is not required.
- The system oscillators are all disabled to provide additional power savings over SLEEP mode.
- The LPTMR0 can be active and is an optional wake-up source.

This mode corresponds to the Arm Cortex-M4 processor's DEEPSLEEP mode.

BACKUP

This mode places the CPU in a static, low-power state. The BACKUP mode supports the same wake-up sources as DEEPSLEEP mode.

The device status is as follows:

- CPU is powered down.
- SRAM retention as per *Table 1*.
- LPTMR0 can be active and is an optional wake-up source.

Table 1. BACKUP Mode SRAM Retention

SRAM BLOCK	SRAM SIZE	RETAINED SRAM
SYSRAM0	20KB	17KB
SYSRAM1	20KB	18KB
SYSRAM2	20KB	19KB
SYSRAM3	20KB	20KB

Note: The boot ROM uses certain ranges of system RAM during a system reset, watchdog timer reset, an external reset, and an exit from BACKUP. The device uses this RAM to perform system checks. As a result, not all of each RAM can be retained during an exit from BACKUP. Refer to the *MAX32662 User Guide* for additional details.

STORAGE

The device status is as follows:

- The CPU is powered off.
- All peripherals are powered off.
- Wake up from GPIO interrupt.
- The RTC can be enabled by software before entering STORAGE mode.
- No SRAM retention.

Wake-Up Sources

The wake-up sources from the SLEEP, DEEPSLEEP, BACKUP, and STORAGE modes are summarized in *Table 2*.

Table 2. Wake-Up Sources

OPERATING MODE	WAKE-UP SOURCE
SLEEP	Interrupts (GPIO or any active peripheral), RSTN assertion
DEEPSLEEP	Interrupts (RTC, GPIO), RSTN assertion, LPTMR0
BACKUP	Interrupts (RTC, GPIO), RSTN assertion, LPTMR0
STORAGE	Interrupts (RTC, GPIO), RSTN assertion

Real-Time Clock (RTC)

An RTC keeps the time of day in absolute seconds. The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software.

The RTC provides a time-of-day alarm programmed by software to any future value between 1 second and 12 days. When configured for long intervals, the time-of-day alarm can be used as a power-saving timer, allowing the device to remain in an extremely low-power mode but still awaken periodically to perform assigned tasks. Software can program a second independent 32-bit 1/4096 sub-second alarm between 244µs and 12 days. Both can be configured as recurring alarms. When enabled, either alarm can cause an interrupt or wake the device from most low-power modes.

The time base is generated by a 32.768kHz crystal or an external clock source that must meet the electrical/timing requirements in the *Electrical Characteristics* table.

An RTC calibration feature allows the software to compensate for minor variations in the RTC oscillator, crystal, temperature, and board layout. Enabling the 32KCAL alternate function outputs a timing signal derived from the RTC. External hardware can measure the frequency and adjust the RTC frequency in increments of ±127ppm with a 1ppm resolution. Under most circumstances, the oscillator does not require any calibration.

Windowed Watchdog Timer (WDT)

Microcontrollers are often used in harsh environments where electrical noise and electromagnetic interference (EMI) are abundant. Without proper safeguards, these hazards can disturb device operation and corrupt program execution. One of the most effective countermeasures is the WDT, which detects runaway code or system unresponsiveness.

The WDT is a 32-bit, free-running counter with a configurable prescaler. When enabled, the WDT must be periodically reset by the application software. Failure to reset the WDT within the user-configurable timeout period indicates that the application software is not operating correctly and results in a WDT timeout. A WDT timeout can trigger an interrupt, system reset, or both. Either response forces the instruction pointer to a known good location before resuming instruction execution. The windowed timeout period feature provides more detailed monitoring of system operation, requiring the WDT to be reset within a specific time window.

The WDT supports multiple clock options:

- IPO
- ERFO (external crystal required)
- IBRO
- INRO
- ERTCO (external crystal required)
- External clock input
- Peripheral clock (PCLK)

32-Bit Timer/Counter/PWM

General-purpose, 32-bit timers provide timing, capture/compare, or generate pulse-width modulated (PWM) signals with minimal software interaction.

The timer provides the following features:

- 32-bit up/down auto-reload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External pin multiplexed with GPIO for timer input, clock gating, or capture
- Timer output pin
- TMR0-TMR3 configurable as 2 × 16-bit general-purpose timers
- Timer interrupt

I/O functionality is supported for all of the timers. Note that the function of a port can be multiplexed with other functions on the GPIO pins, so it might not be possible to use all the ports depending on the device configuration. See *Table 3* for individual timer features.

Table 3. Timer Configuration Options

INSTANCE	32-BIT	DUAL 16-BIT	MODE	CLOCK SOURCE						
				PCLK	IBRO	ERFO	INRO	ERTCO	HF_EXT_CLK	LP_EXT_CLK
TMR0	Yes	Yes	ACTIVE	Yes	Yes	Yes	No	No	Yes	No
TMR1	Yes	Yes	ACTIVE	Yes	Yes	Yes	No	No	Yes	No
TMR2	Yes	Yes	ACTIVE	Yes	Yes	Yes	No	No	Yes	No
LPTMR0	Yes	No	ACTIVE/SLEEP/ DEEPSLEEP/ BACKUP	Yes	No	No	Yes	Yes	No	Yes

Serial Peripherals

Controller Area Network (CAN) 2.0B

The integrated CAN 2.0B interface is compliant with the Bosch CAN 2.0B (active) specification according to ISO 11898-1.

The following are the key features of the interface:

- Compliant with ISO 11898-1:2015 specification
- Supports up to 8-byte data frame
- Selectable ID type
  - 11-bit standard ID
  - 11-bit standard ID + 18-bit extended ID
- Selectable frame type.
  - Data frame (remote transmission request (RTR) = 0)
  - Remote frame (RTR = 1)
- Hardware message filtering (dual/single filters)
- DMA support for transmit and receive
- 128-byte transmit buffer and 256-byte receive buffer
- Overload frame is generated on a FIFO overflow
- Protocol exception event detection
- Normal and Listen Only modes supported
- Transmitter delay compensation up to 3 data bits long
- Single-shot transmission
- Readable error counters

- Last error code
- Sleep mode and wake-up unit

I2C Interface

The I2C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many, or many-to-many communications medium. These engines support Standard-mode, Fast-mode, Fast-mode Plus, and High-speed mode I2C speeds.

The I2C interface provides the following features:

- Controller or Target mode operation
  - Supports up to four different addresses in Target mode
- Supports standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive receive mode
- Transmit FIFO preloading
- Support for clock stretching to allow slower target devices to operate on higher speed busses
- Multiple transfer rates
  - Standard-mode: 100kbps
  - Fast-mode: 400kbps
  - Fast-mode Plus: 1000kbps
  - High-speed mode: 3400kbps
- Internal filter to reject noise spikes
- 8-byte receive FIFO
- 8-byte transmit FIFO

Serial Peripheral Interface (SPI)

The SPI is a highly configurable, flexible, and efficient synchronous interface between multiple SPI devices on a single bus. The bus uses a single clock signal and multiple data signals and one or more target select lines to address only the intended target device. The SPI operates independently and requires minimal processor overhead.

The provided SPI peripherals can operate in either target or controller mode and provide the following features:

- SPI modes 0, 1, 2, and 3 for single-bit communication
- 3- or 4-wire mode for single-bit target device communication
- Full-duplex operation in single-bit, 4-wire mode
- Multicontroller mode fault detection
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- 32-byte transmit FIFO
- 32-byte receive FIFO
- Target select assertion and deassertion timing relative to leading/trailing SCK edge

See *Table 4* for configuration options.

Table 4. SPI Configuration Options

INSTANCE	INTERFACE FORMAT	TARGET SELECT LINES	MAXIMUM FREQUENCY (CONTROLLER MODE) (MHz)	MAXIMUM FREQUENCY (TARGET MODE) (MHz)
SPI0	3 wire, 4 wire	1	50	50
SPI1	3 wire, 4 wire	1	50	50

I²S Interface

The I²S interface is a bidirectional, 4-wire serial bus that provides serial communications for codecs and audio amplifiers compliant with the I²S Bus Specification, June 5, 1996.

The I²S interface provides the following features:

- Controller and Target mode operation
- Support for four channels
- 8-, 16-, 24-, and 32-bit frames
- Receive and transmit DMA support
- Wake-up on FIFO status (full/empty/threshold)
- Pulse density modulation support for the receive channel
- Word select polarity control
- First-bit position selection
- Interrupts generated for FIFO status
- 32-byte receive FIFO
- 32-byte transmit FIFO

Universal Asynchronous Receiver Transmitter (UART) Interface

The UART interface supports full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry-standard request-to-send (RTS) and clear-to-send (CTS) flow control signaling. Each UART is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 8-byte receive FIFO
- 8-byte transmit FIFO
- Full-duplex operation for asynchronous data transfers
- Interrupts available for:
  - Frame error
  - Parity error
  - CTS
  - Receive FIFO overrun
  - FIFO full/partially full conditions
- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th-bit parity support
- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Two DMA channels can be connected (read and write FIFOs)
- Programmable word size (5 bits to 8 bits)

See *Table 5* for configuration options.

Table 5. UART Configuration Options

INSTANCE	PACKAGE		MODE	CLOCK SOURCES					
	20 WLP	32 TQFN		PCLK	IBRO	ERFO	INRO	ERTCO	HF_EXT_CLK
UART0	4 wire	4 wire	ACTIVE	Yes	Yes	Yes	No	No	Yes
UART1	2 wire	4 wire	ACTIVE	Yes	Yes	Yes	No	No	Yes

Analog-to-Digital Converter (ADC)

The 12-bit SAR ADC provides an integrated reference generator and a single-ended input multiplexer. The multiplexer selects an input channel from one of the four external analog alternate function input signals (AIN0–AIN3) and the internal power supply inputs.

The reference for the ADC can be:

- External alternate function V_{REF} input shared with AIN0, AIN_C0_N1, and AIN_C1_N1.
- Internal 1.25V
- Internal 2.048V

The ADC measures the following voltages:

- AIN[3:0] up to V_{DDIO}
- $V_{DDIO} \div 4$
- V_{CORE}
- $V_{DDA} \div 2$
- V_{SSA}

Security

AES

The dedicated hardware-based AES engine supports the following algorithms:

- AES-128
- AES-192
- AES-256

The AES keys are generated by the TRNG and the application software can store the keys in secure NV memory.

True Random Number Generator (TRNG)

Random numbers are a vital part of a secure application. They are used as cryptographic seeds or to create strong encryption keys to ensure data privacy. Software can use random numbers to trigger asynchronous events that cause nondeterministic behavior. This helps thwart replay or key search attacks.

The TRNG is continuously fed by a physically-unpredictable, high-entropy source. It generates a 128-bit true random number in 128 system clock cycles.

The TRNG can support the system-level validation of many security standards.

CRC Module

A cyclic redundancy check (CRC) hardware module provides fast calculations and data integrity checks by application software. The CRC polynomial is programmable to support custom CRC algorithms as well as the common algorithms shown in *Table 6*.

Table 6. Common CRC Polynomials

ALGORITHM	POLYNOMIAL EXPRESSION
CRC-32-ETHERNET	$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + x^0$
CRC-CCITT	$x^{16} + x^{12} + x^5 + x^0$
CRC-16	$x^{16} + x^{15} + x^2 + x^0$
USB DATA	$x^{16} + x^{15} + x^2 + x^0$
PARITY	$x^1 + x^0$

Root of Trust

On devices that support SCPBL, the root of trust starts with trusted software and the microcontroller's complement of security features. Communications between a host and the device must be secure and authenticated, and program integrity must be verified each time before execution to ensure the device's trustworthiness. The device's root of trust is based on a secret Analog Devices root verification key and a signed customer verification key (CVK). Customers submit their public CVK, which is then signed, and a certificate is sent back to the customer. This process is quick and required only once, before the software is released for the first time, and is unnecessary during the software development. A customer can then load their own key and download their signed binary executable code.

Secure Communications Protocol Bootloader (SCPBL)

On devices that support SCPBL, communication between a host system and the device uses a system of ECDSA-256 digitally signed packets. This guarantees the integrity and authenticity of all communication before executing configuration commands and the loading or verification of program memory. One or more serial interfaces are available for communication. This also enables the assembly and programming of the customer's final product by third-party assembly houses without the required cost and complexity of ensuring that the assembly house implements and maintains a secure production facility. It also allows for in-field software upgrades to deployed products, thus eliminating the costly need to return a product to the manufacturer for any software changes.

The serial interfaces available for SCPBL communication are shown in *Table 7*. Following any reset or exit from certain low-power modes, the device tests the assigned stimulus pin and, if active, begins an SCPBL session. The stimulus pin can be reassigned once an SCPBL session begins. The host can disable the bootloader interface before deployment to prevent any changes to program memory.

See the *Ordering Information* table for availability.

Secure Boot

On devices that support SCPBL, following every reset, the device performs a secure boot to confirm the root of trust has not been compromised. The secure boot verifies the digital signature of the program memory to confirm it has not been modified or corrupted, ensuring the trustworthiness of the application software. Failure to verify the digital signature transitions the device to safe mode, which prevents execution of the customer code. If not previously deactivated, the bootloader can be reactivated and a new, trusted program memory loaded.

Debug and Development Interface

The serial wire debug (SWD) interface is used for code loading and in-circuit emulator (ICE) debug activities.

Additional Documentation

Designers must have the following documents to use all the features of this device:

- This data sheet, which contains electrical/timing specifications, package information, and pin descriptions
- The corresponding revision-specific errata sheet
- The corresponding *MAX32662 User Guide*, which contains detailed information and programming guidelines for core features and peripherals

Applications Information

Bootloader Activation

The SCPBL can use the interfaces shown in *Table 7*.

Table 7. Bootloader Activation Summary

PART NUMBER	BOOTLOADER INTERFACE	DEFAULT STIMULUS PIN
	UART0	
All versions	UART0_RX UART0_TX RSTN	P0.6 (active low)

On devices that support SCPBL, the SCPBL is activated following any reset or exiting certain low-power modes if the assigned stimulus pin is asserted. The design must ensure that the desired bootloader interface and stimulus pin is accessible by the host or the SCPBL cannot be activated. A different stimulus pin may be assigned once an SCPBL session has been started. The stimulus pin must be driven externally to a known state at all times.

The RSTN signal must also be accessible by the host for initial synchronization with the SCPBL.

Bypass Capacitors

The proper use of bypass capacitors reduces noise generated by the IC into the ground plane. The *Pin Descriptions* indicate which pins should be connected to bypass capacitors and the appropriate ground plane.

It is recommended that one instance of a bypass capacitor should be connected to each pin/ball of the IC package. For example, if the *Pin Descriptions* show four device pins associated with voltage supply A, a separate capacitor should be connected to each pin for a total of four capacitors.

Place capacitors as close as possible to their corresponding device pins. When more than one value of capacitor is recommended per pin, the capacitors should be placed in parallel starting with the lowest value capacitor closest to the pin.

Typical Fixed Current Consumption Temperature Variance

Single-Supply ACTIVE Mode f_{SYS_OSC} = IPO

Table 8. Single-Supply Operation Fixed V_{DDIO} Current Consumption ACTIVE Mode f_{SYS_OSC} = IPO

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DDIO} Current, ACTIVE Mode	I_{DD_FACTS}	Fixed, IPO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 3.3V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	595	685	835	1155	1310	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	505	585	705	940	1100	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	440	510	610	805	945	µA
		Fixed, IPO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 1.8V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	575	665	810	1090	1285	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	490	565	685	915	1075	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	425	490	590	780	920	µA

Single-Supply SLEEP Mode f_{SYS_OSC} = IPO

Table 9. Single-Supply Operation Fixed V_{DDIO} Current Consumption SLEEP Mode f_{SYS_osc} = IPO

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DDIO} Current, SLEEP Mode	I_{DDIO_FSLPS}	Fixed, IPO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 3.3V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	595	685	835	1155	1310	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	505	585	705	940	1100	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	440	510	610	805	945	µA
		Fixed, IPO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 1.8V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	575	665	810	1090	1285	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	490	565	685	915	1075	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	425	490	590	780	920	µA

Single-Supply ACTIVE Mode f_{SYS_OSC} = IBRO

Table 10. Single-Supply Operation Fixed V_{DDIO} Current Consumption ACTIVE Mode f_{SYS_OSC} = IBRO

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DDIO} Current, ACTIVE Mode	I_{DDIO_FACTS}	Fixed, IBRO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 3.3V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	210	280	410	675	865	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	200	255	360	575	735	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	190	230	320	500	635	µA
		Fixed, IBRO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 1.8V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	185	255	385	645	835	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	175	230	335	550	705	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	170	210	295	470	605	µA

Single-Supply SLEEP Mode f_{SYS_OSC} = IBRO

Table 11. Single-Supply Operation Fixed V_{DDIO} Current Consumption SLEEP Mode f_{SYS_OSC} = IBRO

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DDIO} Current, SLEEP Mode	I_{DDIO_FSLPS}	Fixed, IBRO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 3.3V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	210	280	410	675	865	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	200	255	360	575	735	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	190	230	320	500	635	µA
		Fixed, IBRO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 1.8V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	185	255	385	645	835	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	175	230	335	550	705	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	170	210	295	470	605	µA

Single-Supply DEEPSLEEP Mode

Table 12. Single-Supply Operation Fixed V_{DDIO} Current Consumption DEEPSLEEP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DDIO} Fixed Current, DEEPSLEEP Mode	I_{DDIO_FDSLPS}	Standby state with full data retention and 80KB SRAM retained	V_{DDIO} = 3.3V. PWRSEQ_LPCTRL. fastwken = 0, PWRSEQ_LPCTRL. bg_dis = 0.	1.6	3.6	9.6	26	40	µA
			V_{DDIO} = 1.8V. PWRSEQ_LPCTRL. fastwken = 0, PWRSEQ_LPCTRL. bg_dis = 0.	1.4	3.3	9.2	25	39	µA

Single-Supply BACKUP Mode

Table 13. Single-Supply Operation Fixed V_{DDIO} Current Consumption BACKUP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DDIO} Fixed Current, BACKUP Mode	I_{DDIO_FBKUS}	V_{DDIO} = 3.3V, RTC disabled	0KB SRAM retained, retention regulator disabled	0.35	0.45	0.7	1.3	1.9	µA
			20KB SRAM retained, retention regulator disabled	0.77	1.25	2.35	5.4	8.2	µA
			40KB SRAM retained, retention regulator disabled	0.9	1.6	3.45	8.5	13	µA
			60KB SRAM retained, retention regulator disabled	1.1	2	4.7	11.5	18	µA
			80KB SRAM retained, retention regulator disabled	1.2	2.4	5.8	14.6	23	µA
		V_{DDIO} = 1.8V, RTC disabled	0KB SRAM retained, retention regulator disabled	0.2	0.23	0.35	0.8	1.2	µA
			20KB SRAM retained, retention regulator disabled	0.6	1	2	4.8	7.5	µA
			40KB SRAM retained, retention regulator disabled	0.8	1.4	3.1	7.8	12.1	µA
			60KB SRAM retained, retention regulator disabled	0.9	1.8	4.3	11	17	µA
			80KB SRAM retained, retention regulator disabled	1.1	2.15	5.4	14	22	µA

Single-Supply STORAGE Mode

Table 14. Single-Supply Operation Fixed V_{DDIO} Current Consumption STORAGE Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	25°C	55°C	85°C	105°C	
V_{DDIO} Fixed Current, STORAGE Mode	I_{DDIO_FSTOS}	V_{DDIO} = 3.3V	0.12	0.23	0.5	1.1	1.7	µA
		V_{DDIO} = 1.8V	0.02	0.06	0.2	0.6	1.1	µA

Dual-Supply ACTIVE Mode f_{SYS_OSC} = IPO

Table 15. Dual-Supply Operation Fixed V_{CORE} Current Consumption ACTIVE Mode f_{SYS_OSC} = IPO

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{CORE} Current, ACTIVE Mode	I_{CORE_FACTD}	Fixed, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode 0MHz operation, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V	190	250	380	640	830	µA
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V	100	145	250	470	620	µA
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V	40	70	150	310	430	µA

Table 16. Dual-Supply Operation Fixed V_{DDIO} Current Consumption ACTIVE Mode f_{SYS_OSC} = IPO

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DDIO} Current, ACTIVE Mode	I_{DDIO_FACTD}	Fixed, IPO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 3.3V, CPU in ACTIVE mode 0MHz operation, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	355	385	400	420	430	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	355	385	400	420	430	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	355	385	400	420	430	µA
		Fixed, IPO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 1.8V, CPU in ACTIVE mode 0MHz operation, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	340	370	385	400	410	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	340	370	385	400	410	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	340	370	385	400	410	µA

Dual-Supply SLEEP Mode f_{SYS_OSC} = IPO

Table 17. Dual-Supply Operation Fixed V_{CORE} Current Consumption SLEEP Mode f_{SYS_OSC} = IPO

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{CORE} Current, SLEEP Mode	I_{CORE_FSLPD}	Fixed, IPO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V	190	250	380	640	830	µA
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V	100	145	250	465	620	µA
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V	40	70	150	310	430	µA

Table 18. Dual-Supply Operation Fixed V_{DDIO} Current Consumption SLEEP Mode f_{SYS_OSC} = IPO

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DDIO} Current, SLEEP Mode	I_{DDIO_FSLPD}	Fixed, IPO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 3.3V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	355	385	400	420	430	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	355	385	400	420	430	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	355	385	400	420	430	µA
		Fixed, IPO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 1.8V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	340	370	385	400	415	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	340	370	385	400	415	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	340	370	385	400	415	µA

Dual-Supply ACTIVE Mode f_{SYS_OSC} = IBRO

Table 19. Dual-Supply Operation Fixed V_{CORE} Current Consumption ACTIVE Mode f_{SYS_OSC} = IBRO

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{CORE} Current, ACTIVE Mode	I_{CORE_FACTD}	Fixed, IBRO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode 0MHz operation, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V	40	105	225	465	690	µA
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V	30	80	175	370	560	µA
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V	20	55	120	270	410	µA

Table 20. Dual-Supply Operation Fixed V_{DDIO} Current Consumption ACTIVE Mode f_{SYS_OSC} = IBRO

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DDIO} Current, ACTIVE Mode	I_{DDIO_FACTD}	Fixed, IBRO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 3.3V, CPU in ACTIVE mode 0MHz operation, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	105	115	120	125	130	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	105	115	120	125	130	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	105	115	120	125	130	µA
		Fixed, IBRO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 1.8V, CPU in ACTIVE mode 0MHz operation, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	85	90	95	100	105	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	85	90	95	100	105	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	85	90	95	100	105	µA

Dual-Supply SLEEP Mode f_{SYS_OSC} = IBRO

Table 21. Dual-Supply Operation Fixed V_{CORE} Current Consumption SLEEP Mode f_{SYS_OSC} = IBRO

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{CORE} Current, SLEEP Mode	I_{CORE_FSLPD}	Fixed, IBRO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, V_{CORE} = 1.1V	190	250	380	645	830	µA
			PWRSEQ_LPCTRL.ovr = 0b01, V_{CORE} = 1.0V	100	145	255	465	620	µA
			PWRSEQ_LPCTRL.ovr = 0b00, V_{CORE} = 0.9V	40	70	150	310	430	µA

Table 22. Dual-Supply Operation Fixed V_{DDIO} Current Consumption SLEEP Mode f_{SYS_OSC} = IBRO

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DDIO} Current, SLEEP Mode	I_{DD_FSLPD}	Fixed, IBRO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 3.3V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	105	115	120	125	130	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	105	115	120	125	130	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	105	115	120	125	130	µA
		Fixed, IBRO enabled, total current into V_{DDIO} and V_{DDA} pins, V_{DDIO} = 1.8V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DDIO}, outputs source/sink 0mA	PWRSEQ_LPCTRL.ovr = 0b10, internal regulator set to 1.1V	85	90	95	100	105	µA
			PWRSEQ_LPCTRL.ovr = 0b01, internal regulator set to 1.0V	85	90	95	100	105	µA
			PWRSEQ_LPCTRL.ovr = 0b00, internal regulator set to 0.9V	85	90	95	100	105	µA

Dual-Supply DEEPSLEEP Mode

Table 23. Dual-Supply Operation Fixed V_{CORE} Current Consumption DEEPSLEEP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{CORE} Fixed Current, DEEPSLEEP Mode	I_{CORE_FDSLPD}	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	PWRSEQ_LPCTRL.fastwk_en = 0, PWRSEQ_LPCTRL.bg_dis = 0	3.4	6.8	15.4	36	54	µA
		V_{DDIO} = 3.3V, V_{CORE} = 0.855V	PWRSEQ_LPCTRL.fastwk_en = 0, PWRSEQ_LPCTRL.bg_dis = 0	0.9	2.7	8	22	35	µA
		V_{DDIO} = 1.8V, V_{CORE} = 1.1V	PWRSEQ_LPCTRL.fastwk_en = 0, PWRSEQ_LPCTRL.bg_dis = 0	3.4	6.8	15	36	54	µA
		V_{DDIO} = 1.8V, V_{CORE} = 0.855V	PWRSEQ_LPCTRL.fastwk_en = 0, PWRSEQ_LPCTRL.bg_dis = 0	0.9	2.7	8	22	35	µA

Table 24. Dual-Supply Operation Fixed V_{DDIO} Current Consumption DEEPSLEEP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DDIO} Fixed Current, DEEPSLEEP Mode	I_{DDIO_FDSLPD}	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	PWRSEQ_LPCTRL.fastwk_en = 0, PWRSEQ_LPCTRL.bg_dis = 0	0.1	0.19	0.4	0.9	1.5	µA
		V_{DDIO} = 3.3V, V_{CORE} = 0.855V	PWRSEQ_LPCTRL.fastwk_en = 0, PWRSEQ_LPCTRL.bg_dis = 0	0.1	0.19	0.4	0.9	1.5	µA
		V_{DDIO} = 1.8V, V_{CORE} = 1.1V	PWRSEQ_LPCTRL.fastwk_en = 0, PWRSEQ_LPCTRL.bg_dis = 0	0.015	0.05	0.17	0.55	1	µA
		V_{DDIO} = 1.8V, V_{CORE} = 0.855V	PWRSEQ_LPCTRL.fastwk_en = 0, PWRSEQ_LPCTRL.bg_dis = 0	0.015	0.05	0.17	0.55	1	µA

Dual-Supply BACKUP Mode

Table 25. Dual-Supply Operation Fixed V_{CORE} Current Consumption BACKUP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{CORE} Fixed Current, BACKUP Mode	I_{CORE_FBKUD}	0KB SRAM retained with RTC disabled, retention regulator disabled.	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	0.3	0.33	1	3.1	5.15	µA
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V	0.07	0.18	0.7	2.45	4.2	µA
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V	0.3	0.33	1	3.05	5.15	µA
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V	0.07	0.18	0.7	2.45	4.2	µA
		20KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	0.8	1.28	2.95	7.5	11.5	µA
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V	0.2	0.54	1.7	5.05	8.3	µA
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V	0.8	1.28	2.95	7.5	11.5	µA
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V	0.2	0.54	1.7	5.05	8.3	µA
		40KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	1.3	2.23	4.95	11.9	18	µA
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V	0.32	0.9	2.7	7.7	12.5	µA
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V	1.3	2.23	4.95	11.9	18	µA
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V	0.32	0.9	2.7	7.7	12.5	µA
		60KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	1.85	3.2	6.85	16	24	µA
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V	0.45	1.25	3.65	10	16	µA
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V	1.85	3.2	6.85	16	24	µA
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V	0.45	1.25	3.65	10	16	µA
		80KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	2.35	4.1	8.8	20.5	30	µA
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V	0.6	1.6	4.6	12.7	20	µA
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V	2.35	4.1	8.8	20.5	30	µA
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V	0.6	1.6	4.6	12.7	20	µA

Table 26. Dual-Supply Operation Fixed V_{DDIO} Current Consumption BACKUP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
	I_{DDIO_FBKUD}	0KB SRAM retained with	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	0.09	0.19	0.4	0.93	1.45	µA

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DDIO} Fixed Current, BACKUP Mode		RTC disabled, retention regulator disabled.	V_{DDIO} = 3.3V, V_{CORE} = 0.855V	0.09	0.19	0.4	0.93	1.45	µA
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V	0.013	0.05	0.17	0.55	0.96	µA
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V	0.013	0.05	0.17	0.55	0.96	µA
		20KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	0.09	0.19	0.4	0.93	1.45	µA
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V	0.09	0.19	0.4	0.93	1.45	µA
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V	0.013	0.05	0.17	0.55	0.96	µA
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V	0.013	0.05	0.17	0.55	0.96	µA
		40KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	0.09	0.19	0.4	0.93	1.45	µA
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V	0.09	0.19	0.4	0.93	1.45	µA
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V	0.013	0.05	0.17	0.55	0.96	µA
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V	0.013	0.05	0.17	0.55	0.96	µA
		60KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	0.09	0.19	0.4	0.93	1.45	µA
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V	0.09	0.19	0.4	0.93	1.45	µA
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V	0.013	0.05	0.17	0.55	0.96	µA
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V	0.013	0.05	0.17	0.55	0.96	µA
		80KB SRAM retained with RTC disabled	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	0.09	0.19	0.4	0.93	1.45	µA
			V_{DDIO} = 3.3V, V_{CORE} = 0.855V	0.09	0.19	0.4	0.93	1.45	µA
			V_{DDIO} = 1.8V, V_{CORE} = 1.1V	0.013	0.05	0.17	0.55	0.96	µA
			V_{DDIO} = 1.8V, V_{CORE} = 0.855V	0.013	0.05	0.17	0.55	0.96	µA

Dual-Supply STORAGE Mode

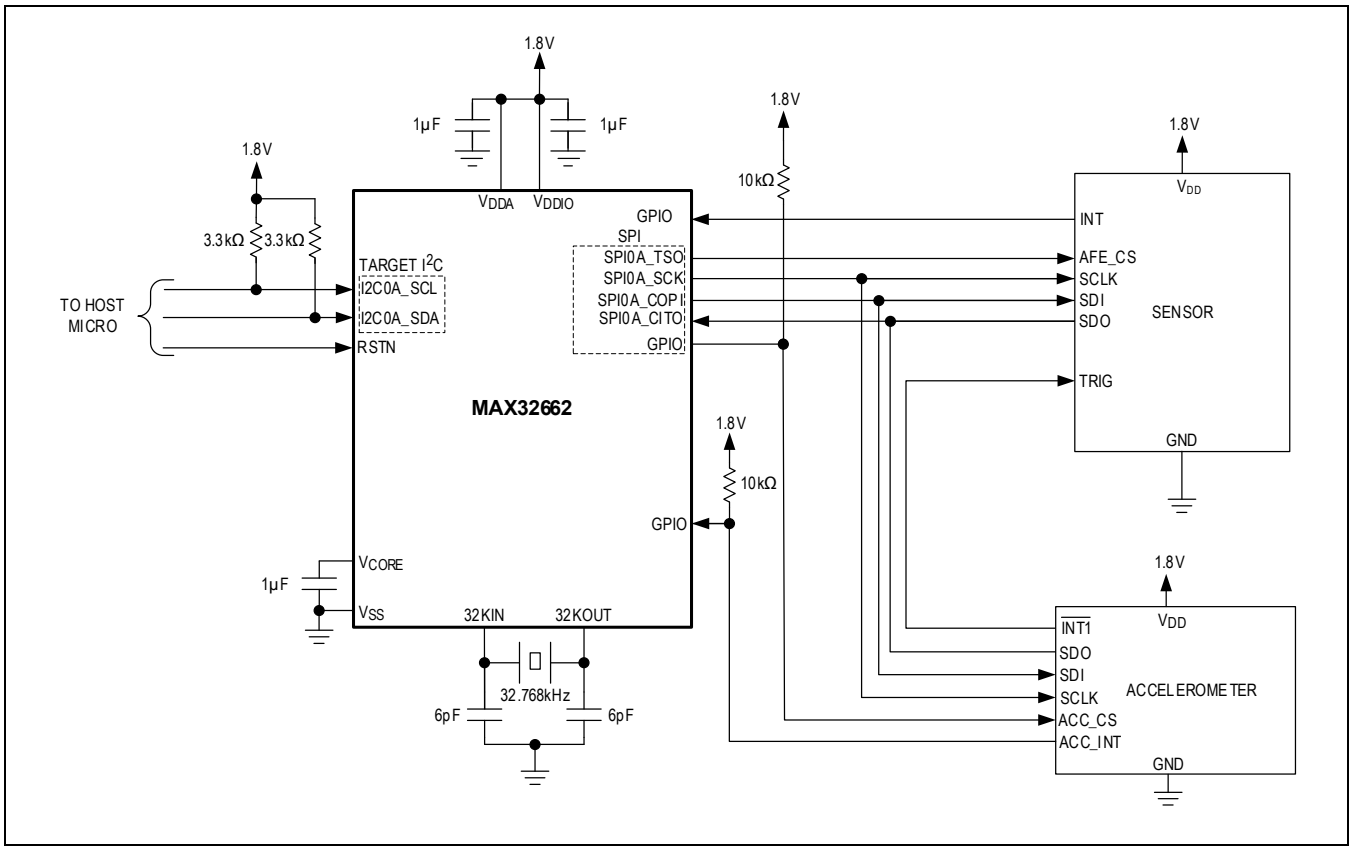
Table 27. Dual-Supply Operation Fixed V_{CORE} Current Consumption STORAGE Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	25°C	55°C	85°C	105°C	
V_{CORE} Fixed Current, STORAGE Mode	I_{CORE_FSTOD}	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	0.3	0.33	1	3.05	5.15	µA
		V_{DDIO} = 3.3V, V_{CORE} = 0.855V	0.07	0.18	0.72	2.45	4.2	µA
		V_{DDIO} = 1.8V, V_{CORE} = 1.1V	0.3	0.33	1	3.05	5.15	µA
		V_{DDIO} = 1.8V, V_{CORE} = 0.855V	0.07	0.18	0.72	2.45	4.2	µA

Table 28. Dual-Supply Operation Fixed V_{DDIO} Current Consumption STORAGE Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	25°C	55°C	85°C	105°C	
V_{DDIO} Fixed Current, STORAGE Mode	I_{DDIO_FSTOD}	V_{DDIO} = 3.3V, V_{CORE} = 1.1V	0.11	0.22	0.45	1.1	1.7	µA
		V_{DDIO} = 3.3V, V_{CORE} = 0.855V	0.11	0.22	0.45	1.1	1.7	µA
		V_{DDIO} = 1.8V, V_{CORE} = 1.1V	0.02	0.06	0.19	0.65	1.11	µA
		V_{DDIO} = 1.8V, V_{CORE} = 0.855V	0.02	0.06	0.19	0.65	1.11	µA

Typical Application Circuits



Ordering Information

PART NUMBER	SCPBL	SWD	TMR	LPTMR	I2C	SPI	CMP	12-BIT SAR ADC INPUTS	UART	GPIO	PIN-PACKAGE
MAX32662GTJ+	No	Yes	3	1	2	2	2	4	2	21	32 TQFN-EP, 5mm x 5mm x 0.5mm pitch
MAX32662GTJ+T	No	Yes	3	1	2	2	2	4	2	21	32 TQFN-EP, 5mm x 5mm x 0.5mm pitch
MAX32662GTJBL+*	Yes	Yes	3	1	2	2	2	4	2	21	32 TQFN-EP, 5mm x 5mm x 0.5mm pitch
MAX32662GTJBL+T*	Yes	Yes	3	1	2	2	2	4	2	21	32 TQFN-EP, 5mm x 5mm x 0.5mm pitch
MAX32662GWP+*	No	Yes	3	1	2	2	2	4	2	12	20 WLP, 2.30mm x 1.92mm x 0.4mm pitch
MAX32662GWP+T*	No	Yes	3	1	2	2	2	4	2	12	20 WLP, 2.30mm x 1.92mm x 0.4mm pitch
MAX32662GWPBL+*	Yes	Yes	3	1	2	2	2	4	2	12	20 WLP, 2.30mm x 1.92mm x 0.4mm pitch
MAX32662GWPBL+T*	Yes	Yes	3	1	2	2	2	4	2	12	20 WLP, 2.30mm x 1.92mm x 0.4mm pitch

All packages contain CAN 2.0B, I²S, and four PT.

SWD = serial wire debug; TMR = timer; LPTMR = low-power timer; CMP = comparator; PT = pulse train

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

** Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/23	Initial release	—