19-4337; Rev 2; 4/11

EVALUATION KIT AVAILABLE

Complete Single-Conversion Television Tuner

MAX3542

General Description

The MAX3542 complete single-conversion television tuner is designed for use in analog/digital terrestrial applications and digital set-top boxes. This television tuner draws only 760mW of power from a +3.3V supply voltage.

The MAX3542 is designed to convert PAL or DVB-T signals in the 47MHz to 862MHz band to an intermediate frequency (IF) of 36MHz.

The MAX3542 includes a variable-gain low-noise amplifier (LNA), multiband tracking filters, a harmonic-rejection mixer, a low-noise IF amplifier, an IF power detector, and a variable-gain IF amplifier. The MAX3542 also includes fully monolithic VCOs and tank circuits, as well as a complete frequency synthesizer. This highly integrated design allows for low-power tuner-on-board applications without the cost and power dissipation issues of dual-conversion tuner solutions.

The MAX3542 is specified for operation in the 0°C to +70°C temperature range and is available in a lead-free 48-pin flip-chip (fcLGA) package.

Applications

Televisions

Analog/Digital Terrestrial Receivers

Digital Set-Top Boxes

Features

- **Low Power Consumption: 760mW (typ) from a +3.3V Supply Voltage**
- **Integrated Tracking Filters**
- **Low Noise Figure: 4.9dB (typ)**
- **Small 7mm x 7mm fcLGA Lead-Free Package**
- **IF Overload Detector Controls RF Variable-Gain Amplifier**
- **2-Wire, I²C-Compatible Serial Control Interface**

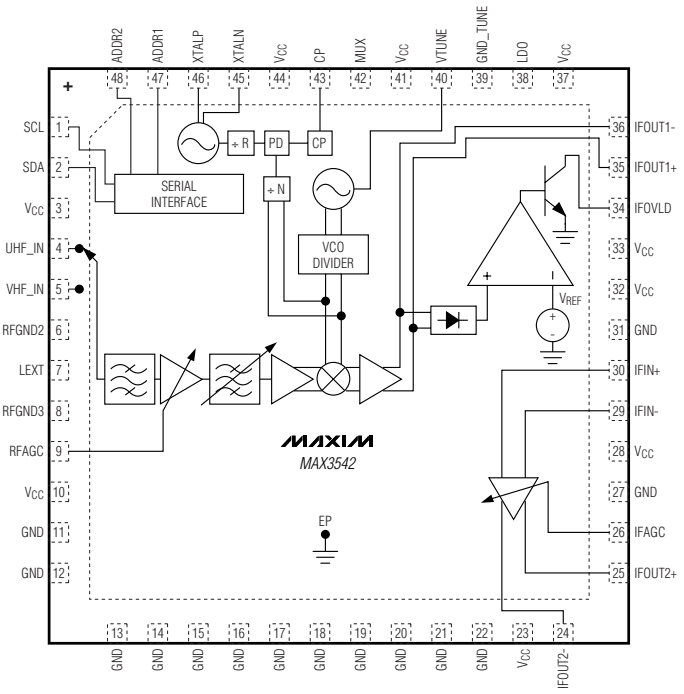
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3542CLM+	0°C to +70°C	48 LGA-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed paddle.*

Pin Configuration/Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V, +3.6V
UHF_IN, VHF_IN, IFIN_, IFOUT1_, IFOUT2_, IFAGC, RFAGC, VTUNE, LDO, MUX, CP, XTAL_ to GND .....-0.3V to (V_{CC} + 0.3V)
SDA, SCL, ADDR2, ADDR1 to GND.....-0.3V to +3.6V
IFOUT__ Short-Circuit Duration .....Indefinite
RF Input Power .....+10dBm
Continuous Power Dissipation (T_A = +70°C)
48-Pin LGA (derate 25mW/°C above +70°C) 1.4W
Operating Temperature Range.....0°C to +70°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+250°C
Soldering Temperature (reflow) .....+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(MAX3542 EV kit, V_{CC} = +3.1V to +3.5V, T_A = 0°C to +70°C, no RF signals at RF inputs, default register settings, V_{RFAGC} = V_{IFAGC} = +3V (minimum attenuation), unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE AND CURRENT					
Supply Voltage		+3.1		+3.5	V
Supply Current	Receive mode		230	275	mA
	Shutdown mode		5		
RF and IF AGC Input Bias Current	At +0.5V and +3V	-50		+50	µA
RF and IF AGC Control Voltage (Note 2)	Minimum attenuation	+3			V
	Maximum attenuation			+0.5	
Digital Input Logic-Level Low				0.3 x V_{CC}	V
Digital Input Logic-Level High		0.7 x V_{CC}			V
SERIAL INTERFACE					
Input Logic-Level Low				0.3 x V_{CC}	V
Input Logic-Level High		0.7 x V_{CC}			V
Input Hysteresis			0.05 x V_{CC}		V
SDA, SCL Input Current		-10		+10	µA
Output Logic-Level Low	3mA sink current			0.4	V
Output Logic-Level High		V_{CC} - 0.5			V

AC ELECTRICAL CHARACTERISTICS

(MAX3542 EV kit, V_{CC} = +3.1V to +3.5V, T_A = 0°C to +70°C, 75Ω system impedance, default register settings, V_{RFAGC} = V_{IFAGC} = +3V (minimum attenuation), unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF INPUT TO IFOUT1_ OUTPUT						
Operating Frequency Range (see Table 7)	Gain specification met across this frequency band		47		862	MHz
Output Frequency	Analog channel PIX carrier			38.9		MHz
	Digital channel center frequency			36		
Voltage Gain	Source impedance = 75Ω, load impedance = 200Ω	Maximum gain (V_{RFAGC} = 3V)	34	41	49.5	dB
		Minimum gain (V_{RFAGC} = 0.5V)		-10		
Input Return Loss	Selected channel			10		dB
Noise Figure	Maximum gain (V_{RFAGC} = 3V)			4.9		dB
Input IP2 (In-Band and Out-of-Band Tones)	Maximum gain (V_{RFAGC} = 3V)			20		dBm
	At 12.5dB of gain			30		
Input IP3 (In-Band and Out-of-Band Tones)	Maximum gain (V_{RFAGC} = 3V)			-10		dBm
	At 12.5dB of gain		13			
Input P_{1dB}	Maximum gain (V_{RFAGC} = 3V)			-38		dBm
	At 12.5dB of gain			-5		
Beats Within Output	0dBmV PIX carrier level			-40		dBc
Beats, Converted to Output	VHF input, 140MHz to 500MHz			-60		dBc
	VHF input, 500MHz to 1400MHz			-50		
	UHF input, 950MHz to 1400MHz			-60		
Gain Flatness	47MHz to 54MHz				2.5	dB_{P-P}
Isolation	5MHz to 50MHz, RF input to IF output, relative to desired channel			60		dBc
Port-to-Port Isolation	Isolation between RF input ports at 215MHz			27		dB
Image Rejection	Measured at 77.8MHz above desired channel's center frequency		57	70		dBc
Spurious Leakage at RF Input	5Hz to 65MHz			-40		dBmV
	65MHz to 878MHz			-40		
Phase Noise (Single-Sideband)	1kHz			-80		dBc/Hz
	10kHz offset			-85		
	100kHz offset (1.5kHz loop bandwidth)			-105		
	1MHz offset (1.5kHz loop bandwidth)			-125		
Output Return Loss	Balanced 50Ω load			20		dB
IF VARIABLE-GAIN AMPLIFIER						
Input Impedance	Balanced			2000		Ω
Output Impedance	Balanced (Note 2)				300	Ω

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AC ELECTRICAL CHARACTERISTICS (continued)

(MAX3542 EV kit, V_{CC} = +3.1V to +3.5V, T_A = 0°C to +70°C, 75Ω system impedance, default register settings, V_{RFAGC} = V_{IFAGC} = +3V (minimum attenuation), unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

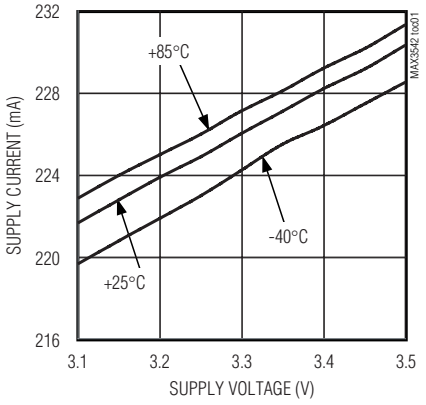
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Voltage Gain	Source load = 1.1kΩ, output load = 1kΩ	Maximum gain setting (V_{IFAGC} = 3V)	54	59	63	dB
		Minimum gain setting (V_{IFAGC} = 0.5V)			21	
Passband Gain Flatness	32MHz to 40MHz (Note 2)				1.2	dB
Output Voltage	V_{IFAGC} = 3V (Note 2)				2.5	V_{P-P}
AGC Gain Slope	V_{IFAGC} = 3V to 0.5V (Note 2)				27	dB/V
Equivalent Input-Voltage Noise Density	At 36MHz, maximum gain (V_{IFAGC} = 3V) (Note 2)				7.3	nV/√Hz
Noise Figure Change vs. Attenuation				< 0.35		dB/dB
IM3	V_{OUT} = 1V_{P-P}, 40dB < gain < 60dB (Note 2)		-56			dBc
IF OVERLOAD DETECTOR (See the *IF Overload Detector* Section)						
Output Overload Attack Point				0.7		V_{P-P}
Attack Point Accuracy	OD REG = 3			±1		dB
Detector Output-Voltage Range	Negative polarity, overload reduces V_{DET} (open collector, 0.3mA sink)		0.5		3.0	V
Detector Gain				70		V/V
FREQUENCY SYNTHESIZER—REFERENCE OSCILLATOR						
Frequency				8		MHz
DIVIDERS						
RF N-Divider Ratio			256		32,767	
RF R-Divider Ratio			16		127	
LO PHASE DETECTOR AND CHARGE PUMP						
Comparison Frequency			63		500	kHz
Charge-Pump Current	CP = 00			0.5		mA
	CP = 01			1		
	CP = 10			1.5		
	CP = 11			2		
Charge-Pump Three-State Current				±5		nA
Charge-Pump Compliance Range			0.4		V_{CC} - 0.4	V
Charge-Pump Current Matching				5		%
LOCAL OSCILLATOR						
VCO Tuning Range	Tank frequency		2200		4400	MHz
VCO Tuning Gain	Tank oscillator gain				500	MHz/V
2-WIRE SERIAL INTERFACE						
Clock Frequency					400	kHz

Note 1: Min/max values are production tested at T_A = +70°C.
Note 2: Guaranteed by design and characterization.

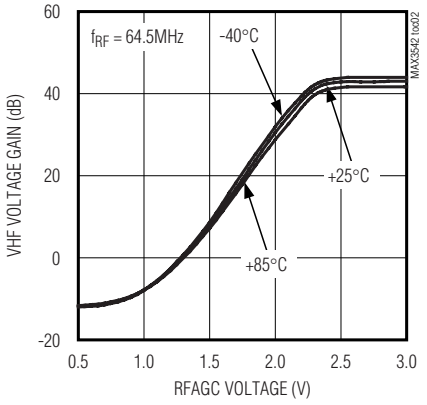
Typical Operating Characteristics

(MAX3542 EV kit, V_{CC} = +3.3V, V_{IFAGC} = 3.0V, V_{RFAGC} = 3.0V, T_A = +25°C, unless otherwise noted.)

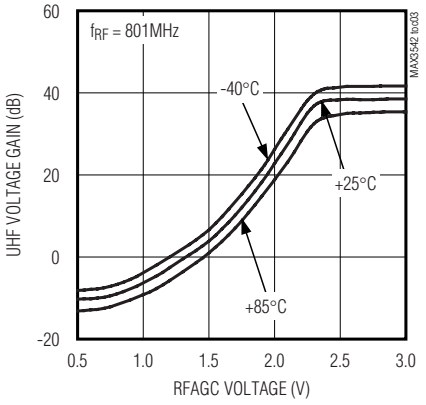
SUPPLY CURRENT vs. SUPPLY VOLTAGE



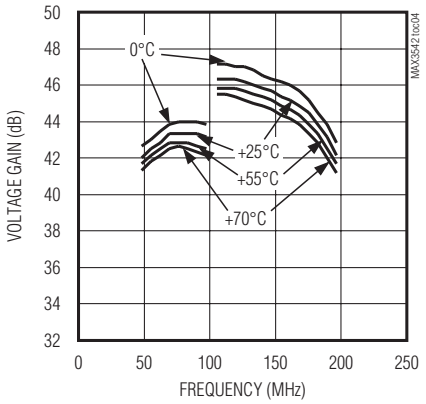
VHF VOLTAGE GAIN vs. RFAGC VOLTAGE



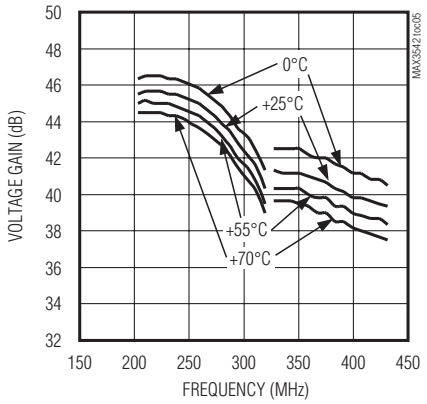
UHF VOLTAGE GAIN vs. RFAGC VOLTAGE



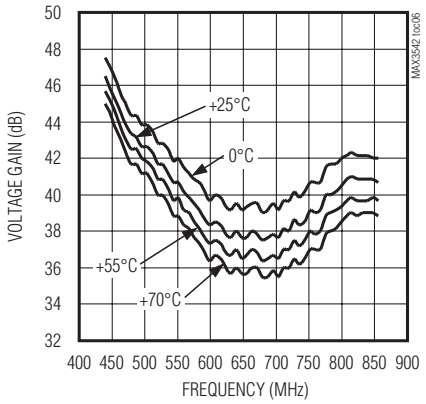
VHF LO VOLTAGE GAIN vs. FREQUENCY



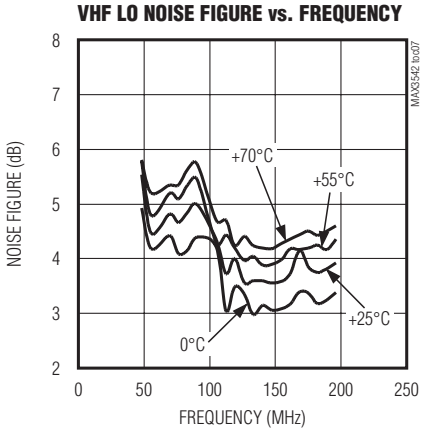
VHF HI VOLTAGE GAIN vs. FREQUENCY



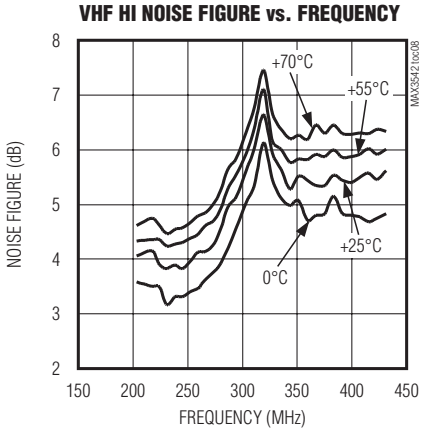
UHF VOLTAGE GAIN vs. FREQUENCY



VHF LO NOISE FIGURE vs. FREQUENCY



VHF HI NOISE FIGURE vs. FREQUENCY



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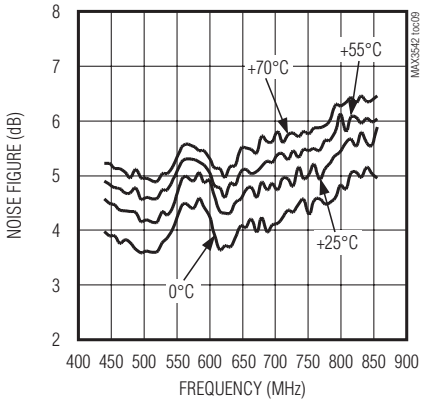
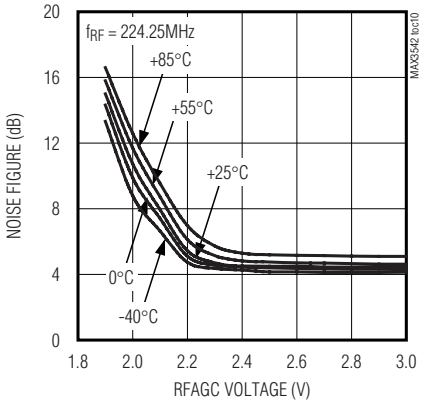
Typical Operating Characteristics (continued)

(MAX3542 EV kit, V_{CC} = +3.3V, V_{IFAGC} = 3.0V, V_{RFAGC} = 3.0V, T_A = +25°C, unless otherwise noted.)

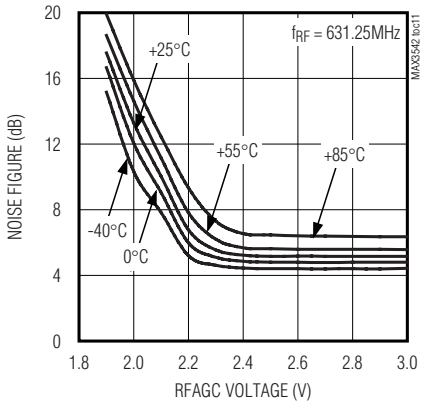
UHF NOISE FIGURE vs. FREQUENCY



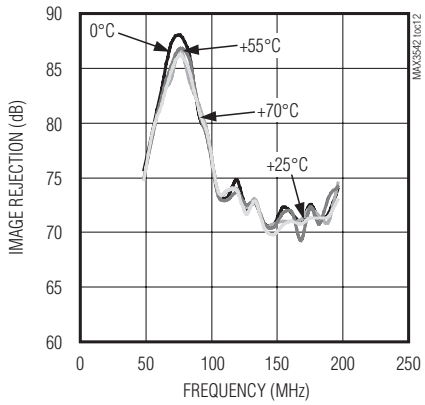
VHF NOISE FIGURE vs. RFAGC VOLTAGE



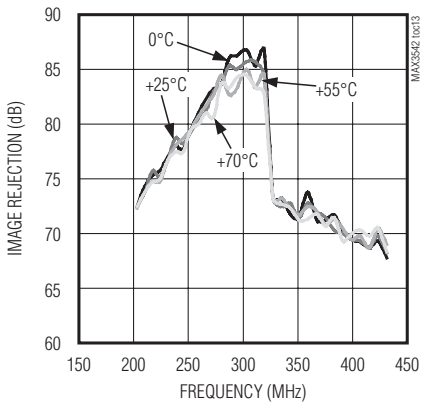
UHF NOISE FIGURE vs. RFAGC VOLTAGE



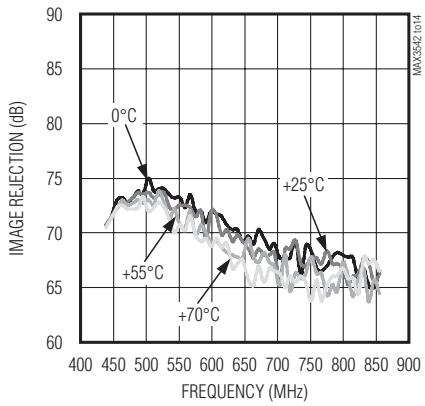
VHF LO IMAGE REJECTION vs. FREQUENCY



VHF HI IMAGE REJECTION vs. FREQUENCY



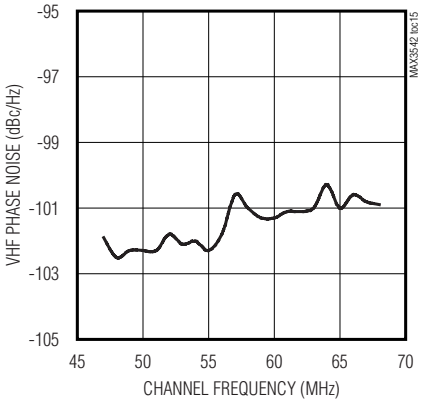
UHF IMAGE REJECTION vs. FREQUENCY



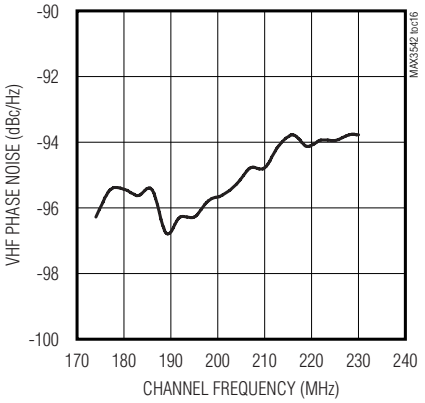
Typical Operating Characteristics (continued)

(MAX3542 EV kit, V_{CC} = +3.3V, V_{IFAGC} = 3.0V, V_{RFAGC} = 3.0V, T_A = +25°C, unless otherwise noted.)

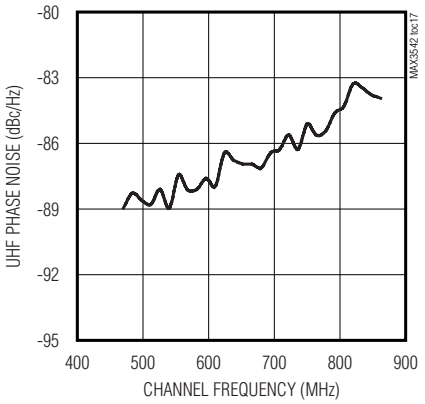
VHF PHASE NOISE AT 10kHz OFFSET vs. CHANNEL FREQUENCY



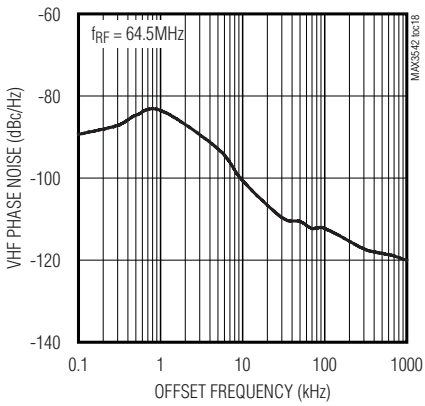
VHF PHASE NOISE AT 10kHz OFFSET vs. CHANNEL FREQUENCY



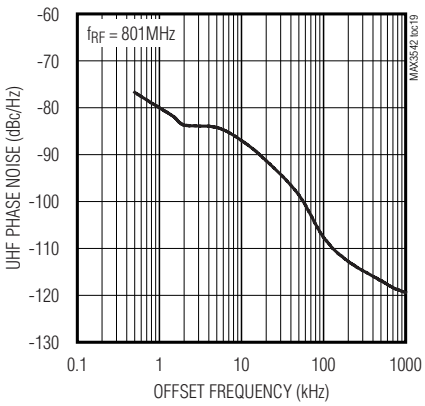
UHF PHASE NOISE AT 10kHz OFFSET vs. CHANNEL FREQUENCY



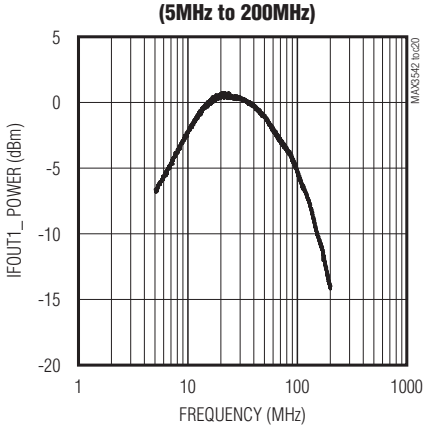
VHF PHASE NOISE vs. OFFSET FREQUENCY



UHF PHASE NOISE vs. OFFSET FREQUENCY



IFOUT1_ NORMALIZED FREQUENCY RESPONSE (5MHz to 200MHz)



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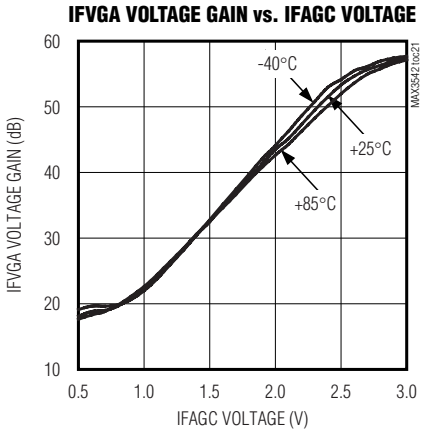
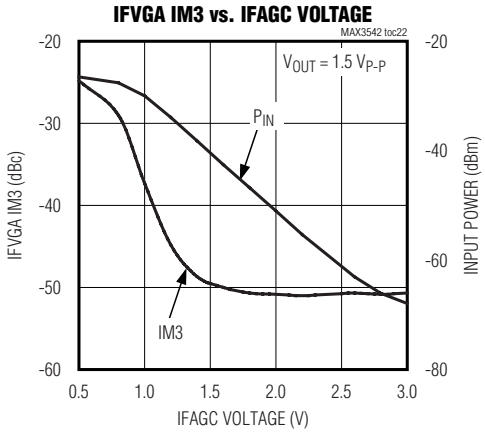
Typical Operating Characteristics (continued)

(MAX3542 EV kit, V_{CC} = +3.3V, V_{IFAGC} = 3.0V, V_{RFAGC} = 3.0V, T_A = +25°C, unless otherwise noted.)





Pin Description

PIN	NAME	FUNCTION
1	SCL	2-Wire Serial-Clock Interface. Requires a pullup resistor to V_{CC}.
2	SDA	2-Wire Serial-Data Interface. Requires a pullup resistor to V_{CC}.
3, 10, 23, 28, 32, 33, 37, 41, 44	V_{CC}	Power-Supply Connections. Bypass each supply pin to ground with a 1000pF capacitor.
4	UHF_IN	UHF RF Input. Requires a DC-blocking capacitor.
5	VHF_IN	VHF RF Input. Requires a DC-blocking capacitor.
6	RFGND2	RF Ground. Bypass to the PCB's ground plane with a 1000pF capacitor. **Do not connect RFGND2 and RFGND3 together.**
7	LEXT	RF VGA Supply Voltage. Connect through a 270nH pullup inductor to V_{CC}.
8	RFGND3	RF Ground. Bypass to the PCB's ground plane with a 1000pF capacitor. **Do not connect RFGND2 and RFGND3 together.**
9	RFAGC	RF VGA Gain Control Voltage. Accepts a DC voltage from 0.5V (minimum gain) to 3V (maximum gain).
11–22, 27, 31	GND	Ground. Connect to the PCB's ground plane.
24	IFOUT2-	Inverting IF VGA Output. Connect to the input of an anti-aliasing filter. Requires a DC-blocking capacitor.
25	IFOUT2+	Noninverting IF VGA Output. Connect to the input of an anti-aliasing filter. Requires a DC-blocking capacitor.
26	IFAGC	IF VGA Gain Control Voltage. Accepts a DC voltage from 0.5V (minimum gain) to 3V (maximum gain).
29	IFIN-	Inverting IF VGA Input. Connect to the output of an IF-SAW filter.
30	IFIN+	Noninverting IF VGA Input. Connect to the output of an IF-SAW filter.
34	IFOVLD	IF Overload Detector Open-Collector Output. Requires a 10kΩ pullup resistor to V_{CC}.
35	IFOUT1+	Noninverting IF LNA Output. Requires a DC-blocking capacitor.
36	IFOUT1-	Inverting IF LNA Output. Requires a DC-blocking capacitor.
38	LDO	VCO LDO Bypass. Bypass to ground with a 0.47µF capacitor.

Pin Description (continued)

PIN	NAME	FUNCTION
39	GND_TUNE	VTUNE Ground Connection. Connect to the PCB ground plane. All loop filter component GNDs must be connected to this pin (see the *Typical Application Circuit*).
40	VTUNE	VCO Tuning Input. Connect to the PLL loop filter output.
42	MUX	Test Output. Leave this pin unconnected during normal operation.
43	CP	Charge-Pump Output. Connect to PLL loop filter input.
45	XTALN	Crystal Oscillator Feedback. See the *Typical Application Circuit.*
46	XTALP	Crystal Oscillator Feedback. See the *Typical Application Circuit.*
47	ADDR1	2-Wire Serial-Interface Address Line 1. This pin along with ADDR2 sets the device address for the I^2C-compatible serial interface.
48	ADDR2	2-Wire Serial-Interface Address Line 2. This pin along with ADDR1 sets the device address for the I^2C-compatible serial interface.
—	EP	Exposed Paddle. Internally connected to GND. Solder evenly to the PCB ground plane for proper operation.

Complete Single-Conversion Television Tuner

Detailed Description

Register Descriptions

The MAX3542 includes 11 programmable registers and two read-only registers. The 11 programmable registers include two N-divider registers, an R-divider register, a VCO register, an IFOVLD/Charge Pump/Filter Select register, a Control register, a Shutdown register, and Tracking Filter Control registers. These 11 programmable registers are also readable. The read-only registers include a Status register and a ROM Table Data register.

Recommended default bit settings are provided for user convenience only and are not guaranteed. The user must write all registers after power-up and no earlier than 100µs after power-up.

Table 1. Register Configuration

REGISTER NAME	READ/ WRITE	REGISTER ADDRESS	MSB							LSB
			DATA BYTE							
			D7	D6	D5	D4	D3	D2	D1	D0
N-DIV High	Both	0x00	0	N14	N13	N12	N11	N10	N9	N8
N-DIV Low	Both	0x01	N7	N6	N5	N4	N3	N2	N1	N0
R-DIV	Both	0x02	0	R6	R5	R4	R3	R2	R1	R0
VCO	Both	0x03	VCO4	VCO3	VCO2	VCO1	VCO0	LD	VDIV1	VDIV0
IFOVLD, Charge Pump, and Filter Select	Both	0x04	0	IFOVLD2	IFOVLD1	IFOVLD0	CP1	CP0	TF1	TF0
Control	Both	0x05	0	0	0	0	SHDN _RF	SHDN _IFVGA	INPT1	INPT0
Shutdown	Both	0x06	SHDN _MIX1	SHDN _MIX0	SHDN _IF	SHDN _OD	SHDN _SYN	0	0	0
Tracking Filter Series Capacitor	Both	0x07	TFS7	TFS6	TFS5	TFS4	TFS3	TFS2	TFS1	TFS0
Tracking Filter Parallel Capacitor	Both	0x08	FLD	0	TFP5	TFP4	TFP3	TFP2	TFP1	TFP0
Tracking Filter ROM Address	Both	0x09	0	0	0	0	TFA3	TFA2	TFA1	TFA0
Reserved	Both	0x0A	X	X	X	X	X	X	X	X
ROM Table Data Readback	Read	0x0B	TFR7	TFR6	TFR5	TFR4	TFR3	TFR2	TFR1	TFR0
Status	Read	0x0C	POR	LD2	LD1	LD0	X	X	X	X

Table 2. N-DIV High Register (Address: 0000_b)

BIT NAME	BIT LOCATION (0 = LSB)	RECOMMENDED DEFAULT	FUNCTION
RESERVED	7	0	Must be set to 0.
N[14:8]	6–0	0000001	Sets the most significant bits of the PLL integer divider (N). Default integer divider value is N = 4688. N can range from 256 to 32,767.

Table 3. N-DIV Low Register (Address: 0001_b)

BIT NAME	BIT LOCATION (0 = LSB)	RECOMMENDED DEFAULT	FUNCTION
N[7:0]	7–0	10101011	Sets the least significant bits of the PLL integer divider (N). Default integer divider value is N = 4688. N can range from 256 to 32,767.

Table 4. R-DIV Register (Address: 0010_b)

BIT NAME	BIT LOCATION (0 = LSB)	RECOMMENDED DEFAULT	FUNCTION
RESERVED	7	0	Must be set to 0.
R[6:0]	6–0	0010000	Sets the PLL reference divider (R). Default reference divider value is R = 64. R can range from 16 to 127.

Table 5. VCO Register (Address: 0011_b)

BIT NAME	BIT LOCATION (0 = LSB)	RECOMMENDED DEFAULT	FUNCTION
VCO[4:3]	7–6	10	VCO select. Selects one of three possible VCOs. 00 = VCOs shut down 01 = Selects VCO1 10 = Selects VCO2 11 = Selects VCO3
VCO[2:0]	5–3	111	VCO sub-band select. Selects one of eight possible VCO sub-bands. 000 = Selects SB0 001 = Selects SB1 010 = Selects SB2 011 = Selects SB3 100 = Selects SB4 101 = Selects SB5 110 = Selects SB6 111 = Selects SB7
LD	2	1	Lock detect enable. 0 = Disabled 1 = Enabled
VDIV[1:0]	1–0	10	VCO divider ratio select. 00 = Sets VCO divider to 4 01 = Sets VCO divider to 8 10 = Sets VCO divider to 16 11 = Sets VCO divider to 32

Table 6. IFOVLD, Charge Pump, and Filter Select Register (Address: 0100_b)

BIT NAME	BIT LOCATION (0 = LSB)	RECOMMENDED DEFAULT	FUNCTION
RESERVED	7	0	Must be set to 0.
IFOVLD[2:0]	6–4	000	Write content of ROM register OD[2:0] to this location.
CP[1:0]	3–2	00	Selects the typical charge-pump current. 00 = 0.5mA 01 = 1mA 10 = 1.5mA 11 = 2mA
TF[1:0]	1–0	00	Selects the tracking filter band of operation. 00 = VHF_LO 01 = VHF_HI 10 = UHF 11 = Factory use only

Table 7. Control Register (Address: 0101_b)

BIT NAME	BIT LOCATION (0 = LSB)	RECOMMENDED DEFAULT	FUNCTION
RESERVED	7–4	0000	Must be set to 0000.
SHDN_RF	3	0	RF shutdown. 0 = RF circuitry enabled 1 = RF circuitry disabled
SHDN_IFVGA	2	0	IF VGA shutdown. 0 = IF VGA enabled 1 = IF VGA disabled
INPT[1:0]	1–0	01	Selects the RF input. 00 = Selects VHF_IN, LPF enabled 01 = Selects VHF_IN, LPF disabled 10 = Selects UHF_IN 11 = Factory use only

Table 8. Shutdown Register (Address: 0110_b)

BIT NAME	BIT LOCATION (0 = LSB)	RECOMMENDED DEFAULT	FUNCTION
SHDN_MIX [1:0]	7–6	00	Mixer shutdown. 00 = Mixer enabled 01,10 = Factory use only 11 = Mixer disabled
SHDN_IF	5	0	IF shutdown. 0 = IF section enabled 1 = IF section disabled
SHDN_OD	4	0	IFOVLD shutdown. 0 = Power detector enabled 1 = Power detector disabled
SHDN_SYN	3	0	Frequency synthesizer shutdown. 0 = Synthesizer enabled 1 = Synthesizer disabled
RESERVED	2–0	000	Must be set to 000.

Table 9. Tracking Filter Series Capacitor Register (Address: 0111_b)

BIT NAME	BIT LOCATION (0 = LSB)	RECOMMENDED DEFAULT	FUNCTION
TFS[7:0]	7–0	00001111*	Programs series capacitor values in the tracking filter.

*See the *RF Tracking Filter* section.

Table 10. Tracking Filter Parallel Capacitor Register (Address: 1000_b)

BIT NAME	BIT LOCATION (0 = LSB)	RECOMMENDED DEFAULT	FUNCTION
FLD	7	0	Filter load bit. A 0 to 1 transition of this bit forces the loading of the ROM Table Data Readback register.
RESERVED	6	0	Must be set to 0.
TFP[5:0]	5–0	001001*	Programs parallel capacitor values in the tracking filter.

*See the *RF Tracking Filter* section.

Table 11. Tracking Filter ROM Address Register (Address: 1001_b)

BIT NAME	BIT LOCATION (0 = LSB)	RECOMMENDED DEFAULT	FUNCTION
RESERVED	7–4	0000	Must be set to 0000.
TFA[3:0]	3–0	0000*	Address bits of the ROM register to be read.

*See the *RF Tracking Filter* section.

Table 12. Reserved Register (Address: 1010_b)

BIT NAME	BIT LOCATION (0 = LSB)	RECOMMENDED DEFAULT	FUNCTION
RESERVED	7–0	N/A	Reserved. Do not program these bits during normal operation.

Table 13. ROM Table Data Readback Register (Address: 1011_b)

BIT NAME	BIT LOCATION (0 = LSB)	RECOMMENDED DEFAULT	FUNCTION
TFR[7:0]	7–0	00000000*	Tracking filter data bits read from the device's ROM table.

*See the *RF Tracking Filter* section.

Table 14. Status Register (Address: 1100_b)

BIT NAME	BIT LOCATION (0 = LSB)	RECOMMENDED DEFAULT	FUNCTION
POR	7	N/A	Power-on reset. 0 = Status register has been read 1 = Power reset since last status register read
LD[2:0]	6–4	N/A	VCO tuning voltage indicators. 000 = PLL not in lock, tune to the next lowest sub-band 001–110 = PLL in lock 111 = PLL not in lock, tune to the next higher sub-band
RESERVED	3–0	N/A	Reserved.

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2-Wire Serial Interface

The MAX3542 uses a 2-wire I²C-compatible serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX3542 and the master at clock frequencies up to 400kHz. The master initiates a data transfer on the bus and generates the SCL signal to permit data transfer. The MAX3542 behaves as a slave device that transfers and receives data to and from the master. Pull SDA and SCL high with external pullup resistors (1kΩ or greater) for proper bus operation.

One bit is transferred during each SCL clock cycle. A minimum of nine clock cycles is required to transfer a byte in or out of the MAX3542 (8 data bits and an ACK/NACK). The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *START and STOP Conditions* section). Both SDA and SCL remain high when the bus is not busy.

START and STOP Conditions

The master initiates a transmission with a START condition (S), which is a high-to-low transition on SDA while SCL is high. The master terminates a transmission with a STOP condition (P), which is a low-to-high transition on SDA while SCL is high.

Acknowledge and Not-Acknowledge Conditions

Data transfers are framed with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX3542 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse.

To generate a not-acknowledge condition, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse, and leaves SDA high during the high period of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master must reattempt communication at a later time.

Slave Address

The MAX3542 has a 7-bit slave address that must be sent to the device following a START condition to initiate communication. The slave address is determined by the state of the ADDR2 and ADDR1 pins and is equal to 11000[ADDR2][ADDR1]. The 8th bit (R/$\overline{W}$) following the 7-bit address determines whether a read or write operation occurs. Table 15 shows the possible address configurations.

The MAX3542 continuously awaits a START condition followed by its slave address. When the device recognizes its slave address, it acknowledges by pulling the SDA line low for one clock period; it is ready to accept or send data depending on the R/$\overline{W}$ bit (Figure 1).

Table 15. MAX3542 Address Configurations

ADDR2	ADDR1	WRITE ADDRESS	READ ADDRESS
0	0	0xC0	0xC1
0	1	0xC2	0xC3
1	0	0xC4	0xC5
1	1	0xC6	0xC7

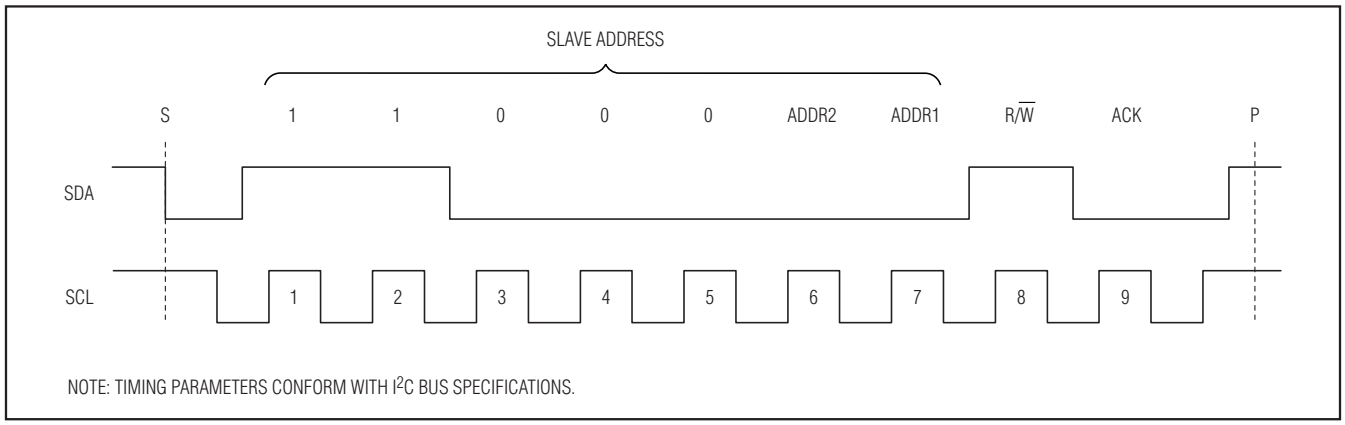

Figure 1. MAX3542 Slave Address Byte

Write Cycle

When addressed with a write command, the MAX3542 allows the master to write to a single register or to multiple successive registers.

A write cycle begins with the bus master issuing a START condition followed by the seven slave address bits and a write bit (R/$\overline{W}$ = 0). The MAX3542 issues an ACK if the slave address byte is successfully received. The bus master must then send to the slave the address of the first register it wishes to write to. If the slave acknowledges the address, the master can then write one byte to the register at the specified address. Data is written beginning with the most significant bit. The MAX3542 again issues an ACK if the data is successfully written to the register. The master can continue to write data to the successive internal registers with the MAX3542 acknowledging each successful transfer, or it can terminate transmission by issuing a STOP condition. The write cycle does not terminate until the master issues a STOP condition.

Figure 2 illustrates an example in which registers 0 through 2 are written with 0x0E, 0xD8, and 0xE1, respectively.

Read Cycle

A read cycle begins with the bus master issuing a START condition followed by the seven slave address bits and a write bit (R/$\overline{W}$ = 0). The MAX3542 issues an ACK if the slave address byte is successfully received. The master then sends the 8-bit address of the first register that it wishes to read. The MAX3542 then issues another ACK. Next, the master must issue a START condition followed by the seven slave address bits and a read bit (R/$\overline{W}$ = 1). The MAX3542 issues an ACK if it successfully recognizes its address and begins sending data from the specified register address starting with the most significant bit (MSB). Data is clocked out of the MAX3542 on the rising edge of SCL. On the 9th rising edge of SCL, the master can issue an ACK and continue reading successive registers or it can issue a NACK followed by a STOP condition to terminate transmission. The read cycle does not terminate until the master issues a STOP condition. Figure 3 illustrates an example in which registers 0 and 1 are read back.

START	WRITE DEVICE ADDRESS	R/$\overline{W}$	ACK	WRITE REGISTER ADDRESS	ACK	WRITE DATA TO REGISTER 0x00	ACK	WRITE DATA TO REGISTER 0x01	ACK	WRITE DATA TO REGISTER 0x02	ACK	STOP
	11000[ADDR2][ADDR1]	0	—	0x00	—	0x0E	—	0xD8	—	0xE1	—	

Figure 2. Example: Write Registers 0 through 2 with 0x0E, 0xD8, and 0xE1, Respectively

START	WRITE DEVICE ADDRESS	R/$\overline{W}$	ACK	WRITE 1ST REGISTER ADDRESS	ACK	START	WRITE DEVICE ADDRESS	R/$\overline{W}$	ACK	READ DATA REG 0	ACK	READ DATA REG 1	NACK	STOP
	11000[ADDR2][ADDR1]	0	—	0x00	—		11000[ADDR2][ADDR1]	1	—	D7–D0	—	D7–D0	—	

Figure 3. Example: Read Data from Registers 0 and 1

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Applications Information

RF Inputs

The MAX3542 features separate UHF and VHF inputs that are matched to 75Ω. Both inputs require a DC-blocking capacitor. The active inputs are selected by the input registers. In addition, the input registers enable or disable the lowpass filter, which can be used when the VHF input is selected. For 47MHz to 100MHz, select the VHF_IN with the LPF filter enabled (INPT = 00). For 100MHz to 326MHz, select VHF_IN with LPF disabled (INPT = 01). For 326MHz to 862MHz, select UHF_IN (INPT = 10).

The separate VHF and UHF inputs can be driven from a single RF source using a diplex filter. For diplex filter schematic and component values, refer to the MAX3542 Evaluation Kit data sheet.

RF Gain Control

The gain of the RF LNA can be adjusted over a typical range of 45dB with the RFAGC pin. The RFAGC input accepts a DC voltage from 0.5V to 3V, with 3V providing maximum gain. This pin can be controlled with the IF power-detector output to form a closed RF gain-control loop. See the *Closed-Loop RF Gain Control* section for more information.

RF Tracking Filter

The MAX3542 includes a programmable tracking filter for each band of operation to optimize rejection of out-of-band interference while minimizing insertion loss for the desired received signal. The center frequency of each tracking filter is selected by a switched-capacitor array that is programmed by the TFS[7:0] bits in the Tracking Filter Series Capacitor register and the TFP[5:0] bits in the Tracking Filter Parallel Capacitor register.

Optimal tracking filter settings for each channel vary from part to part due to process variations. To accommodate part-to-part variations, each part is factory calibrated by Maxim. During calibration, the y-intercept and slope for the series and parallel tracking capacitor arrays are calculated and written into an internal ROM table. The user must read the ROM table upon power-up and store the data in local memory (8 bytes total) to calculate the optimal TFS[7:0] and TFP[5:0] settings for each channel. Table 16 shows the address and bits for each ROM table entry. See the *Interpolating Tracking Filter Coefficients* section for more information on how to calculate the required values.

Reading the ROM Table

Each ROM table entry must be read using a two-step process. First, the address of the ROM bits to be read must be programmed into the TFA[3:0] bits in the Tracking Filter ROM Address register (Table 11).

Once the address has been programmed, the data stored in that address is transferred to the TFR[7:0] bits in the ROM Table Data Readback register (Table 13). The ROM data at the specified address can then be read from the TFR[7:0] bits and stored in the microprocessor's local memory.

Table 16. ROM Table

DESCRIPTION	ADDRESS	MSB							LSB
		DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Reserved	0x0	OD[2]	OD[1]	OD[0]	X	X	X	X	X
VHF Low	0x1	LS0[5]	LS0[4]	LS0[3]	LS0[2]	LS0[1]	LS0[0]	LS1[3]	LS1[2]
VHF Low	0x2	LS1[1]	LS1[0]	LP0[5]	LP0[4]	LP0[3]	LP0[2]	LP0[1]	LP0[0]
VHF Low VHF High	0x3	LP1[3]	LP1[2]	LP1[1]	LP1[0]	HS0[5]	HS0[4]	HS0[3]	HS0[2]
VHF High	0x4	HS0[1]	HS0[0]	HS1[3]	HS1[2]	HS1[1]	HS1[0]	HP0[5]	HP0[4]
VHF High	0x5	HP0[3]	HP0[2]	HP0[1]	HP0[0]	HP1[3]	HP1[2]	HP1[1]	HP1[0]
UHF	0x6	US0[5]	US0[4]	US0[3]	US0[2]	US0[1]	US0[0]	US1[5]	US1[4]
UHF	0x7	US1[3]	US1[2]	US1[1]	US1[0]	UP0[5]	UP0[4]	UP0[3]	UP0[2]
UHF	0x8	UP0[1]	UP0[0]	UP1[5]	UP1[4]	UP1[3]	UP1[2]	UP1[1]	UP1[0]

Interpolating Tracking Filter Coefficients

The TFS[7:0] and TFP[5:0] bits must be reprogrammed for each channel frequency to optimize performance. The optimal settings for each channel can be calculated from the ROM table data using the equations below:

Analog (PAL) Channels:

VHF_LO Filter:

$$TFS = INT[10^{[(1.1 \times \frac{LS0}{64} + 2.2) + (4 \times \frac{LS1}{16} - 12) \times f_{RF} \times 10^{-3}]}] - 10$$

$$TFP = INT[10^{[(0.8 \times \frac{LP0}{64} + 1.6) + (8 \times \frac{LP1}{16} - 14) \times f_{RF} \times 10^{-3}]}]$$

VHF_HI Filter:

$$TFS = INT[10^{[(1.3 \times \frac{HS0}{64} + 2.5) + (4 \times \frac{HS1}{16} - 8) \times f_{RF} \times 10^{-3}]}] - 10$$

$$TFP = INT[10^{[(0.8 \times \frac{HP0}{64} + 1.6) + (1.6 \times \frac{HP1}{16} - 3.2) \times f_{RF} \times 10^{-3}]}]$$

UHF Filter:

$$TFS = INT[10^{[(\frac{US0}{64} + 3) + (2 \times \frac{US1}{64} - 3) \times f_{RF} \times 10^{-3}]}] - 20$$

$$TFP = INT[10^{[(0.8 \times \frac{UP0}{64} + 1.6) + (2 \times \frac{UP1}{64} - 2.5) \times f_{RF} \times 10^{-3}]}] - 10$$

where:

f_{RF} = operating frequency in megahertz.

TFS = decimal value of the optimal TFS[7:0] setting (Table 9) for the given operating frequency.

TFP = decimal value of the optimal TFP[5:0] setting (Table 10) for the given operating frequency.

LS0, LS1, LP0, LP1, HS0, HS1, HP0, HP1, US0, US1, UP0, and UP1 = the decimal values of the ROM table coefficients (Table 16).

Digital (DVB-T) channels:

Consult the factory for DVB-T coefficients.

IF Overload Detector

The MAX3542 includes a broadband IF overload detector, which provides an indication of the total power present at the RF input. The overload-detector output voltage is compared to a reference voltage, and the difference is amplified. This error signal drives an open-collector transistor whose collector is connected to the IFOVLD pin, causing the IFOVLD pin to sink current. The nominal full-scale current sunk by the IFOVLD pin is 300µA. The IFOVLD pin requires a 10kΩ pullup resistor to V_{CC}.

The IF overload detector is calibrated at the factory to attack at $0.7V_{P-P}$ at the IFOUT1. Upon power-up, the baseband processor must read OD[2:0] from the ROM table and store it in the IFOVLD register.

Closed-Loop RF Gain Control

Closed-loop RF gain control can be implemented by connecting the IFOVLD output to the RFAGC input. Using a 10kΩ pullup resistor on the IFOVLD pin as shown in the *Typical Application Circuit* results in a nominal control voltage range of 0.5V to 3V.

VCO and VCO Divider Selection

The MAX3542 frequency synthesizer includes three VCOs and eight VCO sub-bands to guarantee a 2200MHz to 4400MHz VCO frequency range. The frequency synthesizer also features an additional VCO frequency divider that must be programmed to either 4, 8, 16, or 32 by the VDIV[1:0] bits in the VCO register based on the channel being received.

To ensure PLL lock, the proper VCO and VCO sub-band for the channel being received must be chosen by iteratively selecting a VCO and VCO sub-band, then reading the LD[2:0] bits to determine if the PLL is locked. Any reading from 001 to 110 indicates the PLL is locked. If LD[2:0] reads 000, the PLL is unlocked and the selected VCO is at the bottom of its tuning range; a lower VCO sub-band must be selected. If LD[2:0] reads 111, the PLL is unlocked and the selected VCO is at the top of its tuning range; a higher VCO sub-band must be selected. The VCO and VCO sub-band settings should be progressively increased or decreased until the LD[2:0] reading falls in the 001 to 110 range.

Due to overlap between VCO sub-band frequencies, it is possible that multiple VCO settings can be used to tune to the same channel frequency. System performance at a given channel should be similar between the various possible VCO settings, so it is sufficient to select the first VCO and VCO sub-band that provides lock.

Layout Considerations

The MAX3542 EV kit can serve as a guide for PCB layout. Keep RF signal lines as short as possible to minimize losses and radiation. Use controlled impedance on all high-frequency traces. The exposed paddle must be soldered evenly to the board's ground plane for proper operation. Use abundant vias beneath the exposed paddle for maximum heat dissipation. Use abundant ground vias between RF traces to minimize undesired coupling.

To minimize coupling between different sections of the IC, the ideal power-supply layout is a star configuration, which has a large decoupling capacitor at the central V_{CC} node. The V_{CC} traces branch out from this node, with each trace going to separate V_{CC} pins of the MAX3542. Each V_{CC} pin must have a bypass capacitor with a low impedance to ground at the frequency of interest. Do not share ground vias among multiple connections to the PCB ground plane.

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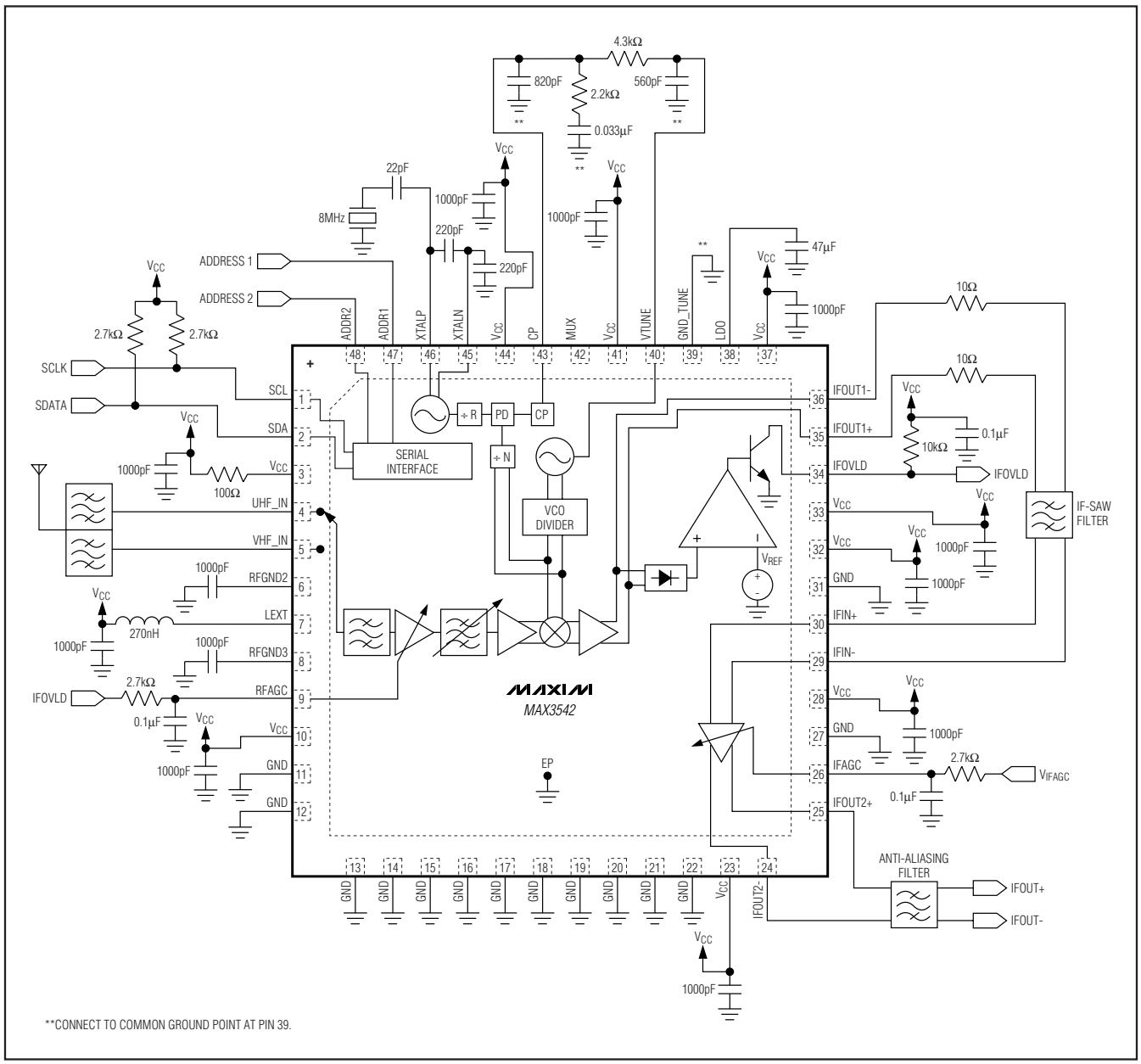
Typical Application Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 LGA-EP	L4877A+1	21-0157	90-0302

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/07	Initial release	—
1	12/07	Correct TOC01 graph and a few errors	1, 2, 5, 7
2	4/11	Added soldering temperature and corrected lead temperature in the *Absolute Maximum Ratings*	2