19-2727; Rev 2; 6/04

EVALUATION KIT AVAILABLE

1.5Gbps Serial ATA-Compatible Mux/Buffer with Loopback and Equalization

General Description

The MAX3786 is an AC-coupled, serial-ATA (SATA)-compatible, 1.5Gbps multiplexer/buffer (mux/buffer) IC that provides the capability to switch a single serial data signal between two redundant I/O channels.

SATA out-of-band (OOB) signaling is supported using loss-of-signal (LOS) detect on all three inputs and shutdown on the corresponding outputs. The high-speed inputs and outputs are all internally terminated, compatible with 100Ω differential systems, and must be AC-coupled to the controller IC and SATA-compatible disk drive.

Receive equalization (EQ) and transmit preemphasis (PE) are provided on the dual I/O channels to mitigate the effects of intersymbol interference in the signal path. Loopback can be enabled on the nonselected I/O channel.

The MAX3786 operates from a single +3.3V supply and typically consumes 520mW with PE and EQ enabled. It is available in a 5mm x 5mm, 32-lead thin QFN exposed-pad package and operates over a 0°C to +85°C temperature range.

Applications

1.5Gbps Serial ATA Redundancy

Features

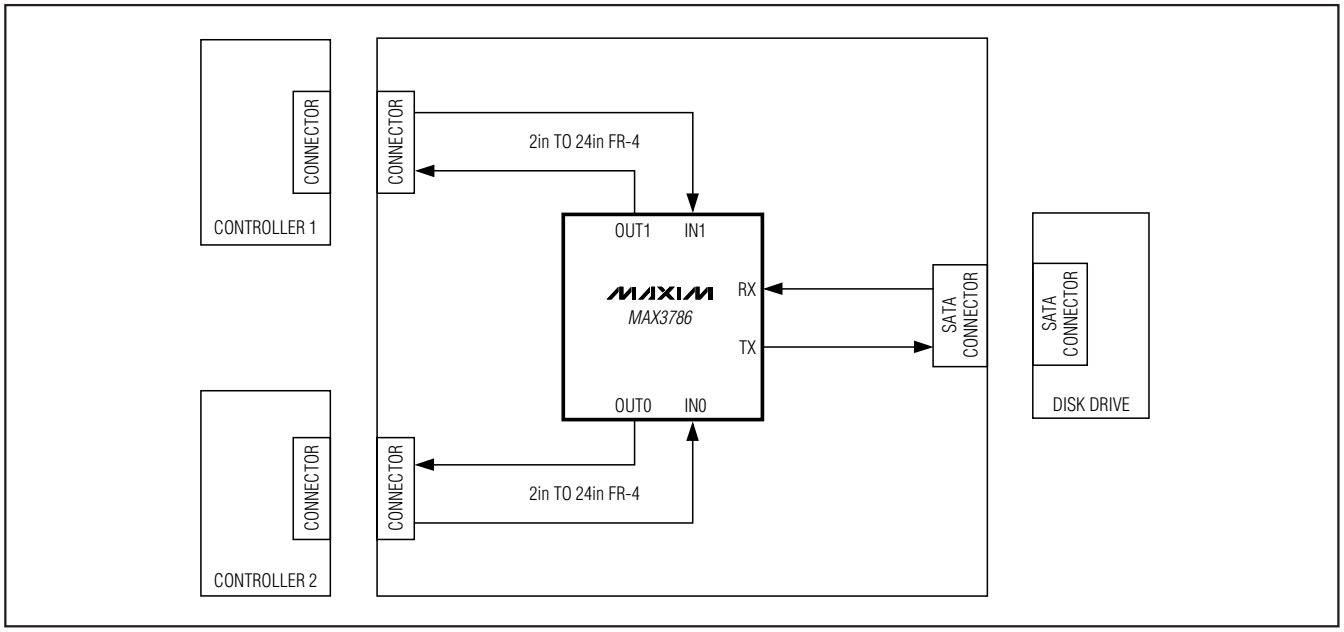
- **< 50psP-P Total Residual Jitter (20in FR-4, EQ and PE On)**
- **Supports SATA OOB Signaling**
- **Loopback of Nonselected Channel**
- **Receive Equalization and Transmit Preemphasis on Controller-Side I/O Channels**
- **0°C to +85°C Operation**
- **32-Pin, 5mm × 5mm Thin QFN Package**
- **+3.3V Power Supply**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3786UTJ	0°C to +85°C	32 Thin QFN-EP* (5mm × 5mm)	T3255-2
MAX3786UTJ+	0°C to +85°C	32 Thin QFN-EP* (5mm × 5mm)	—

+Denotes lead-free package.
**EP = Exposed pad.*

Typical Application Circuit



Pin Configuration and Functional Diagram appear at end of data sheet.

1.5Gbps Serial ATA-Compatible Mux/Buffer with Loopback and Equalization

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .....-0.5V to +5.0V
Continuous Current at Outputs
(TX±, OUT1±, OUT0±).....±22mA
Input Voltage
(RX±, IN1±, IN0±) .....-0.5V to (V_{CC} + 0.5V)
Differential Input Voltage
(RX±, IN1±, IN0±).....±2.0V

Voltage at $\overline{PE1EN}$, $\overline{PE0EN}$, $\overline{EQ1EN}$, $\overline{EQ0EN}$, $\overline{LB\_EN}$, SEL, CM1, CM0.....-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
32-Pin Thin QFN (derate 21.3mW/°C above +85°C) .1384mW
Operating Temperature Range.....0°C to +85°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	EQ and PE off		125	150	mA
		EQ and PE on		158	220	
Maximum Data Rate		(Note 1)	1.5			Gbps
Differential Input Voltage (RX, IN1, IN0)		(Note 2)	250		600	mV_{P-P}
Input Termination		Differential	85	100	115	Ω
Input Return Loss	|S11|	100MHz to 2.5GHz		14		dB
Input Equalization		At 750MHz		4.5		dB
Differential Output Voltage (TX, OUT0, OUT1) (Note 2)		PE off	400	500	600	mV_{P-P}
		Output disabled by OOB signaling			30	
Output Termination		Single ended to V_{CC}	42.5	50	57.5	Ω
Output Transition Time		1.5Gbps data, 20% to 80% (Notes 1, 3)	135	200	270	ps
Output Preemphasis		At 750MHz (Note 4)		4.5		dB
Output Jitter		DJ + 14RJ, EQ and PE off (Notes 1, 5, 8)		30	40	ps_{P-P}
Total Residual Jitter		DJ + 14RJ, EQ and PE on (Notes 1, 6, 8)		40	50	ps_{P-P}
Differential Output Skew		(Note 1)			20	ps
LOS Detector Threshold			50		150	mV_{P-P}
Output Startup/Shutdown Time		(Note 7)			5	ns
LVCMOS Input High Voltage	V_{IH}		1.5			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

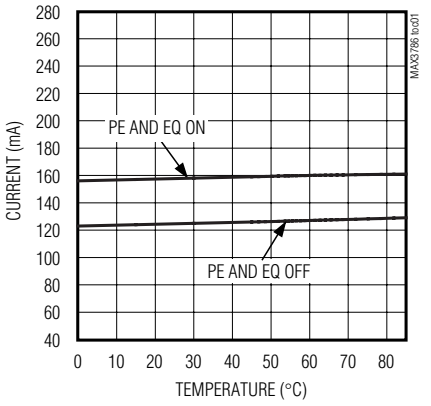
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVCMOS Input Low Voltage	V_{IL}				0.5	V
LVCMOS Input High Current	I_{OH}	V_{IH} = +2.0V to (V_{CC} + 0.3V)			150	µA
LVCMOS Input Low Current	I_{OL}	V_{IL} = -0.3V to +0.8V			150	µA

Note 1: AC specifications are guaranteed by design and characterization.
Note 2: Differential voltage is defined as V_{P-P} = (V+ - V-). Inputs and outputs must be AC-coupled for proper operation.
Note 3: Output transition time measured using a 0000011111 pattern, with transmit PE off.
Note 4: Transmit PE compensates for 20in of 6-mil-wide differential stripline in FR-4 or equivalent path loss.
Note 5: Jitter after paths from RX to OUT_ or IN_ to TX. Measured with no jitter on the input, using a ±K28.5 pattern, and a path consisting of the MAX3786 alone.
Note 6: Jitter after EQ for the paths from RX to OUT_ or IN_ to TX. Measured with no jitter on the input, using a ±K28.5 pattern, and a path consisting of the MAX3786 plus 20in of 6-mil-wide differential stripline in FR-4 on the output.
Note 7: Total time for LOS to enable/disable the outputs.
Note 8: Measured with a 100mV sinusoidal common-mode signal in the 2MHz ≤ f ≤ 200MHz range.

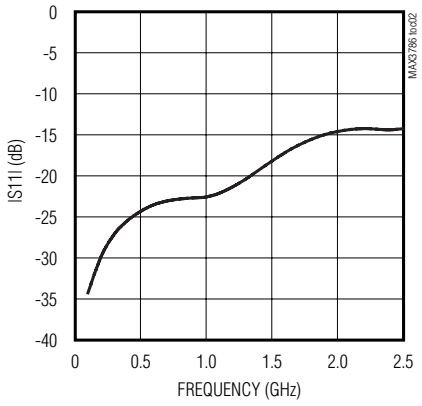
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

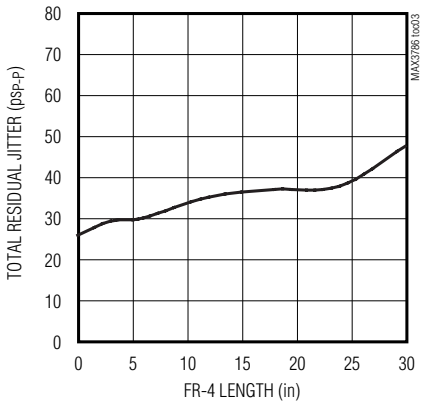
SUPPLY CURRENT vs. TEMPERATURE



DIFFERENTIAL INPUT RETURN LOSS



TOTAL RESIDUAL JITTER vs. PATH LENGTH (FR-4 STRIPLINE AT OUT0, ±K28.5 PATTERN)

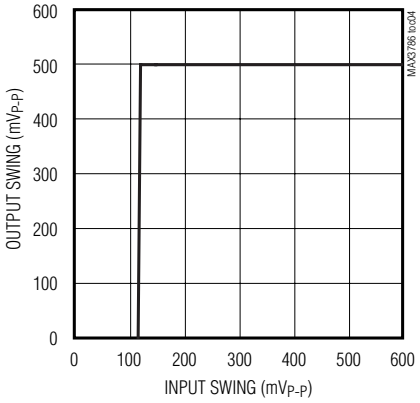


1.5Gbps Serial ATA-Compatible Mux/Buffer with Loopback and Equalization

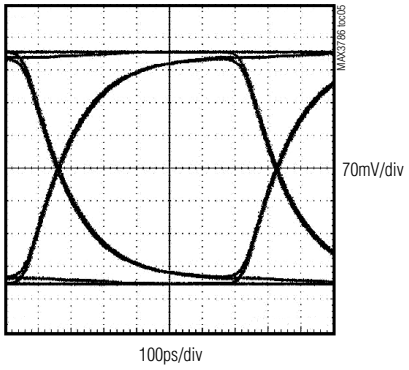
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

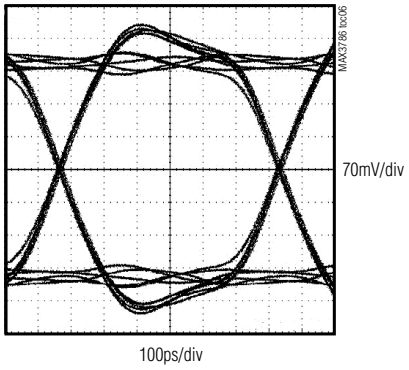
OUTPUT SWING vs. INPUT SWING (±K28.5 PATTERN)



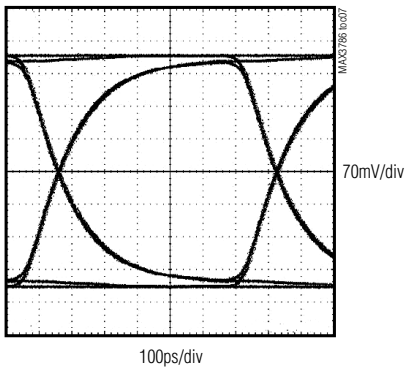
OUTPUT EYE DIAGRAM, RECEIVE EQ ON (10in FR-4 STRIPLINE AT IN0, ±K28.5 PATTERN)



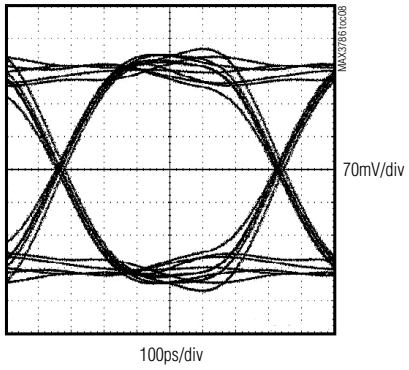
OUTPUT EYE DIAGRAM, TRANSMIT PE ON (10in FR-4 STRIPLINE AT OUT0, ±K28.5 PATTERN)



OUTPUT EYE DIAGRAM, RECEIVE EQ ON (20in FR-4 STRIPLINE AT IN0, ±K28.5 PATTERN)



OUTPUT EYE DIAGRAM, TRANSMIT PE ON (20in FR-4 STRIPLINE AT OUT0, ±K28.5 PATTERN)



Pin Description

PIN	NAME	FUNCTION
1, 4, 8, 15, 17, 20, 21, 24, 26, 30	V_{CC}	+3.3V Supply Voltage
2	TX+	Positive TX Data Output, CML. Serial ATA compatible.
3	TX-	Negative TX Data Output, CML. Serial ATA compatible.
5	SEL	Multiplex Select Control Input, LVCMOS. Set high to connect RX/TX to OUT1/IN1.
6	RX-	Negative RX Data Input, CML. Serial ATA compatible.
7	RX+	Positive RX Data Input, CML. Serial ATA compatible.
9	$\overline{PE1EN}$	Channel 1 Preemphasis Enable Input, LVCMOS. Set low to enable OUT1 PE.
10	$\overline{EQ1EN}$	Channel 1 Equalization Enable Input, LVCMOS. Set low to enable IN1 EQ.
11	$\overline{LB\_EN}$	Loopback Enable Input, LVCMOS. Set low to loopback data on nonselected channel.
12	CM1	Input 1 Common-Mode Point. Normally not connected; can be connected to V_{CC} through 1.0µF capacitor. See Figure 1.
13	IN1-	Negative Channel 1 Data Input, CML. Serial ATA compatible.
14	IN1+	Positive Channel 1 Data Input, CML. Serial ATA compatible.
16, 25	GND	Supply Ground
18	OUT1-	Negative Channel 1 Data Output, CML. Serial ATA compatible.
19	OUT1+	Positive Channel 1 Data Output, CML. Serial ATA compatible.
22	OUT0-	Negative Channel 0 Data Output, CML. Serial ATA compatible.
23	OUT0+	Positive Channel 0 Data Output, CML. Serial ATA compatible.
27	IN0-	Negative Channel 0 Data Input, CML. Serial ATA compatible.
28	IN0+	Positive Channel 0 Data Input, CML. Serial ATA compatible.
29	CM0	Input 0 Common-Mode Point. Normally not connected; can be connected to V_{CC} through 1.0µF capacitor. See Figure 1.
31	$\overline{EQ0EN}$	Channel 0 Equalization Enable Input, LVCMOS. Set low to enable IN0 EQ.
32	$\overline{PE0EN}$	Channel 0 Preemphasis Enable Input, LVCMOS. Set low to enable OUT0 PE.
EP	Exposed pad	Ground. The exposed pad must be soldered to the circuit board ground for proper thermal and electrical performance.

Detailed Description

The MAX3786 consists of three multiplexers, I/O buffers, and LOS-detection circuitry (see the *Functional Diagram*). The buffers on the controller side provide EQ on the inputs and PE on the outputs.

Mux/Buffer Logic

By means of the LVCMOS input SEL, a SATA-compatible device at TX/RX can be connected to either IN0/OUT0 or IN1/OUT1. When SEL is low, TX/RX are connected to IN0/OUT0, and when SEL is high, TX/RX are connected to IN1/OUT1. Use of the SEL input provides the ability to operate a single SATA disk drive from redundant controllers. Loopback is provided on the IN_/OUT_ side and is controlled by the LVCMOS input $\overline{LB\_EN}$. When $\overline{LB\_EN}$ is low, the nonselected IN_/OUT_ loops back (see Table 1). The SEL and $\overline{LB\_EN}$ control lines are internally pulled high through 40kΩ resistors (see the *Functional Diagram*).

Loss-of-Signal Logic

At each high-speed input to the MAX3786, an LOS circuit is provided. In this circuit, a differential signal of $50mV_{P-P}$ or less is detected as OFF, and a signal of greater than $150mV_{P-P}$ is detected as ON. The LOS detectors, in combination with the select logic, control their associated high-speed output-disable circuits, so

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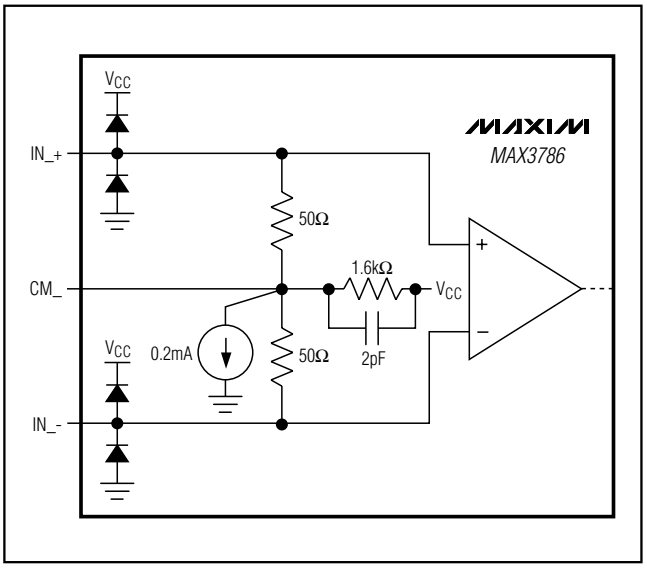

Figure 1. Input Structure (IN0, IN1)

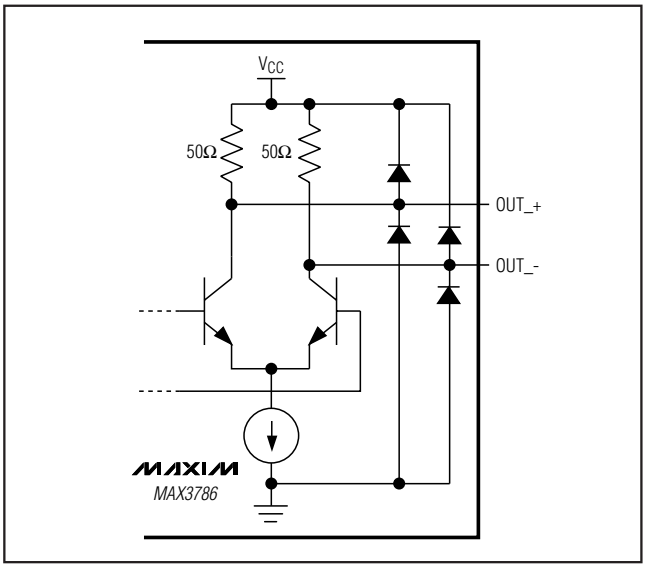

Figure 2. Output Structure (OUT0, OUT1)

that OOB signaling is transmitted through the MAX3786 (see Table 1). The time for the LOS circuit to detect an inactive input and disable the associated output, or detect an active input and enable the output, is less than 5ns.

Equalization and Preemphasis

High-speed inputs IN0 and IN1 have integrated equalization, and high-speed outputs OUT0 and OUT1 have integrated PE to mitigate the effects of intersymbol interference in an FR-4 transmission line signal path. These circuits provide EQ or PE that matches the typical path loss of a 20in, 6-mil FR-4 differential stripline.

Four active-low LVCMOS inputs, $\overline{EQ0EN}$, $\overline{EQ1EN}$, $\overline{PE0EN}$, and $\overline{PE1EN}$ are provided to enable EQ and PE independently. All four control lines are internally pulled high through 40kΩ resistors (see the *Functional Diagram*). EQ and PE should be enabled when the total path loss exceeds approximately 2.5dB.

Input Terminations

All high-speed inputs accept current-mode logic (CML) and are SATA compatible. The inputs contain internal 100Ω differential termination, and must be AC-coupled to the controller IC and SATA-compatible disk drive for proper operation.

Two pins (CM0 and CM1) provide access to the IN0 and IN1 common-mode points. CM0 and CM1 are normally left unconnected; however, a capacitor up to 1.0µF can be connected from each CM_ pin to V_{CC}, providing a low-impedance AC common-mode path to V_{CC} (see Figure 1).

Output Terminations

The MAX3786 uses CML for its high-speed outputs. They are SATA compatible and provide 50Ω terminations to V_{CC} (see Figure 2). The high-speed outputs must be AC-coupled to the controller IC and SATA-compatible disk drive for proper operation.

Applications Information

Hot Swap

The MAX3786 is designed so that arbitrary sequencing of V_{CC} and I/O signals during startup does not affect operation of the part.

Exposed-Pad Package

The MAX3786 is available in a 5mm × 5mm, 32-pin thin QFN package with EP for signal integrity and placement flexibility. The exposed pad provides thermal and electrical connectivity to the IC, and must be soldered to a high-frequency ground plane. It is recommended to use at least nine vias to connect the ground pad underneath the 32-lead thin QFN package to the PC board ground plane.

Layout Considerations

Use controlled-impedance transmission lines to interface with the MAX3786 high-speed inputs and outputs. Power-supply decoupling capacitors should be placed as close as possible to the V_{CC} pins.

Table 1. Operation Truth Table

INPUT CONTROLS		LOSS-OF-SIGNAL DETECT			OUTPUT FUNCTION		
SEL	$\overline{LB\_EN}$	LOS_RX	LOS_0	LOS_1	TX	OUT0	OUT1
Low	Low	False	False	False	IN0	RX	IN1
Low	Low	False	False	True	IN0	RX	OFF
Low	Low	False	True	False	Off	RX	IN1
Low	Low	False	True	True	Off	RX	Off
Low	Low	True	False	False	IN0	Off	IN1
Low	Low	True	False	True	IN0	Off	Off
Low	Low	True	True	False	Off	Off	IN1
Low	Low	True	True	True	Off	Off	Off
Low	High	False	False	X	IN0	RX	Off
Low	High	False	True	X	Off	RX	Off
Low	High	True	False	X	IN0	Off	Off
Low	High	True	True	X	Off	Off	Off
High	Low	False	False	False	IN1	IN0	RX
High	Low	False	False	True	Off	IN0	RX
High	Low	False	True	False	IN1	Off	RX
High	Low	False	True	True	Off	Off	RX
High	Low	True	False	False	IN1	IN0	Off
High	Low	True	False	True	Off	IN0	Off
High	Low	True	True	False	IN1	Off	Off
High	Low	True	True	True	Off	Off	Off
High	High	False	X	False	IN1	Off	RX
High	High	False	X	True	Off	Off	RX
High	High	True	X	False	IN1	Off	Off
High	High	True	X	True	Off	Off	Off

SEL = Low connects TX/RX to IN0/OUT0, high connects TX/RX to IN1/OUT1.

LOS = True indicates loss of signal.

$\overline{LB\_EN}$ = Low enables loopback of nonselected channel.

X = Don't care.

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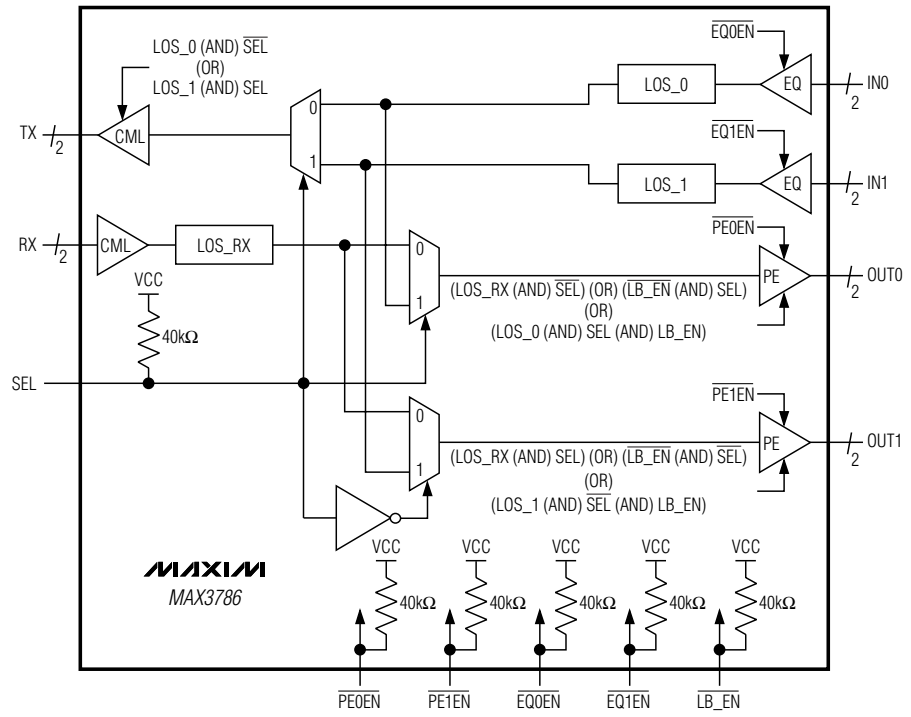
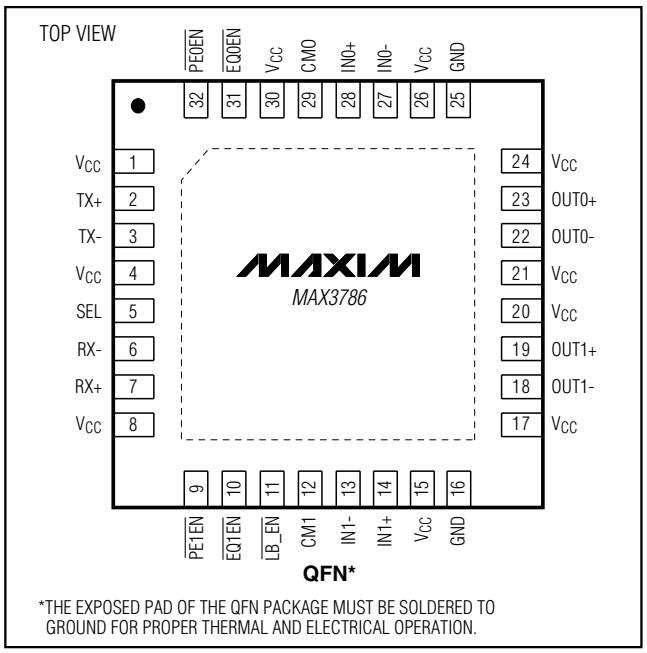
Functional Diagram



Pin Configuration



QFN*

*THE EXPOSED PAD OF THE QFN PACKAGE MUST BE SOLDERED TO GROUND FOR PROPER THERMAL AND ELECTRICAL OPERATION.

Chip Information

TRANSISTOR COUNT: 2848

PROCESS: SiGe BiCMOS

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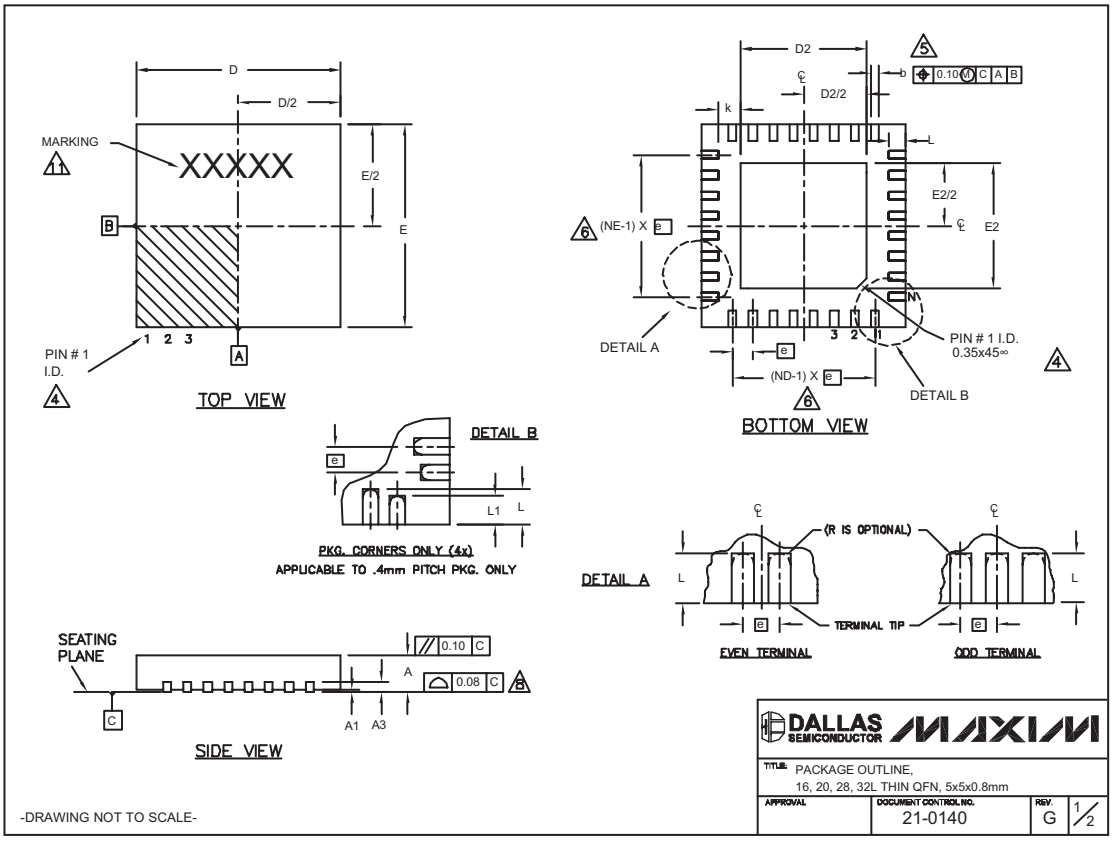
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS												
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
L1	-	-	-	-	-	-	-	-	-	-	-	-
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	Y
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	Y
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	N
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO

** SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32L THIN QFN, 5x5x0.8mm

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