19-1522; Rev 4; 11/09

Ultra-Small, Low-Cost, 210MHz, Single-Supply Op Amps with Rail-to-Rail Outputs

MAX4450/MAX4451

General Description

The MAX4450 single and MAX4451 dual op amps are unity-gain-stable devices that combine high-speed performance with rail-to-rail outputs. Both devices operate from a +4.5V to +11V single supply or from ±2.25V to ±5.5V dual supplies. The common-mode input voltage range extends beyond the negative power-supply rail (ground in single-supply applications).

The MAX4450/MAX4451 require only 6.5mA of quiescent supply current per op amp while achieving a 210MHz -3dB bandwidth and a 485V/µs slew rate. Both devices are an excellent solution in low-power/low-voltage systems that require wide bandwidth, such as video, communications, and instrumentation.

The MAX4450 is available in the ultra-small 5-pin SC70 package, while the MAX4451 is available in space-saving 8-pin SOT23 and SO packages.

Features

- **Ultra-Small SC705 and SOT23 Packages**
- **Low Cost**
- **High Speed**
  - **210MHz -3dB Bandwidth**
  - **55MHz 0.1dB Gain Flatness**
  - **485V/µs Slew Rate**
- **Single +4.5V to +11V Operation**
- **Rail-to-Rail Outputs**
- **Input Common-Mode Range Extends Beyond V_{EE}**
- **Low Differential Gain/Phase: 0.02%/0.08°**
- **Low Distortion at 5MHz**
  - **-65dBc SFDR**
  - **-63dB Total Harmonic Distortion**

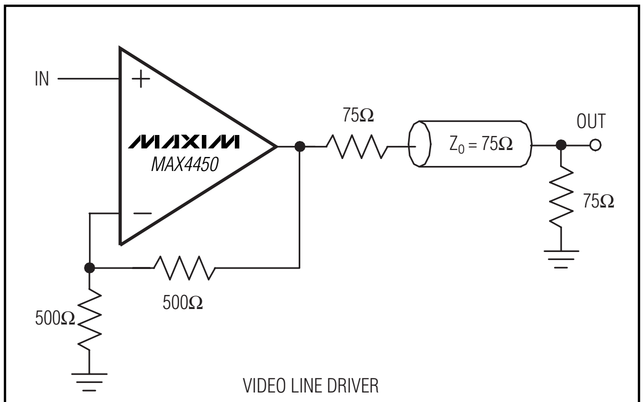
Applications

Set-Top Boxes
Surveillance Video Systems
Battery-Powered Instruments
Video Line Driver
Analog-to-Digital Converter Interface
CCD Imaging Systems
Video Routing and Switching Systems
Digital Cameras

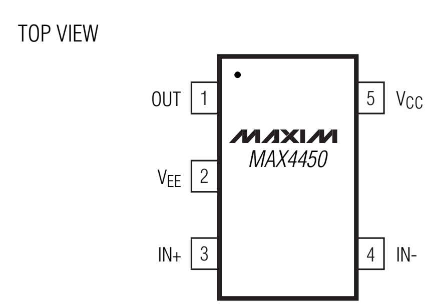
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4450EXK-T	-40°C to +85°C	5 SC70	AAA
MAX4450EUK-T	-40°C to +85°C	5 SOT23	ADKP
MAX4451EKA-T	-40°C to +85°C	8 SOT23	AAAA
MAX4451ESA	-40°C to +85°C	8 SO	—

Typical Operating Circuit



Pin Configurations



SC70/SOT23

Pin Configurations continued at end of data sheet.

Ultra-Small, Low-Cost, 210MHz, Single-Supply Op Amps with Rail-to-Rail Outputs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE})..+12V
IN_-, IN_+, OUT_..............................(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Output Short-Circuit Current to V_{CC} or V_{EE} 150mA
Continuous Power Dissipation (T_A = +70°C)
  5-Pin SC70-5 (derate 2.5mW/°C above +70°C)..........200mW
  5-Pin SOT23-5 (derate 7.1mW/°C above +70°C)........571mW
  8-Pin SOT23-8 (derate 5.26mW/°C above +70°C)......421mW
  8-Pin SO (derate 5.9mW/°C above +70°C).................471mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or at any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = 0V, R_L = ∞ to V_{CC}/2, V_{OUT} = V_{CC}/2, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by CMRR test		V_{EE} - 0.20		V_{CC} 2.25	V
Input Offset Voltage (Note 2)	V_{OS}				4	26	mV
Input Offset Voltage Matching					1.0		mV
Input Offset Voltage Temperature Coefficient	TC_{VOS}				8		µV/°C
Input Bias Current	I_B	(Note 2)			6.5	20	µA
Input Offset Current	I_{OS}	(Note 2)			0.5	4	µA
Input Resistance	R_{IN}	Differential mode (-1V ≤ V_{IN} ≤ +1V)			70		kΩ
		Common mode (-0.2V ≤ V_{CM} ≤ +2.75V)			3		MΩ
Common-Mode Rejection Ratio	CMRR	(V_{EE} - 0.2V) ≤ V_{CM} ≤ (V_{CC} - 2.25V)		70	95		dB
Open-Loop Gain (Note 2)	A_{VOL}	0.25V ≤ V_{OUT} ≤ 4.75V, R_L = 2kΩ		50	60		dB
		0.5V ≤ V_{OUT} ≤ 4.5V, R_L = 150Ω		48	58		
		1V ≤ V_{OUT} ≤ 4V, R_L = 50Ω			57		
Output Voltage Swing (Note 2)	V_{OUT}	R_L = 2kΩ	V_{CC} - V_{OH}		0.05	0.20	V
			V_{OL} - V_{EE}		0.05	0.15	
		R_L = 150Ω	V_{CC} - V_{OH}		0.30	0.50	
			V_{OL} - V_{EE}		0.25	0.80	
		R_L = 75Ω	V_{CC} - V_{OH}		0.5	0.80	
			V_{OL} - V_{EE}		0.5	1.75	
Output Current	I_{OUT}	R_L = 50Ω	Sourcing	45	70		mA
			Sinking	25	50		
Output Short-Circuit Current	I_{SC}	Sinking or sourcing			±120		mA
Open-Loop Output Resistance	R_{OUT}				8		Ω
Power-Supply Rejection Ratio (Note 3)	PSRR	V_{CC} = 5V	V_{EE} = 0V, V_{CM} = 2V	46	62		dB
			V_{EE} = -5V, V_{CM} = 0V	54	69		
Operating Supply-Voltage Range	V_S	V_{CC} to V_{EE}		4.5		11.0	V
Quiescent Supply Current (per amplifier)	I_S				6.5	9.0	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = +2.5V, R_F = 24Ω, R_L = 100Ω to V_{CC}/2, V_{OUT} = V_{CC}/2, A_{VCL} = +1V/V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{SS}	V_{OUT} = 100mV_{P-P}			210		MHz
Large-Signal -3dB Bandwidth	BW_{LS}	V_{OUT} = 2V_{P-P}			175		MHz
Bandwidth for 0.1dB Gain Flatness	$BW_{0.1dB}$	V_{OUT} = 100mV_{P-P}			55		MHz
Slew Rate	SR	V_{OUT} = 2V step			485		V/µs
Settling Time to 0.1%	t_S	V_{OUT} = 2V step			16		ns
Rise/Fall Time	t_R, t_F	V_{OUT} = 100mV_{P-P}			4		ns
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, V_{OUT} = 2V_{P-P}			-65		dBc
Harmonic Distortion	HD	f_C = 5MHz, V_{OUT} = 2V_{P-P}	2nd harmonic		-65		dBc
			3rd harmonic		-58		
			Total harmonic distortion		-63		
Two-Tone, Third-Order Intermodulation Distortion	IP3	f1 = 4.7MHz, f2 = 4.8MHz, V_{OUT} = 1V_{P-P}			66		dBc
Channel-to-Channel Isolation	CH_{ISO}	Specified at DC			102		dB
Input 1dB Compression Point		f_C = 10MHz, A_{VCL} = +2V/V			14		dBm
Differential Phase Error	DP	NTSC, R_L = 150Ω			0.08		degrees
Differential Gain Error	DG	NTSC, R_L = 150Ω			0.02		%
Input Noise-Voltage Density	e_n	f = 10kHz			10		nV/√Hz
Input Noise-Current Density	i_n	f = 10kHz			1.8		pA/√Hz
Input Capacitance	C_{IN}				1		pF
Output Impedance	Z_{OUT}	f = 10MHz			1.5		Ω

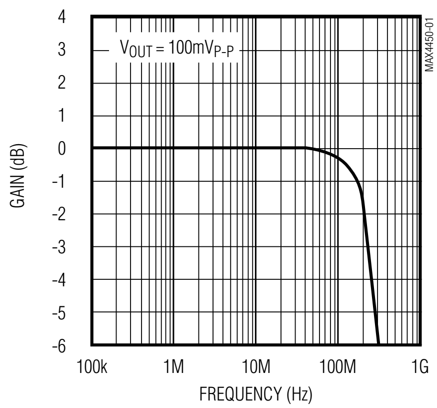
Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 2: Tested with V_{CM} = +2.5V.
Note 3: PSR for single +5V supply tested with V_{EE} = 0V, V_{CC} = +4.5V to +5.5V; PSR for dual ±5V supply tested with V_{EE} = -4.5V to -5.5V, V_{CC} = +4.5V to +5.5V.

Ultra-Small, Low-Cost, 210MHz, Single-Supply Op Amps with Rail-to-Rail Outputs

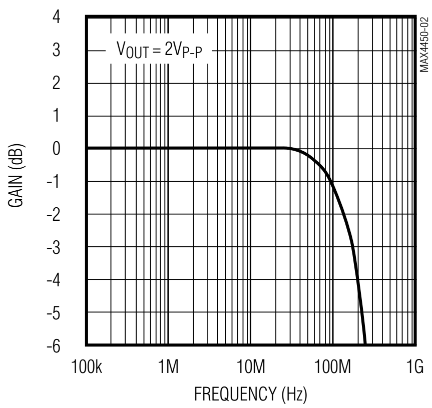
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = +2.5V, A_{VCL} = +1V/V, R_F = 24Ω, R_L = 100Ω to V_{CC}/2, T_A = +25°C, unless otherwise noted.)

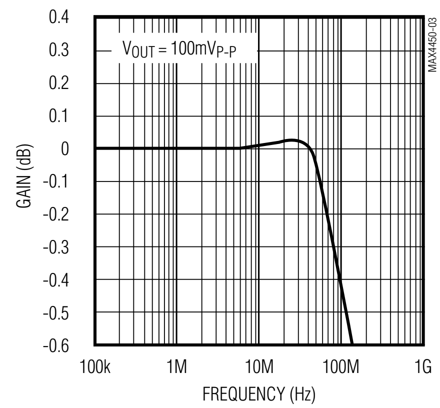
SMALL-SIGNAL GAIN vs. FREQUENCY



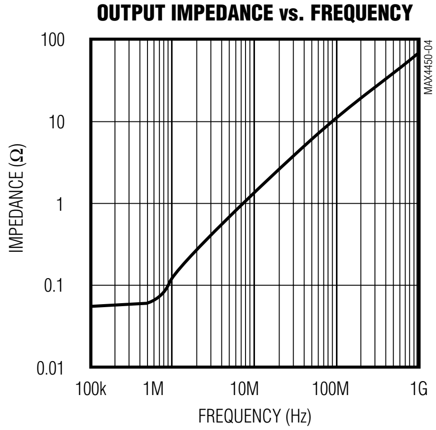
LARGE-SIGNAL GAIN vs. FREQUENCY



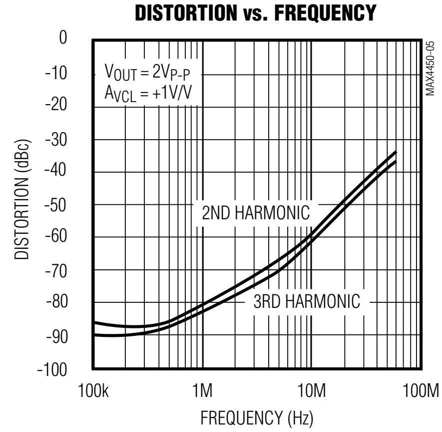
GAIN FLATNESS vs. FREQUENCY



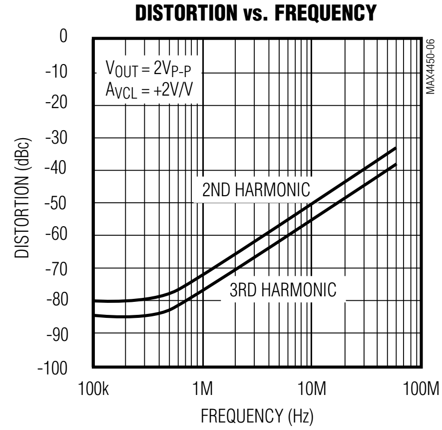
OUTPUT IMPEDANCE vs. FREQUENCY



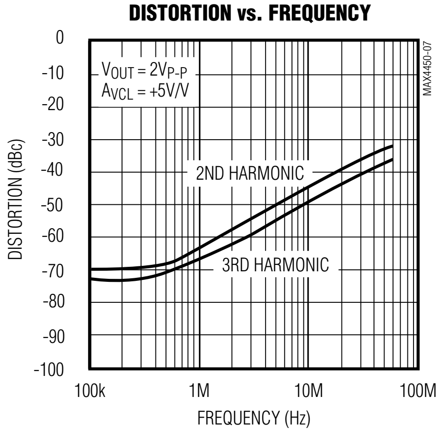
DISTORTION vs. FREQUENCY



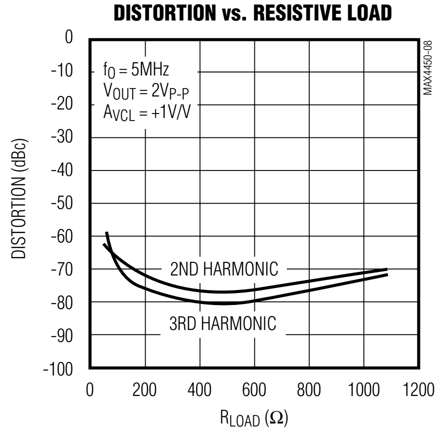
DISTORTION vs. FREQUENCY



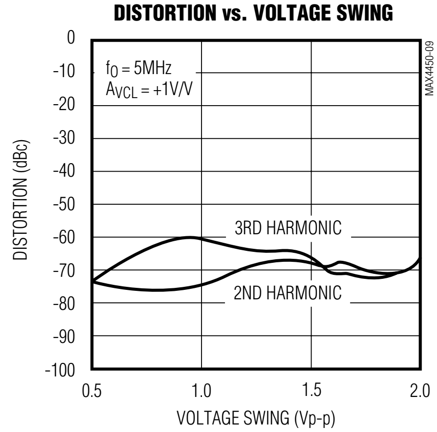
DISTORTION vs. FREQUENCY



DISTORTION vs. RESISTIVE LOAD



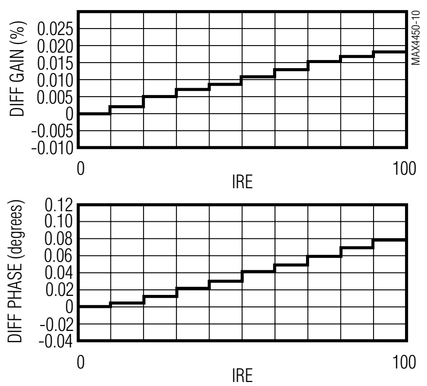
DISTORTION vs. VOLTAGE SWING



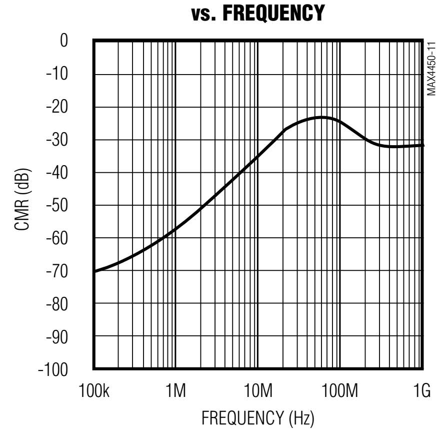
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0, V_{CM} = +2.5V, A_{VCL} = +1V/V, R_F = 24Ω, R_L = 100Ω to $V_{CC}/2$, T_A = +25°C, unless otherwise noted.)

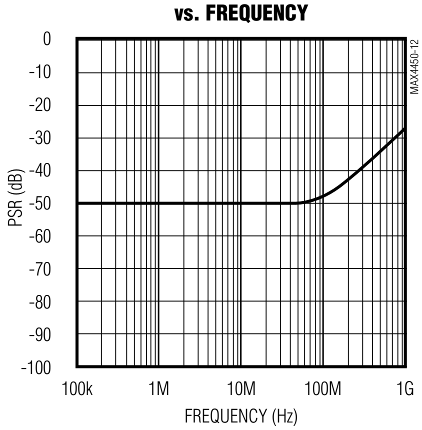
DIFFERENTIAL GAIN AND PHASE



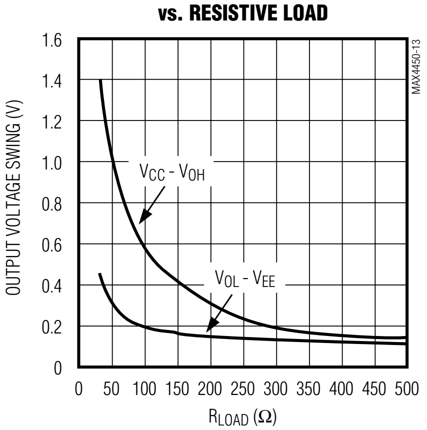
COMMON-MODE REJECTION vs. FREQUENCY



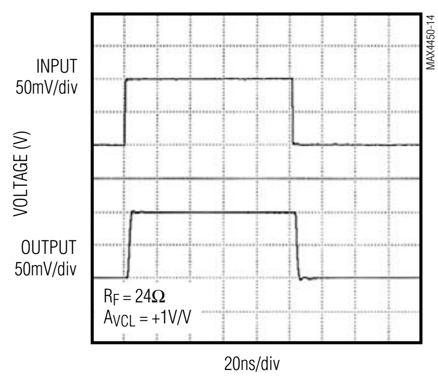
POWER-SUPPLY REJECTION vs. FREQUENCY



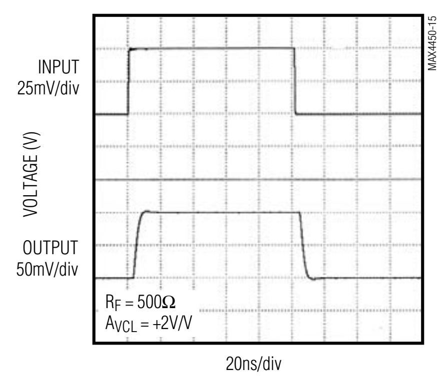
OUTPUT VOLTAGE SWING vs. RESISTIVE LOAD



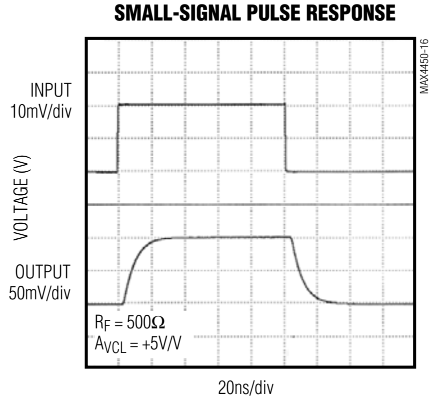
SMALL-SIGNAL PULSE RESPONSE



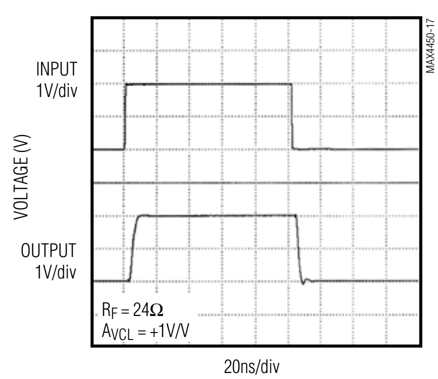
SMALL-SIGNAL PULSE RESPONSE



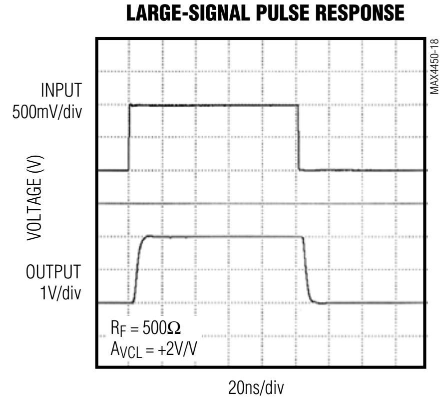
SMALL-SIGNAL PULSE RESPONSE



LARGE-SIGNAL PULSE RESPONSE



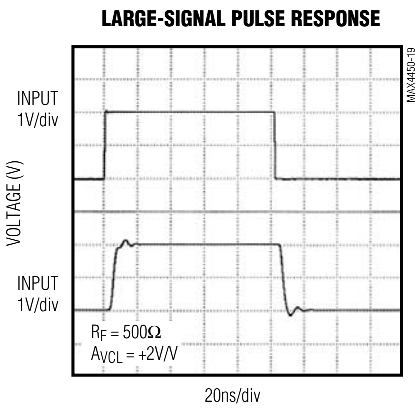
LARGE-SIGNAL PULSE RESPONSE

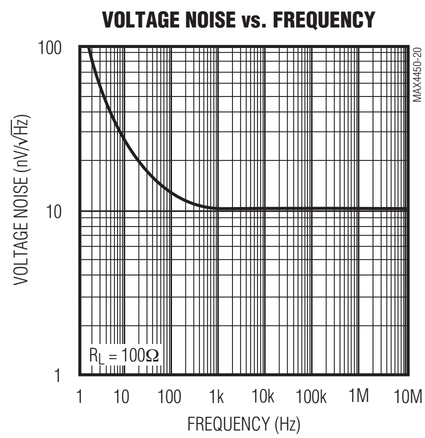


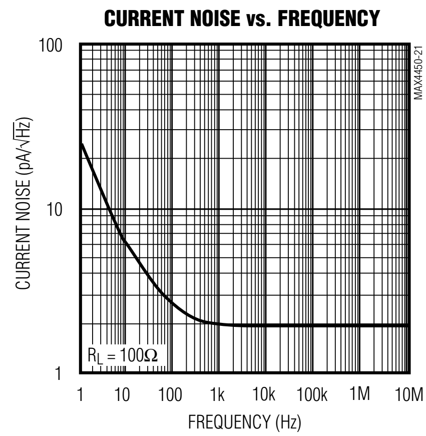
Ultra-Small, Low-Cost, 210MHz, Single-Supply Op Amps with Rail-to-Rail Outputs

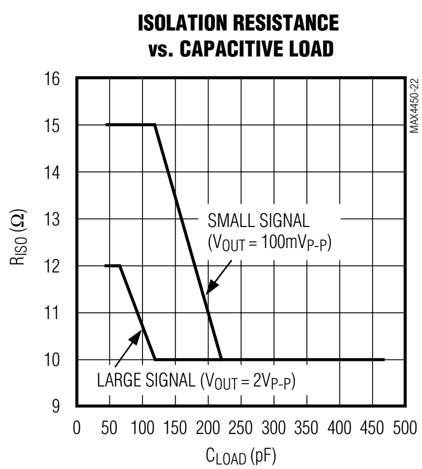
Typical Operating Characteristics (continued)

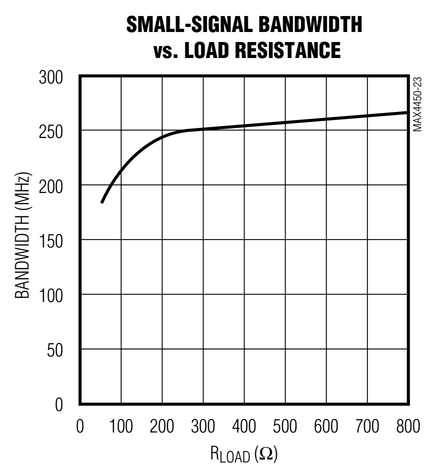
(V_{CC} = +5V, V_{EE} = 0, V_{CM} = +2.5V, A_{VCL} = +1V/V, R_F = 24Ω, R_L = 100Ω to $V_{CC}/2$, T_A = +25°C, unless otherwise noted.)

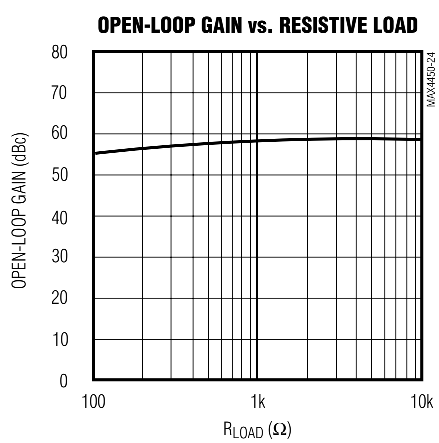


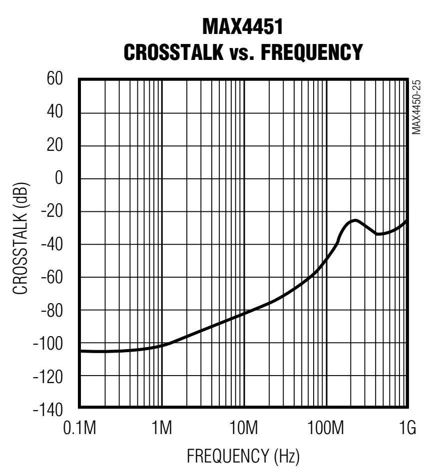












Pin Description

PIN		NAME	FUNCTION
MAX4450	MAX4451		
1	—	OUT	Amplifier Output
2	4	V_{EE}	Negative Power Supply or Ground (in single-supply operation)
3	—	IN+	Noninverting Input
4	—	IN-	Inverting Input
5	8	V_{CC}	Positive Power Supply
—	1	OUTA	Amplifier A Output
—	2	INA-	Amplifier A Inverting Input
—	3	INA+	Amplifier A Noninverting Input
—	7	OUTB	Amplifier B Output
—	6	INB-	Amplifier B Inverting Input
—	5	INB+	Amplifier B Noninverting Input

Detailed Description

The MAX4450/MAX4451 are single-supply, rail-to-rail, voltage-feedback amplifiers that employ current-feedback techniques to achieve 485V/µs slew rates and 210MHz bandwidths. Excellent harmonic distortion and differential gain/phase performance make these amplifiers an ideal choice for a wide variety of video and RF signal-processing applications.

The output voltage swings to within 55mV of each supply rail. Local feedback around the output stage ensures low open-loop output impedance to reduce gain sensitivity to load variations. The input stage permits common-mode voltages beyond the negative supply and to within 2.25V of the positive supply rail.

Applications Information

Choosing Resistor Values

Unity-Gain Configuration

The MAX4450/MAX4451 are internally compensated for unity gain. When configured for unity gain, the devices require a 24Ω resistor (R_F) in series with the feedback path. This resistor improves AC response by reducing the Q of the parallel LC circuit formed by the parasitic feedback capacitance and inductance.

Inverting and Noninverting Configurations

Select the gain-setting feedback (R_F) and input (R_G) resistor values to fit your application. Large resistor values increase voltage noise and interact with the amplifier's input and PC board capacitance. This can generate undesirable poles and zeros and decrease bandwidth or cause oscillations. For example, a noninverting gain-of-two configuration ($R_F = R_G$) using 1kΩ resistors, combined with 1pF of amplifier input capacitance and 1pF of PC board capacitance, causes a pole at 159MHz. Since this pole is within the amplifier bandwidth, it jeopardizes stability. Reducing the 1kΩ resistors to 100Ω extends the pole frequency to 1.59GHz, but could limit output swing by adding 200Ω in parallel with the amplifier's load resistor. Table 1 lists suggested feedback and gain resistors, and bandwidths for several gain values in the configurations shown in Figures 1a and 1b.

Layout and Power-Supply Bypassing

These amplifiers operate from a single +4.5V to +11V power supply or from dual ±2.25V to ±5.5V supplies. For single-supply operation, bypass V_{CC} to ground with a

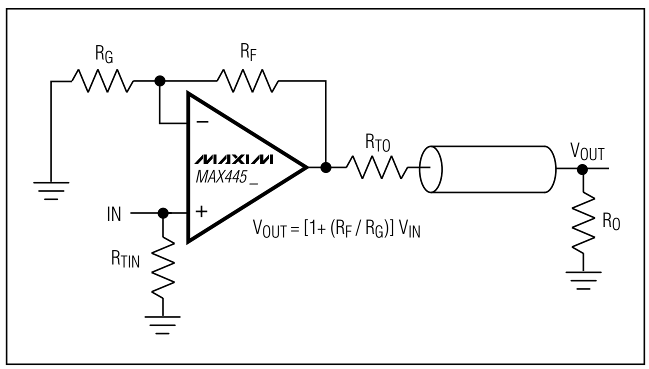


Figure 1a. Noninverting Gain Configuration

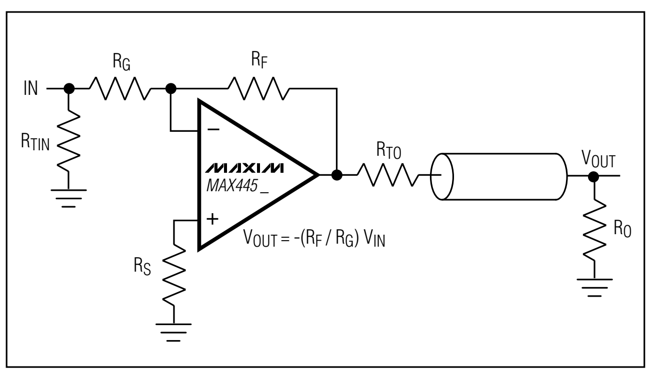


Figure 1b. Inverting Gain Configuration

Ultra-Small, Low-Cost, 210MHz, Single-Supply Op Amps with Rail-to-Rail Outputs

Table 1. Recommended Component Values

COMPONENT	GAIN (V/V)									
	+1	-1	+2	-2	+5	-5	+10	-10	+25	-25
R_F (Ω)	24	500	500	500	500	500	500	500	500	1200
R_G (Ω)	∞	500	500	250	124	100	56	50	20	50
R_S (Ω)	—	0	—	0	—	0	—	0	—	0
R_{TIN} (Ω)	49.9	56	49.9	62	49.9	100	49.9	∞	49.9	∞
R_{TO} (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9
Small-Signal -3dB Bandwidth (MHz)	210	100	95	50	25	25	11	15	5	10

Note: *$R_L = R_O + R_{TO}$; R_{TIN} and R_{TO} are calculated for 50Ω applications. For 75Ω systems, R_{TO} = 75Ω; calculate R_{TIN} from the following equation:*

$$R_{TIN} = \frac{75}{1 - \frac{75}{R_G}} \Omega$$

0.1µF capacitor as close to the pin as possible. If operating with dual supplies, bypass each supply with a 0.1µF capacitor.

Maxim recommends using microstrip and stripline techniques to obtain full bandwidth. To ensure that the PC board does not degrade the amplifier's performance, design it for a frequency greater than 1GHz. Pay careful attention to inputs and outputs to avoid large parasitic capacitance. Whether or not you use a constant-impedance board, observe the following design guidelines:

- Don't use wire-wrap boards; they are too inductive.
- Don't use IC sockets; they increase parasitic capacitance and inductance.
- Use surface-mount instead of through-hole components for better high-frequency performance.
- Use a PC board with at least two layers; it should be as free from voids as possible.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.

Rail-to-Rail Outputs, Ground-Sensing Input

The input common-mode range extends from (V_{EE} - 200mV) to (V_{CC} - 2.25V) with excellent common-mode rejection. Beyond this range, the amplifier output is a nonlinear function of the input, but does not undergo phase reversal or latchup.

The output swings to within 55mV of either power-supply rail with a 2kΩ load. The input ground sensing and the rail-to-rail output substantially increase the dynamic range. With a symmetric input in a single +5V application, the input can swing $2.95V_{P-P}$ and the output can swing $4.9V_{P-P}$ with minimal distortion.

Output Capacitive Loading and Stability

The MAX4450/MAX4451 are optimized for AC performance. They are not designed to drive highly reactive loads, which decrease phase margin and may produce excessive ringing and oscillation. Figure 2 shows a circuit that eliminates this problem. Figure 3 is a graph of the optimal isolation resistor (R_S) vs. capacitive load. Figure 4 shows how a capacitive load causes excessive peaking of the amplifier's frequency response if the capacitor is not isolated from the amplifier by a resistor. A small isolation resistor (usually 20Ω to 30Ω) placed before the reactive load prevents ringing and oscillation. At higher capacitive loads, AC performance is controlled by the interaction of the load capacitance and the isolation resistor. Figure 5 shows the effect of a 27Ω isolation resistor on closed-loop response.

Coaxial cable and other transmission lines are easily driven when properly terminated at both ends with their characteristic impedance. Driving back-terminated transmission lines essentially eliminates the line's capacitance.

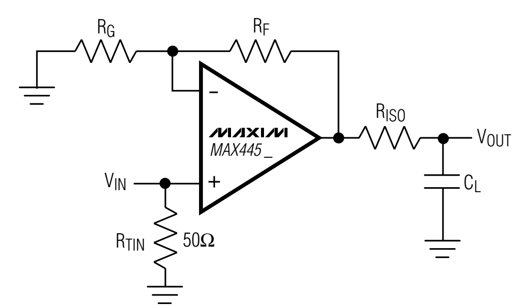


Figure 2. Driving a Capacitive Load Through an Isolation Resistor

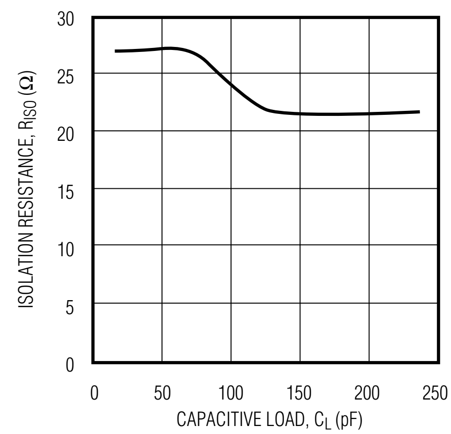


Figure 3. Capacitive Load vs. Isolation Resistance

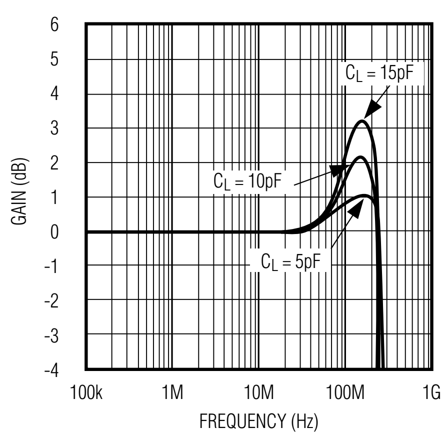


Figure 4. Small-Signal Gain vs. Frequency with Load Capacitance and No Isolation Resistor

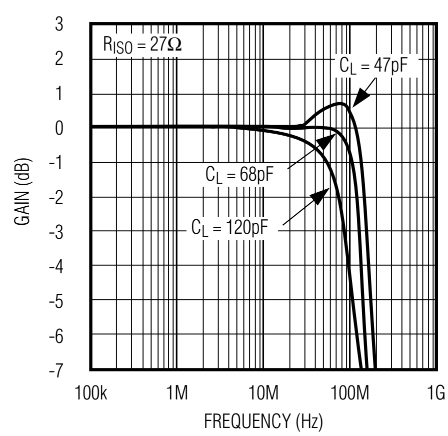
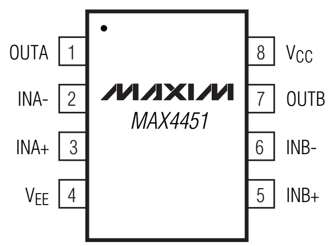


Figure 5. Small-Signal Gain vs. Frequency with Load Capacitance and 27Ω Isolation Resistor

Ultra-Small, Low-Cost, 210MHz, Single-Supply Op Amps with Rail-to-Rail Outputs

Pin Configurations (continued)

TOP VIEW



SOT23/SO

Chip Information

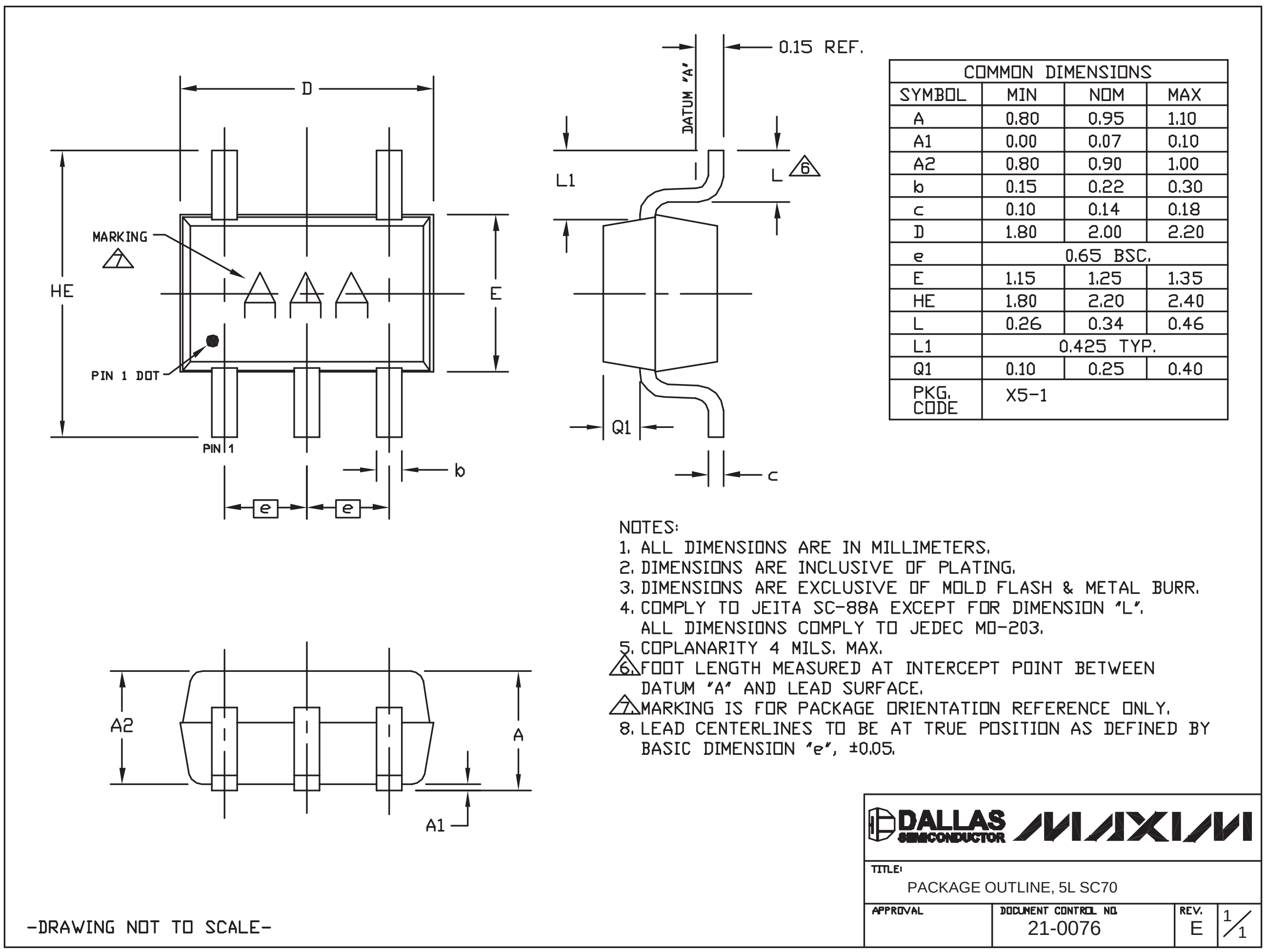
MAX4450 TRANSISTOR COUNT: 86

MAX4451 TRANSISTOR COUNT: 170

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
5 SC70	X5-1	21-0076
5 SOT23	U5-2	21-0057
8 SOT23	K8-2	21-0078
8 SO	S8-5	21-0041



COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.07	0.10
A2	0.80	0.90	1.00
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.80	2.00	2.20
e	0.65 BSC.		
E	1.15	1.25	1.35
HE	1.80	2.20	2.40
L	0.26	0.34	0.46
L1	0.425 TYP.		
Q1	0.10	0.25	0.40
PKG. CODE	X5-1		

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COMPLY TO JEITA SC-88A EXCEPT FOR DIMENSION "L". ALL DIMENSIONS COMPLY TO JEDEC MO-203.
5. COPLANARITY 4 MILS. MAX.
6. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
8. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

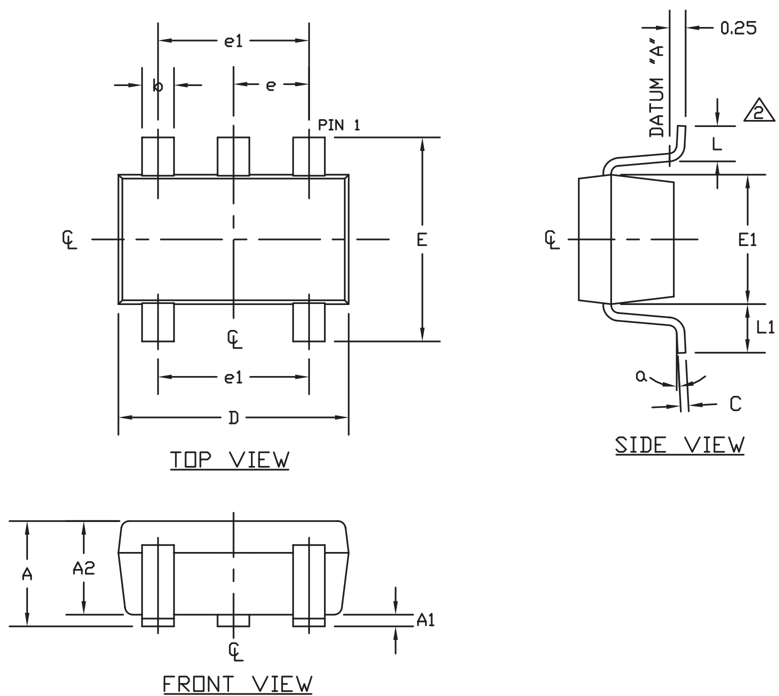
TITLE: PACKAGE OUTLINE, 5L SC70

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0076	E	1/1

Ultra-Small, Low-Cost, 210MHz, Single-Supply Op Amps with Rail-to-Rail Outputs

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1	0.60 REF		
e	0.95 BSC.		
e1	1.90 BSC.		
α	0°	2.5°	8°
PKG CODES: U5-1, U5-2			

SOT-23 5L .EPS

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. MEETS JEDEC MO178, VARIATION AA.
6. LEADS TO BE COPLANAR WITHIN 0.10 mm.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.

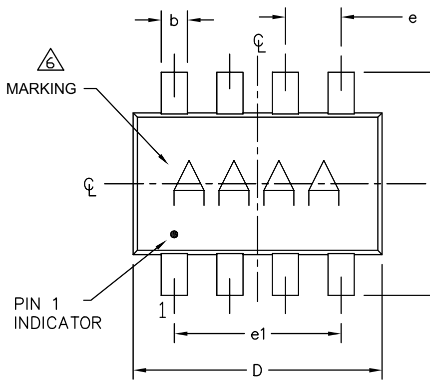
DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

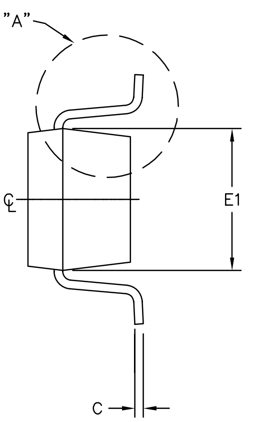
TITLE: PACKAGE OUTLINE, SOT-23, 5L

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0057	F	1/1

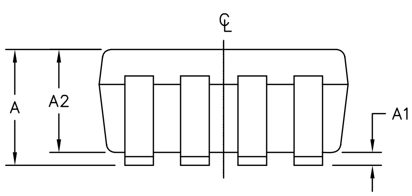
Package Information (continued)

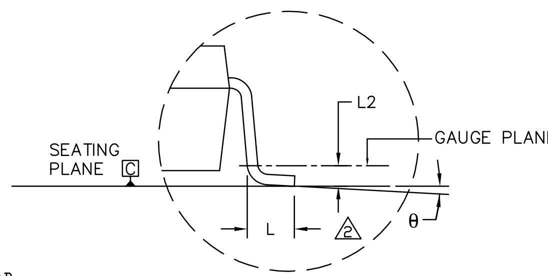
For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.





SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.06	0.15
A2	0.90	1.10	1.30
b	0.22	0.30	0.38
C	0.08	0.15	0.22
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.30	0.45	0.60
L2	0.25 BSC.		
e	0.65 BSC.		
e1	1.95 REF.		
θ	0°	3°	8°
PKG CODES: K8-1, K8-2, K8F-4, K8FH-4, K8-5, K8C-6; K8SN-1; K8CN-2			





DETAIL "A"

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178 VARIATION BA.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

MAXIM

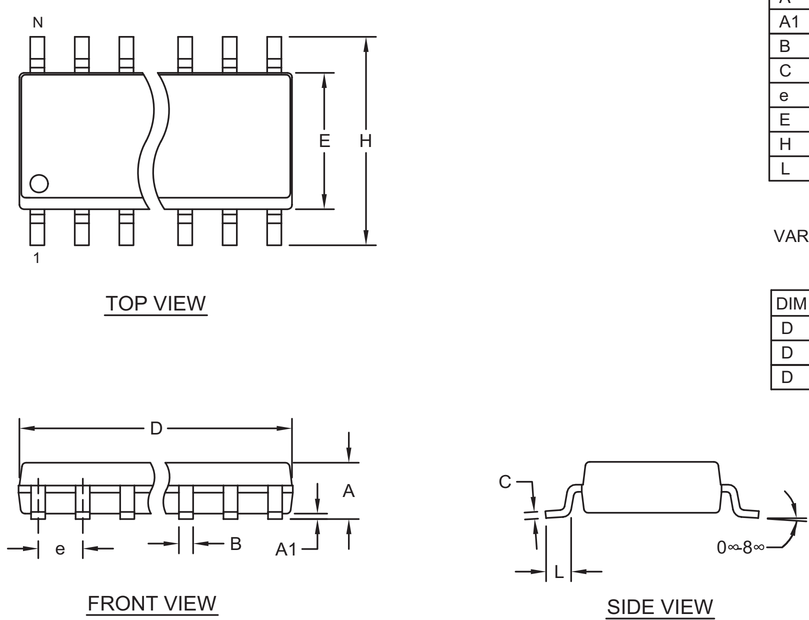
TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0078	I	1/1

Ultra-Small, Low-Cost, 210MHz, Single-Supply Op Amps with Rail-to-Rail Outputs

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	11/09	Corrected TOC 20	6